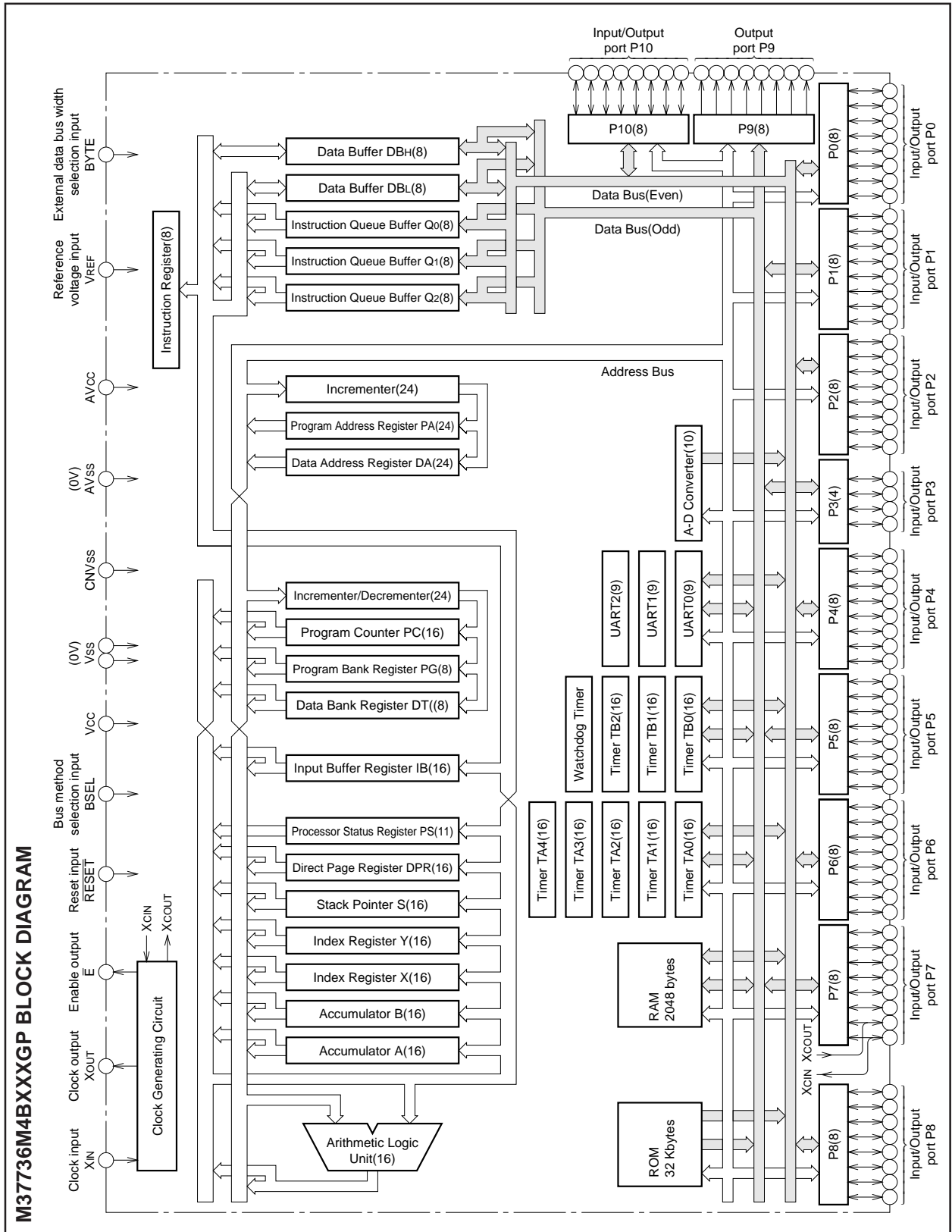


PRELIMINARY
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MITSUBISHI MICROCOMPUTERS
M37736M4BXXXGP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER



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FUNCTIONS OF M37736M4BXXXGP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		160 ns (the fastest instruction at external clock 25 MHz frequency)
Memory size	ROM	32 Kbytes
	RAM	2048 bytes
Input/Output ports	P0 – P2, P4 – P8, P10	8-bit X 9
	P3	4-bit X 1
Output port	P9	8-bit X 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit X 5
	TB0, TB1, TB2	16-bit X 3
Serial I/O		(UART or clock synchronous serial I/O) X 3
A-D converter		10-bit X 1 (8 channels)
Watchdog timer		12-bit X 1
Interrupts		3 external types, 16 internal types Each interrupt can be set to the priority level (0 – 7.)
Clock generating circuit		2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Supply voltage		5 V ± 10%
Power dissipation		47.5 mW (at external clock 25 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		External bus mode A; maximum 16 Mbytes, External bus mode B; maximum 1 Mbytes
Operating temperature range		–20 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		100-pin plastic molded QFP (100P6S-A)

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PIN DESCRIPTION

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source		Apply 5 V ± 10% to Vcc and 0 V to Vss.
CNVss	CNVss input	Input	This pin controls the processor mode. Connect to Vss for the single-chip mode and the memory expansion mode, and to Vcc for the microprocessor mode.
RESET	Reset input	Input	When "L" level is applied to this pin, the microcomputer enters the reset state.
XIN	Clock input	Input	These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between XIN and XOUT. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.
XOUT	Clock output	Output	
E	Enable output	Output	This pin functions as the enable signal output pin which indicates the access status in the internal bus. In the external bus mode B and the memory expansion mode or the microprocessor mode, this pin output signal RDE.
BYTE	External data bus width selection input	Input	In the memory expansion mode or the microprocessor mode, this pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when "L" signal is input and an 8-bit width when "H" signal is input.
BSEL	Bus method select input	Input	In the memory expansion mode or the microprocessor mode, this pin determines the external bus mode. The bus mode becomes the external bus mode A when "H" signal is input, and the external bus mode B when "L" signal is input.
AVcc, AVss	Analog power source input		Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.
VREF	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
P00 – P07	I/O port P0	I/O	In the single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset. In the memory expansion mode or the microprocessor mode, these pins output address (A0 – A7) at the external bus mode A, and these pins output signals CS0 – CS4 and RSMP, and addresses (A16, A17) at the external bus mode B.
P10 – P17	I/O port P1	I/O	In the single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in the memory expansion mode or the microprocessor mode and external data bus has a 16-bit width, high-order data (D8 – D15) is input/output or an address (A8 – A15) is output. When the BYTE pin is "H" and an external data bus has an 8-bit width, only address (A8 – A15) is output.
P20 – P27	I/O port P2	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, low-order data (D0 – D7) is input/output or an address is output. When using the external bus mode A, the address is A16 – A23. When using the external bus mode B, the address is A0 – A7.
P30 – P33	I/O port P3	I/O	In the single-chip mode, these pins have the same function as port P0. In the memory expansion mode or the microprocessor mode, R/W, BHE, ALE, and HLDA signals are output at the external bus mode A, and WEL, WEH, ALE, and HLDA signals are output at the external bus mode B.
P40 – P47	I/O port P4	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, P40, P41 and P42 become HOLD and RDY input pins, and a clock φ1 output pin, respectively. Functions of the other pins are the same as in the single-chip mode. However, in the memory expansion mode, P42 can be selected as an I/O port.
P50 – P57	I/O port P5	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0 to A3.
P60 – P67	I/O port P6	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input (INT0 – INT2) and input pins for timers B0 to B2. P67 also functions as sub-clock φSUB output pin.
P70 – P77	I/O port P7	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins function as input pins for A-D converter. Additionally, P76 and P77 have the function as the output pin (XcOUT) and the input pin (XcIN) of the sub-clock (32 kHz) oscillation circuit, respectively. When P76 and P77 are used as the XcOUT and XcIN pins, connect a resonator or an oscillator between the both.
P80 – P87	I/O port P8	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART 0 and UART 1.
P90 – P97	Output port P9	Output	Port P9 is an 8-bit I/O port. These ports are floating when reset. When writing to the port latch, these ports become the output mode. P90 – P93 also function as I/O port for UART 2.
P100 – P107	I/O port P10	I/O	In addition to having the same functions as port P0 in the single-chip mode, P104 – P107 also function as input pins for key input interrupt input (KI0 – KI3).
EVL0, EVL1	—	Output	These pins should be left open.

BASIC FUNCTION BLOCKS

The M37736M4BXXXGP has the same functions as the M37736MHBXXXGP except for the memory allocation and the ROM area modification function. Refer to the section on the M37736MHBXXXGP.

MEMORY

The memory map is shown in Figure 1. The address space has a capacity of 16 Mbytes and is allocated to addresses from 0₁₆ to FFFFFFF₁₆. The address space is divided by 64-Kbyte unit called bank. The banks are numbered from 0₁₆ to FF₁₆. However, banks 10₁₆ – FF₁₆ cannot be accessed in the external bus mode B. Built-in ROM, RAM and control registers for internal peripheral devices are assigned to bank 0₁₆. The 32-Kbyte area from addresses 8000₁₆ to FFFF₁₆ is the built-in ROM. Addresses FFD6₁₆ to FFFF₁₆ are the RESET and interrupt vector addresses and contain the interrupt vectors. Refer to the section on interrupts for details. The 2048-byte area allocated to addresses from 80₁₆ to 87F₁₆ is the

built-in RAM. In addition to storing data, the RAM is used as stack during a subroutine call or interrupts. Peripheral devices such as I/O ports, A-D converter, serial I/O, timer, and interrupt control registers are allocated to addresses from 0₁₆ to 7F₁₆. Additionally, the internal ROM area can be modified by software. Refer to the section on ROM area modification function for details. A 256-byte direct page area can be allocated anywhere in bank 0₁₆ by using the direct page register (DPR). In the direct page addressing mode, the memory in the direct page area can be accessed with two words. Hence program steps can be reduced.

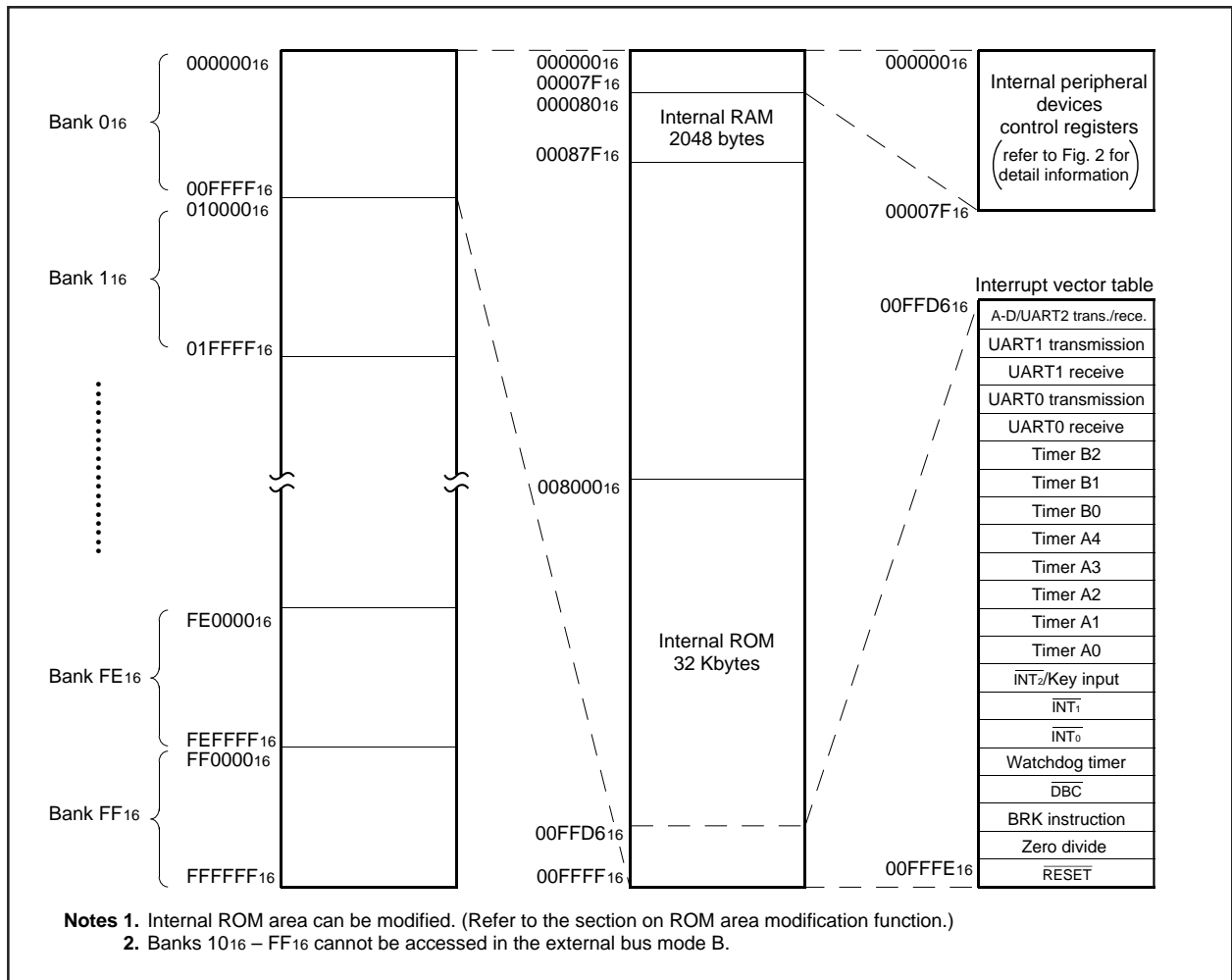


Fig. 1 Memory map

PRELIMINARY
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Address (Hexadecimal notation)		Address (Hexadecimal notation)	
000000		000040	Count start flag
000001		000041	
000002	Port P0 register	000042	One-shot start flag
000003	Port P1 register	000043	
000004	Port P0 direction register	000044	Up-down flag
000005	Port P1 direction register	000045	
000006	Port P2 register	000046	Timer A0 register
000007	Port P3 register	000047	
000008	Port P2 direction register	000048	Timer A1 register
000009	Port P3 direction register	000049	
00000A	Port P4 register	00004A	Timer A2 register
00000B	Port P5 register	00004B	
00000C	Port P4 direction register	00004C	Timer A3 register
00000D	Port P5 direction register	00004D	
00000E	Port P6 register	00004E	Timer A4 register
00000F	Port P7 register	00004F	
000010	Port P6 direction register	000050	Timer B0 register
000011	Port P7 direction register	000051	
000012	Port P8 register	000052	Timer B1 register
000013	Port P9 register	000053	
000014	Port P8 direction register	000054	Timer B2 register
000015		000055	
000016	Port P10 register	000056	Timer A0 mode register
000017		000057	Timer A1 mode register
000018	Port P10 direction register	000058	Timer A2 mode register
000019		000059	Timer A3 mode register
00001A		00005A	Timer A4 mode register
00001B		00005B	Timer B0 mode register
00001C	Reserved area (Note)	00005C	Timer B1 mode register
00001D	Reserved area (Note)	00005D	Timer B2 mode register
00001E	A-D control register 0	00005E	Processor mode register 0
00001F	A-D control register 1	00005F	Processor mode register 1
000020		000060	Watchdog timer register
000021	A-D register 0	000061	Watchdog timer frequency selection flag
000022		000062	Reserved area (Note)
000023	A-D register 1	000063	Memory allocation control register
000024		000064	UART 2 transmit/receive mode register
000025	A-D register 2	000065	UART 2 baud rate register (BRG2)
000026		000066	UART 2 transmission buffer register
000027	A-D register 3	000067	UART 2 transmit/receive control register 0
000028		000068	UART 2 transmit/receive control register 1
000029	A-D register 4	000069	
00002A		00006A	UART 2 receive buffer register
00002B	A-D register 5	00006B	
00002C		00006C	Oscillation circuit control register 0
00002D	A-D register 6	00006D	Port function control register
00002E		00006E	Serial transmit control register
00002F	A-D register 7	00006F	Oscillation circuit control register 1
000030	UART 0 transmit/receive mode register	000070	A-D/UART 2 trans./rece. interrupt control register
000031	UART 0 baud rate register (BRG0)	000071	UART 0 transmission interrupt control register
000032		000072	UART 0 receive interrupt control register
000033	UART 0 transmission buffer register	000073	UART 1 transmission interrupt control register
000034	UART 0 transmit/receive control register 0	000074	UART 1 receive interrupt control register
000035	UART 0 transmit/receive control register 1	000075	Timer A0 interrupt control register
000036	UART 0 receive buffer register	000076	Timer A1 interrupt control register
000037		000077	Timer A2 interrupt control register
000038	UART 1 transmit/receive mode register	000078	Timer A3 interrupt control register
000039	UART 1 baud rate register (BRG1)	000079	Timer A4 interrupt control register
00003A		00007A	Timer B0 interrupt control register
00003B	UART 1 transmission buffer register	00007B	Timer B1 interrupt control register
00003C	UART 1 transmit/receive control register 0	00007C	Timer B2 interrupt control register
00003D	UART 1 transmit/receive control register 1	00007D	INT ₀ interrupt control register
00003E		00007E	INT ₁ interrupt control register
00003F	UART 1 receive buffer register	00007F	INT ₂ /Key input interrupt control register

Note. Do not write to this address.

Fig. 2 Location of internal peripheral devices and interrupt control registers

ROM AREA MODIFICATION FUNCTION

The internal ROM size and its address area of the M37736M4BXXXGP can be modified by the memory allocation control register's bit 0 shown in Figure 3.

Figure 5 shows the memory allocation in which the internal ROM size and its address area are modified.

Make sure to write data in the memory allocation control register as the flow shown in Figure 4.

This ROM area modification function is valid in memory expansion mode and single-chip mode.

Table 1 shows the relationship between memory allocation selection

bits and address corresponding to chip-select signals \overline{CS}_0 and \overline{CS}_1 in the external bus mode B.

When ordering a mask ROM, Mitsubishi Electric corp. produces the mask ROM using the data within 32 Kbytes (addresses 008000₁₆ – 00FFFF₁₆). It is regardless of the selected ROM size (refer to MASK ROM ORDER CONFIRMATION FORM.) Therefore, program "FF₁₆" to the addresses out of the selected ROM area in the EPROM which you tender when ordering a mask ROM.

Address 00FFFF₁₆ of this microcomputer corresponds to the lowest address of the EPROM which you tender.

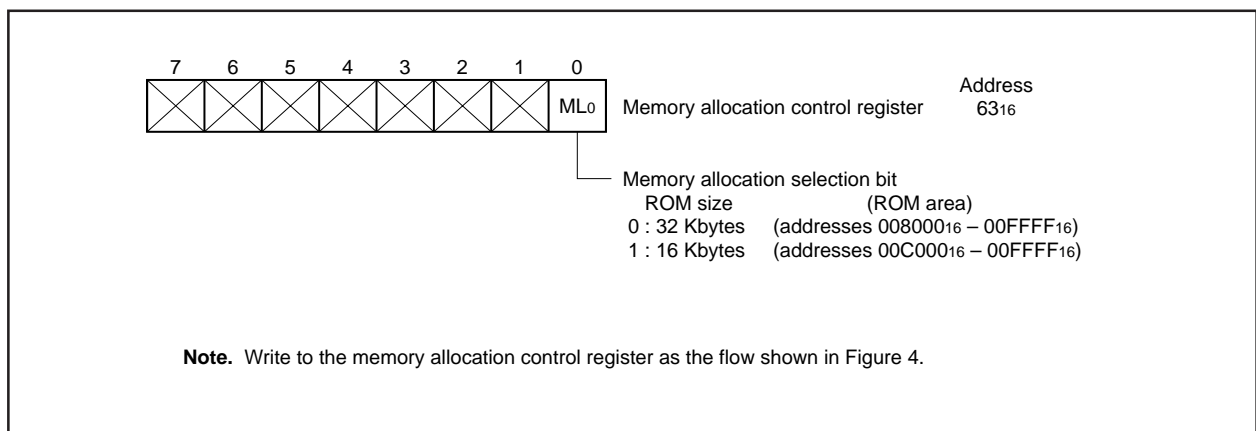


Fig. 3 Bit configuration of memory allocation control register

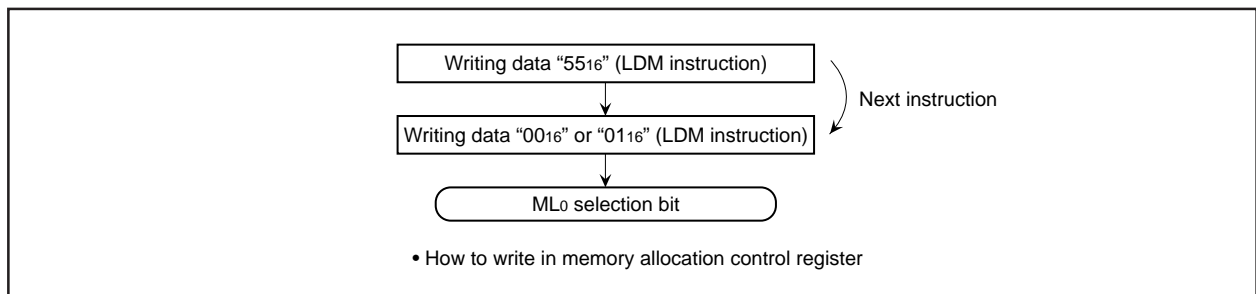


Fig. 4 How to write data in memory allocation control register

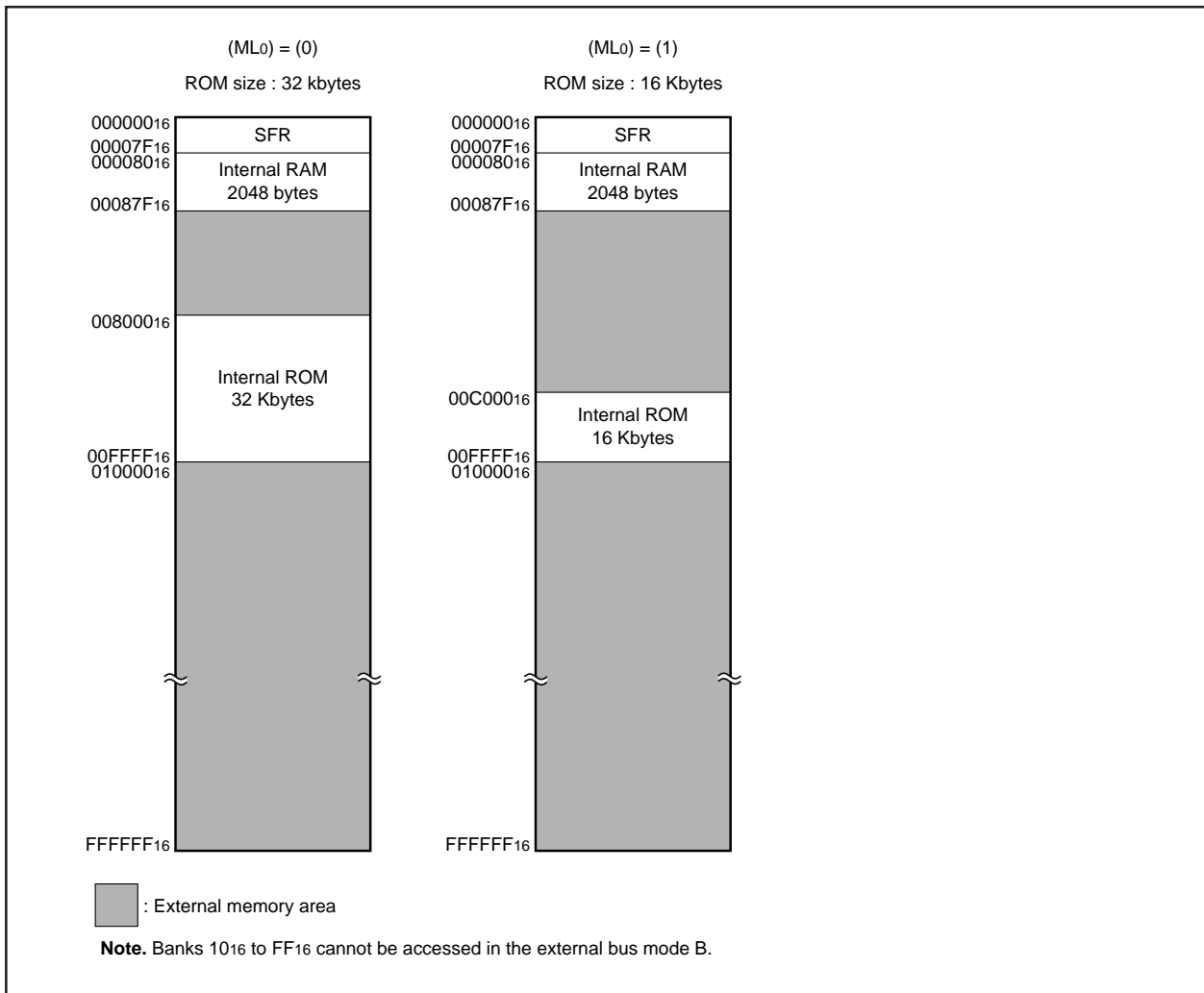


Fig. 5 Memory allocation (modification of internal ROM area by memory allocation selection bit)

Table 1. Relationship between memory allocation selection bits and addresses corresponding to chip-select signals \overline{CS}_0 and \overline{CS}_1 in external bus mode B

Memory allocation select bit ML ₀	Internal ROM area	Access address	
		\overline{CS}_0	\overline{CS}_1
0	008000 ₁₆ – 00FFFF ₁₆	000880 ₁₆ – 007FFF ₁₆	010000 ₁₆ – 03FFFF ₁₆
1	00C000 ₁₆ – 00FFFF ₁₆	000880 ₁₆ – 007FFF ₁₆	008000 ₁₆ – 00BFFF ₁₆ 010000 ₁₆ – 03FFFF ₁₆

ADDRESSING MODES

The M37736M4BXXXGP has 28 powerful addressing modes. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for the details of each addressing mode.

MACHINE INSTRUCTION LIST

The M37736M4BXXXGP has 103 machine instructions. Refer to the

MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for details.

DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

- (1) M37736M4BXXXGP mask ROM order confirmation form
- (2) 100P6S mark specification form
- (3) ROM data (EPROM 3 sets)

PRELIMINARY
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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Power source voltage		-0.3 to +7	V
AV _{cc}	Analog power source voltage		-0.3 to +7	V
V _i	Input voltage RESET, CNV _{ss} , BYTE		-0.3 to +12	V
V _i	Input voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P107, V _{REF} , X _{IN} , BSEL		-0.3 to V _{cc} + 0.3	V
V _o	Output voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107, X _{OUT} , E		-0.3 to V _{cc} + 0.3	V
P _d	Power dissipation	T _a = 25 °C	300	mW
T _{opr}	Operating temperature		-20 to +85	°C
T _{stg}	Storage temperature		-40 to +150	°C

RECOMMENDED OPERATING CONDITIONS (V_{cc} = 5 V ± 10%, T_a = -20 to +85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit	
		Min.	Typ.	Max.		
V _{cc}	Power source voltage	f(X _{IN}) : Operating	4.5	5.0	5.5	V
		f(X _{IN}) : Stopped, f(X _{CIN}) = 32.768 kHz	2.7		5.5	
AV _{cc}	Analog power source voltage		V _{cc}		V	
V _{ss}	Power source voltage		0		V	
AV _{ss}	Analog power source voltage		0		V	
V _{IH}	High-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P107, X _{IN} , RESET, CNV _{ss} , BYTE, BSEL, X _{CIN} (Note 3)	0.8 V _{cc}		V _{cc}	V	
V _{IH}	High-level input voltage P10 – P17, P20 – P27 (in single-chip mode)	0.8 V _{cc}		V _{cc}	V	
V _{IH}	High-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)	0.5 V _{cc}		V _{cc}	V	
V _{IL}	Low-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P107, X _{IN} , RESET, CNV _{ss} , BYTE, BSEL, X _{CIN} (Note 3)	0		0.2V _{cc}	V	
V _{IL}	Low-level input voltage P10 – P17, P20 – P27 (in single-chip mode)	0		0.2V _{cc}	V	
V _{IL}	Low-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)	0		0.16V _{cc}	V	
I _{OH(peak)}	High-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107			-10	mA	
I _{OH(avg)}	High-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107			-5	mA	
I _{OL(peak)}	Low-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P104 – P107			10	mA	
I _{OL(peak)}	Low-level peak output current P44 – P47, P100 – P103			20	mA	
I _{OL(avg)}	Low-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P104 – P107			5	mA	
I _{OL(avg)}	Low-level average output current P44 – P47, P100 – P103			15	mA	
f(X _{IN})	Main-clock oscillation frequency (Note 4)			25	MHz	
f(X _{CIN})	Sub-clock oscillation frequency		32.768	50	kHz	

- Notes**
1. Average output current is the average value of a 100 ms interval.
 2. The sum of I_{OL(peak)} for ports P0, P1, P2, P3, P8, and P9 must be 80 mA or less, the sum of I_{OH(peak)} for ports P0, P1, P2, P3, P8, and P9 must be 80 mA or less, the sum of I_{OL(peak)} for ports P4, P5, P6, P7, and P10 must be 100 mA or less, and the sum of I_{OH(peak)} for ports P4, P5, P6, P7, and P10 must be 80 mA or less.
 3. Limits V_{IH} and V_{IL} for X_{CIN} are applied when the sub clock external input selection bit = "1".
 4. The maximum value of f(X_{IN}) = 12.5 MHz when the main clock division selection bit = "1".

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ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 25\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107	$I_{OH} = -10\text{ mA}$	3			V
V_{OH}	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	$I_{OH} = -400\text{ }\mu\text{A}$	4.7			V
V_{OH}	High-level output voltage P30 – P32	$I_{OH} = -10\text{ mA}$ $I_{CH} = -400\text{ }\mu\text{A}$	3.1 4.8			V
V_{OH}	High-level output voltage \bar{E}	$I_{OH} = -10\text{ mA}$ $I_{OH} = -400\text{ }\mu\text{A}$	3.4 4.8			V
V_{OL}	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P97, P100 – P107	$I_{OL} = 10\text{ mA}$			2	V
V_{OL}	Low-level output voltage P44 – P47, P100 – P103	$I_{OL} = 20\text{ mA}$			2	V
V_{OL}	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	$I_{OL} = 2\text{ mA}$			0.45	V
V_{OL}	Low-level output voltage P30 – P32	$I_{OL} = 10\text{ mA}$ $I_{OL} = 2\text{ mA}$			1.9 0.43	V
V_{OL}	Low-level output voltage \bar{E}	$I_{OL} = 10\text{ mA}$ $I_{OL} = 2\text{ mA}$			1.6 0.4	V
$V_{T+} - V_{T-}$	Hysteresis \overline{HOLD} , \overline{RDY} , $\overline{TA0IN} - \overline{TA4IN}$, $\overline{TB0IN} - \overline{TB2IN}$, $\overline{INT0} - \overline{INT2}$, \overline{ADTRG} , $\overline{CTS0}$, $\overline{CTS1}$, $\overline{CTS2}$, $\overline{CLK0}$, $\overline{CLK1}$, $\overline{CLK2}$, $\overline{KI0} - \overline{KI3}$		0.4		1	V
$V_{T+} - V_{T-}$	Hysteresis \overline{RESET}		0.2		0.5	V
$V_{T+} - V_{T-}$	Hysteresis X_{IN}		0.1		0.4	V
$V_{T+} - V_{T-}$	Hysteresis X_{CIN} (When external clock is input)		0.1		0.4	V
I_{IH}	High-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P107, X_{IN} , \overline{RESET} , \overline{CNVss} , \overline{BYTE} , \overline{BSEL}	$V_I = 5\text{ V}$			5	μA
I_{IL}	Low-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60, P61, P65 – P67, P70 – P77, P80 – P87, P90 – P92, P100 – P103, X_{IN} , \overline{RESET} , \overline{CNVss} , \overline{BYTE} , \overline{BSEL}	$V_I = 0\text{ V}$			-5	μA
I_{IL}	Low-level input current P104 – P107, P62 – P64	$V_I = 0\text{ V}$, without a pull-up transistor $V_I = 0\text{ V}$, with a pull-up transistor			-5	μA
I_{IL}			-0.25	-0.5	-1.0	mA
V_{RAM}	RAM hold voltage	When clock is stopped.	2			V

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
I _{CC}	Power source current	In single-chip mode, output pins are open, and other pins are V _{SS} .	$V_{CC} = 5\text{ V}$, $f(X_{IN}) = 25\text{ MHz}$ (square waveform), $f(f_2) = 12.5\text{ MHz}$, $f(X_{CIN}) = 32.768\text{ kHz}$, in operating (Note 1)		9.5	19	mA
			$V_{CC} = 5\text{ V}$, $f(X_{IN}) = 25\text{ MHz}$ (square waveform), $f(f_2) = 1.5625\text{ MHz}$, $f(X_{CIN}) = \text{Stopped}$, in operating (Note 1)		1.3	2.6	mA
			$V_{CC} = 5\text{ V}$, $f(X_{IN}) = 25\text{ MHz}$ (square waveform), $f(X_{CIN}) = 32.768\text{ kHz}$, when a WIT instruction is executed (Note 2)		10	20	μA
			$V_{CC} = 5\text{ V}$, $f(X_{IN}) : \text{Stopped}$, $f(X_{CIN}) : 32.768\text{ kHz}$, in operating (Note 3)		50	100	μA
			$V_{CC} = 5\text{ V}$, $f(X_{IN}) : \text{Stopped}$, $f(X_{CIN}) : 32.768\text{ kHz}$, when a WIT instruction is executed (Note 4)		5	10	μA
			$T_a = 25\text{ }^\circ\text{C}$, when clock is stopped			1	μA
			$T_a = 85\text{ }^\circ\text{C}$, when clock is stopped			20	μA

- Notes**
1. This applies when the main clock external input selection bit = "1", the main clock division selection bit = "0", and the signal output stop bit = "1".
 2. This applies when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1".
 3. This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.
 4. This applies when the X_{COUT} drivability selection bit = "0" and the system clock stop bit at wait state = "1".

A-D CONVERTER CHARACTERISTICS

($V_{CC} = AV_{CC} = 5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 25\text{ MHz}$ (Note), unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC}$			10	Bits
—	Absolute accuracy	$V_{REF} = V_{CC}$			± 3	LSB
RLADDER	Ladder resistance	$V_{REF} = V_{CC}$	10		25	$\text{k}\Omega$
t _{CONV}	Conversion time		9.44			μs
V _{REF}	Reference voltage		2		V_{CC}	V
V _{IA}	Analog input voltage		0		V_{REF}	V

Note. This applies when the main clock division selection bit = "0" and $f(f_2) = 12.5\text{ MHz}$.

TIMING REQUIREMENTS ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 25\text{ MHz}$, unless otherwise noted (Note))

Notes 1. This applies when the main clock division selection bit = "0" and $f(f_2) = 12.5\text{ MHz}$.

2. Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time (Note 3)	40		ns
$t_{w(H)}$	External clock input high-level pulse width (Note 4)	15		ns
$t_{w(L)}$	External clock input low-level pulse width (Note 4)	15		ns
t_r	External clock rise time		8	ns
t_f	External clock fall time		8	ns

Notes 3. When the main clock division selection bit = "1", the minimum value of $t_c = 80\text{ ns}$.

4. When the main clock division selection bit = "1", values of $t_{w(H)} / t_c$ and $t_{w(L)} / t_c$ must be set to values from 0.45 through 0.55.

Single-chip mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(P0D-E)}$	Port P0 input setup time	60		ns
$t_{su(P1D-E)}$	Port P1 input setup time	60		ns
$t_{su(P2D-E)}$	Port P2 input setup time	60		ns
$t_{su(P3D-E)}$	Port P3 input setup time	60		ns
$t_{su(P4D-E)}$	Port P4 input setup time	60		ns
$t_{su(P5D-E)}$	Port P5 input setup time	60		ns
$t_{su(P6D-E)}$	Port P6 input setup time	60		ns
$t_{su(P7D-E)}$	Port P7 input setup time	60		ns
$t_{su(P8D-E)}$	Port P8 input setup time	60		ns
$t_{su(P10D-E)}$	Port P10 input setup time	60		ns
$t_{h(E-P0D)}$	Port P0 input hold time	0		ns
$t_{h(E-P1D)}$	Port P1 input hold time	0		ns
$t_{h(E-P2D)}$	Port P2 input hold time	0		ns
$t_{h(E-P3D)}$	Port P3 input hold time	0		ns
$t_{h(E-P4D)}$	Port P4 input hold time	0		ns
$t_{h(E-P5D)}$	Port P5 input hold time	0		ns
$t_{h(E-P6D)}$	Port P6 input hold time	0		ns
$t_{h(E-P7D)}$	Port P7 input hold time	0		ns
$t_{h(E-P8D)}$	Port P8 input hold time	0		ns
$t_{h(E-P10D)}$	Port P10 input hold time	0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(D-E)}$	Data input setup time (external bus mode A)	32		ns
$t_{su(D-RDE)}$	Data input setup time (external bus mode B)	32		ns
$t_{su(RDY-\phi 1)}$	RDY input setup time	55		ns
$t_{su(HOLD-\phi 1)}$	HOLD input setup time	55		ns
$t_{h(E-D)}$	Data input hold time (external bus mode A)	0		ns
$t_{h(RDE-D)}$	Data input hold time (external bus mode B)	0		ns
$t_{h(\phi 1-RDY)}$	RDY input hold time	0		ns
$t_{h(\phi 1-HOLD)}$	HOLD input hold time	0		ns

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

Timer A input (Count input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TAiIN input cycle time	80		ns
t _w (TAH)	TAiIN input high-level pulse width	40		ns
t _w (TAL)	TAiIN input low-level pulse width	40		ns

Timer A input (Gating input in timer mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TAiIN input cycle time (Note)	320		ns
t _w (TAH)	TAiIN input high-level pulse width (Note)	160		ns
t _w (TAL)	TAiIN input low-level pulse width (Note)	160		ns

Note. Limits change depending on f(X_{IN}). Refer to "DATA FORMULAS".

Timer A input (External trigger input in one-shot pulse mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TAiIN input cycle time (Note)	320		ns
t _w (TAH)	TAiIN input high-level pulse width	80		ns
t _w (TAL)	TAiIN input low-level pulse width	80		ns

Note. Limits change depending on f(X_{IN}). Refer to "DATA FORMULAS".

Timer A input (External trigger input in pulse width modulation mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _w (TAH)	TAiIN input high-level pulse width	80		ns
t _w (TAL)	TAiIN input low-level pulse width	80		ns

Timer A input (Up-down input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (UP)	TAiOUT input cycle time	2000		ns
t _w (UPH)	TAiOUT input high-level pulse width	1000		ns
t _w (UPL)	TAiOUT input low-level pulse width	1000		ns
t _{su} (UP-T _{IN})	TAiOUT input setup time	400		ns
t _h (T _{IN} -UP)	TAiOUT input hold time	400		ns

Timer A input (Two-phase pulse input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TAjIN input cycle time	800		ns
t _{su} (TAjIN-TAjOUT)	TAjIN input setup time	200		ns
t _{su} (TAjOUT-TAjIN)	TAjOUT input setup time	200		ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _c (TB)	TBiN input cycle time (one edge count)	80		ns
t _w (TBH)	TBiN input high-level pulse width (one edge count)	40		ns
t _w (TBL)	TBiN input low-level pulse width (one edge count)	40		ns
t _c (TB)	TBiN input cycle time (both edges count)	160		ns
t _w (TBH)	TBiN input high-level pulse width (both edges count)	80		ns
t _w (TBL)	TBiN input low-level pulse width (both edges count)	80		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _c (TB)	TBiN input cycle time (Note)	320		ns
t _w (TBH)	TBiN input high-level pulse width (Note)	160		ns
t _w (TBL)	TBiN input low-level pulse width (Note)	160		ns

Note. Limits change depending on f(X_{IN}). Refer to "DATA FORMULAS".

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _c (TB)	TBiN input cycle time (Note)	320		ns
t _w (TBH)	TBiN input high-level pulse width (Note)	160		ns
t _w (TBL)	TBiN input low-level pulse width (Note)	160		ns

Note. Limits change depending on f(X_{IN}). Refer to "DATA FORMULAS".

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _c (AD)	ADTRG input cycle time (minimum allowable trigger)	1000		ns
t _w (ADL)	ADTRG input low-level pulse width	125		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _c (CK)	CLK _i input cycle time	200		ns
t _w (CKH)	CLK _i input high-level pulse width	100		ns
t _w (CKL)	CLK _i input low-level pulse width	100		ns
t _d (C-Q)	TxD _i output delay time		80	ns
t _h (C-Q)	TxD _i hold time	0		ns
t _{su} (D-C)	RxD _i input setup time	30		ns
t _h (C-D)	RxD _i input hold time	90		ns

External interrupt INT_i input, key input interrupt KI_i input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _w (INH)	INT _i input high-level pulse width	250		ns
t _w (INL)	INT _i input low-level pulse width	250		ns
t _w (KIL)	KI _i input low-level pulse width	250		ns

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

DATA FORMULAS

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIn input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAH)}$	TAiIn input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAL)}$	TAiIn input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIn input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer B input (In pulse period measurement mode or pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIn input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBH)}$	TBiIn input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBL)}$	TBiIn input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Note. $f(f_2)$ represents the clock f_2 frequency.

For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37736MHBXXXGP".

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85^\circ\text{C}$, $f(X_{IN}) = 25\text{ MHz}$ (Note), unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_d(E-P0Q)$	Port P0 data output delay time	Fig. 6		80	ns
$t_d(E-P1Q)$	Port P1 data output delay time			80	ns
$t_d(E-P2Q)$	Port P2 data output delay time			80	ns
$t_d(E-P3Q)$	Port P3 data output delay time			80	ns
$t_d(E-P4Q)$	Port P4 data output delay time			80	ns
$t_d(E-P5Q)$	Port P5 data output delay time			80	ns
$t_d(E-P6Q)$	Port P6 data output delay time			80	ns
$t_d(E-P7Q)$	Port P7 data output delay time			80	ns
$t_d(E-P8Q)$	Port P8 data output delay time			80	ns
$t_d(E-P9Q)$	Port P9 data output delay time			80	ns
$t_d(E-P10Q)$	Port P10 data output delay time			80	ns

Note. This applies when the main clock division selection bit = "0" and $f(f_2) = 12.5\text{ MHz}$.

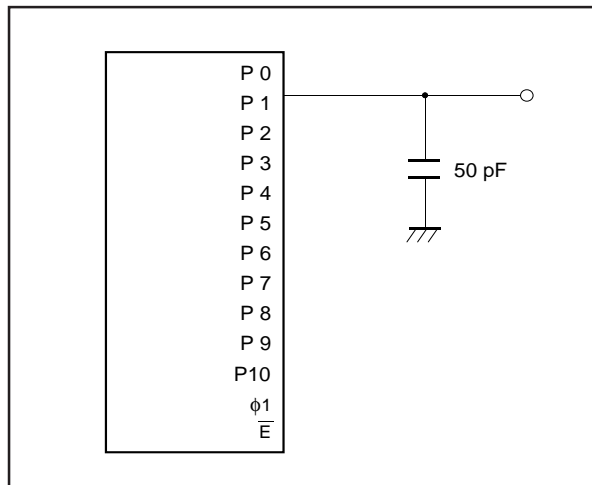


Fig. 6 Measuring circuit for ports P0 – P10 and ϕ_1

[External bus mode A]

Memory expansion mode and microprocessor mode

(V_{CC} = 5 V ± 10%, V_{SS} = 0 V, T_a = 25 °C, f(X_{IN}) = 25 MHz (Note 1), unless otherwise noted)

Symbol	Parameter	(Note 2) Wait mode	Test conditions	Limits		Unit
				Min.	Max.	
td(A _n -E)	Address output delay time	No wait	Fig. 6	12		ns
		Wait 1		87		ns
		Wait 0				ns
td(A-E)	Address output delay time	No wait		12		ns
		Wait 1		75		ns
		Wait 0				ns
th(E-An)	Address hold time			18		ns
tw(ALE)	ALE pulse width	No wait		22		ns
		Wait 1		57		ns
		Wait 0				ns
tsu(A-ALE)	Address output setup time	No wait		5		ns
		Wait 1		45		ns
		Wait 0				ns
th(ALE-A)	Address hold time	No wait		9		ns
		Wait 1		15		ns
		Wait 0			ns	
td(ALE-E)	ALE output delay time	No wait	4		ns	
		Wait 1	10		ns	
		Wait 0			ns	
td(E-DQ)	Data output delay time			45	ns	
th(E-DQ)	Data hold delay time		18		ns	
tw(EL)	E pulse width	No wait	50		ns	
		Wait 1	130		ns	
		Wait 0			ns	
tpxz(E-DZ)	Floating start delay time			5	ns	
tpzx(E-DZ)	Floating release delay time		20		ns	
td(BHE-E)	BHE output delay time	No wait	12		ns	
		Wait 1	87		ns	
		Wait 0			ns	
td(R/W-E)	R/W output delay time	No wait	12		ns	
		Wait 1	87		ns	
		Wait 0			ns	
th(E-BHE)	BHE hold time		18		ns	
th(E-R/W)	R/W hold time		18		ns	
td(E-φ ₁)	φ ₁ output delay time		0	18	ns	
td(φ ₁ -HLDA)	HLDA output delay time			50	ns	

Notes 1. This applies when the main clock division selection bit = "0" and f(f₂) = 12.5 MHz.

2. No wait : Wait bit = "1".

Wait 1 : The external memory area is accessed with wait bit = "0" and wait selection bit = "1".

Wait 0 : The external memory area is accessed with wait bit = "0" and wait selection bit = "0".

[External bus mode A]

Memory expansion mode and microprocessor mode

Bus timing data formulas ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(XIN) = 25\text{ MHz}$ (Max., Note), unless otherwise noted)

Symbol	Parameter	Wait mode	Limits		Unit
			Min.	Max.	
td(An-E)	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
td(A-E)	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 45$		ns
th(E-An)	Address hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
tw(ALE)	ALE pulse width	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 18$		ns
		Wait 1	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 23$		ns
tsu(A-ALE)	Address output setup time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
		Wait 1	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
th(ALE-A)	Address hold time	No wait	9		ns
		Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 25$		ns
td(ALE-E)	ALE output delay time	No wait	4		ns
		Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
td(E-DQ)	Data output delay time			45	ns
th(E-DQ)	Data hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
tw(EL)	\overline{E} pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
		Wait 1	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
tpxz(E-DZ)	Floating start delay time			5	ns
tpzx(E-DZ)	Floating release delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 20$		ns
td(BHE-E)	\overline{BHE} output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
td(R/W-E)	R/\overline{W} output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
th(E-BHE)	\overline{BHE} hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
th(E-R/W)	R/\overline{W} hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
td(E-φ1)	φ1 output delay time		0	18	ns

Notes 1. This applies when the main-clock division selection bit = "0".

2. $f(f_2)$ represents the clock f_2 frequency.

For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37736MHBXXXGP".

[External bus mode B]
Memory expansion mode and microprocessor mode

(V_{CC} = 5 V ± 10%, V_{SS} = 0 V, T_a = -20 to 85 °C, f(XIN) = 25 MHz (Note 1), unless otherwise noted)

Symbol	Parameter	(Note 2) Wait mode	Test conditions	Limits		Unit
				Min.	Max.	
t _d (CS-WE) t _d (CS-RDE)	Chip-select output delay time	No wait	Fig. 6	12		ns
		Wait 1		87		ns
		Wait 0				ns
t _h (WE-CS) t _h (RDE-CS)	Chip-select hold time			4		ns
						ns
						ns
t _d (An-WE) t _d (An-RDE)	Address output delay time	No wait		12		ns
		Wait 1		87		ns
		Wait 0				ns
t _d (A-WE) t _d (A-RDE)	Address output delay time	No wait		12		ns
		Wait 1		75		ns
		Wait 0				ns
t _h (WE-An) t _h (RDE-An)	Address hold time			18		ns
						ns
						ns
t _w (ALE)	ALE pulse width	No wait		22		ns
		Wait 1		57		ns
		Wait 0				ns
t _{su} (A-ALE)	Address output setup time	No wait		5		ns
		Wait 1		45		ns
		Wait 0				ns
t _h (ALE-A)	Address hold time	No wait		9		ns
		Wait 1		15		ns
		Wait 0				ns
t _d (ALE-WE) t _d (ALE-RDE)	ALE output delay time	No wait		4		ns
		Wait 1		10		ns
		Wait 0				ns
t _d (WE-DQ)	Data output delay time				45	ns
t _h (WE-DQ)	Data hold delay time			18		ns
t _w (WE)	WEL/WEH pulse width	No wait		50		ns
		Wait 1		130		ns
		Wait 0				ns
t _{pxz} (RDE-DZ)	Floating start delay time				5	ns
t _{pzx} (RDE-DZ)	Floating release delay time			20		ns
t _w (RDE)	RDE pulse width	No wait		48		ns
		Wait 1		128		ns
		Wait 0				ns
t _d (RSMP-WE) t _d (RSMP-RDE)	RSMP output delay time			10		ns
t _h (φ ₁ -RSMP)	RSMP hold time			0		ns
t _d (WE-φ ₁) t _d (RDE-φ ₁)	φ ₁ output delay time			0	18	ns
t _d (φ ₁ -HLDA)	HLDA output delay time				50	ns

Notes 1. This applies when the main clock division selection bit = "0" and f(f₂) = 12.5 MHz.

2. No wait : Wait bit = "1".

Wait 1 : The external memory area is accessed with wait bit = "0" and wait selection bit = "1".

Wait 0 : The external memory area is accessed with wait bit = "0" and wait selection bit = "0".

[External bus mode B]

Memory expansion mode and microprocessor mode

Bus timing data formulas ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 25\text{ MHz}$ (Max., Note1), unless otherwise noted)

Symbol	Parameter	Wait mode	Limits		Unit
			Min.	Max.	
$t_{d(CS-WE)}$ $t_{d(CS-RDE)}$	Chip-select output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 1			
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
$t_{h(WE-CS)}$ $t_{h(RDE-CS)}$	Chip-select hold time		4		ns
$t_{d(An-WE)}$ $t_{d(An-RDE)}$	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 1			
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
$t_{d(A-WE)}$ $t_{d(A-RDE)}$	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 1			
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 45$		ns
$t_{h(WE-An)}$ $t_{h(RDE-An)}$	Address hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
$t_w(ALE)$	ALE pulse width	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 18$		ns
		Wait 1			
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 23$		ns
$t_{su}(A-ALE)$	Address output setup time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
		Wait 1			
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
$t_{h}(ALE-A)$	Address hold time	No wait	9		ns
		Wait 1			
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 25$		ns
$t_{d}(ALE-WE)$ $t_{d}(ALE-RDE)$	ALE output delay time	No wait	4		ns
		Wait 1			
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
$t_{d}(WE-DQ)$	Data output delay time			45	ns
$t_{h}(WE-DQ)$	Data hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
$t_w(WE)$	$\overline{WEL}/\overline{WEH}$ pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
		Wait 1			
		Wait 0	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
$t_{pxz}(RDE-DZ)$	Floating start delay time			5	ns
$t_{pzx}(RDE-DZ)$	Floating release delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 20$		ns
$t_w(RDE)$	RDE pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 32$		ns
		Wait 1			
		Wait 0	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 32$		ns
$t_{d}(RSMP-WE)$ $t_{d}(RSMP-RDE)$	RSMP output delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
$t_{h}(\phi_1-RSMP)$	RSMP hold time		0		ns
$t_{d}(WE-\phi_1)$ $t_{d}(RDE-\phi_1)$	ϕ_1 output delay time		0	18	ns

Notes 1. This applies when the main-clock division selection bit = "0".

2. $f(f_2)$ represents the clock f_2 frequency.

For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37736MHBXXXGP".

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TIMING DIAGRAM

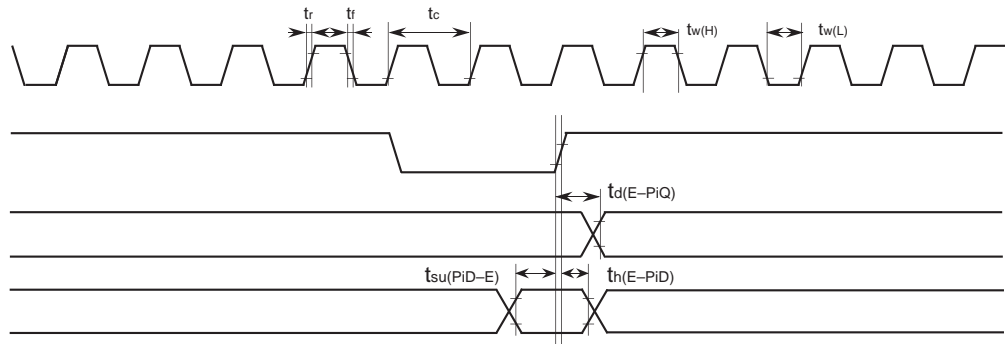
Single-chip mode

XIN

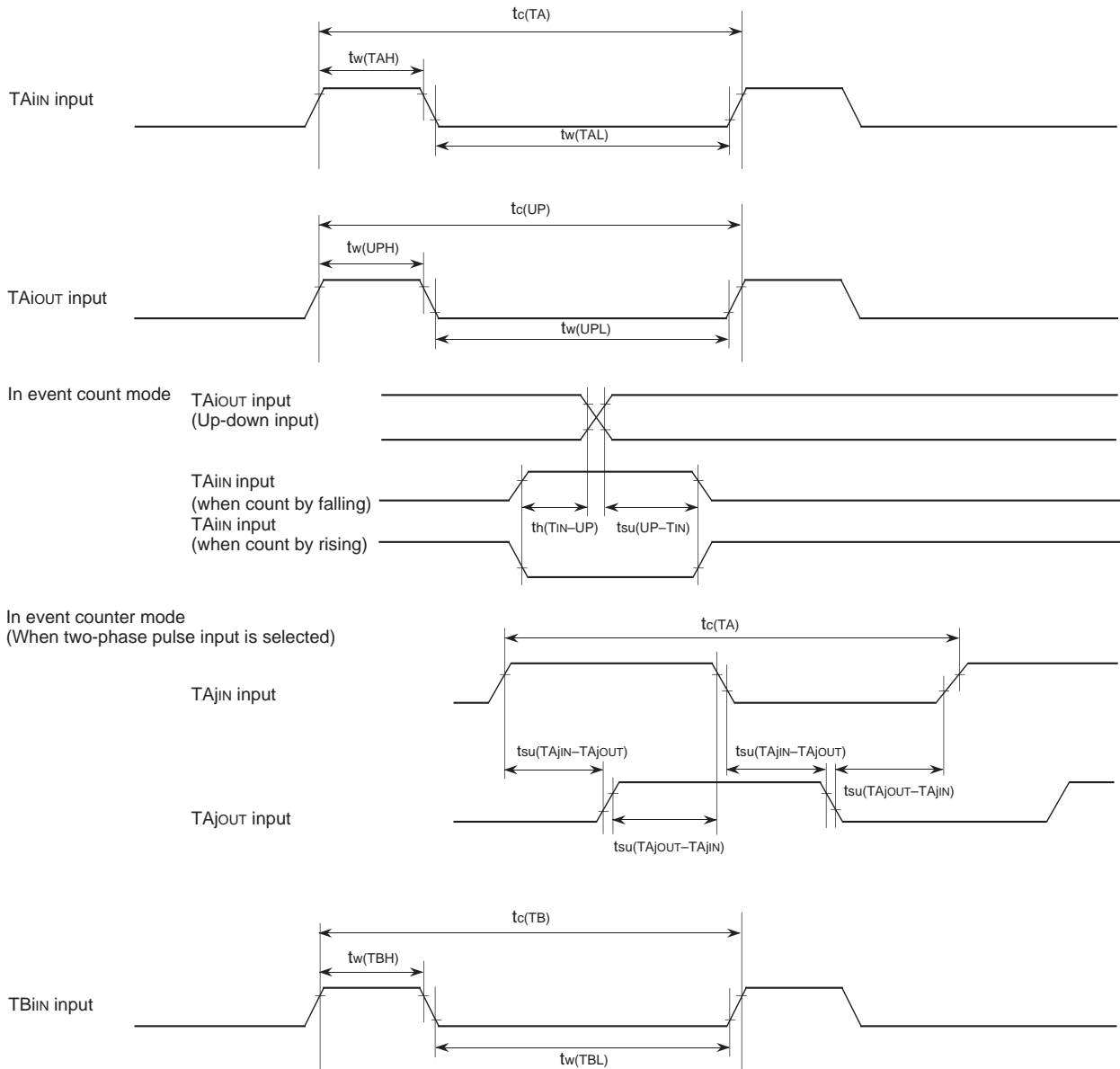
\bar{E}

Port Pi output
(i = 0 - 10)

Port Pi input
(i = 0 - 8, 10)



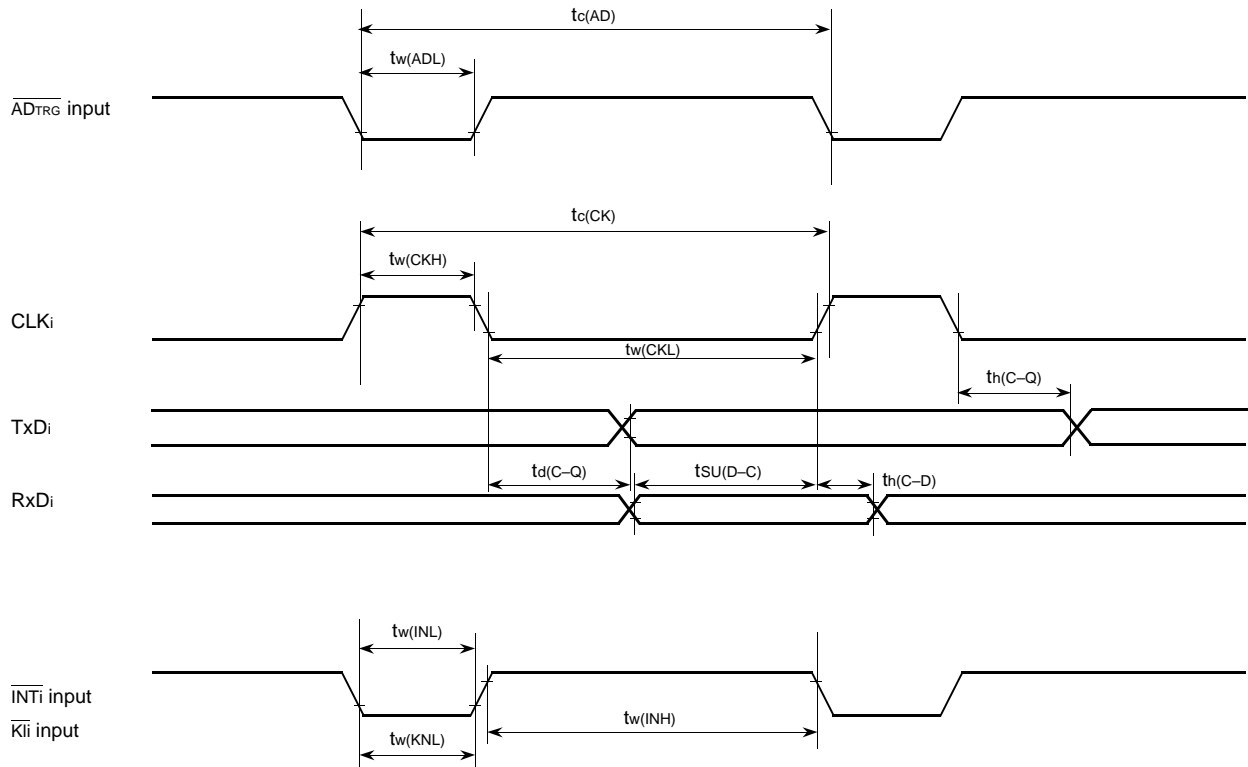
PRELIMINARY
 Notice: This is not a final specification.
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PRELIMINARY
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 Some parametric limits are subject to change.

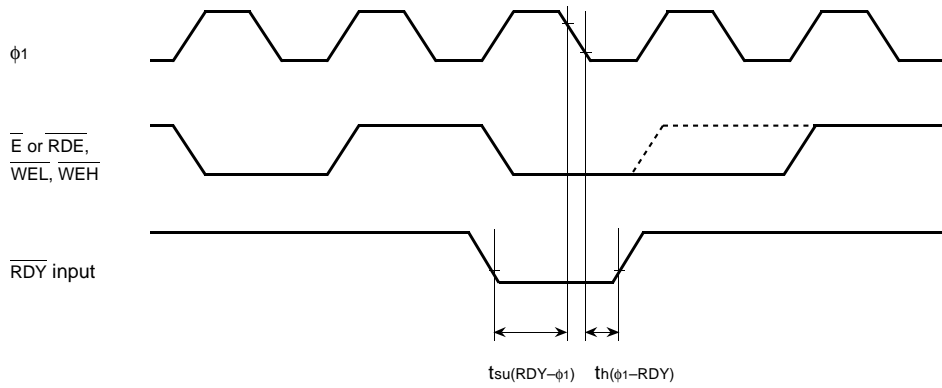
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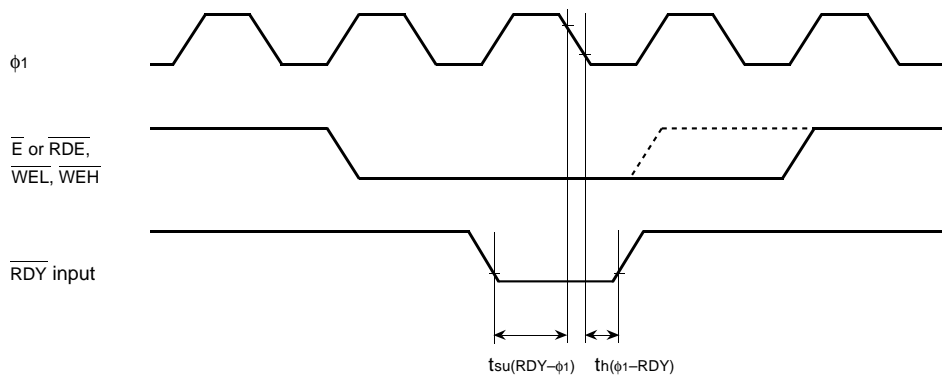


PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

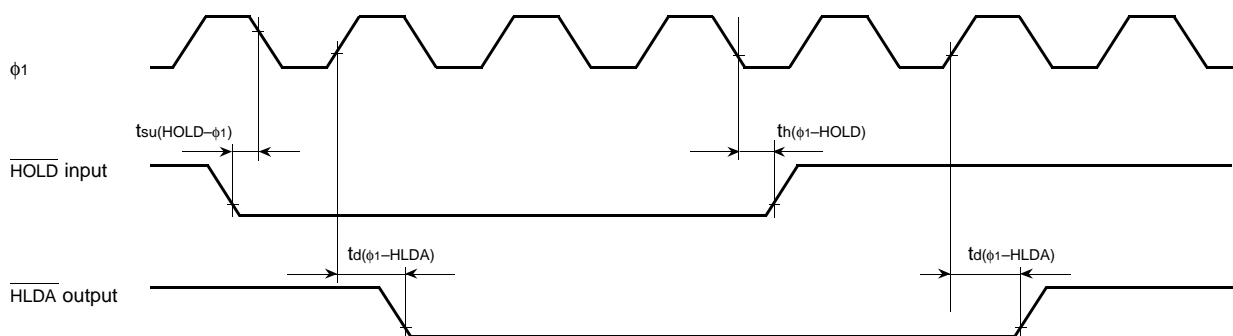
Memory expansion mode and microprocessor mode
 (When wait bit = "1")



(When wait bit = "0")



(When wait bit = "1" or "0" in common)



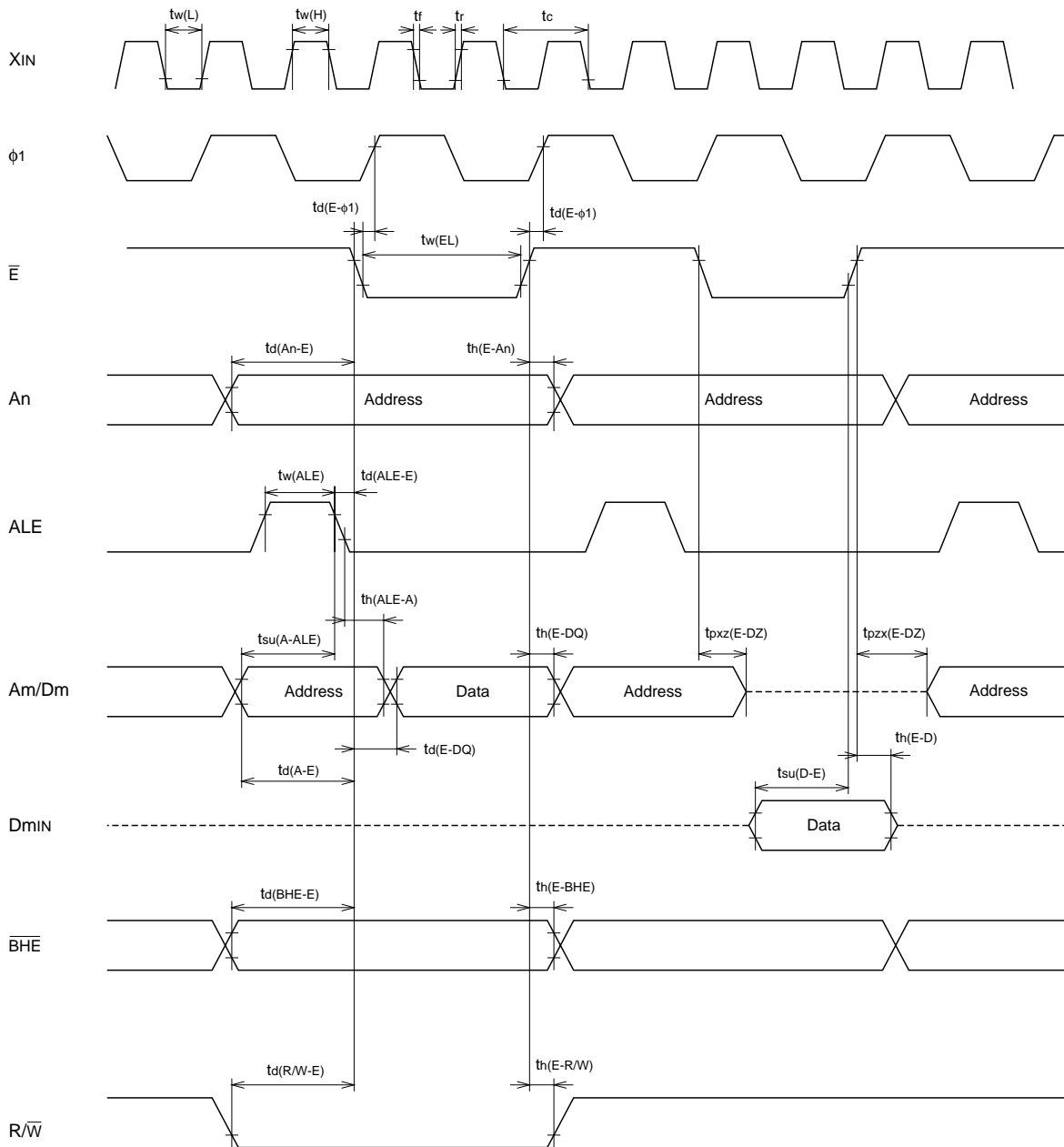
- Test conditions
- $V_{CC} = 5\text{ V} \pm 10\%$
 - Input timing voltage : $V_{IL} = 1.0\text{ V}$, $V_{IH} = 4.0\text{ V}$
 - Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

[External bus mode A]

Memory expansion mode and microprocessor mode

(No wait : When wait bit = "1")



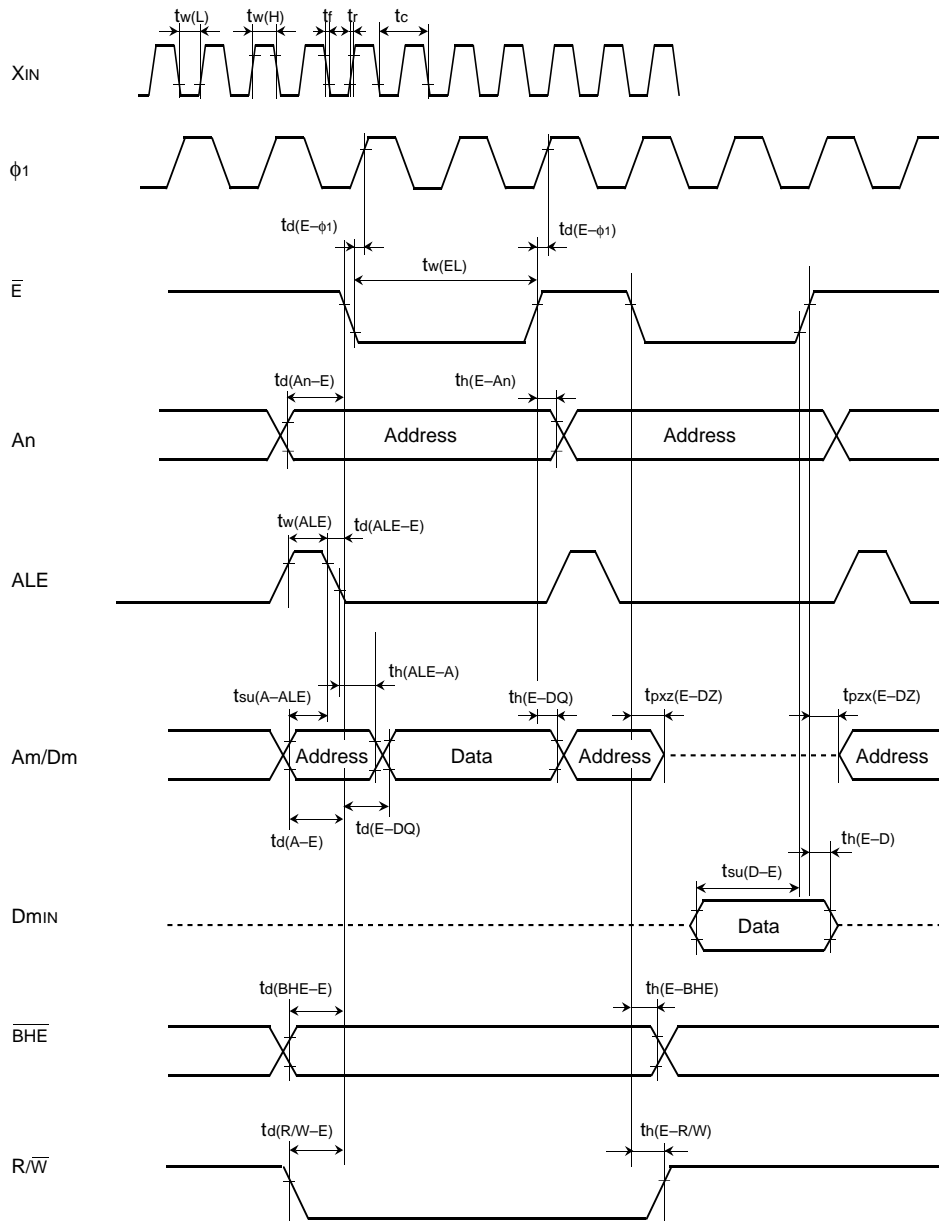
Test conditions

- $V_{CC} = 5 V \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8 V$, $V_{OH} = 2.0 V$
- Data input D_{min} : $V_{IL} = 0.8 V$, $V_{IH} = 2.5 V$

[External bus mode A]

Memory expansion mode and microprocessor mode

(Wait 1 : The external area is accessed when wait bit = "0" and wait selection = "1".)



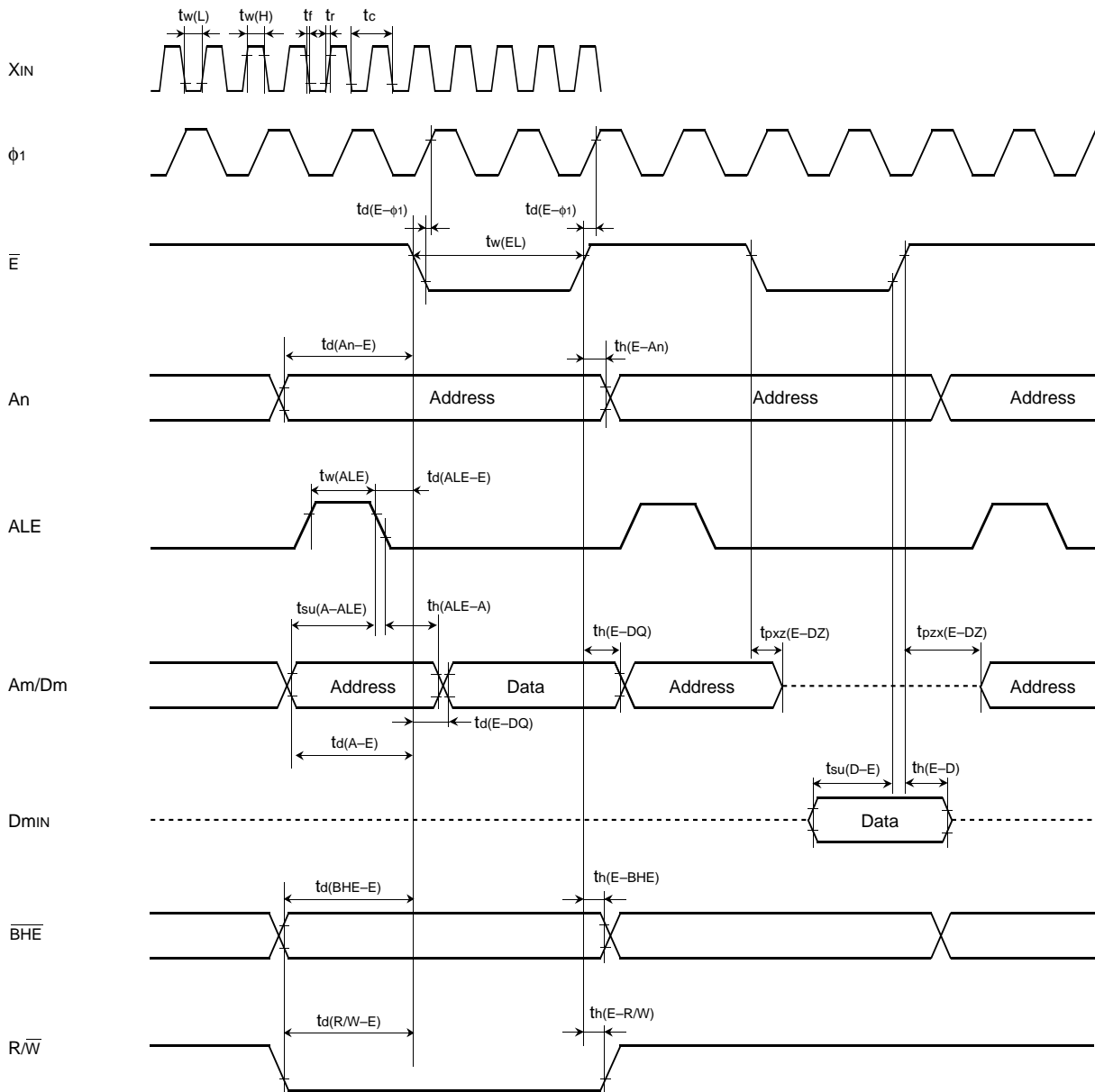
Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{min} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

[External bus mode A]

Memory expansion mode and microprocessor mode

(Wait 0 : The external memory area is accessed when wait bit = "0" and wait selection bit = "0".)



Test conditions

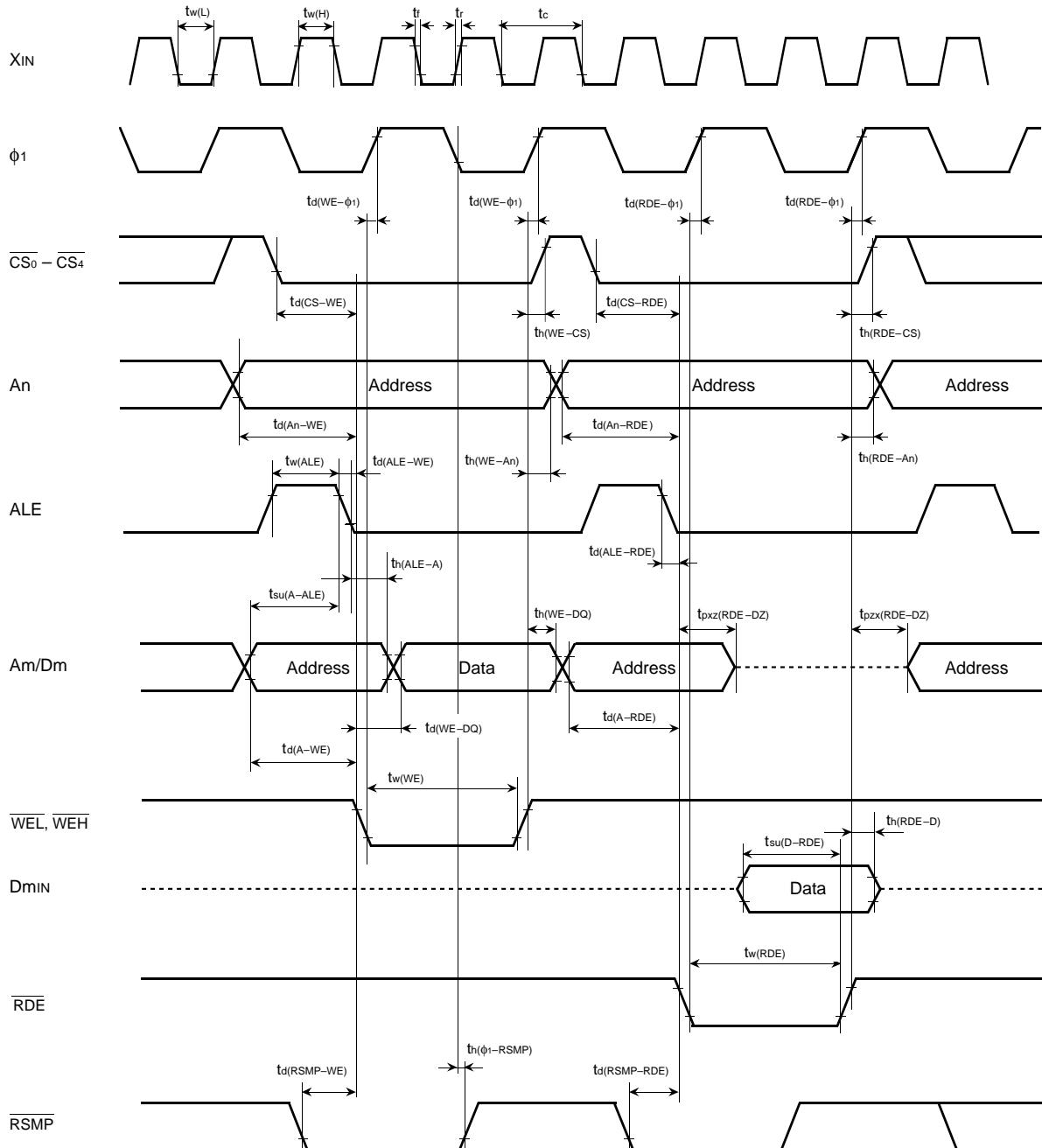
- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{min} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

[External bus mode B]

Memory expansion mode and microprocessor mode

(No wait : When wait bit = "1")



Test conditions

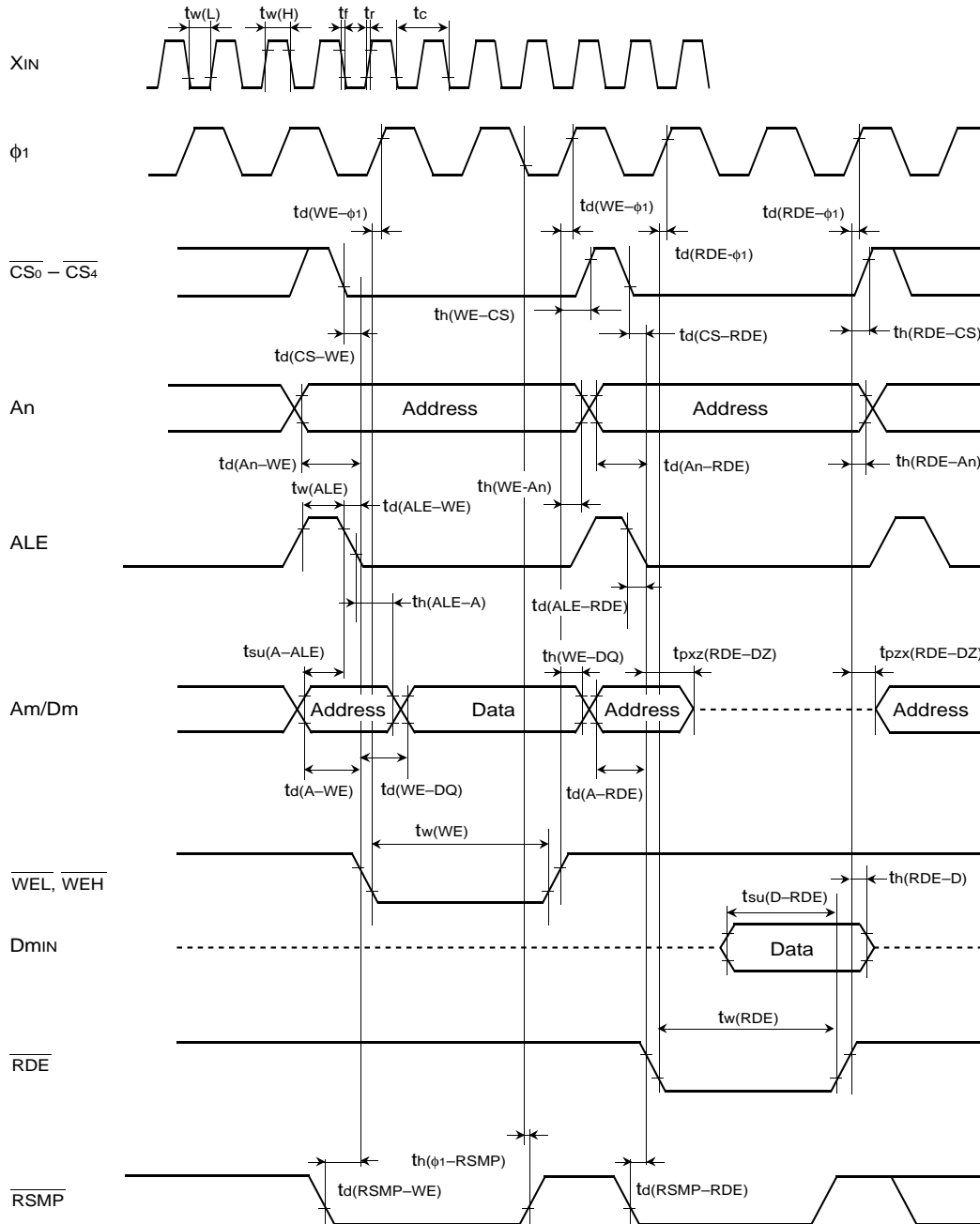
- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{min} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

[External bus mode B]

Memory expansion mode and microprocessor mode

(Wait 1 : The external area is accessed when wait bit = "0" and wait selection bit = "1".)



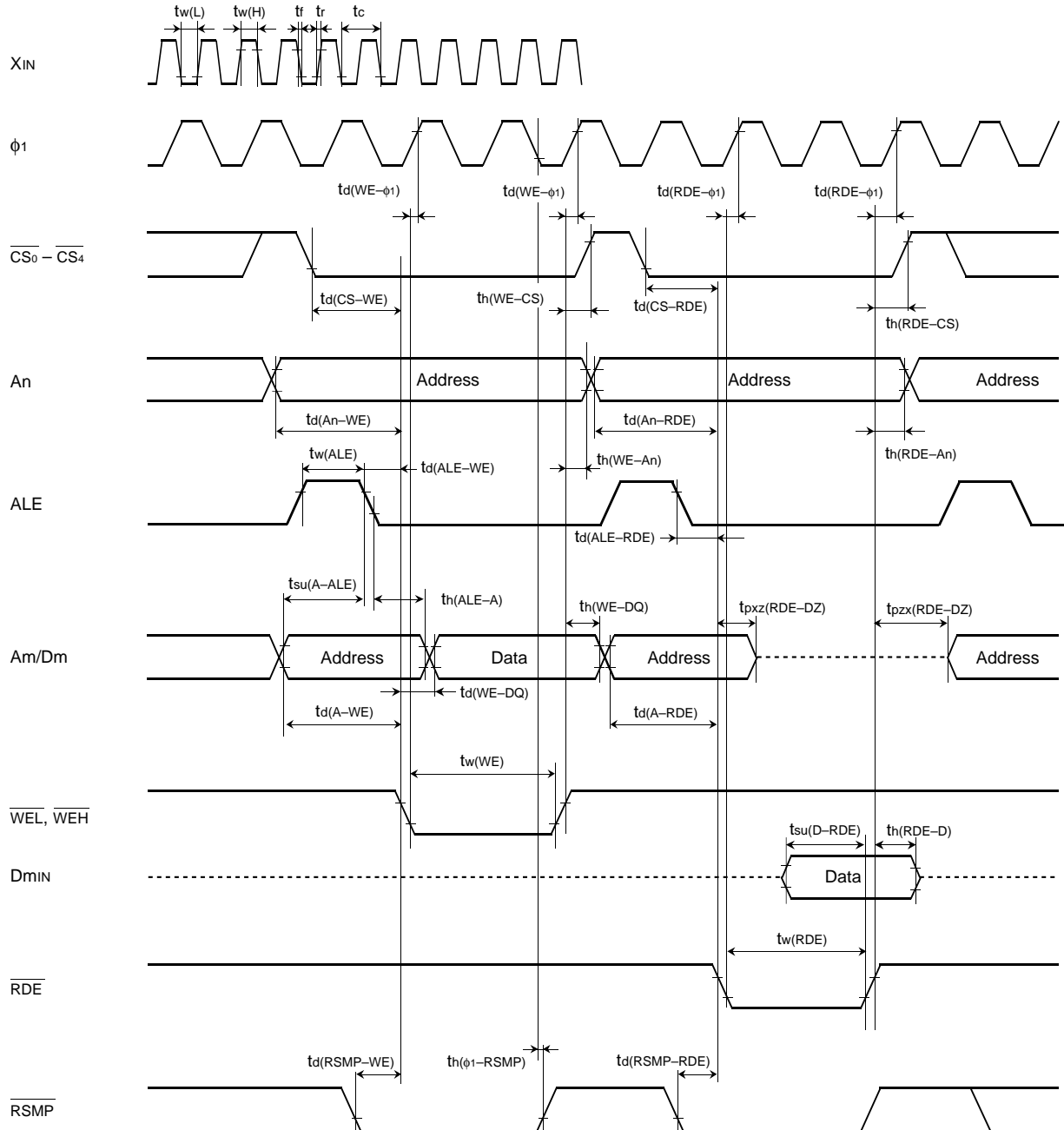
Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{MIN} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

[External bus mode B]

Memory expansion mode and microprocessor mode

(Wait 0 : The external memory area is accessed when wait bit = "0" and wait selection bit = "1".)



Test conditions

- $V_{CC} = 5 V \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8 V$, $V_{OH} = 2.0 V$
- Data input Dmin : $V_{IL} = 0.8 V$, $V_{IH} = 2.5 V$

PRELIMINARY
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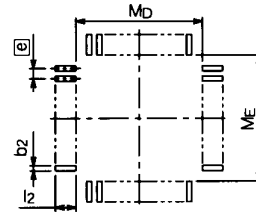
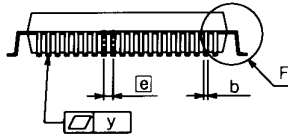
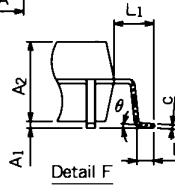
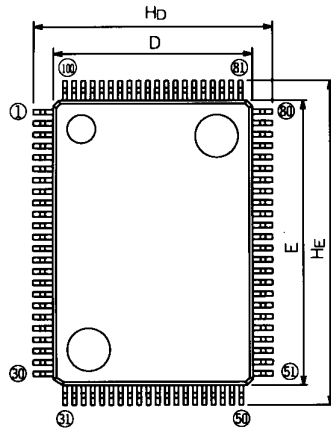
PACKAGE OUTLINE

100P6S-A

Plastic 100pin 14x20mm body QFP

EIAJ Package Code	JEDEC Code	Weight (g)	Lead Material
QFP100-P-1420-0.65	-	1.58	Alloy 42

Scale :



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	3.05
A ₁	0	0.1	0.2
A ₂	-	2.8	-
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
ⓐ	-	0.65	-
H _b	16.5	16.8	17.1
H _E	22.5	22.8	23.1
L	0.4	0.6	0.8
L ₁	-	1.4	-
y	-	-	0.1
θ	0°	-	10°
b ₂	-	0.35	-
l ₂	1.3	-	-
M ₀	-	14.6	-
M _E	-	20.6	-

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