

***8/16-bit Data Bus  
Static RAM Card***

**MF38M1-LCDAGXX  
MF38M1-LSDAGXX**

Connector Type

***Two-piece 68-pin***

**DESCRIPTION**

Mitsubishi's Static RAM cards provide large memory capacities on a device approximately the size of a credit card(85.6mm×54mm×5.0mm). The cards use an 8/16 bit data bus.The devices use a replaceable lithium battery to maintain data.Available in 8Mbyte capacities, Mitsubishi's Static RAM cards are available with a 68-pin, two-piece connector.

- Electrostatic discharge protection to 15kV
- Buffered interface
- 68pin connector
- 8-bit and 16-bit data width
- Write protect switch
- Battery voltage pin
- LS Type Wide Range operating temperature (Ta= -20 to 70°C)

**FEATURES**

- Uses TSOP (Thin Small Outline Package) to achieve very high memory density coupled with high reliability, without enlarging card size.

**APPLICATIONS**

- Office automation
- Data Communication
- Computers
- Industrial
- Telecommunications
- Consumer

**PRODUCT LIST**

Item Type name	Memory capacity	Data Bus width(bits)	Attribute memory	Auxiliary battery	Memory organization	Outline drawing	Main battery holder
MF38M1-LCDAGXX	8MB	8/16	NO	NO	4M bit SRAM×16	68P-010	Screw type
MF38M1-LSDAGXX	8MB	8/16	NO	NO	4M bit SRAM×16	68P-010	Screw type

STATIC RAM CARDS

**PIN ASSIGNMENT**

**Two-Piece Type (68-pin)**

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	35	GND	Ground
2	D3	Data I/O	36	CD1#	Card detect 1
3	D4		37	D11	Data I/O
4	D5		38	D12	
5	D6		39	D13	
6	D7		40	D14	
7	CE1#	Card enable 1	41	D15	
8	A10	Address input	42	CE2#	Card enable 2
9	OE#	Output enable	43	NC	No connection
10	A11	Address input	44	NC	
11	A9		45	NC	
12	A8		46	A17	Address input
13	A13		47	A18	
14	A14		48	A19	
15	WE#	Write enable	49	A20	
16	NC	No connection	50	A21	
17	Vcc	Power supply voltage	51	Vcc	Power supply voltage
18	NC	No connection	52	NC	No connection
19	A16	Address input	53	A22	Address input
20	A15		54	NC	No connection
21	A12		55	NC	
22	A7		56	NC	
23	A6		57	NC	
24	A5		58	NC	
25	A4		59	NC	
26	A3		60	NC	
27	A2		61	REG#	REG function
28	A1		62	BVD2	Battery voltage detect 2
29	A0	63	BVD1	Battery voltage detect 1	
30	D0	Data I/O	64	D8	Data I/O
31	D1		65	D9	
32	D2		66	D10	
33	WP	Write protect	67	CD2#	Card detect 2
34	GND	Ground	68	GND	Ground

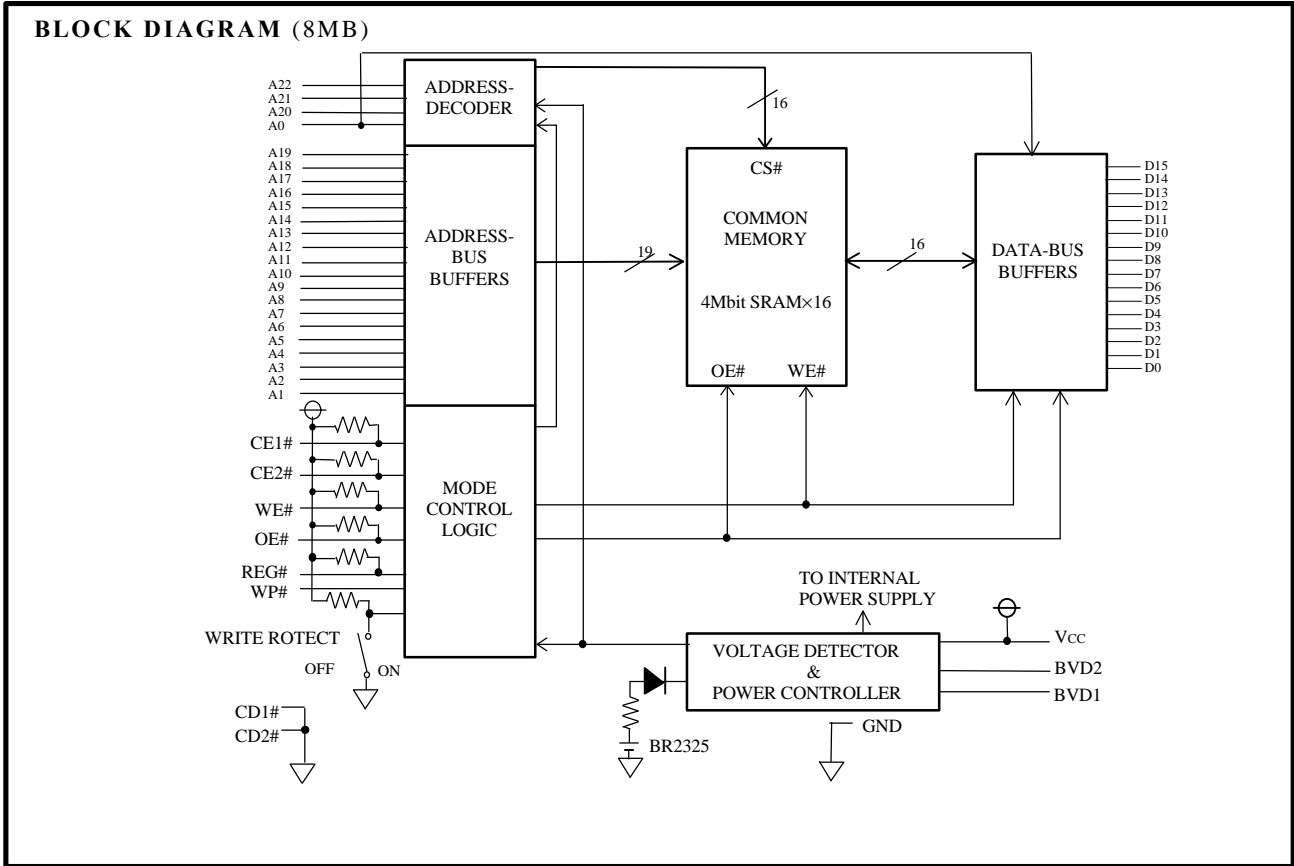
**WRITE PROTECT MODE (WP)**

When the write protect switch is switched on, this card goes into a write protect mode that can read but not write data.

In this mode, WP pin becomes “H” level.

At the shipment the write protect switch is switched off (Normal mode : The card can be written ; WP pin indicates “L” level).

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**FUNCTION TABLE**

Mode	REG#	CE1#	CE2#	OE#	WE#	A0	I/O (D15~D8)	I/O (D7~D0)	Icc
Standby	X	H	H	X	X	X	High-impedance	High-impedance	Standby
Read A (16bit) common	H	L	L	L	H	X	Odd Byte Data out	Even Byte Data out	Active
Write A (16bit) common	H	L	L	H	L	X	Odd Byte Data in	Even Byte Data in	Active
Read B (8bit) common	H	L	H	L	H	L	High-impedance	Even Byte Data out	Active
	H	L	H	L	H	H	High-impedance	Odd Byte Data out	Active
Write B (8bit) common	H	L	H	H	L	L	High-impedance	Even Byte Data in	Active
	H	L	H	H	L	H	High-impedance	Odd Byte Data in	Active
Read C (8bit) common	H	H	L	L	H	X	Odd Byte Data out	High-impedance	Active
Write C (8bit) common	H	H	L	H	L	X	Odd Byte Data in	High-impedance	Active
Output disable	X	X	X	H	H	X	High-impedance	High-impedance	Active
Read A (16bit) attribute	L	L	L	L	H	X	Data out (unknown)	Data out (FFh)	Active
Read B (8bit) attribute	L	L	H	L	H	L	High-impedance	Data out (FFh)	Active
	L	L	H	L	H	H	High-impedance	Data out (unknown)	Active
Read C (8bit) attribute	L	H	L	L	H	X	Data out (unknown)	High-impedance	Active

Note 1 : H=VIH, L=VIL, X=VIH or VIL

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage	With respect to GND	-0.3~6.0	V
V <sub>i</sub>	Input voltage		-0.3~V <sub>CC</sub> +0.3	V
V <sub>o</sub>	Output voltage		0~V <sub>CC</sub>	V
T <sub>opr1</sub>	Operating temperature 1	Read, Write, Operation	LC series 0~70	°C
			LS series -20~70	°C
T <sub>opr2</sub>	Operating temperature 2	Data retention	LC series 0~70	°C
			LS series -20~70	°C
T <sub>stg</sub>	Storage temperature		-30~80	°C

RECOMMENDED OPERATING CONDITIONS (LC series Ta= 0~55°C, unless otherwise noted)  
(LS series Ta=-20~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V <sub>CC</sub>	V <sub>CC</sub> supply voltage	4.50	5.0	5.25	V
GND	System ground		0		V
V <sub>IH</sub>	High input voltage	3.5		V <sub>CC</sub>	V
V <sub>IL</sub>	Low input voltage	0		0.8	V

ELECTRICAL CHARACTERISTICS (LC series Ta= 0~55°C, V<sub>CC</sub>=4.50~5.25V, unless otherwise noted)  
(LS series Ta=-20~70°C, V<sub>CC</sub>=4.50~5.25V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V <sub>OH</sub>	High output voltage	I <sub>OH</sub> =-1.0mA, Other outputs	2.4			V
V <sub>OL</sub>	Low output voltage	I <sub>OL</sub> =2mA			0.4	V
I <sub>IH</sub>	High input current	V <sub>I</sub> =V <sub>CC</sub> V			10	μA
I <sub>IL</sub>	Low input current	V <sub>I</sub> =0V CE1#, CE2#, WE#, OE#, REG#			-70	μA
					-10	
I <sub>OZH</sub>	High output current in off state	CE1#=CE2#=V <sub>IH</sub> or OE#=V <sub>IH</sub> WE#=V <sub>IH</sub> , V <sub>O</sub> =V <sub>CC</sub>			10	μA
I <sub>OZL</sub>	Low output current in off state	CE1#=CE2#=V <sub>IH</sub> or OE#=V <sub>IH</sub> WE#=V <sub>IH</sub> , V <sub>O</sub> =0V			-10	μA
I <sub>CC</sub> 1 • 1	Active supply current 1	CE#=V <sub>IL</sub> , other inputs V <sub>IH</sub> or V <sub>IL</sub> , Outputs=open	16bit		280	mA
			8bit		200	
I <sub>CC</sub> 1 • 2	Active supply current 2	CE# ≤ 0.2V, other inputs ≤ 0.2V or ≥ V <sub>CC</sub> -0.2V, Outputs=open	16bit		270	mA
			8bit		190	
I <sub>CC</sub> 2 • 1	Standby supply current 1	CE1#=CE2#=V <sub>IH</sub> other inputs=V <sub>IH</sub> or V <sub>IL</sub>			10	mA
I <sub>CC</sub> 2 • 2	Standby supply current 2	CE1#=CE2# ≥ V <sub>CC</sub> -0.2V other inputs ≤ 0.2V or ≥ V <sub>CC</sub> -0.2V			1	mA
VBDET1	Battery detect reference voltage 1*	V <sub>CC</sub> =5V, Ta=25°C	2.27	2.37	2.47	V
VBDET2	Battery detect reference voltage 2*	V <sub>CC</sub> =5V, Ta=25°C	2.55	2.65	2.75	V

Note 2 : Currents flowing into the IC are taken as positive (unsigned).

3 : Typical values are measured at V<sub>CC</sub>=5V, Ta=25°C.

\*Pin asserted when battery voltage drops below specified level.

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CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
C <sub>I</sub>	Input capacitance	V <sub>I</sub> =GND, V <sub>I</sub> =25mVrms f=1 MHz, T <sub>a</sub> =25°C			30	pF
C <sub>O</sub>	Output capacitance	V <sub>O</sub> =GND, V <sub>O</sub> =25mVrms f=1 MHz, T <sub>a</sub> =25°C			20	pF

Note 4 : These parameters are not 100% tested.

SWITCHING CHARACTERISTICS

**Read Cycle** (LC series T<sub>a</sub>= 0~55°C, V<sub>CC</sub>=4.50~5.25V, unless otherwise noted)  
(LS series T<sub>a</sub>=-20~70°C, V<sub>CC</sub>=4.50~5.25V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t <sub>CR</sub>	Read cycle time	200			ns
t <sub>a(A)</sub>	Address access time			200	ns
t <sub>a(CE)</sub>	Card enable access time			200	ns
t <sub>a(OE)</sub>	Output enable access time			100	ns
t <sub>dis(CE)</sub>	Output disable time (from CE#)			90	ns
t <sub>dis(OE)</sub>	Output disable time (from OE#)			90	ns
t <sub>en(CE)</sub>	Output enable time (from CE#)	5			ns
t <sub>en(OE)</sub>	Output enable time (from OE#)	5			ns
t <sub>v(A)</sub>	Data valid time (after address change)	0			ns

TIMING REQUIREMENTS

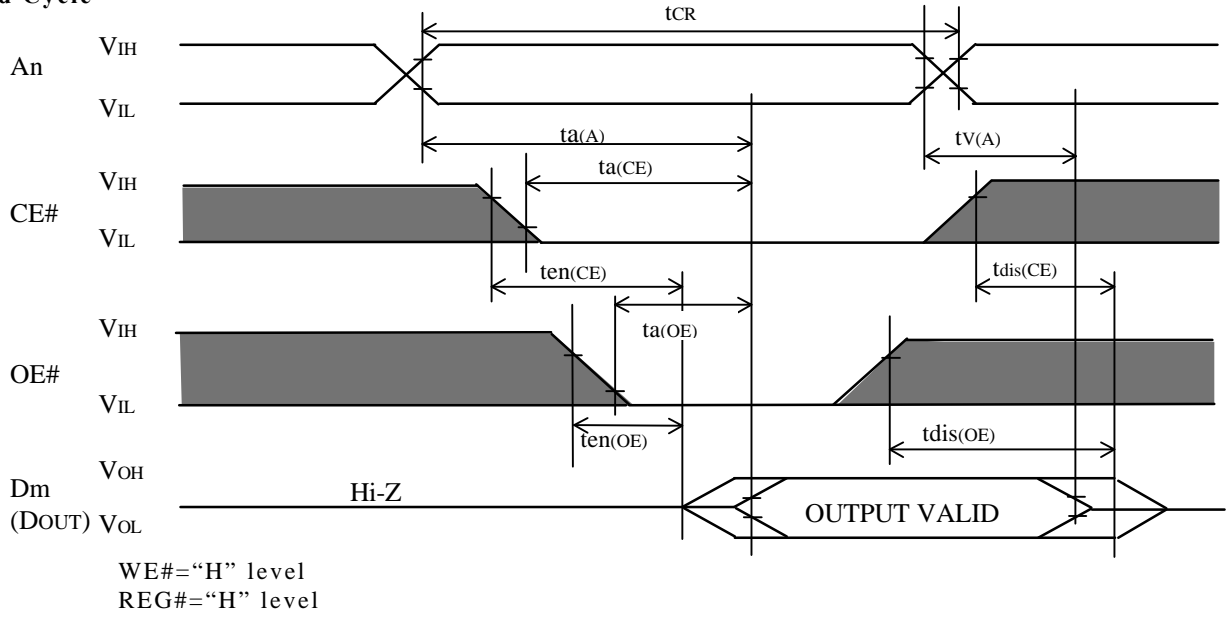
**Write Cycle**(LC series T<sub>a</sub>= 0~55°C, V<sub>CC</sub>=4.50~5.25V, unless otherwise noted)  
(LS series T<sub>a</sub>=-20~70°C, V<sub>CC</sub>=4.50~5.25V, unless otherwise noted)


Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t <sub>CW</sub>	Write cycle time	200			ns
t <sub>w(WE)</sub>	Write pulse width	120			ns
t <sub>su(A)</sub>	Address set up time	20			ns
t <sub>su(A-WEH)</sub>	Address set up time with respect to WE# high	140			ns
t <sub>su(CE-WEH)</sub>	Card enable set up time with respect to WE# high	140			ns
t <sub>su(D-WEH)</sub>	Data set up time with respect to WE# high	60			ns
t <sub>h(D)</sub>	Data hold time	30			ns
t <sub>rec(WE)</sub>	Write recovery time	30			ns
t <sub>dis(WE)</sub>	Output disable time (from WE#)			90	ns
t <sub>dis(OE)</sub>	Output disable time (from OE#)			90	ns
t <sub>en(WE)</sub>	Output enable time (from WE#)	5			ns
t <sub>en(OE)</sub>	Output enable time (from OE#)	5			ns
t <sub>su(OE-WE)</sub>	OE# set up time with respect to WE# low	10			ns
t <sub>h(OE-WE)</sub>	OE# hold time with respect to WE# high	10			ns

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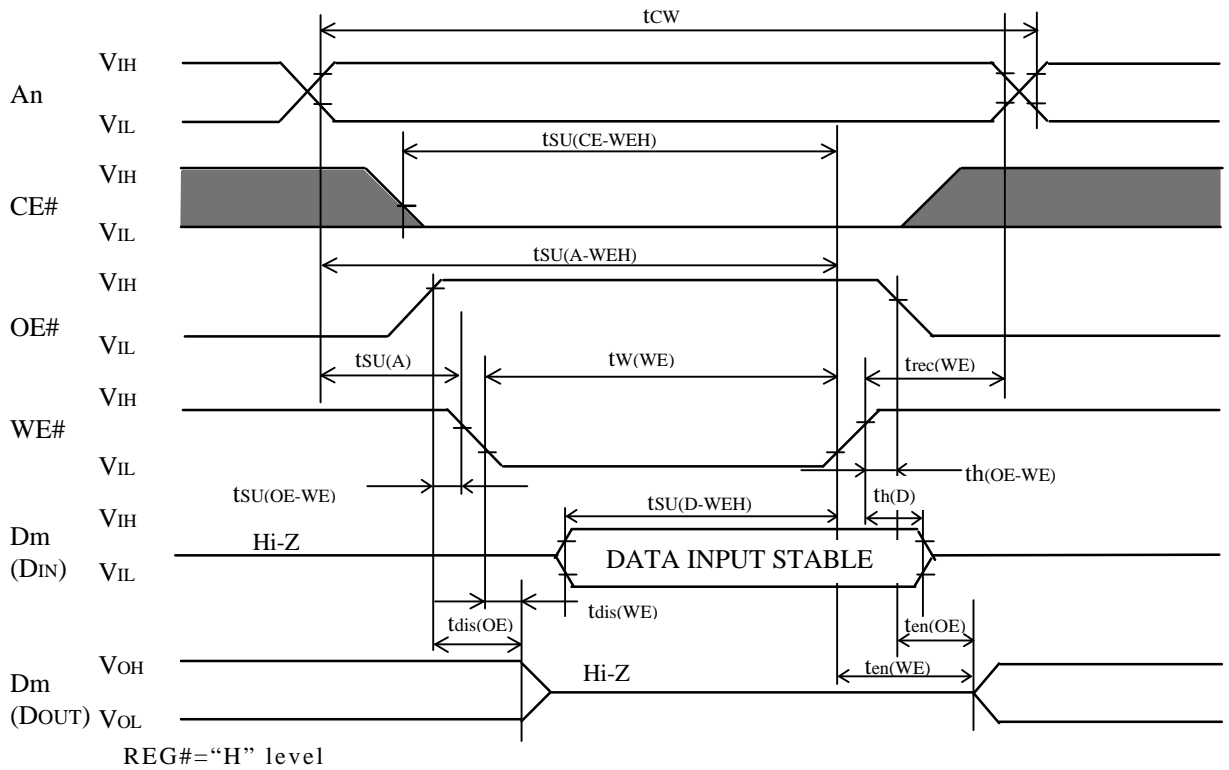
TIMING DIAGRAM

Read Cycle



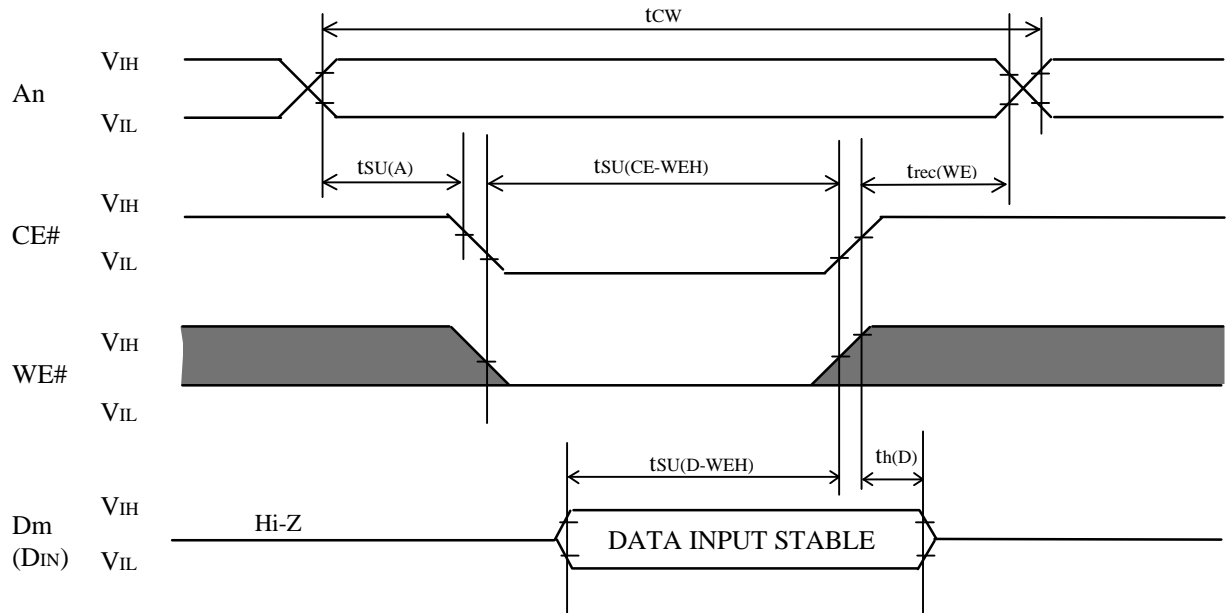
Note 5 :  Indicates the don't care input

Write Cycle (WE# control)



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Write Cycle (CE# control)



OE#="H" level  
REG#="H" level

SWITCHING CHARACTERISTICS (Attribute)

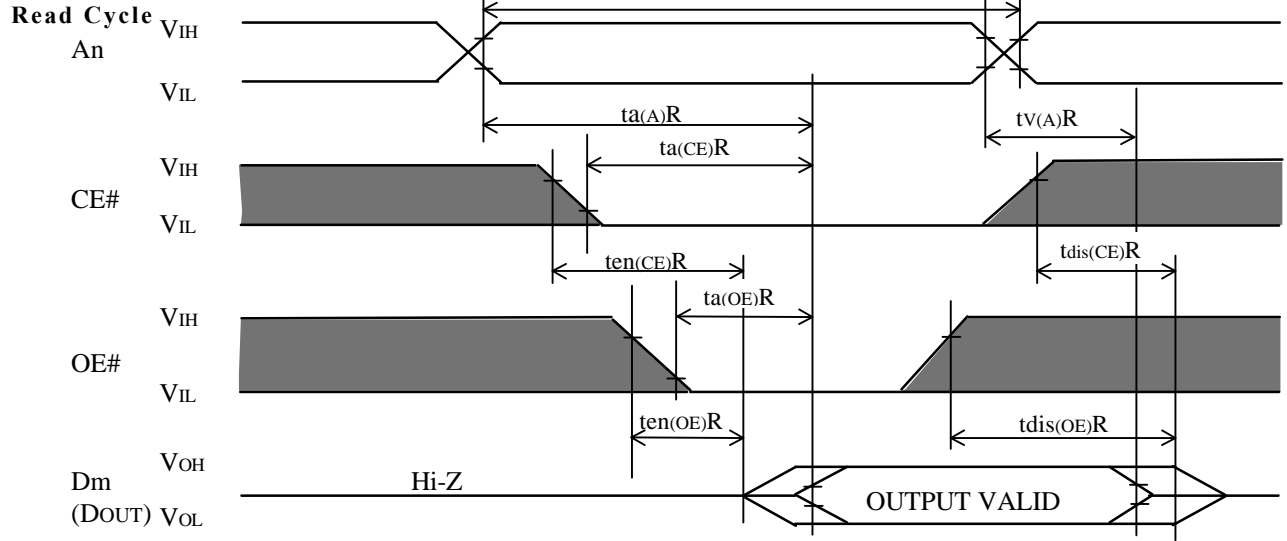
Read Cycle (LC series: Ta=0~55°C, Vcc=4.50~5.25V, unless otherwise noted)

(LS series Ta=-20~70°C, Vcc=4.50~5.25V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tCR	Read cycle time	300			ns
ta(A)R	Address access time			300	ns
ta(CE)R	Card enable access time			300	ns
ta(OE)R	Output enable access time			150	ns
tdis(CE)R	Output disable time (from CE#)			100	ns
tdis(OE)R	Output disable time (from OE#)			100	ns
ten(CE)R	Output enable time (from CE#)	5			ns
ten(OE)R	Output enable time (from OE#)	5			ns
tV(A)R	Data valid time after address change	0			ns

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TIMING DIAGRAM (Attribute)



WE#="H" level  
REG#="L" level

Note 6 : Test Conditions

Input pulse levels :  $V_{IL}=0.4V$ ,  $V_{IH}=4.0V$

Input pulse rise, fall time :  $t_r=t_f=10ns$

Reference voltage

Input :  $V_{IL}=0.8V$ ,  $V_{IH}=3.5V$

Output :  $V_{OL}=0.8V$ ,  $V_{OH}=3.0V$

(ten and tdis are measured when output voltage is  $\pm 500mV$  from steady state. )

Load : 100pF+1 TTL gate

5pF+1 TTL gate (at ten and tdis measuring)

7 : Writing is executed in overlap of CE# and WE# are "L" level. (only for Common Memory)

8 : Don't apply inverted phase signal externally when Dm pin is in output mode.

9 : CE# is indicated as follows:

Read A/Write A : CE#=CE1#=CE2#

Read B/Write B : CE#=CE1#, CE2#="H" level

Read C/Write C : CE#=CE2#, CE1#="H" level



STATIC RAM CARDS

**ELECTRICAL CHARACTERISTICS**

**BATTERY BACKUP** (LC series Ta= 0~55°C, unless otherwise noted)  
 (LS series Ta=-20~70°C, unless otherwise noted)

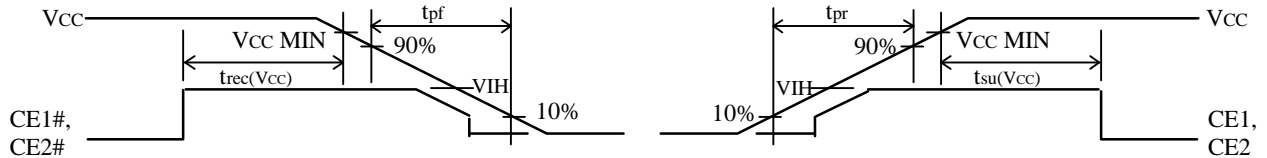
Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
VBATT	Back-up enable battery voltage	All pins open	2.6			V
VI(CE)	Card enable voltage	2.4V ≤ VCC ≤ 5.25V	2.4			V
		0V ≤ VCC < 2.4V	VCC-0.1	VCC	VCC+0.1	
Icc(BUP)	Battery back-up supply current	All pins open, VBATT=3V, Ta=25°C			17	μA
Icc(BUP)	Battery back-up supply current	All pins open, VBATT=3V			400	μA

**TIMING REQUIREMENTS** (LC series Ta= 0~55°C, unless otherwise noted)  
 (LS series Ta=-20~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tpr	Power supply rise time	0.1		300	ms
tpf	Power supply fall time	3		300	ms
tsu(VCC)	Setup time at power on	20			ms
trec(VCC)	Recovery time at power off	1000			ns

**CARD INSERTION/REMOVAL TIMING DIAGRAM**

VCC MIN means Minimum Operating Voltage=4.50V.



Note 10: When the card is holding valuable data, the battery must not be removed unless VCC is present.

**BATTERY SPECIFICATIONS**

A replaceable battery (type BR2325) with a capacity of 165mAH is used:  
 Estimated battery life when the card is left continuously.

MF38M1-LC/LSDAGXX	1.0years
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Conditions

Temperature : 25°C  
 Humidity : 60% RH