SDRAM (Rev. 0.3)

Feb '97 Preliminary

M5M4V4S40CTP-12, -15

4M (2-BANK x 131072-WORD x 16-BIT) Synchronous DRAM

PRELIMINARY

Some of contents are described for general products and are subject to change without notice.

DESCRIPTION

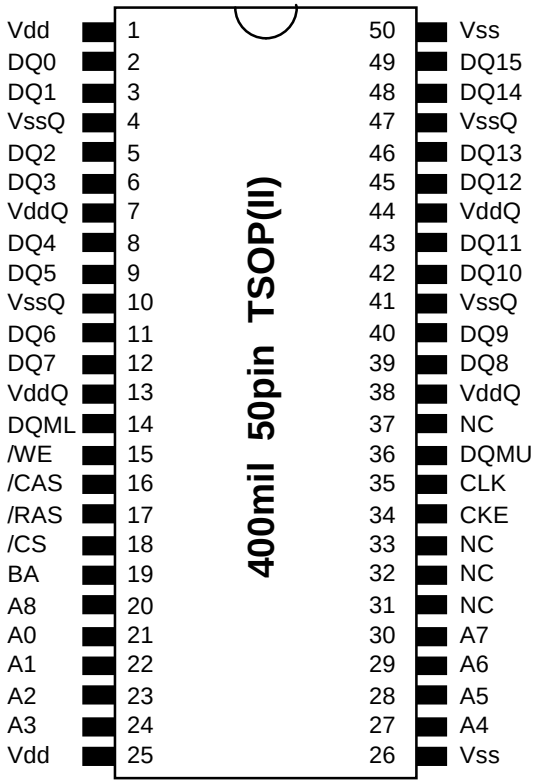
The M5M4V4S40CTP is a 2-bank x 131,072-word x 16-bit Synchronous DRAM, with LVTTL interface. All inputs and outputs are referenced to the rising edge of CLK. The M5M4V4S40CTP achieves very high speed data rates up to 83MHz, and is suitable for main memory or graphic memory in computer systems.

FEATURES

- Single 3.3v±0.3v power supply
- Clock frequency 83MHz / 67MHz
- Fully synchronous operation referenced to clock rising edge
- Dual bank operation controlled by BA(Bank Address)
- /CAS latency- 1/2/3 (programmable)
- Burst length- 1/2/4/8/FP (programmable)
- Sequential and interleave burst (programmable)
- Byte control by DQMU and DQML
- Random column access
- Auto precharge / All bank precharge controlled by A8
- Auto and self refresh
- 1024 refresh cycles /16.4ms
- LVTTL Interface
- 400-mil, 50-pin Thin Small Outline Package (TSOP II) with 0.8mm lead pitch

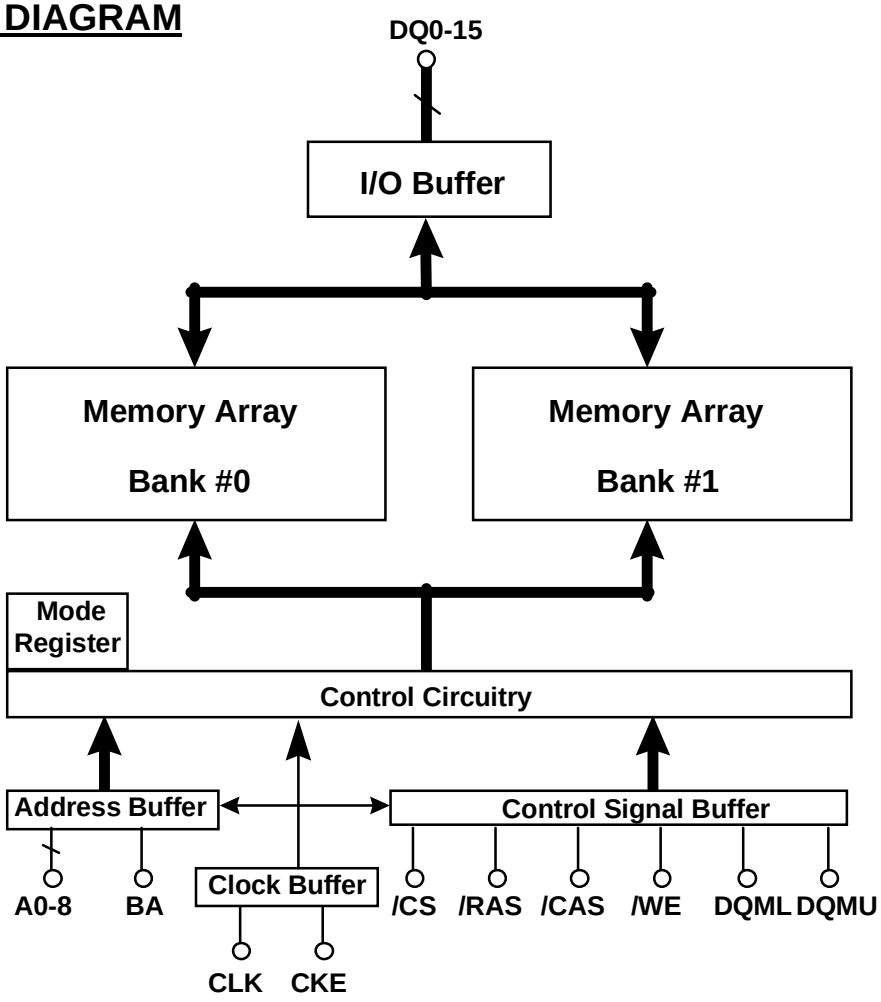
	Max. Frequency	CLK Access Time
M5M4V4S40CTP-12	83MHz	8ns
M5M4V4S40CTP-15	67MHz	9ns

PIN CONFIGURATION (TOP VIEW)



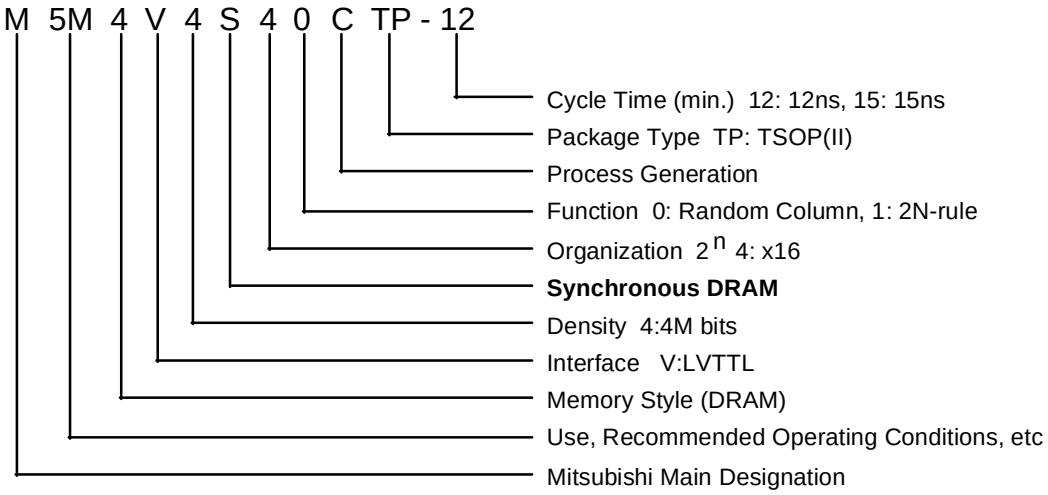
CLK : Master Clock
CKE : Clock Enable
/CS : Chip Select
/RAS : Row Address Strobe
/CAS : Column Address Strobe
/WE : Write Enable
DQ0-15 : Data I/O
DQMU : Upper Output Disable/ Write Mask
DQML : Lower Output Disable/ Write Mask
A0-8 : Address Input
BA : Bank Address
Vdd : Power Supply
VddQ : Power Supply for Output
Vss : Ground
VssQ : Ground for Output

BLOCK DIAGRAM



Type Designation Code

These rules are only applied to the Synchronous DRAM family.



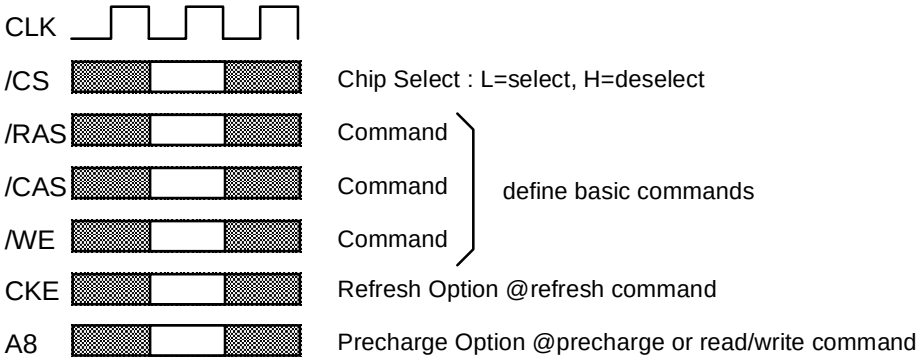
PIN FUNCTION

CLK	Input	Master Clock: All other inputs are referenced to the rising edge of CLK.
CKE	Input	Clock Enable: CKE controls the internal clock. When CKE is low, the internal clock for the following cycle is disabled. CKE is also used to select auto and self refresh. After self-refresh mode is started, CKE acts as an asynchronous input to maintain and exit the mode.
/CS	Input	Chip Select: When /CS is high, all commands are inhibited.
/RAS, /CAS, /WE	Input	/RAS, /CAS, and /WE are used to define basic commands.
A0-8	Input	A0-8 specify the Row and Column addresses within the selected bank. The Row Address is set by A0-8 and the Column Address is set by A0-7. A8 is also used to indicate the precharge option. When A8 is high during read or write command, an auto precharge is performed. When A8 is high during a precharge command, both banks are precharged.
BA	Input	Bank Address: BA is not simply A9. BA specifies the bank to which a command is applied. BA must be set during the ACT, PRE, READ, and WRITE commands.
DQ0-15	Input / Output	Data In and data out are referenced to the rising edge of CLK.
DQML	Input	Lower Din(0-7) Mask; Lower Dout(0-7) Disable; When DQML is high during burst write Din(0-7) for the current cycle is masked. When DQML is high during burst read Dout(0-7) is disabled two cycles later.
DQMU	Input	Upper Din(8-15) Mask; Upper Dout(8-15) Disable; When DQMU is high during burst write Din(8-15) for the current cycle is masked. When DQMU is high during burst read Dout(8-15) is disabled two cycles later.
Vdd, Vss	Power Supply	Power Supply for the memory array and peripheral circuitry.
VddQ, VssQ	Power Supply	Power Supply for the output buffers only.

BASIC FUNCTIONS

The M5M4V4S40CTP has the following basic functions, bank (row) activate, burst read/write, bank (row) precharge, and auto/self refresh. Each command is defined by the control signals (/RAS, /CAS and /WE) at the rising edge of CLK. The inputs /CS ,CKE and A8 are used for chip select, refresh options, and precharge options, respectively.

Please see the command truth table for detailed definitions.



Activate (ACT) [/RAS =L, /CAS =/WE =H]

The ACT command activates a row in an idle bank. The bank address, BA, is used to select which of the two banks will be activated.

Read (READ) [/RAS =H, /CAS =L, /WE =H]

The READ command starts burst read from the active bank indicated by BA. The first output data appears after /CAS latency. If A8 =H when READ is issued the bank is automatically precharged after the last burst read (READA). *Note: READA is not valid for FP burst operations*.

Write (WRITE) [/RAS =H, /CAS =/WE =L]

The WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. If A8 =H when WRITE is issued the bank is automatically precharged after the last burst write (WRITEA). *Note: WRITEA is not valid for FP burst operations*.

Precharge (PRE) [/RAS =L, /CAS =H, /WE =L]

The PRE command deactivates the active bank indicated by BA. This command also terminates burst read and write operations. If A8 =H when PRE is issued both banks are automatically precharged (PREA).

Auto-Refresh (REFA) [/RAS =/CAS =L, /WE =CKE =H]

The REFA command starts an auto-refresh cycle. The refresh address, including the bank address, is generated internally. After this command, the banks are precharged automatically.

COMMAND TRUTH TABLE

COMMAND	MNEMONIC	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	BA	A8	A0-7
Deselect	DESEL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Row Address Entry & Bank Activate	ACT	H	X	L	L	H	H	V	V	V
Single Bank Precharge	PRE	H	X	L	L	H	L	V	L	X
Precharge All Banks	PREA	H	X	L	L	H	L	X	H	X
Column Address Entry & Write	WRITE	H	X	L	H	L	L	V	L	V
Column Address Entry & Write with Auto-Precharge	WRITEA	H	X	L	H	L	L	V	H	V
Column Address Entry & Read	READ	H	X	L	H	L	H	V	L	V
Column Address Entry & Read with Auto-Precharge	READA	H	X	L	H	L	H	V	H	V
Auto-Refresh	REFA	H	H	L	L	L	H	X	X	X
Self-Refresh Entry	REFS	H	L	L	L	L	H	X	X	X
Self-Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X
		L	H	L	H	H	H	X	X	X
Burst Terminate	TBST	H	X	L	H	H	L	X	X	X
Mode Register Set	MRS	H	X	L	L	L	L	V	L	V*1

H=High Level, L=Low Level, V=Valid, X=Don't Care, n=CLK cycle number

NOTE:
1. A7 =0, A0-A6 =Mode Address

FUNCTION TRUTH TABLE

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
IDLE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A8	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	Bank Active, Latch RA
	L	L	H	L	BA, A8	PRE / PREA	NOP*4
	L	L	L	H	X	REFA	Auto-Refresh*5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TBST	NOP
	L	H	L	H	BA, CA, A8	READ / READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A8	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A8	PRE / PREA	Precharge / Precharge All
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	X	TBST	Terminate Burst
	L	H	L	H	BA, CA, A8	READ / READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A8	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge*3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A8	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
WRITE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	X	TBST	Terminate Burst
	L	H	L	H	BA, CA, A8	READ / READA	Terminate Burst, Latch CA, Begin Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A8	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge*3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A8	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	X	TBST	ILLEGAL
	L	H	L	H	BA, CA, A8	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A8	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A8	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	X	TBST	ILLEGAL
	L	H	L	H	BA, CA, A8	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A8	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A8	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
PRE - CHARGING	H	X	X	X	X	DESEL	NOP (Idle after tRP)
	L	H	H	H	X	NOP	NOP (Idle after tRP)
	L	H	H	L	X	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A8	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A8	PRE / PREA	NOP*4 (Idle after tRP)
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP (Row Active after tRCD)
	L	H	H	H	X	NOP	NOP (Row Active after tRCD)
	L	H	H	L	X	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A8	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A8	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RE-COVERING	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A8	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A8	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
RE-FRESHING	H	X	X	X	X	DESEL	NOP (Idle after tRC)
	L	H	H	H	X	NOP	NOP (Idle after tRC)
	L	H	H	L	X	TBST	ILLEGAL
	L	H	L	X	BA, CA, A8	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A8	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Idle after tRSC)
	L	H	H	H	X	NOP	NOP (Idle after tRSC)
	L	H	H	L	X	TBST	ILLEGAL
	L	H	L	X	BA, CA, A8	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A8	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care
BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No Operation

NOTES:
1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

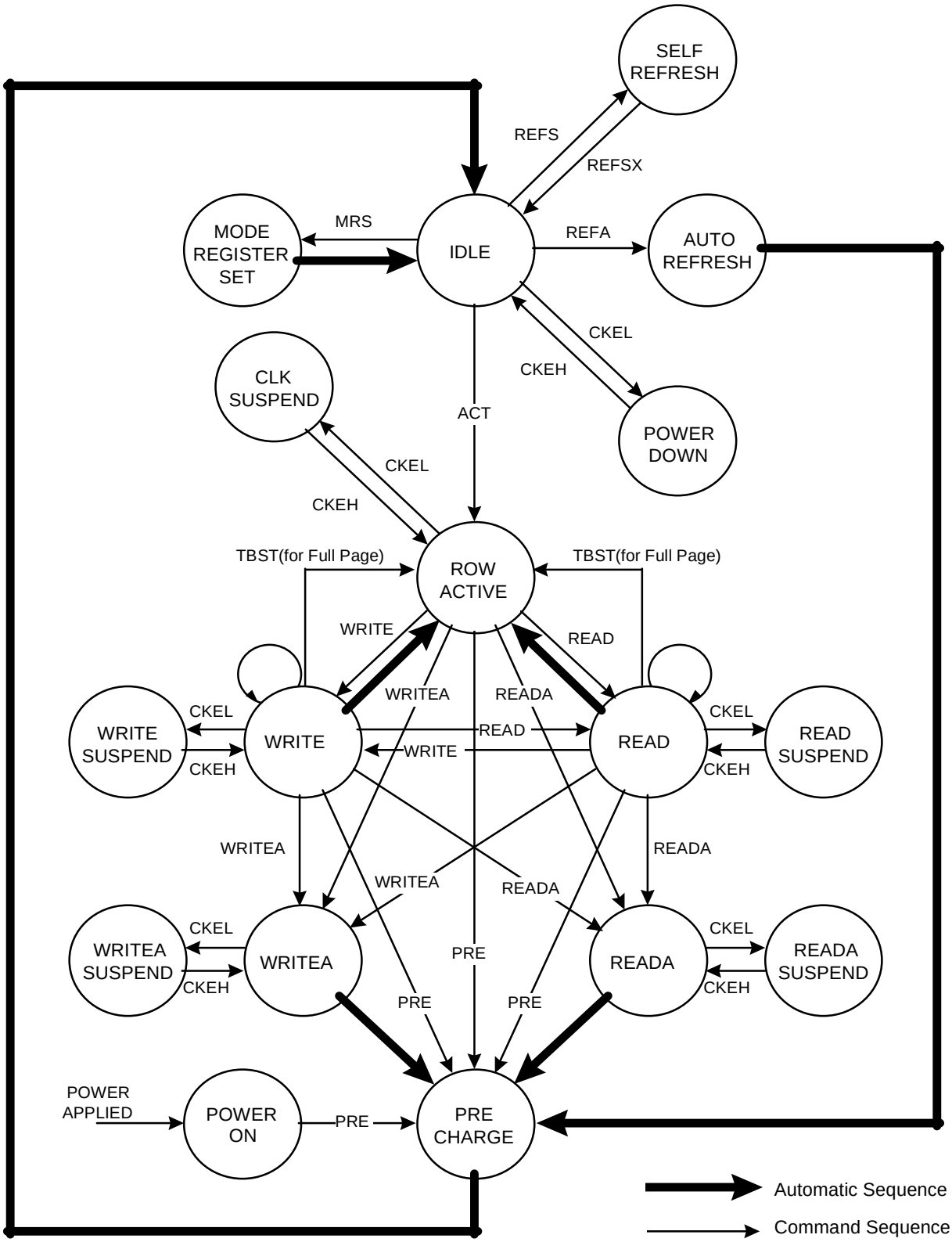
FUNCTION TRUTH TABLE for CKE

Current State	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	Add	Action
SELF-REFRESH*1	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	H	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Power Down to Idle
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
ALL BANKS IDLE*2	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State =Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	X	X	X	X	X	Begin CLK Suspend at Next Cycle*3
	L	H	X	X	X	X	X	Exit CLK Suspend at Next Cycle*3
	L	L	X	X	X	X	X	Maintain CLK Suspend

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care

NOTES:
1. CKE Low to High transition will re-enable CLK and other inputs **asynchronously** . A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
3. Must be legal command.

SIMPLIFIED STATE DIAGRAM



POWER ON SEQUENCE

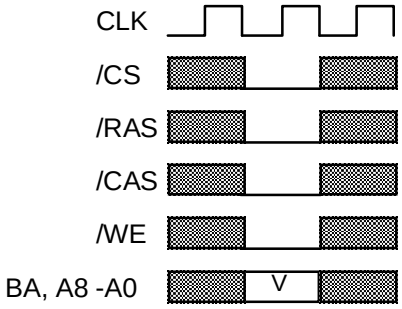
Before starting normal operations, the following power on sequence is necessary to prevent the SDRAM from damage and malfunctions.

1. Apply power and start the clock, CLK. Attempt to maintain CKE high, DQMU/DQML high and NOP conditions on the inputs.
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 500µs.
3. Issue precharge commands for all banks (PRE or PREA).
4. After all banks reach an idle state and after the row the precharge time (tRP) issue 8 or more auto-refresh commands.
5. Finally, issue a mode register set (MRS) command to initialize the mode register.

After tRSC from the MRS command, the SDRAM will be in an idle state and ready for normal operations.

MODE REGISTER

Burst Length, Burst Type, and /CAS Latency can be programmed by setting the mode register (MRS). The mode register stores this data until the next MRS command. An MRS command can only be issued when both banks are idle. After tRSC from an MRS operation, the SDRAM is ready for new commands.



BA	A8	A7	A6	A5	A4	A3	A2	A1	A0

OPCODE	0	LTMODE	BT	BL

	CL	/CAS LATENCY
LATENCY MODE	0 0 0	R
	0 0 1	1
	0 1 0	2
	0 1 1	3
	1 X X	R

	BL	BT= 0	BT= 1
BURST LENGTH	0 0 0	1	1
	0 0 1	2	2
	0 1 0	4	4
	0 1 1	8	8
	1 0 0	R	R
	1 0 1	R	R
	1 1 0	R	R
	1 1 1	F.P.	R

	OP	
OPCODE	0 0	Burst read / Burst write
	0 1	R
	1 0	Burst read / Single write
	1 1	R

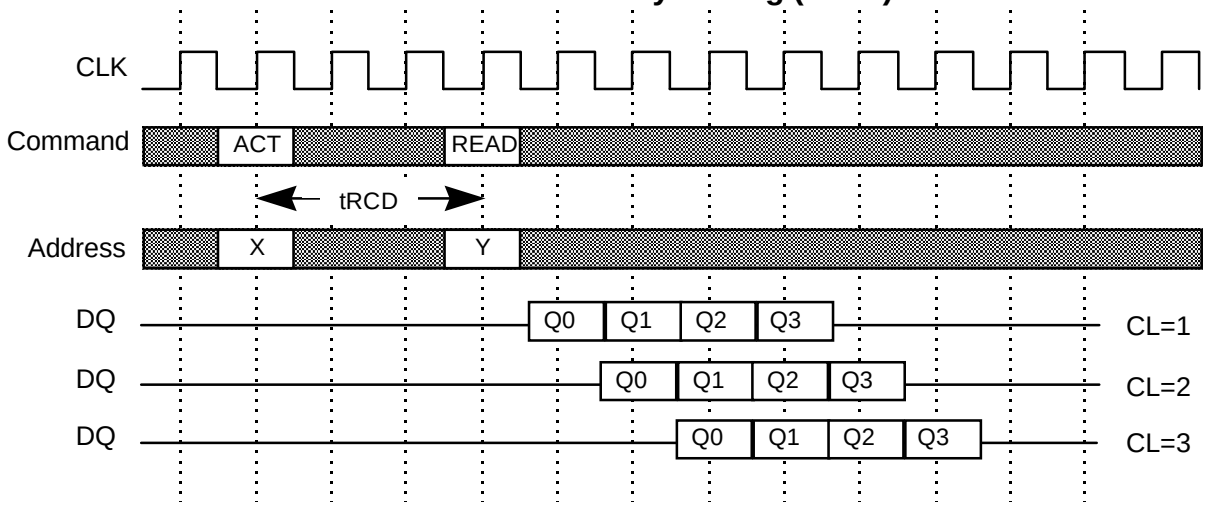
BURST TYPE	0	SEQUENTIAL
	1	INTERLEAVED

R is Reserved for Future Use
F.P. = Full Page (256)

[CAS LATENCY]

/CAS latency, CL, is used to synchronize the first output data with the CLK frequency, i.e., the speed of CLK determines which CL should be used. The DRAM column access, tCAC, determines the CL timing requirements.

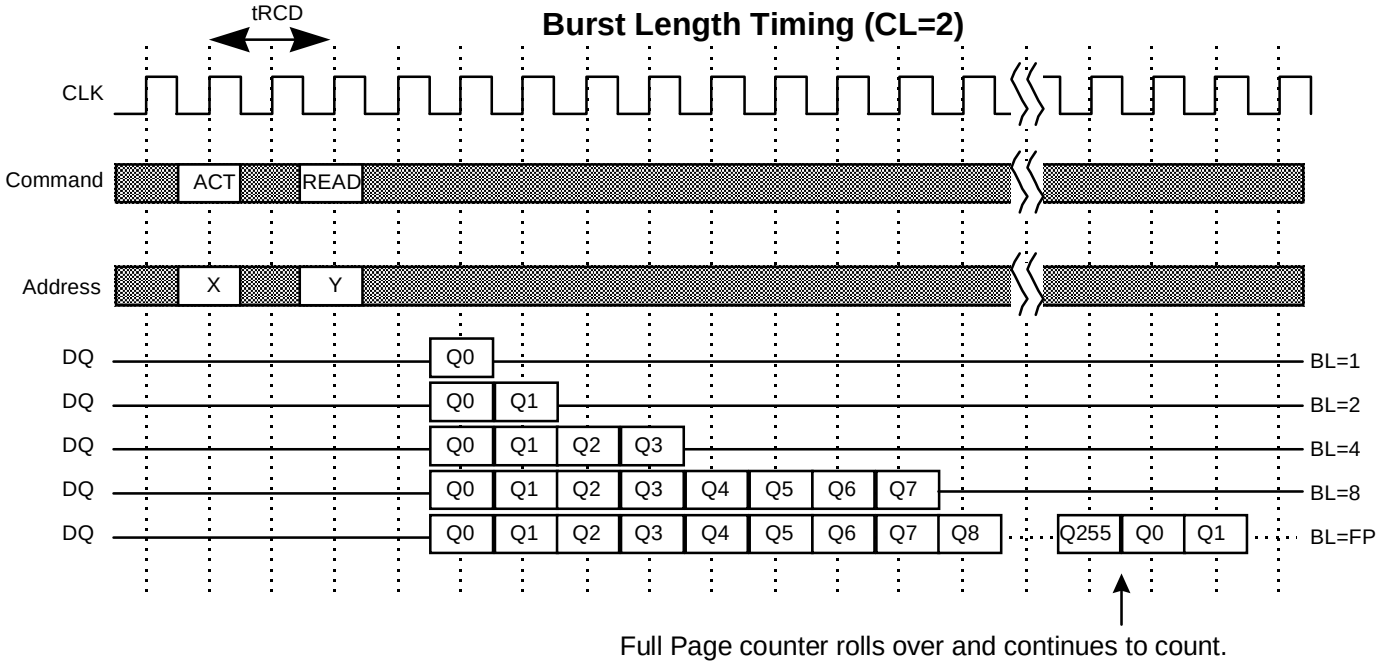
/CAS Latency Timing (BL=4)



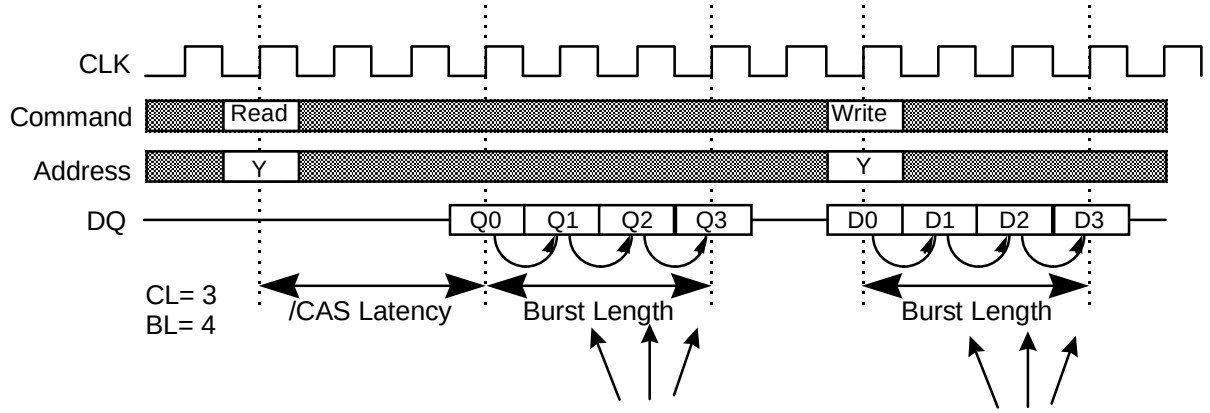
[BURST LENGTH]

The burst length, BL, determines the number of consecutive writes or reads that will be automatically performed after the initial write or read command. For BL=1,2,4,8 the output data is tristated (Hi-Z) after the last read. For BL=FP (Full Page) the TBST (Burst Terminate) command must be used to stop the output of data.

Burst Length Timing (CL=2)



[BURST ADDRESS SEQUENCE]



Internal addresses are determined by Burst Type.

Initial Address			BL	Column Addressing / Burst Type															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

Note: For FP Burst the Burst Type must be set to sequential.

OPERATIONAL DESCRIPTION

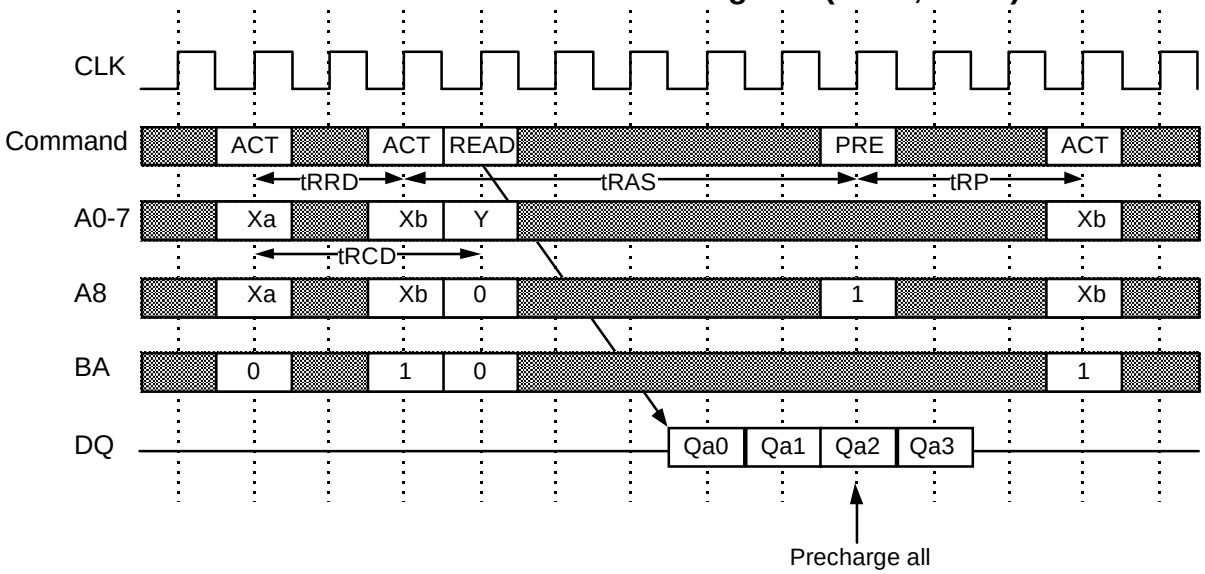
BANK ACTIVATE

The SDRAM has two independent banks. Each bank is activated by the ACT command with the bank address (BA). A row inside the bank is selected by the row address A8-0. The minimum activation interval between one bank and the opposite bank is tRRD.

PRECHARGE

The PRE command deactivates the bank indicated by BA. When both banks are active, the precharge all command (PREA, PRE + A8=H) can be used to deactivate them at the same time. After tRP from the precharge, an ACT command can be issued.

Bank Activation and Precharge All (BL=4, CL=3)

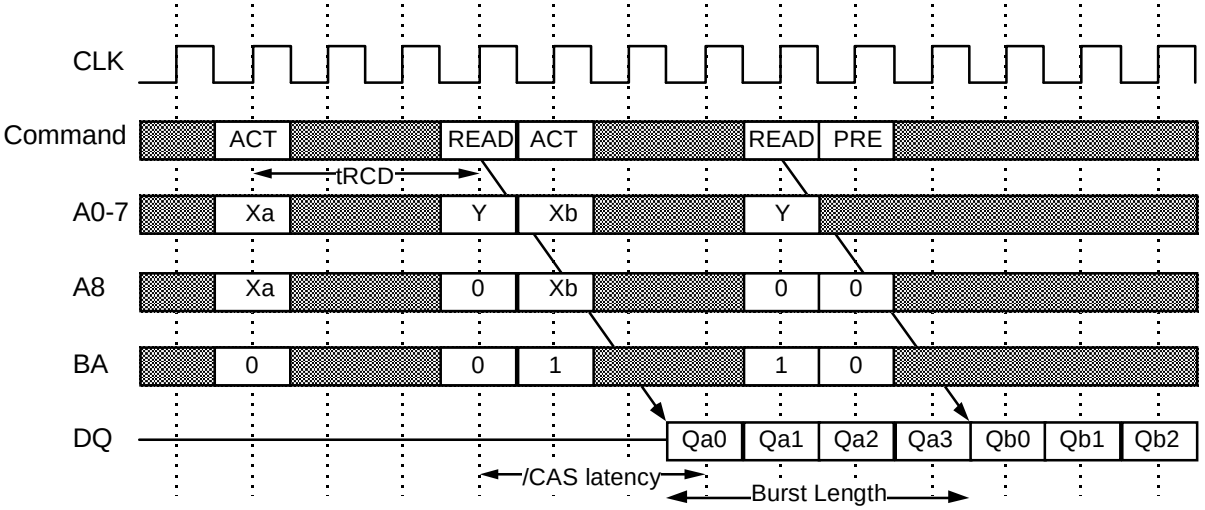


READ

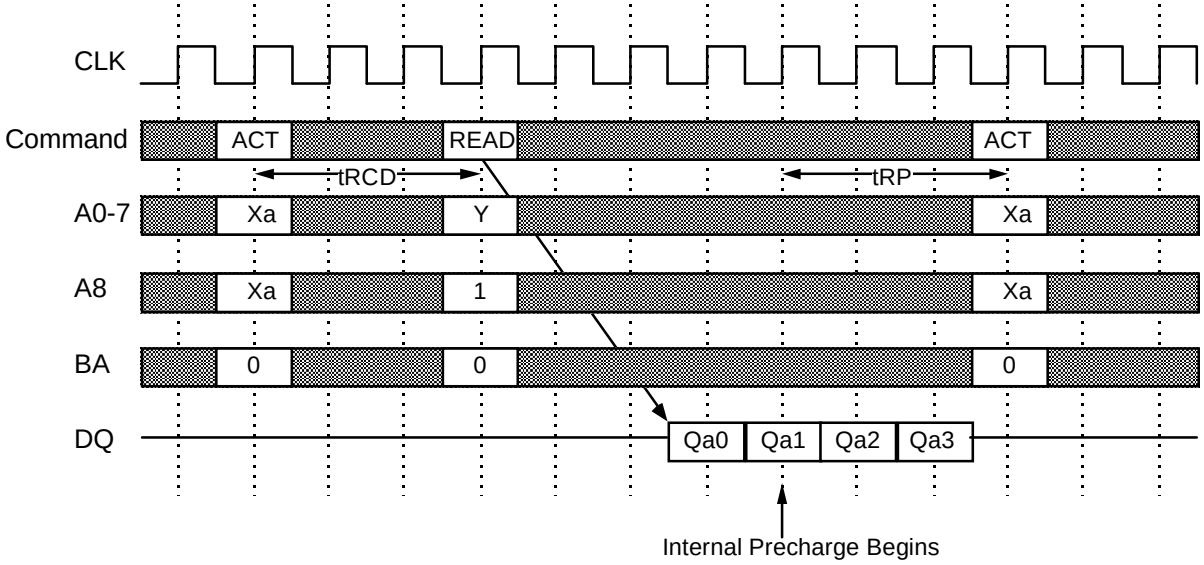
A READ command can be issued after tRCD from bank activation (ACT). Output data is available after the /CAS Latency from the READ, followed by (BL -1) consecutive output data (Burst Length = BL). The start address is specified by A7-0, and the address sequence of the burst data is defined by the Burst Type. A READ command may be applied to any active bank. This allows the row precharge time (tRP) to be hidden behind continuous output data (in case of BL=4) by interleaving the dual banks. When A8 is high at a READ command, the auto-precharge (READA) is performed. During READA the READ, WRITE, PRE, and ACT commands to the same bank are inhibited until the internal precharge is complete. Internal precharge start timing depends on /CAS Latency. The next ACT command can be issued after tRP from the precharge (PRE).

Note: READA is not allowed for FP burst length operations. The SDRAM must be manually precharged.

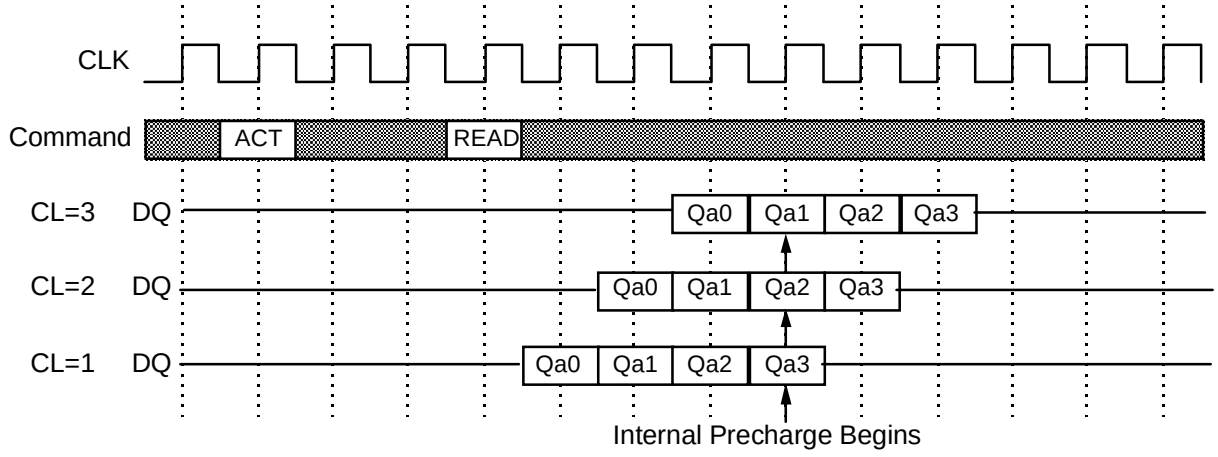
Dual Bank Interleaving READ (BL=4, CL=3)



READ with Auto-Precharge (BL=4, CL=3)



READ Auto-Precharge Timing (BL=4)



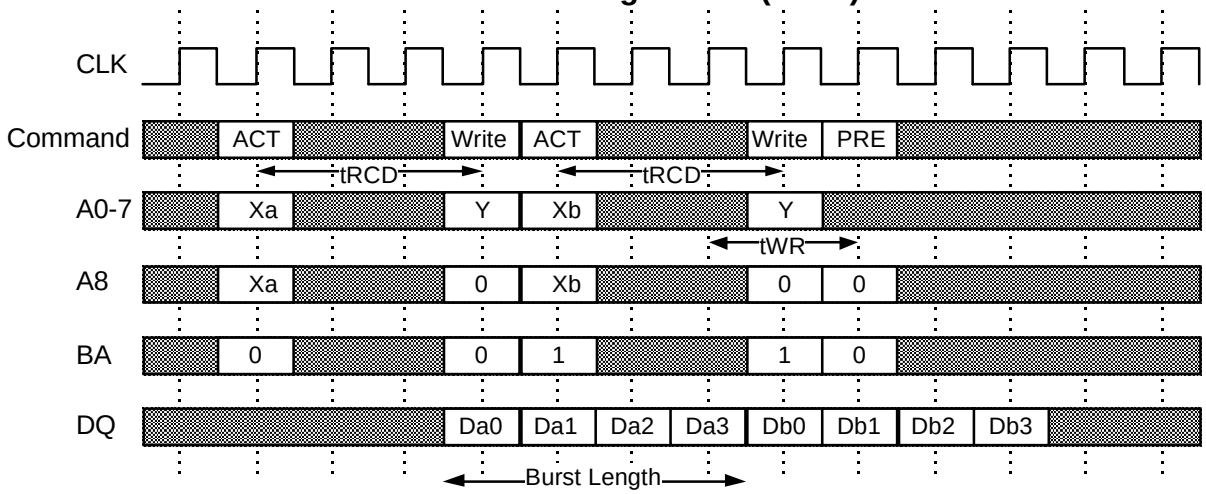
WRITE

A WRITE command can be issued after tRCD from the bank activation (ACT). Input data is written to the SDRAM beginning on the rising edge of CLK in the same cycle that the WRITE command is applied. The remaining input data will be clocked in on the subsequent CLK cycles. The number of writes depends on the BL set in the mode register. The start address is specified by A7-0 and the address sequence is defined by the Burst Type. A WRITE command may be applied to any active bank. This allows the row precharge time (tRP) to be hidden behind continuous input data. Write recovery time (tWR) is required between the last write and subsequent precharge (PRE) inside of a bank.

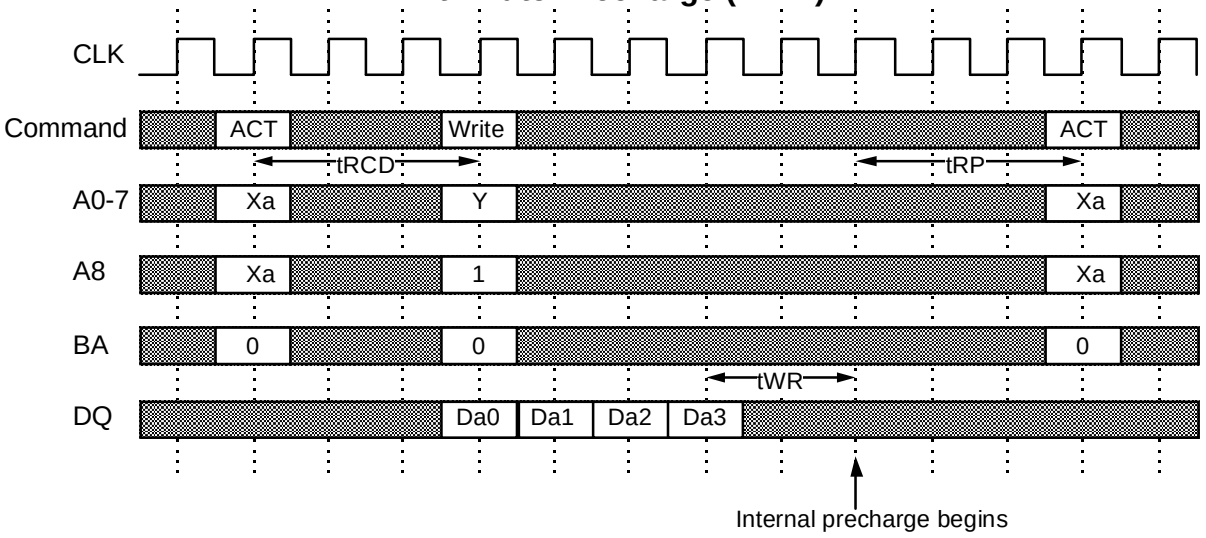
When A8 is high during a WRITE command (WRITEA) , an auto precharge is performed after the last data is input. All commands (READ, WRITE, PRE, ACT) to the same bank are inhibited until the internal precharge is complete. The internal precharge begins at tWR after the last input data cycle. The next ACT command can be issued after tRP. WRITEA **cannot** be used for FP burst length operations.

The Mode Register can be programmed for burst read and single write. In this mode the write data is only clocked in when the WRITE command is issued and the remaining burst length is ignored. The read data burst length is unaffected while in this mode.

Dual Bank Interleaving WRITE (BL=4)



WRITE with Auto-Precharge (BL=4)

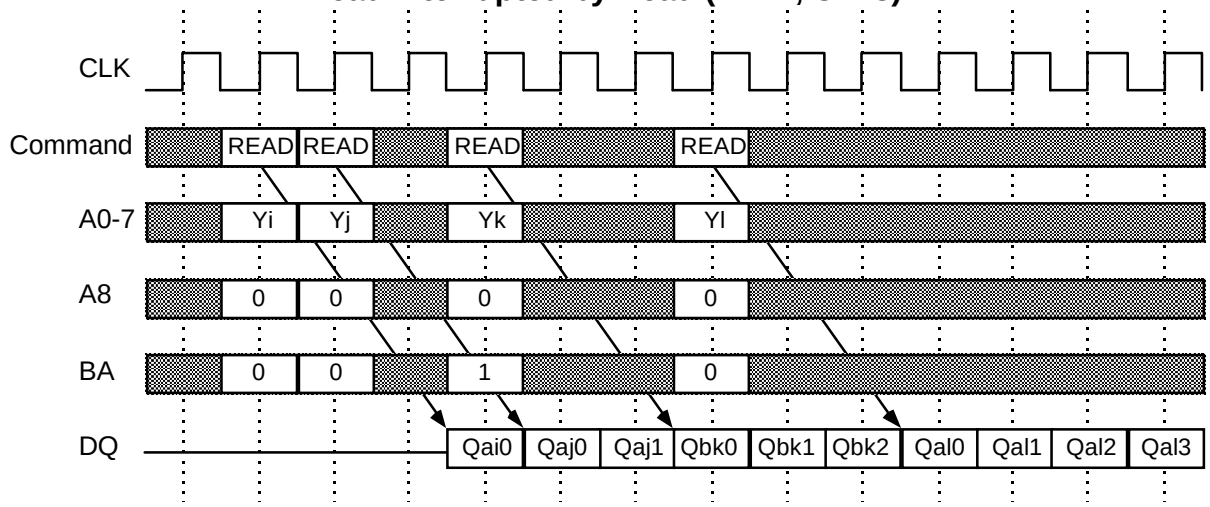


BURST INTERRUPTION

[Read Interrupted by Read]

A burst read operation can be interrupted by a new read of the same or opposite bank. M5M4V4S40CTP allows random column accesses. READ to READ interval is a minimum of one CLK.

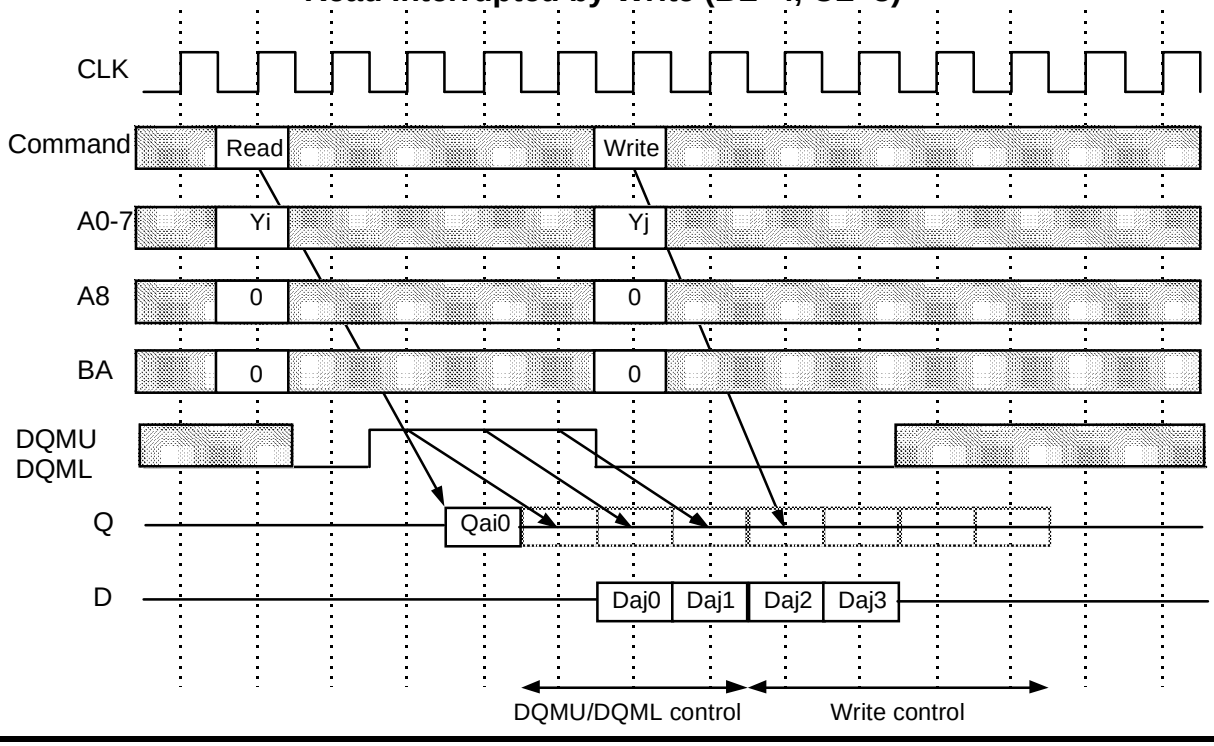
Read Interrupted by Read (BL=4, CL=3)



[Read Interrupted by Write]

A burst read operation can be interrupted by a write to the same or opposite bank. For this operation, the DQ's should be controlled by using DQMU and DQML to prevent bus contention. The output is disabled two cycles automatically after WRITE assertion. Random column access is allowed.

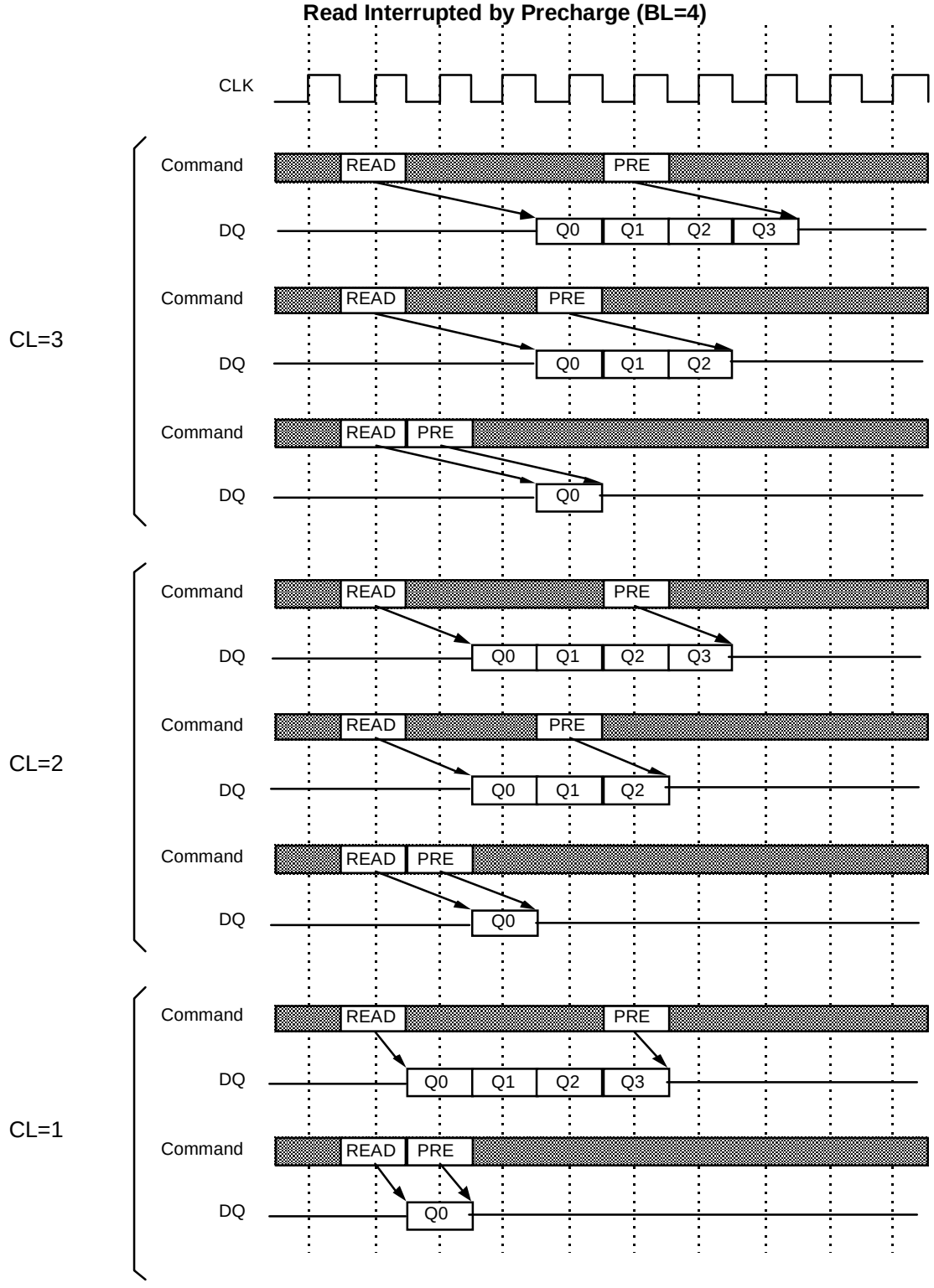
Read Interrupted by Write (BL=4, CL=3)



[Read Interrupted by Precharge]

A burst read operation can be interrupted by a precharge of the same bank. The READ to PRE interval is a minimum of one CLK. A PRE command disables the data output, depending on the /CAS latency. The figures below show examples of how the output data is terminated with a PRE command.

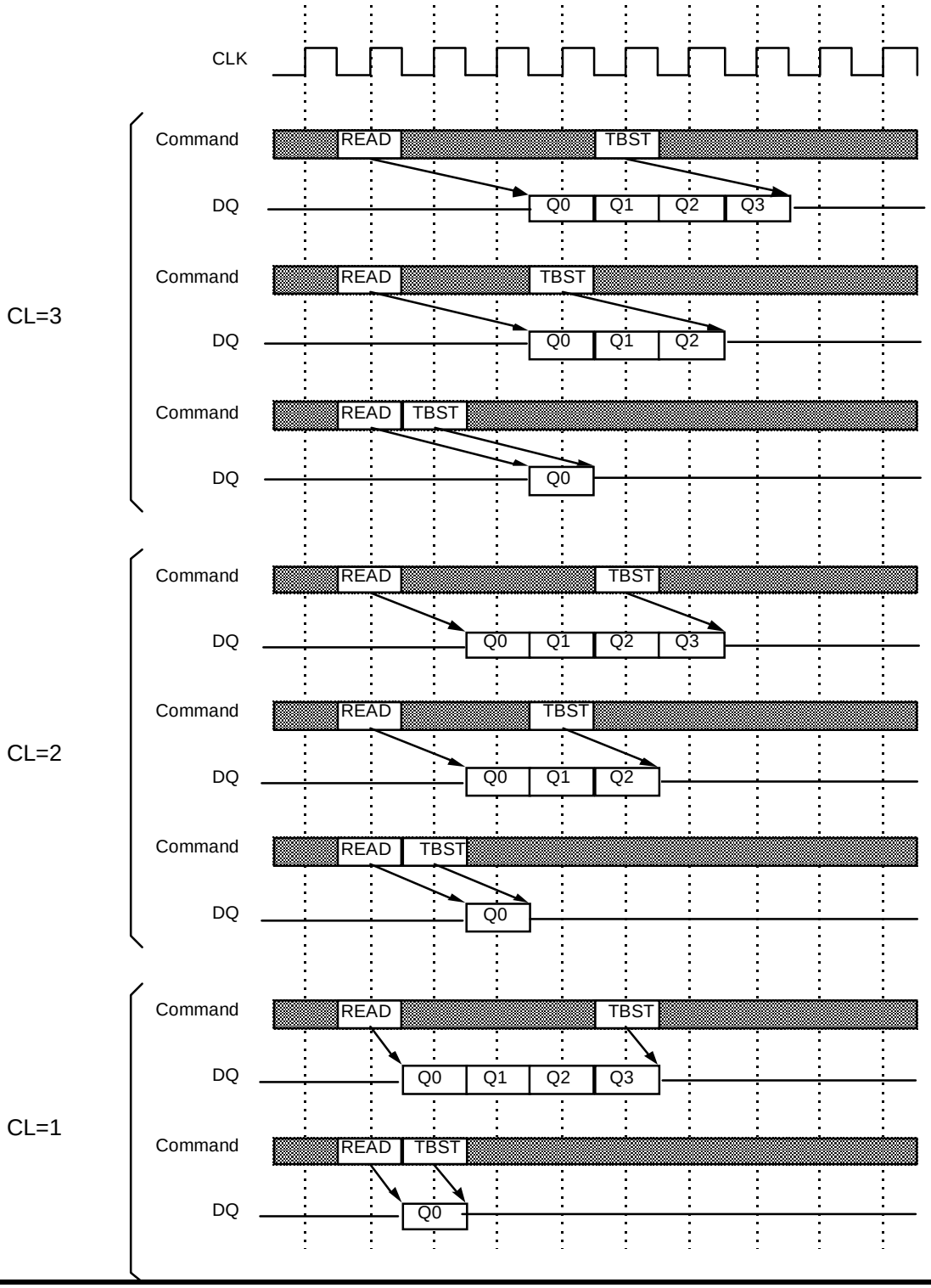
Read Interrupted by Precharge (BL=4)



[Read Interrupted by Burst Terminate]

Similar to a precharge, the burst terminate command, TBST, can interrupt the burst read operation and disable the data output. The READ to TBST interval is a minimum of one CLK. TBST is mainly used to interrupt FP bursts. The figures below show examples, of how the output data is terminated with TBST.

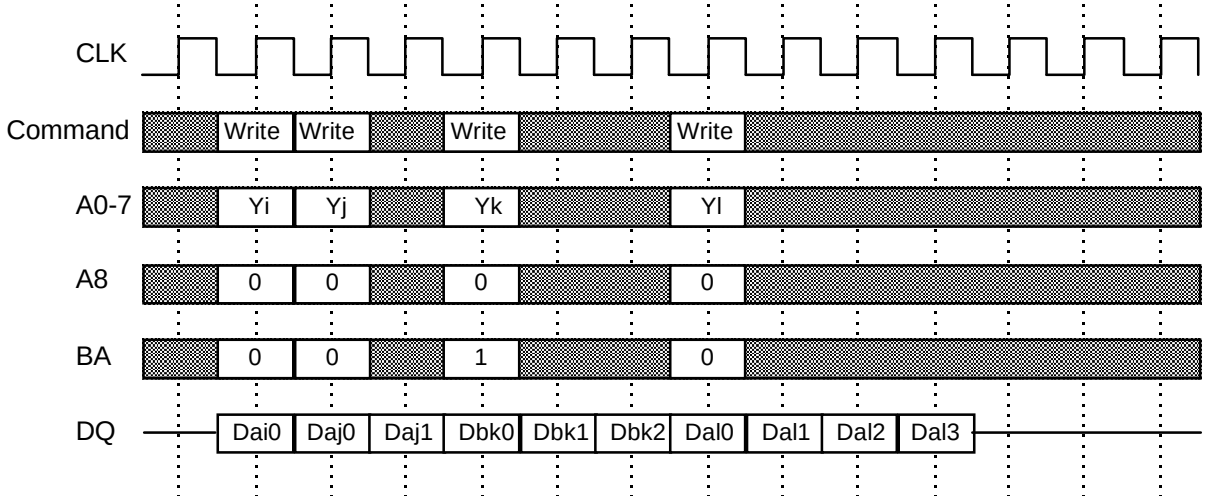
Read Interrupted by Burst Terminate (BL=4)



[Write Interrupted by Write]

A burst write operation can be interrupted by a new write to the same or opposite bank. Random column access is allowed. WRITE to WRITE interval is a minimum of one CLK.

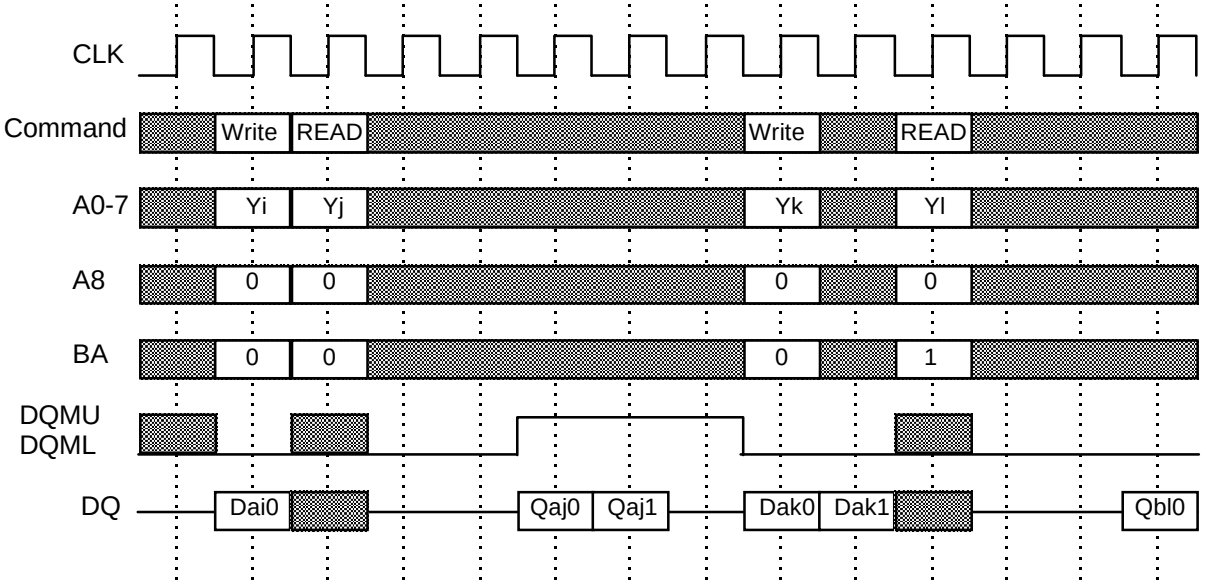
Write Interrupted by Write (BL=4)



[Write Interrupted by Read]

A burst write operation can be interrupted by a read of the same or opposite bank. Random column access is allowed. WRITE to READ interval is a minimum of one CLK. The input data on DQ at the interrupting READ cycle is "don't care".

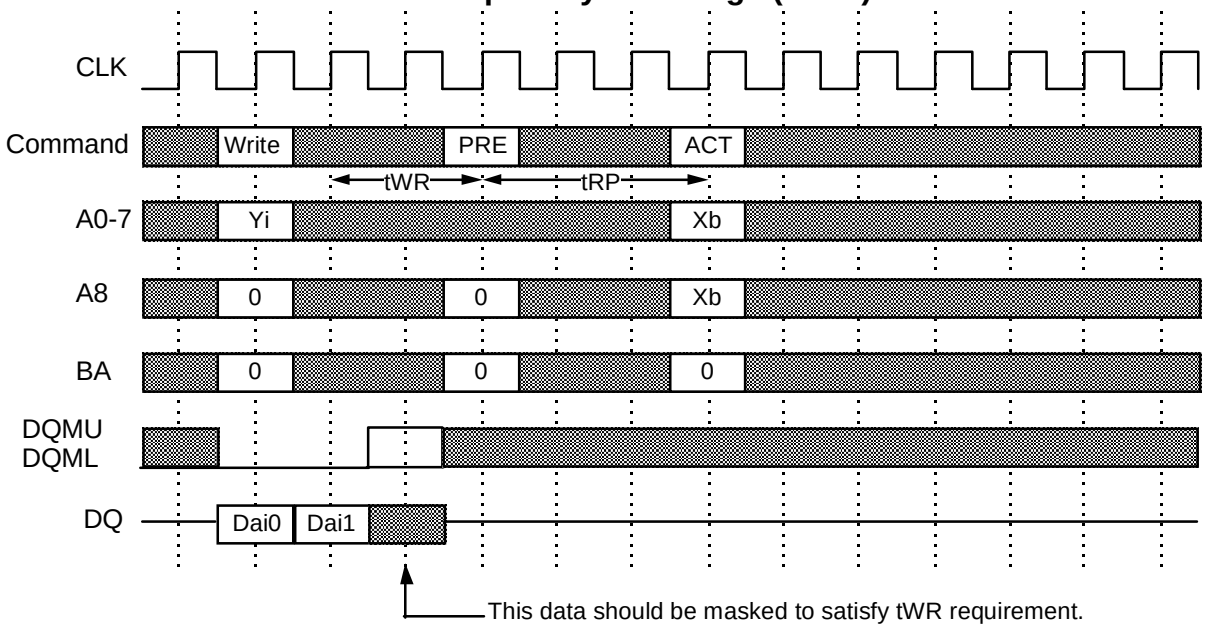
Write Interrupted by Read (BL=4, CL=3)



[Write Interrupted by Precharge]

A burst write operation can be interrupted by precharging (PRE) the same bank. Write recovery time (tWR) is required between the last input data and the next PRE. This may require DQMU/DQML control depending on the CLK frequency and tWR timing. See the example below.

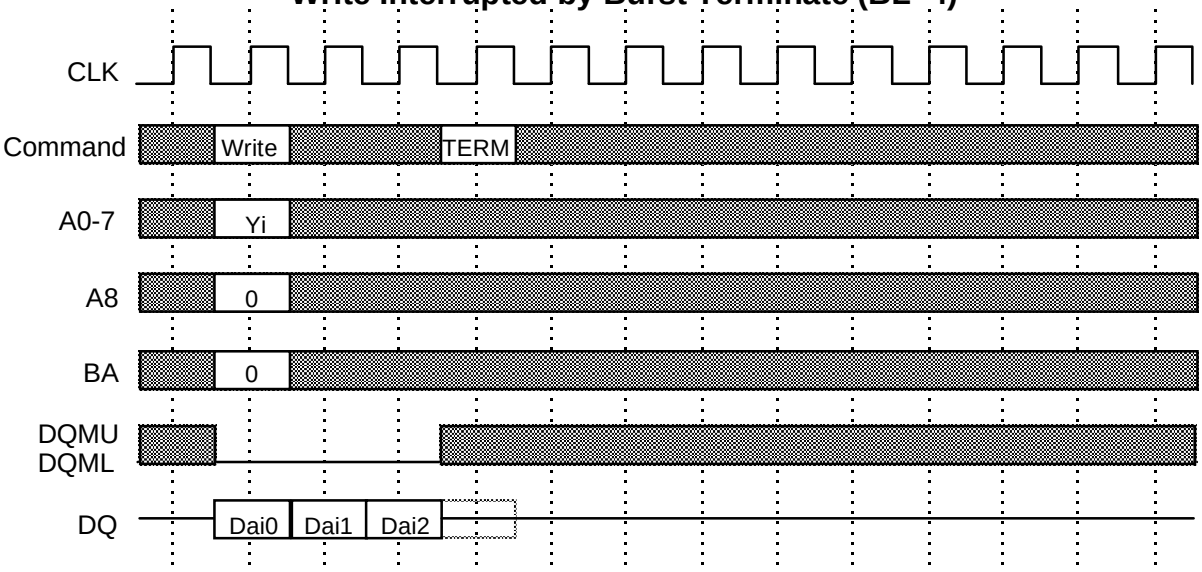
Write Interrupted by Precharge (BL=4)



[Write Interrupted by Burst Terminate]

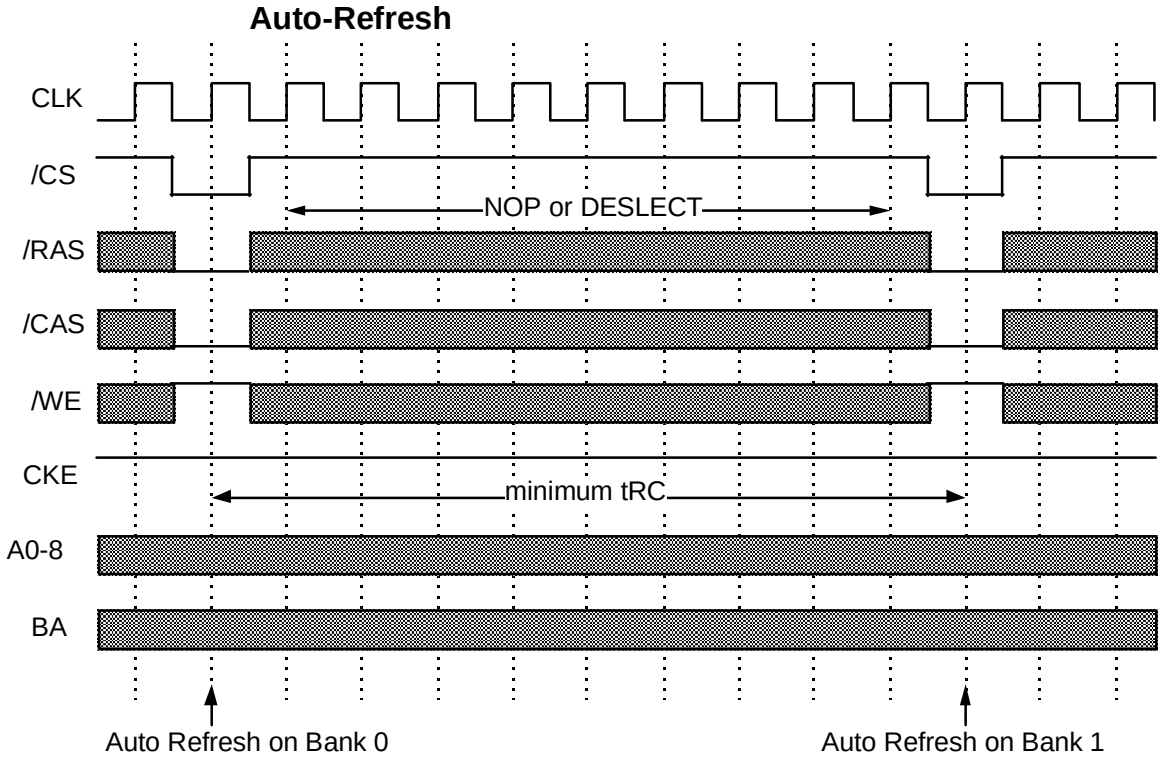
A burst terminate command TBST can be used to terminate a burst write operation. In this case, the write recovery time is not required and the bank remains active (Please see the waveforms below). The WRITE to TERM minimum interval is one CLK.

Write Interrupted by Burst Terminate (BL=4)



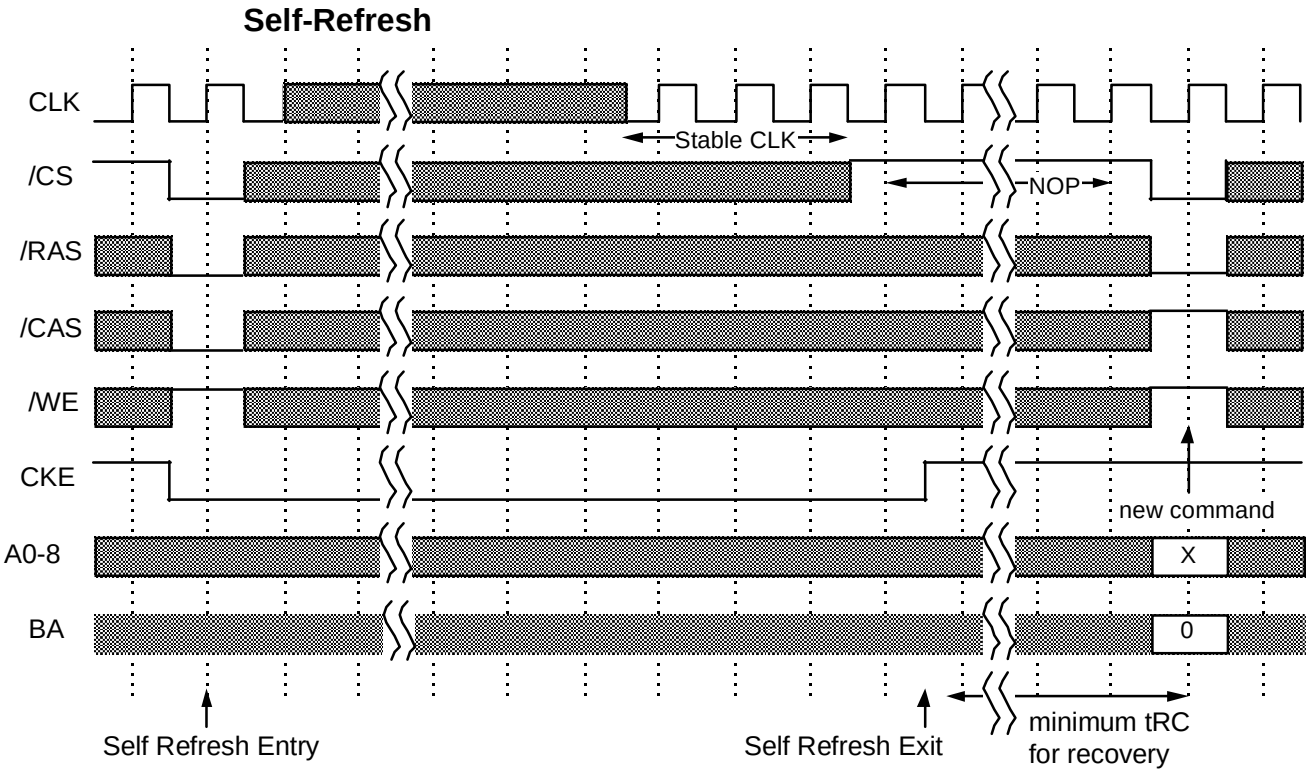
AUTO REFRESH

Auto-refresh is initiated with a REFA command (/CS= /RAS= /CAS= L, /WE= /CKE= H). The refresh address is generated internally. 1024 REFA cycles issued within 16.4ms will refresh the entire 4Mbit memory array. The auto-refresh is alternately performed on each bank (ping-pong). Before performing an auto-refresh, both banks must be in the idle state. Subsequent commands (except NOP or DESELECT) must not be asserted before tRC from the REFA command.



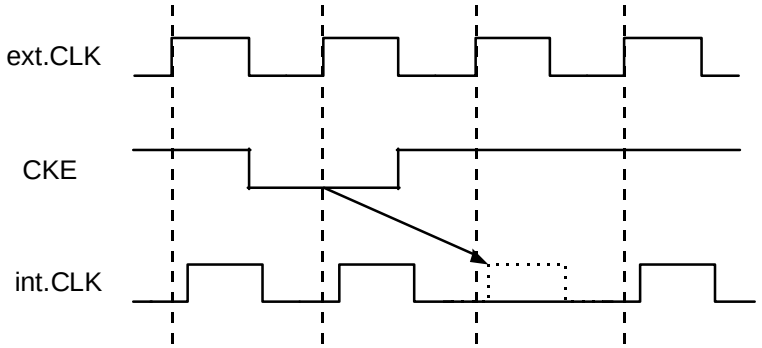
SELF REFRESH

Self-refresh mode is entered by issuing a REFS command (/CS= /RAS= /CAS= L, /WE= H, CKE= L). Once initiated, the self-refresh is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and all other inputs including CLK are disabled and ignored. Disabling all inputs except CKE during self-refresh reduces power consumption. To exit the self-refresh, supply a stable CLK input, issue a DESEL or NOP command, and set CKE=H (REFSX). After tRC from REFSX both banks will be in the idle state new commands can be issued. Until the tRC time has expired, only DESELor NOP commands may be asserted after an REFSX command.

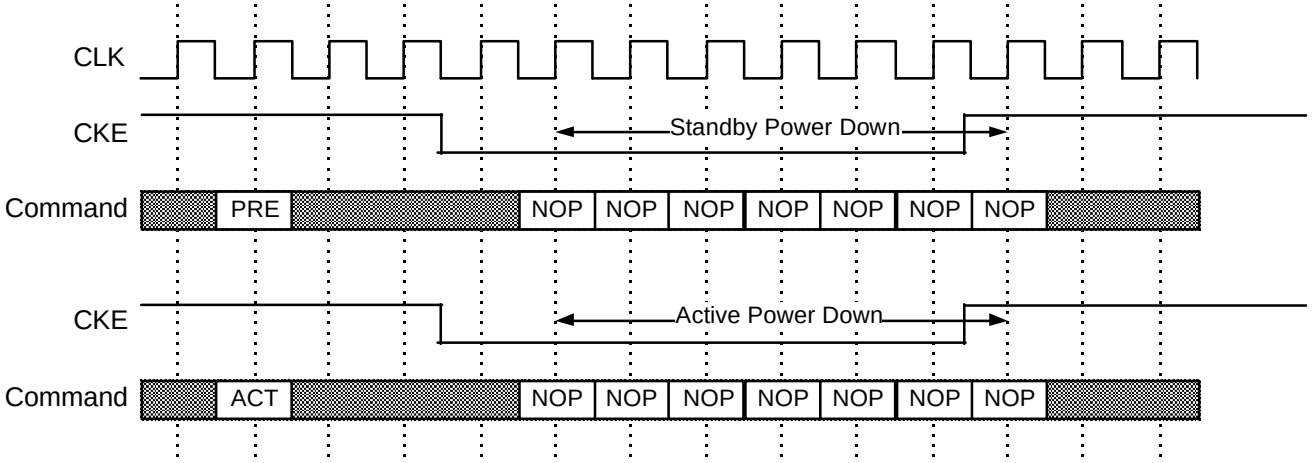


CLK SUSPEND

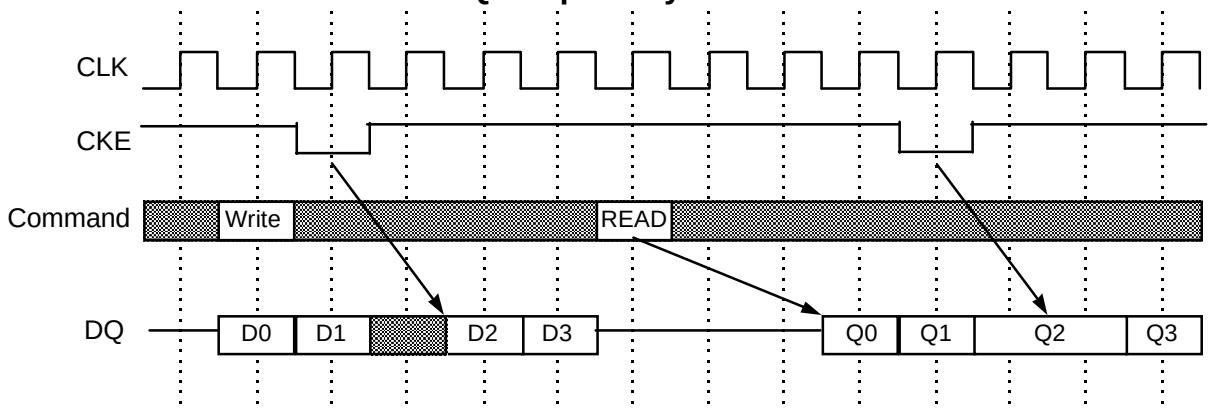
CKE controls the internal CLK in the following cycle. The figure below shows how CKE works. When CKE=L the next internal CLK is suspended. CLK suspend is used to power down, suspend the outputs, and to suspend the inputs. Except during the self-refresh mode, CKE is a synchronous input. CLK suspend can be performed either when the banks are active or idle; however, all commands issued in the following cycle are ignored.



Power Down by CKE



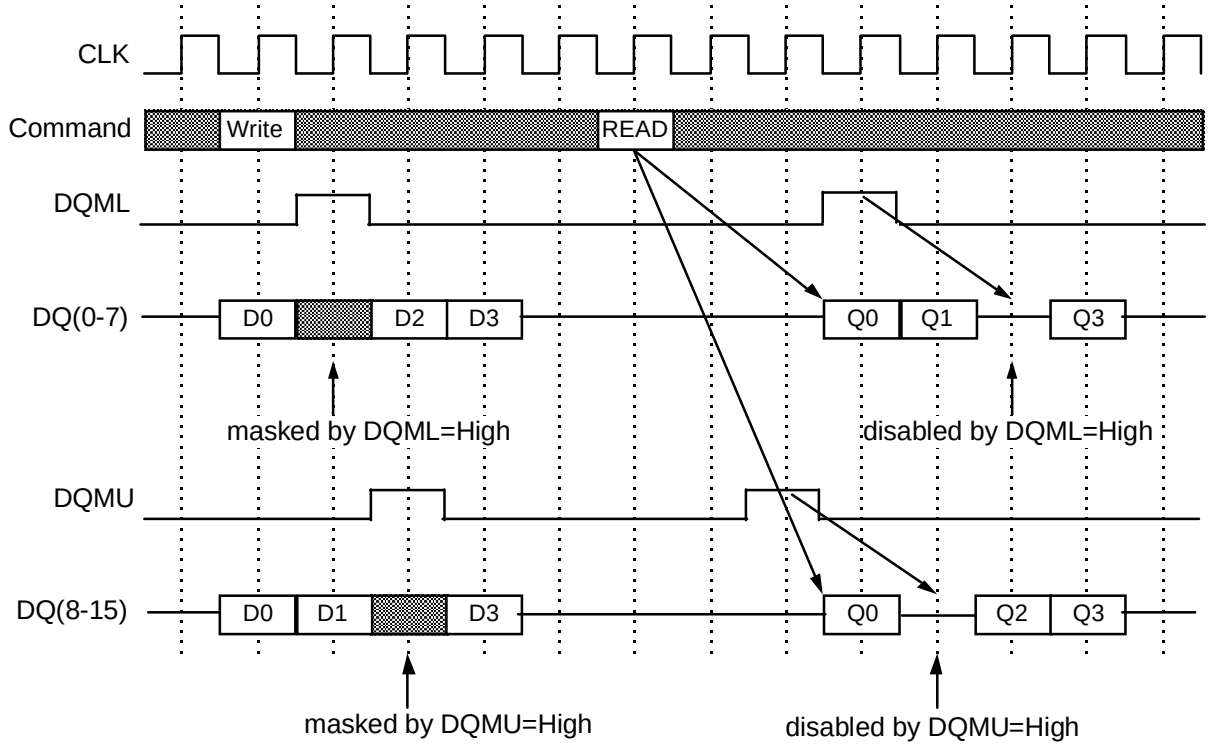
DQ Suspend by CKE



DQMU / DQML CONTROL

DQMU and DQML are used to mask write data and disable read data. During write operations, DQMU and DQML mask the upper and lower bytes of input, respectively. The DQMU and DQML write mask is applied in the same clock cycle. During read operations, DQMU and DQML are used to "Hi-Z" the upper and lower bytes of output data, respectively. The DQMU and DQML to output "Hi-Z" latency is two, i.e., the output will be "Hi-Z" at the rising edge of second clock after DQM is applied.

DQMU/DQML Function



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vdd	Supply Voltage	with respect to Vss	-0.5 ~ 4.6	V
VddQ	Supply Voltage for Output	with respect to VssQ	-0.5 ~ 4.6	V
VI	Input Voltage	with respect to Vss	-0.5 ~ 5.5	V
VO	Output Voltage	with respect to VssQ	-0.5 ~ 4.6	V
IO	Output Current		50	mA
Pd	Power Dissipation	Ta = 25 °C	1000	mW
Topr	Operating Temperature		0 ~ 70	°C
Tstg	Storage Temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta=0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vdd	Supply Voltage	3.0	3.3	3.6	V
Vss	Supply Voltage	0	0	0	V
VddQ	Supply Voltage for Output	3.0	3.3	3.6	V
VssQ	Supply Voltage for Output	0	0	0	V
VIH*1	High-Level Input Voltage all inputs	2.0		5.5	V
VIL*2	Low-Level Input Voltage all inputs	-0.3		0.8	V

NOTES:
1. VIH (max) = 5.75V for pulse width less than 5ns.
2. VIL (min) = -1.0V for pulse width less than 5ns.

CAPACITANCE

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits (max.)	Unit
CI(A)	Input Capacitance, address pin	VI=Vss f=1MHz Vi=25mVrms	5	pF
CI(C)	Input Capacitance, control pin		5	pF
CI(K)	Input Capacitance, CLK pin		5	pF
CI/O	Input Capacitance, I/O pin		7	pF

AVERAGE SUPPLY CURRENT from Vdd

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits(max)		Unit
			-12	-15	
Icc1s*1	operating current, single bank	tRC=min, tCLK=min, BL=1, CL=3	90	75	mA
Icc1d*1	operating current, dual bank	tRC=min, tCLK=min, BL=1, CL=3	130	110	mA
Icc2h	standby current, CKE=H	both banks idle, tCLK=min, CKE=H	18	16	mA
Icc2l	standby current, CKE=L	both banks idle, tCLK=min, CKE=L	2	2	mA
Icc3	active standby current	both banks active, tCLK=min, CKE=H	35	30	mA
Icc4*1	burst current	tCLK=min, BL=4, CL=3, 1 bank idle	120	100	mA
Icc5	auto-refresh current	tRC=min, tCLK=min	60	50	mA
Icc6	self-refresh current	CKE <0.2v	1	1	mA

NOTES:
1. Icc (max) is specified at the output open condition.

AC OPERATING CONDITIONS AND CHARACTERISTICS

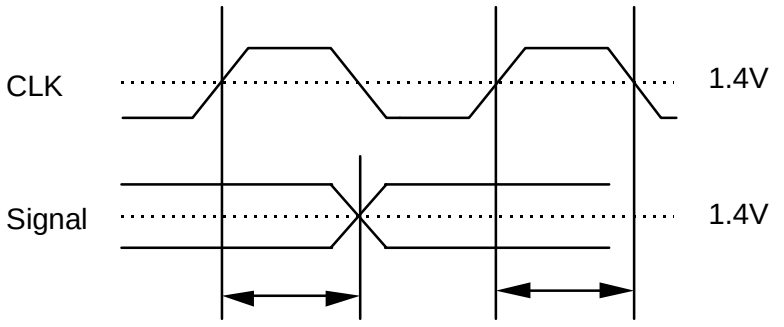
(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits		Unit
			Min.	Max.	
VOH (DC)	High-Level Output Voltage (DC)	IOH=-2mA	2.4		V
VOL (DC)	Low-Level Output Voltage (DC)	IOL= 2mA		0.4	V
IOZ	Off-state Output Current	Q floating VO=0 ~ VddQ	-10	10	µA
I_I	Input Current	VIH = 0 ~ VddQ+0.3V	-10	10	µA

AC TIMING REQUIREMENTS

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)
Input Pulse Levels : 0.8V to 2.0V
Input Timing Measurement Level : 1.4V

Symbol	Parameter		Limits				Unit
			-12		-15		
			Min.	Max.	Min.	Max.	
tCLK	CLK cycle time	CL=1	30		30		ns
		CL=2	15		15		ns
		CL=3	12		15		ns
tCH	CLK High pulse width		4		4		ns
tCL	CLK Low pulse width		4		4		ns
tT	Transition time of CLK		1	10	1	10	ns
tIS	Input Setup time (all inputs)		3		3		ns
tIH	Input Hold time (all inputs)		1		1.5		ns
tRC	Row Cycle time		100		120		ns
tRCD	Row to Column Delay		30		30		ns
tRAS	Row Active time		70	10000	75	10000	ns
tRP	Row Precharge time		30		40		ns
tWR	Write Recovery time		12		15		ns
tRRD	Act to Act Delay time		24		30		ns
tRSC	Mode Register Set Cycle time		24		30		ns
tPDE	Power Down Exit time		12		15		ns
tREF	Refresh Interval time			16.4		16.4	ms



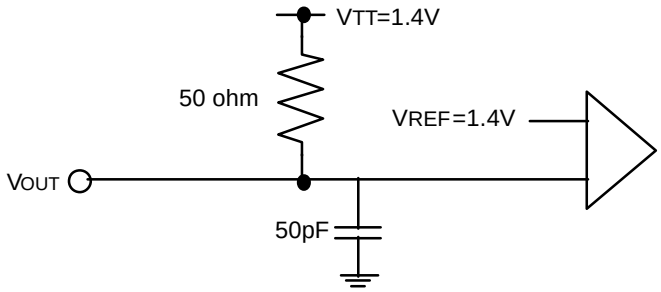
Any AC timing is referenced to the input signal passing through 1.4V.

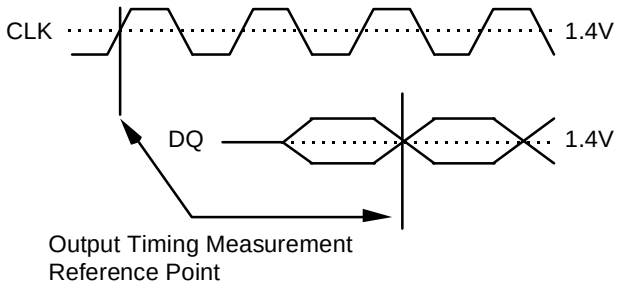
SWITCHING CHARACTERISTICS

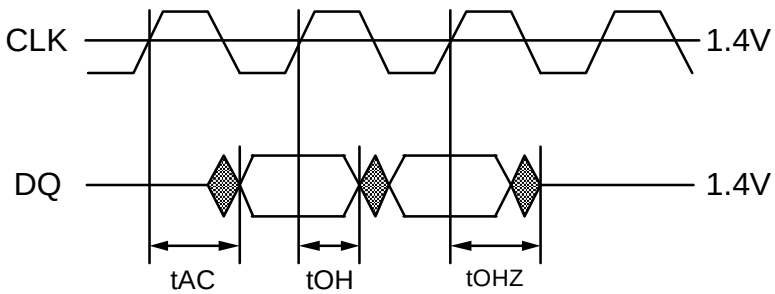
(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)

Symbol	Parameter		Limits				Unit
			-12		-15		
			Min.	Max.	Min.	Max.	
tAC	Access time from CLK	CL=1		27		30	ns
		CL=2		9.5		12	ns
		CL=3		8		9	ns
tCAC	Column Access Time			24.5		30	ns
tRAC	Row Access Time			54.5		60	ns
tOH	Output Hold time from CLK		3		3		ns
tOLZ	Delay time, output low impedance from CLK		0		0		ns
tOHZ	Delay time, output high impedance from CLK		3	8	3	10	ns

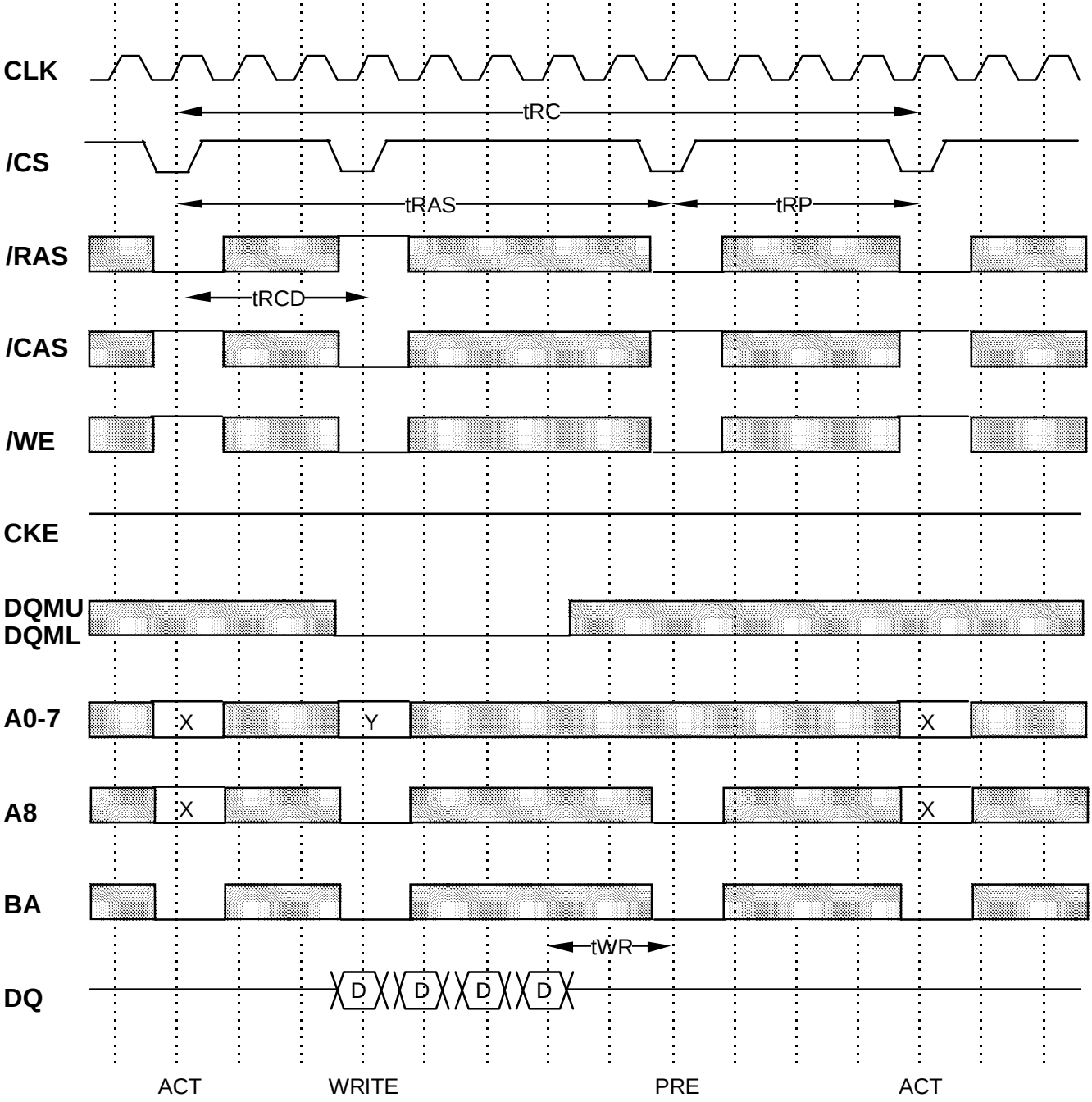
Output Load Condition





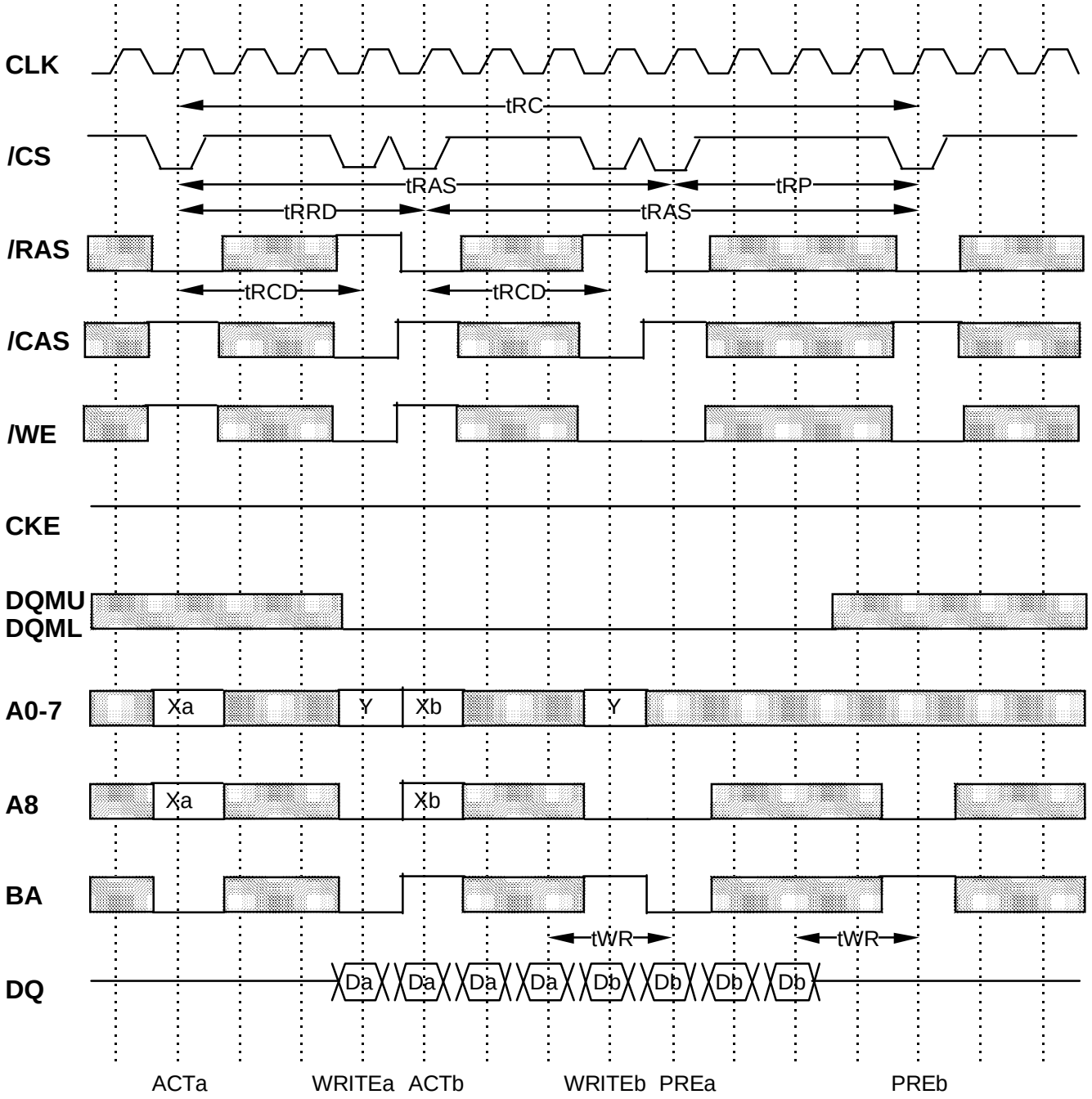


WRITE CYCLE (single bank) BL=4

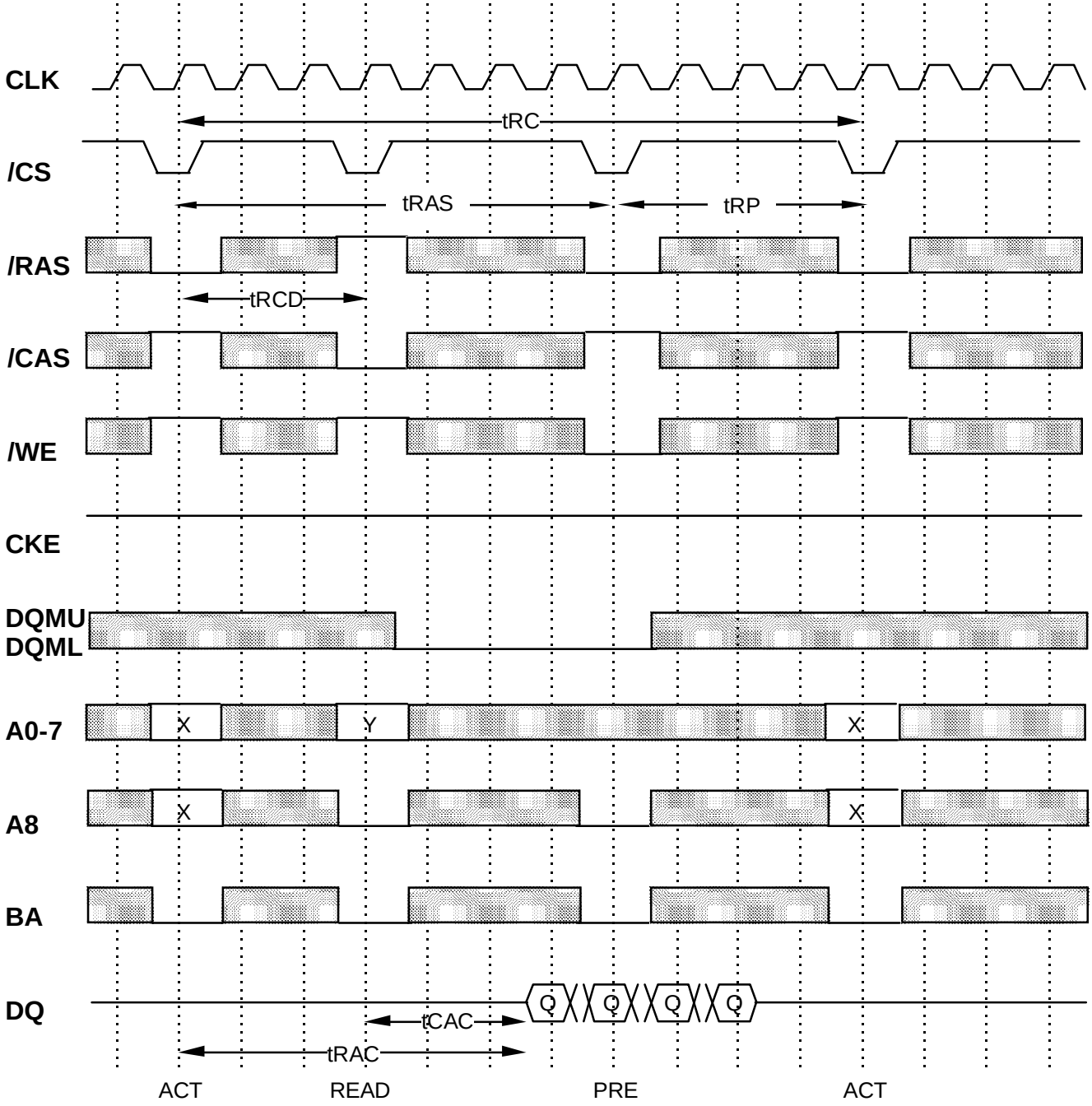


WRITE CYCLE (dual bank)

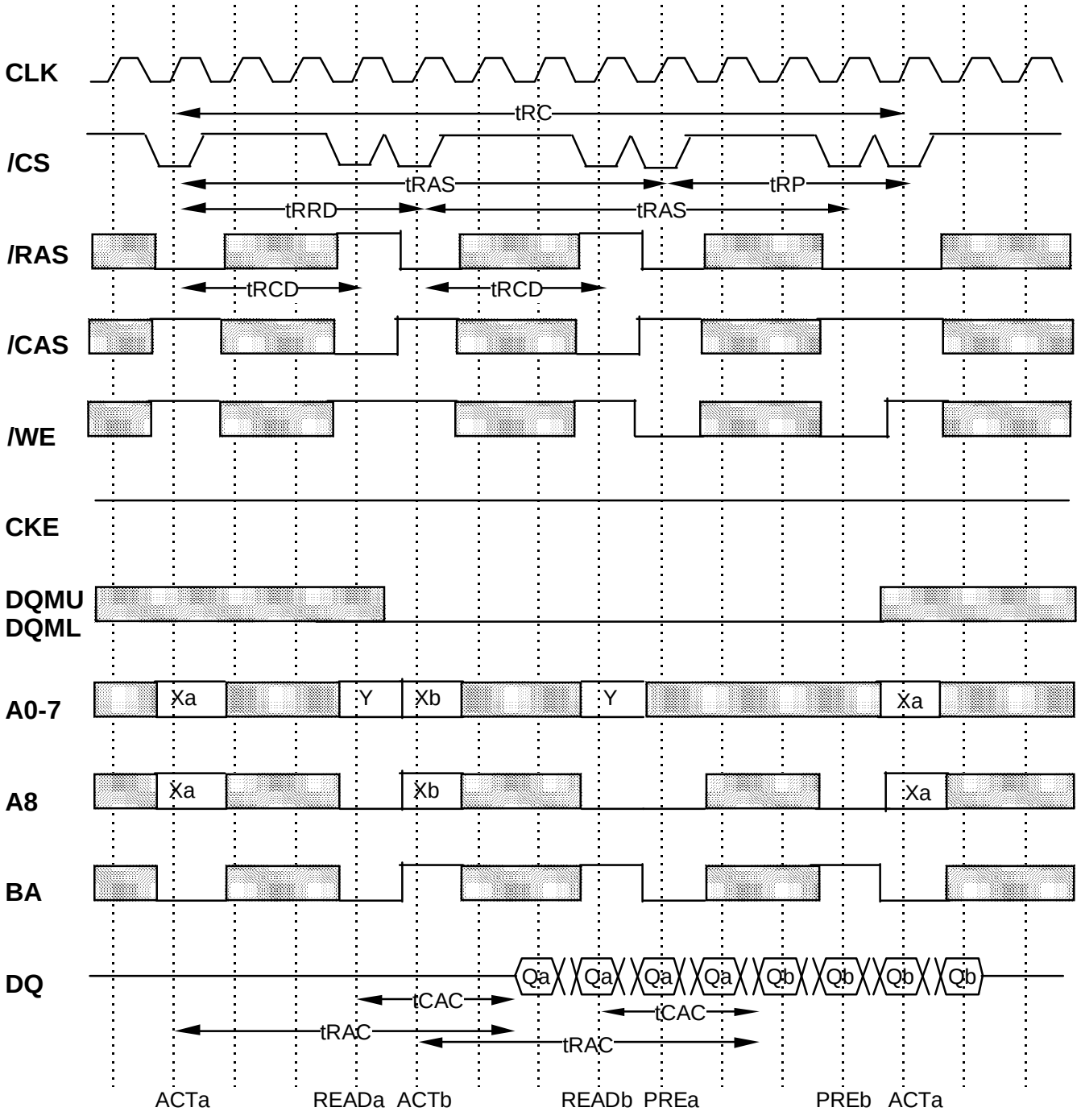
BL=4



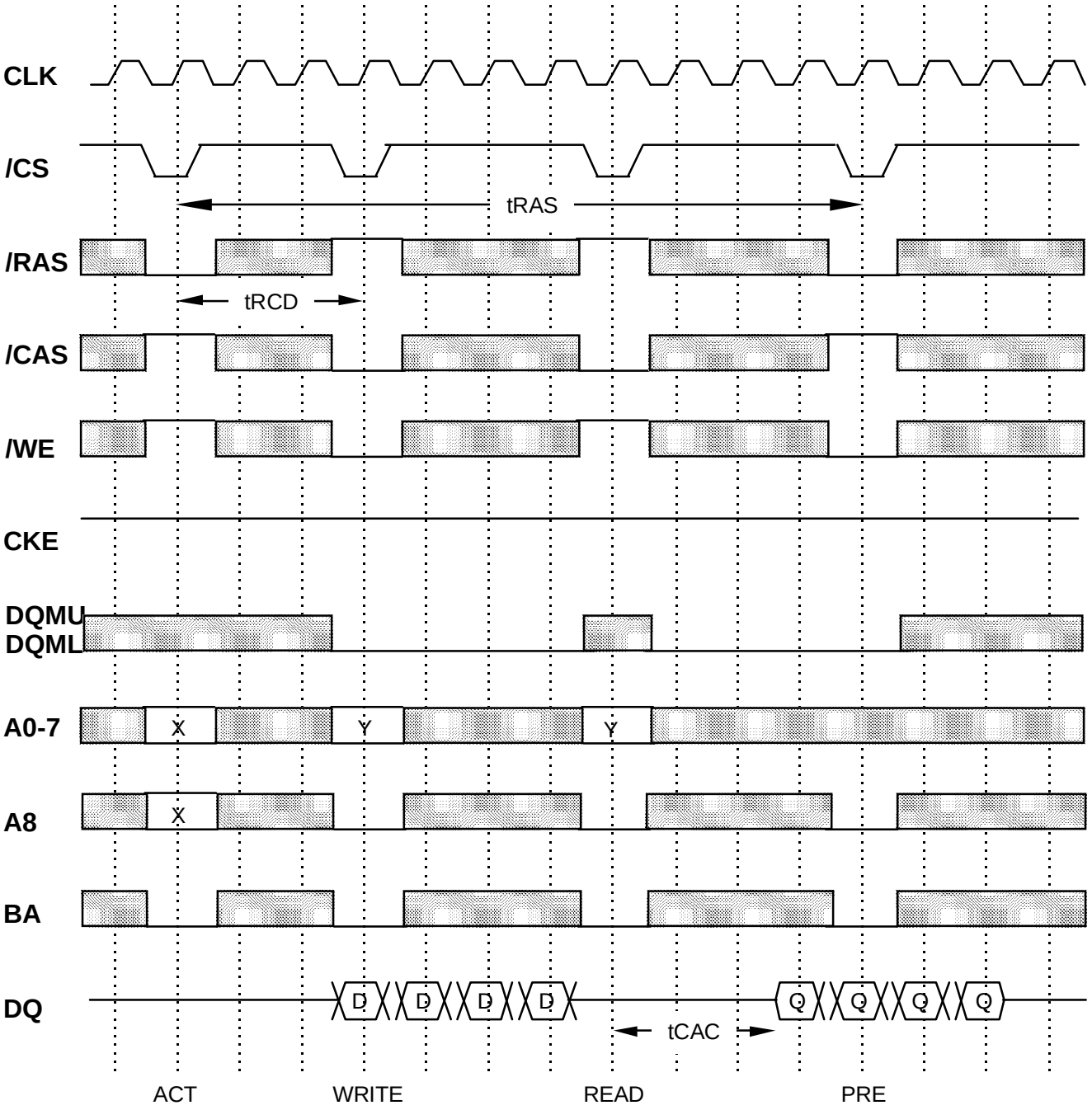
READ CYCLE (single bank) BL=4, CL=3



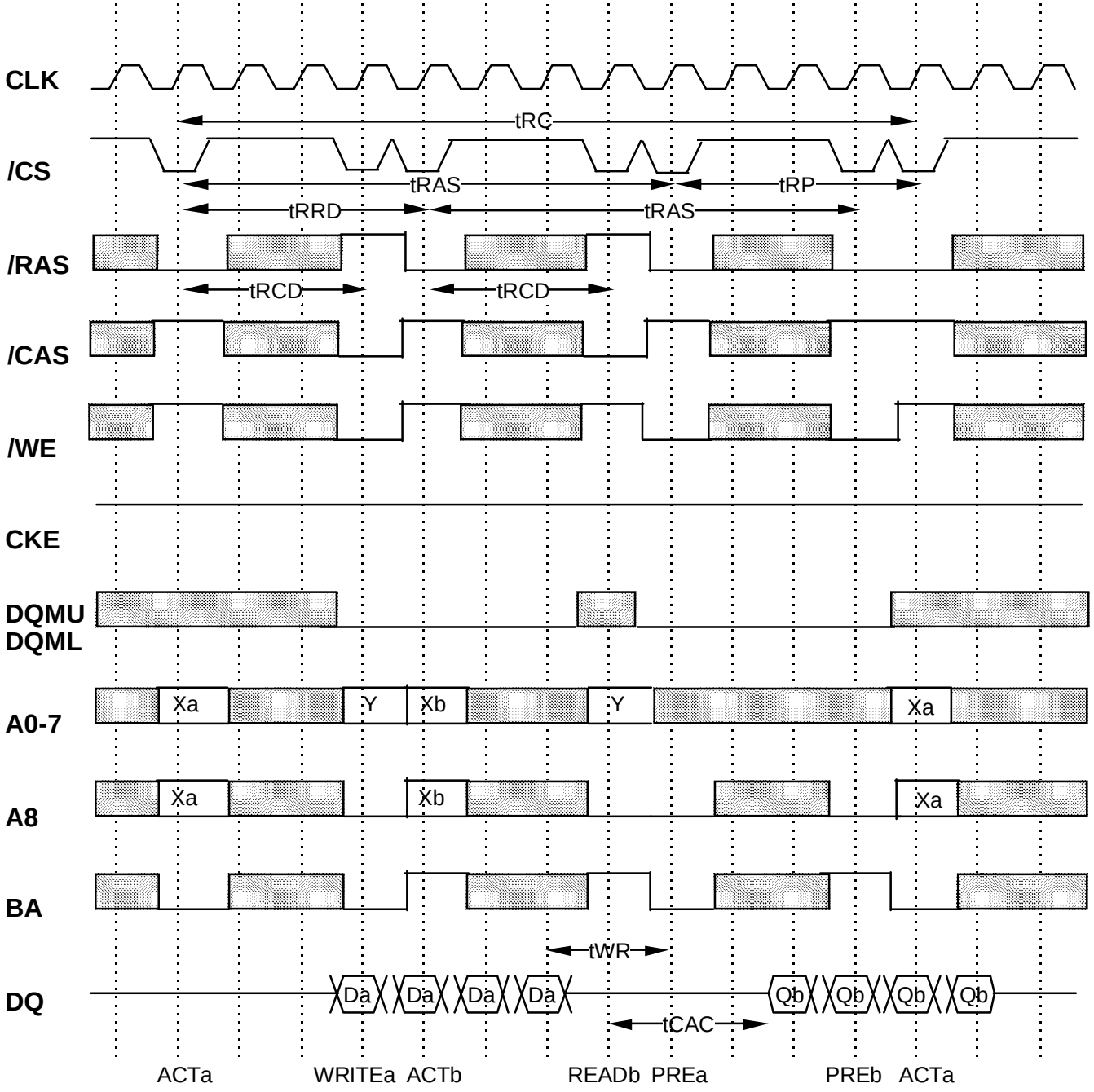
READ CYCLE (dual bank) BL=4, CL=3



WRITE to READ (single bank) BL=4, CL=3

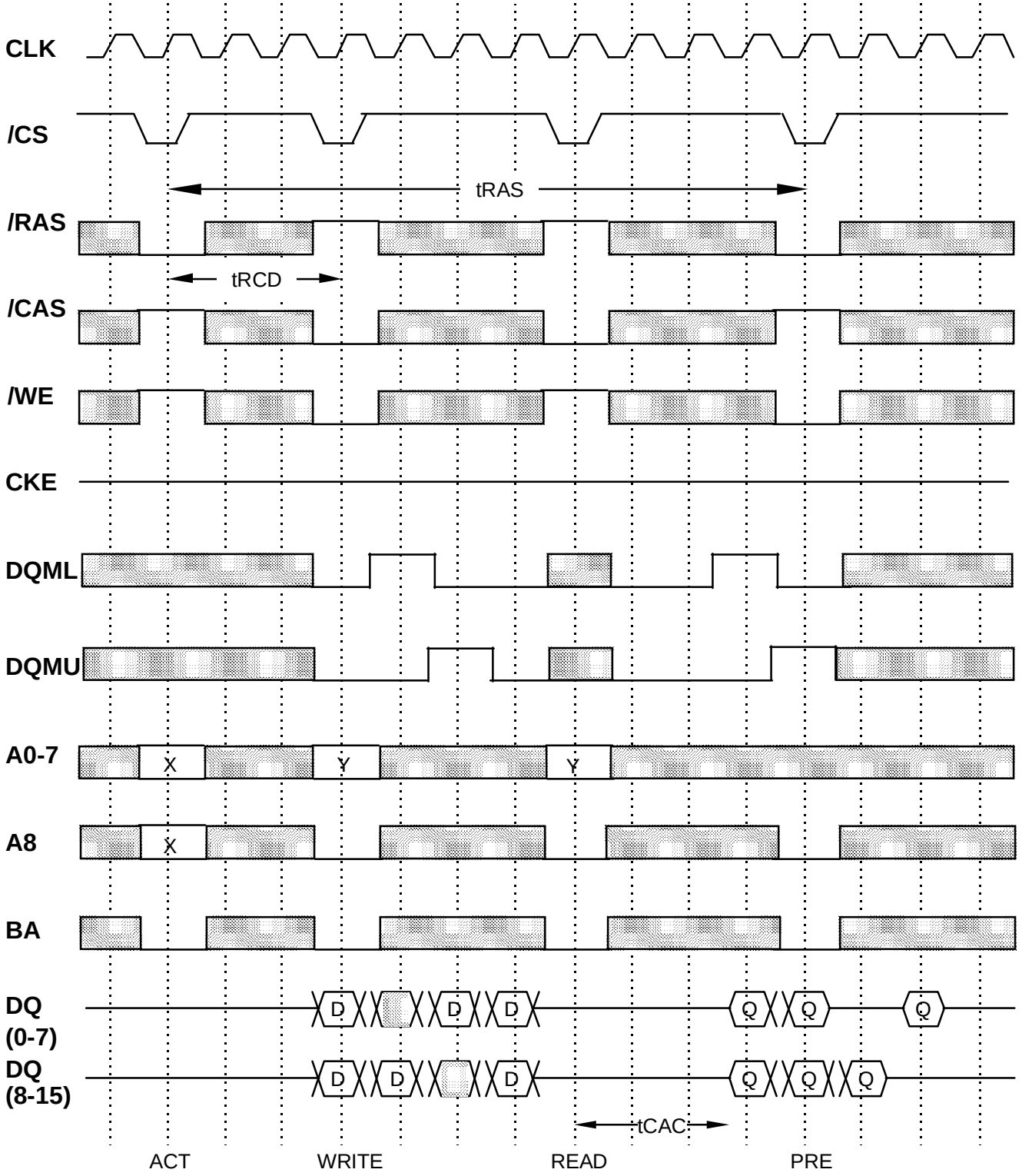


WRITE to READ (dual bank) BL=4, CL=3

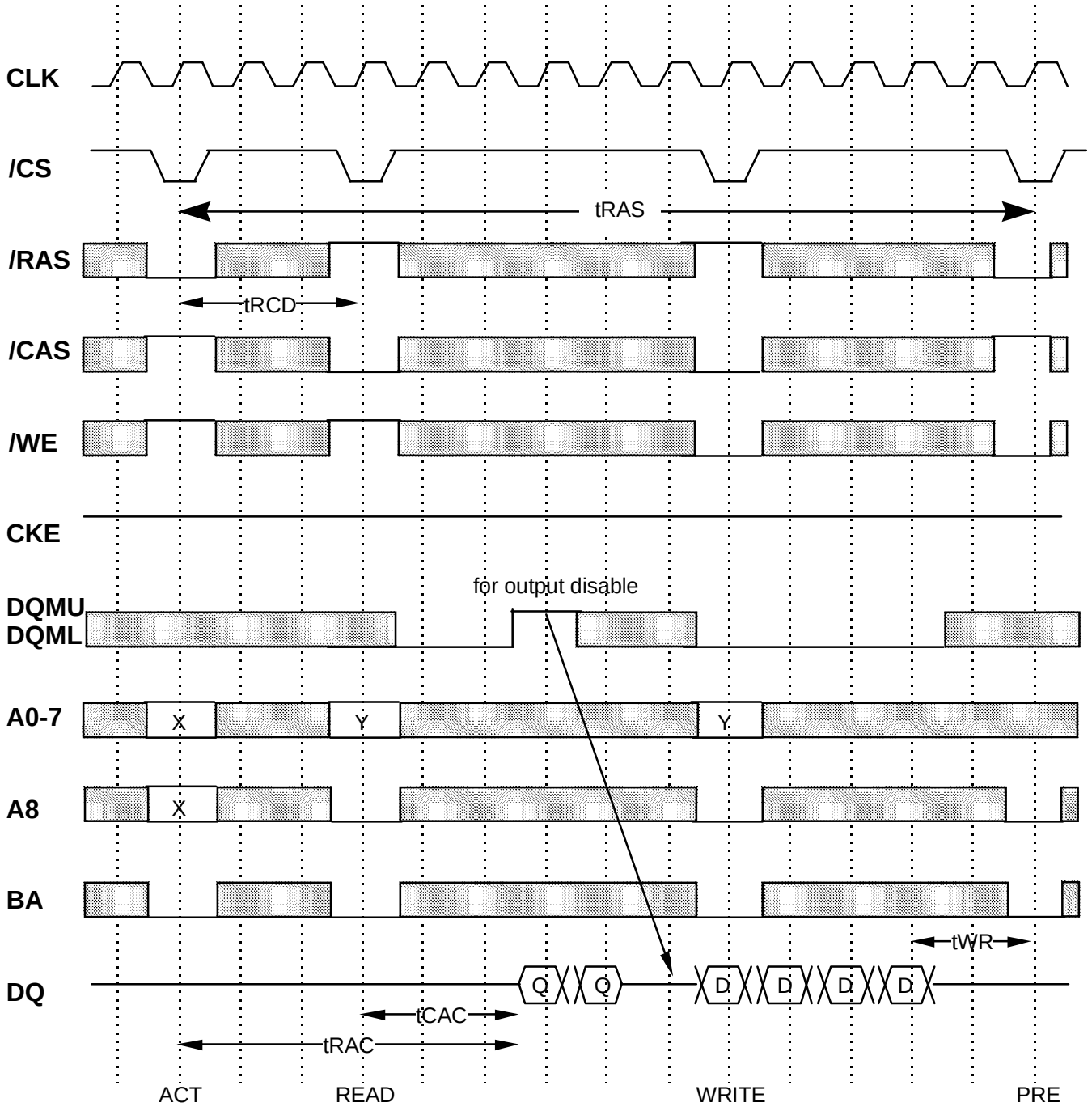


DQM Byte control for WRITE to READ (single bank)

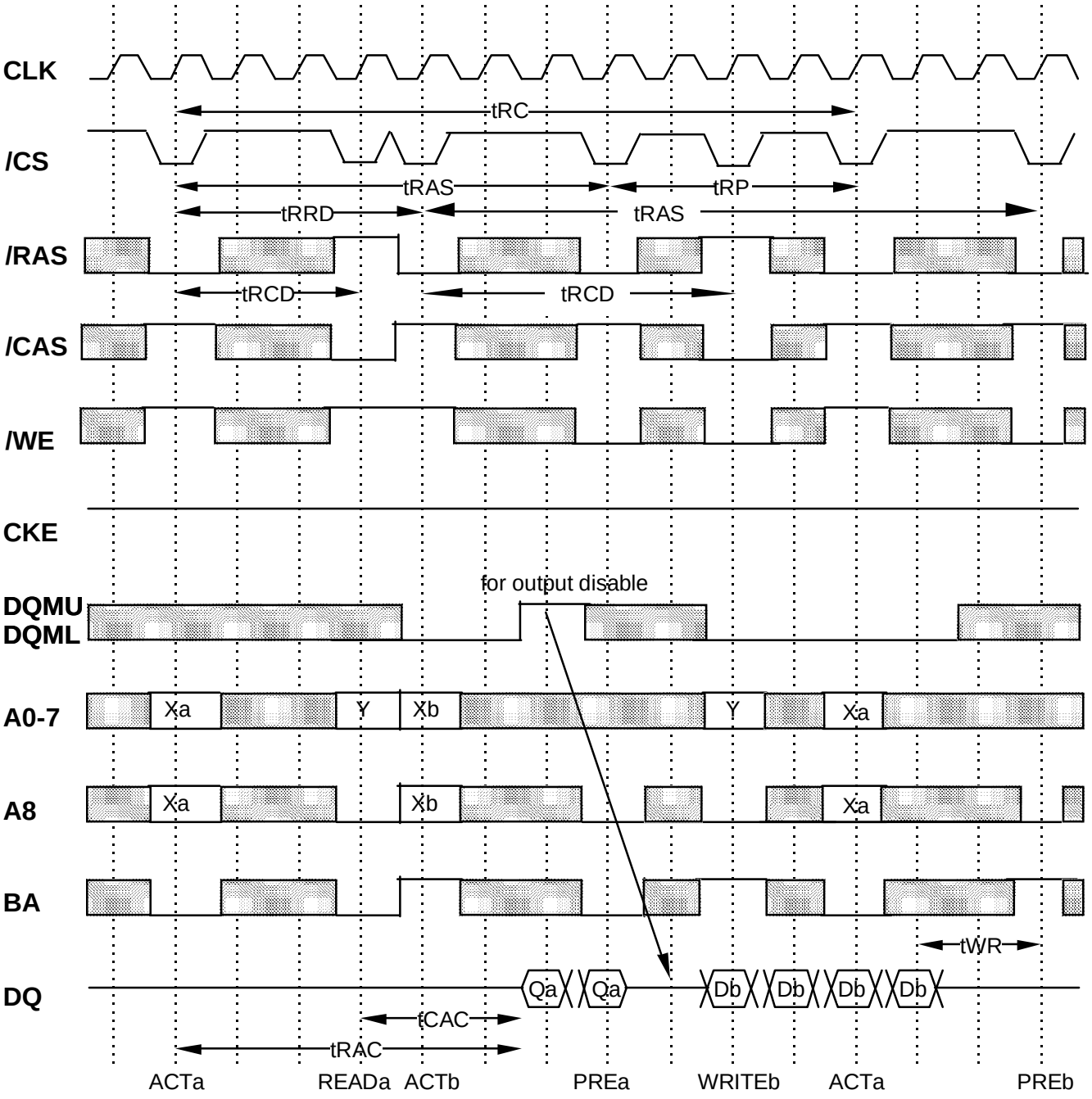
BL=4,CL=3



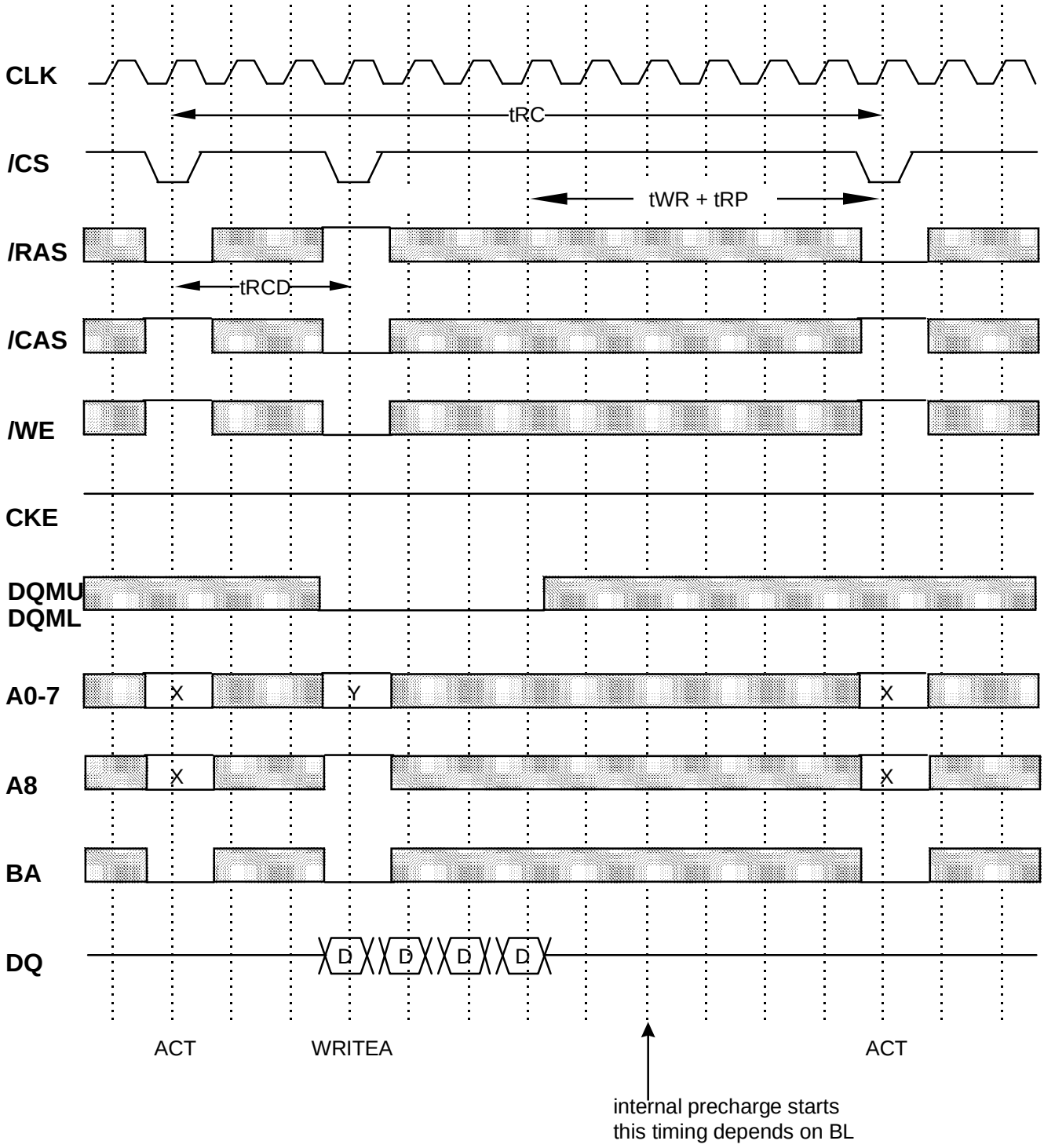
READ to WRITE (single bank) BL=4, CL=3



READ to WRITE (dual bank) BL=4, CL=3

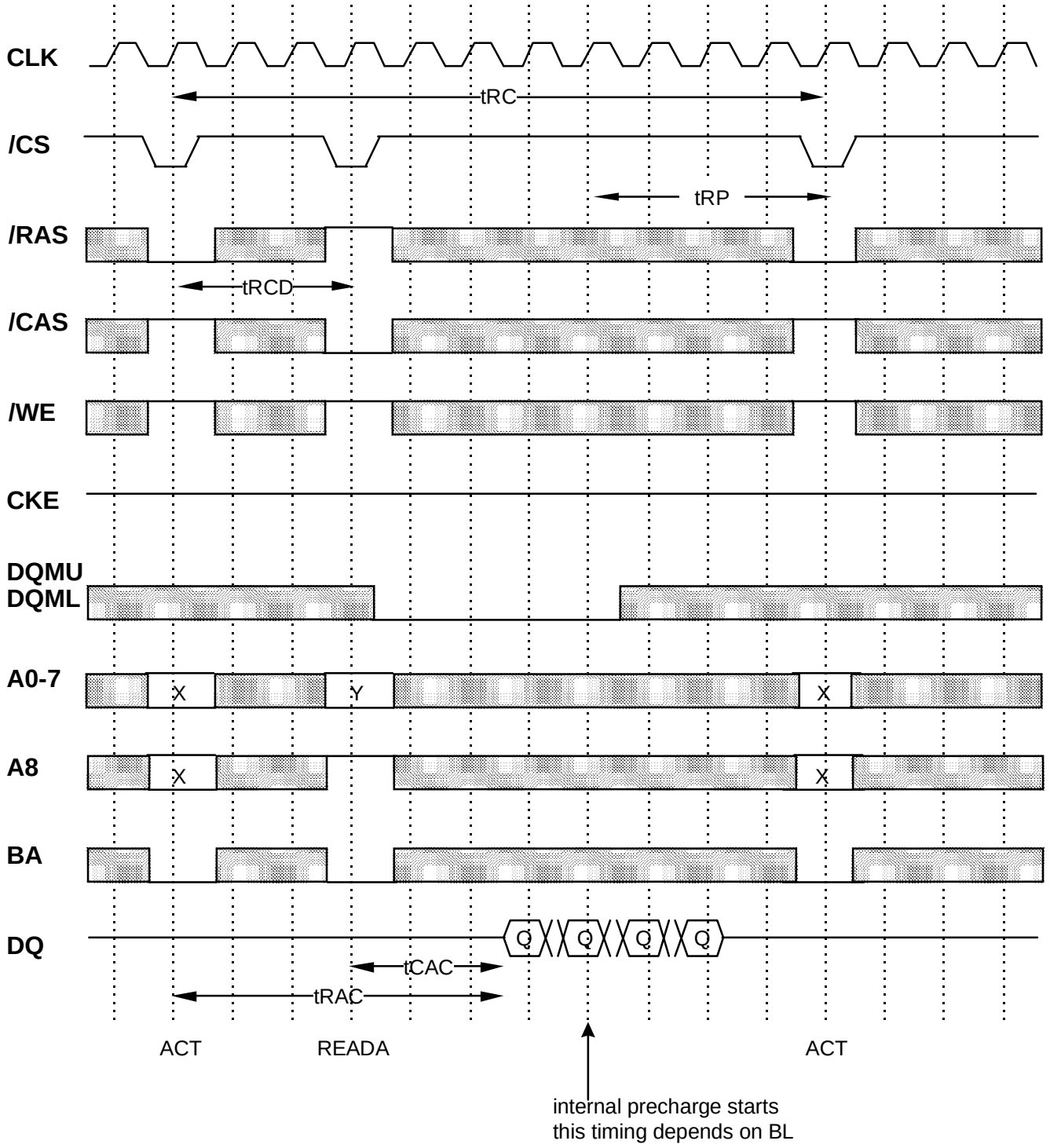


WRITE with AUTO-PRECHARGE (WRITEA) BL=4



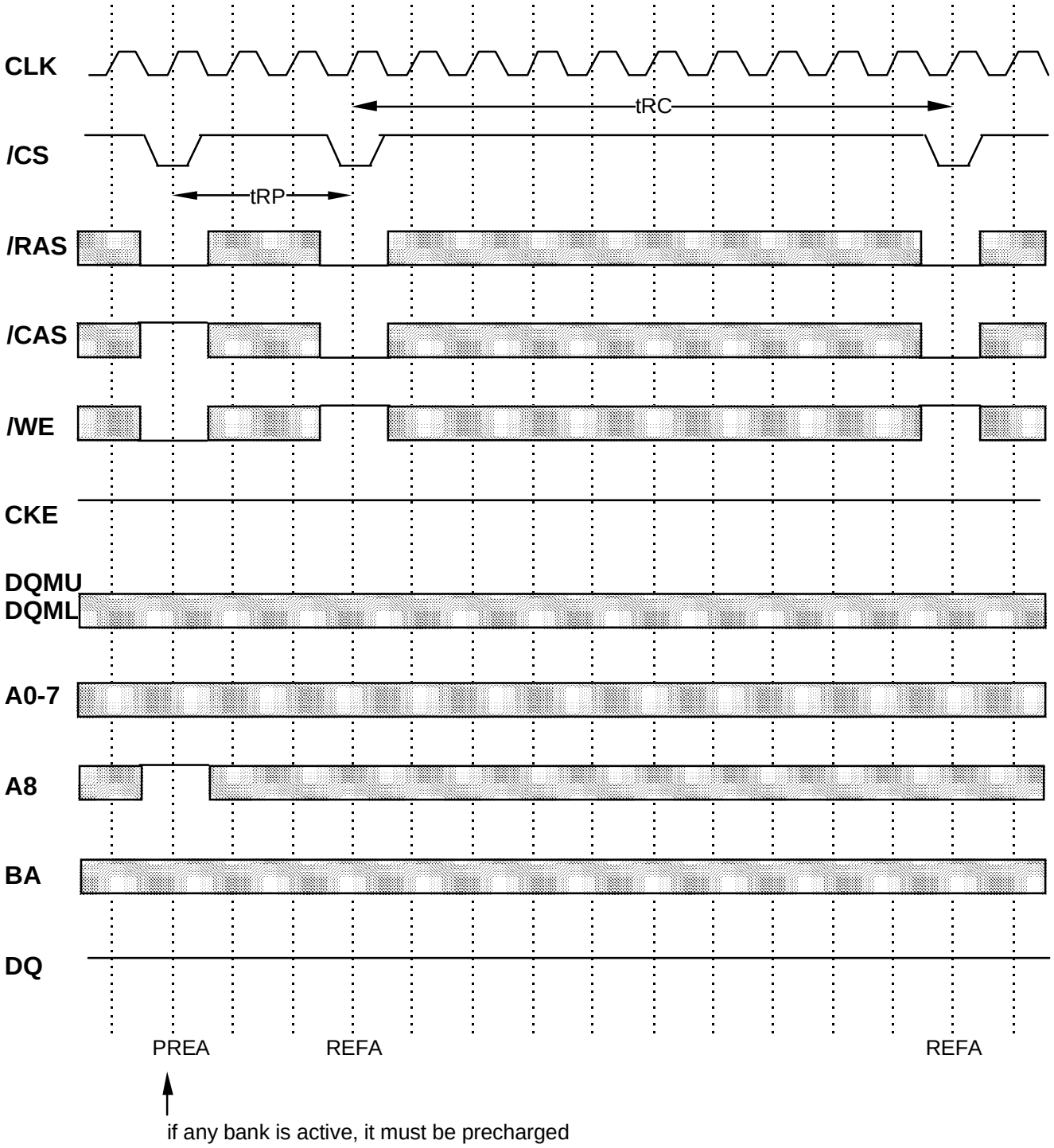
Note: WRITEA should **not** be used for Full Page (FP) burst operations.

READ with AUTO-PRECHARGE (READA) BL=4, CL=3

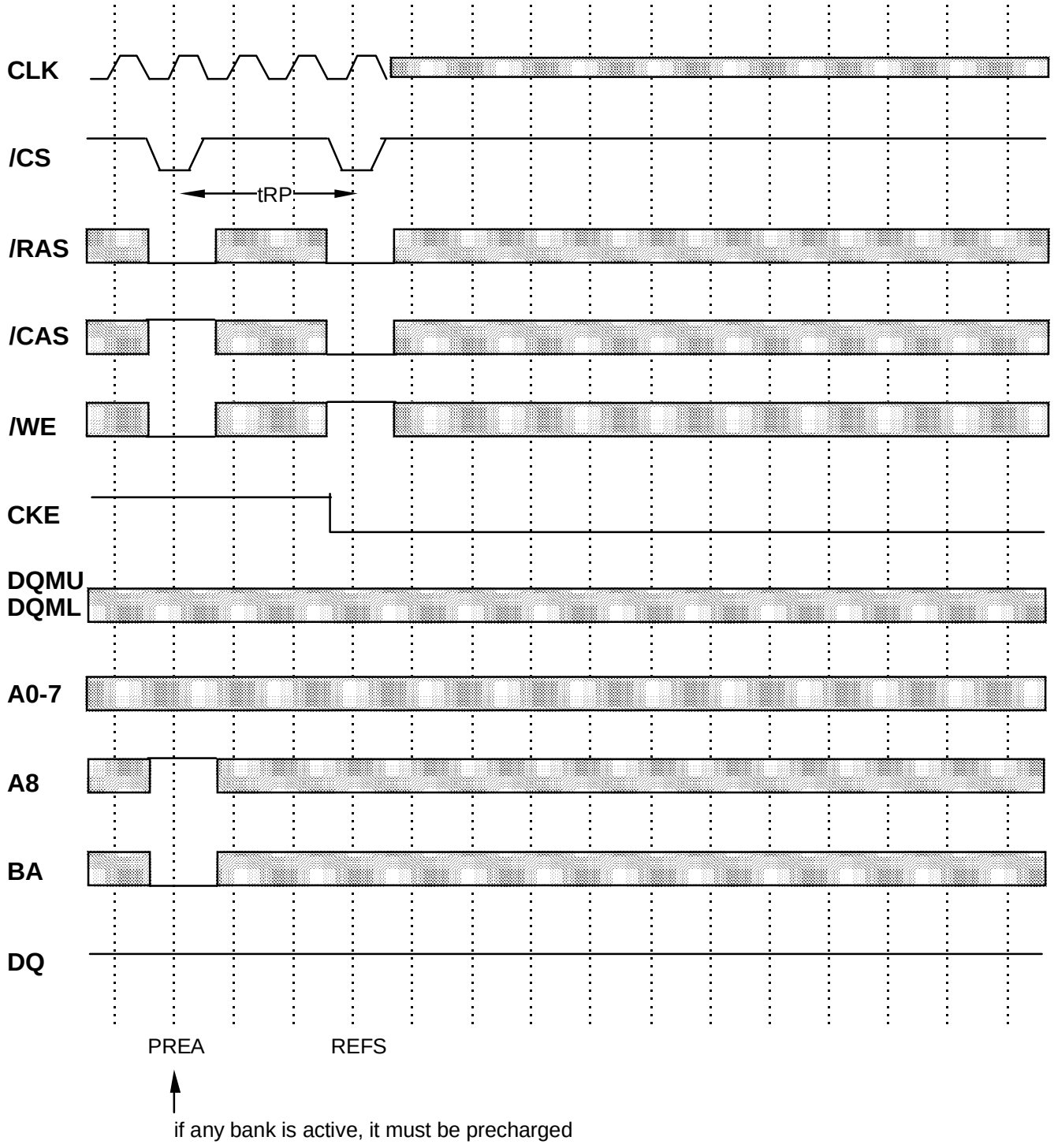


Note: READA should **not** be used for Full Page (FP) burst operations.

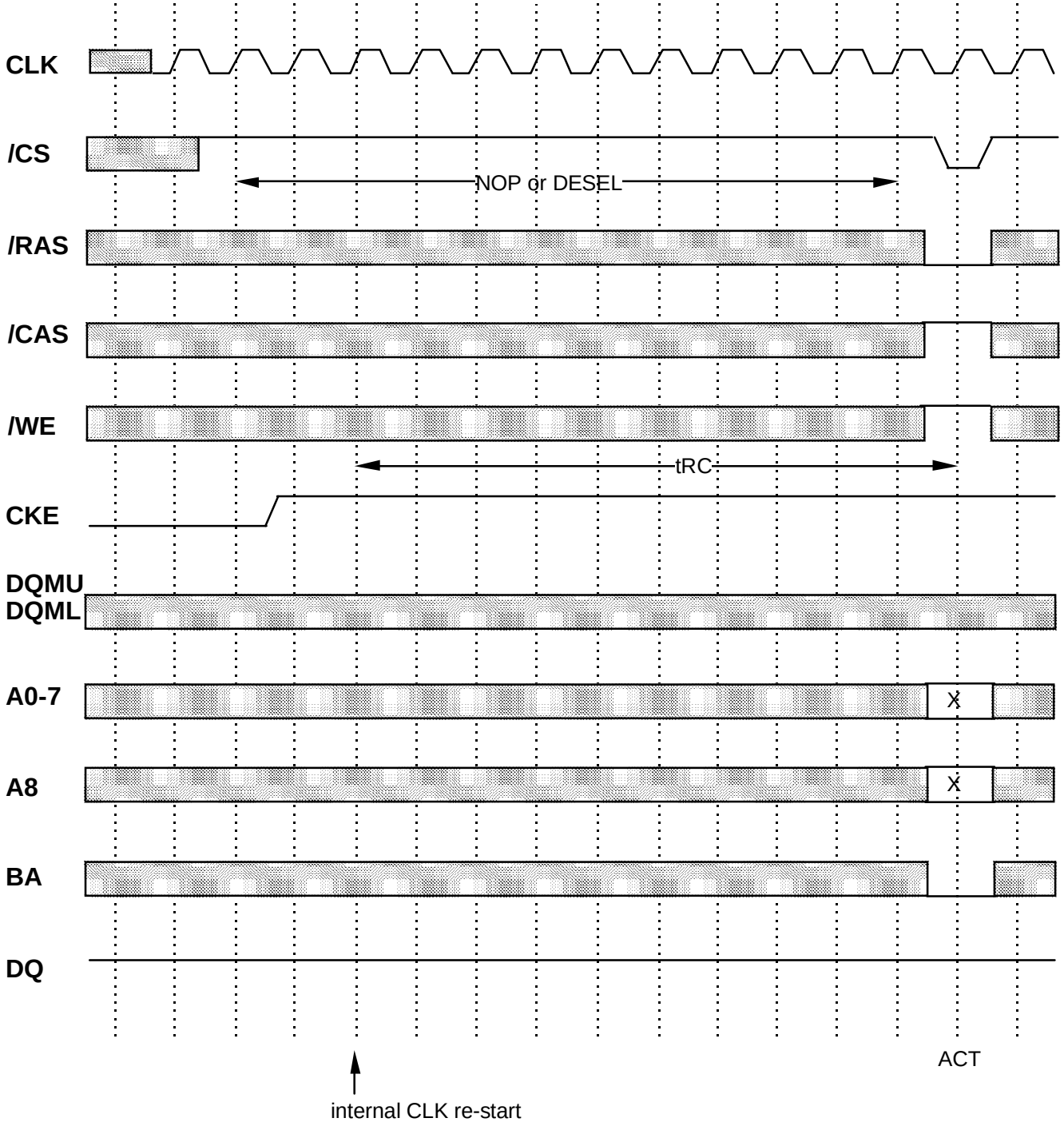
AUTO-REFRESH



SELF-REFRESH ENTRY

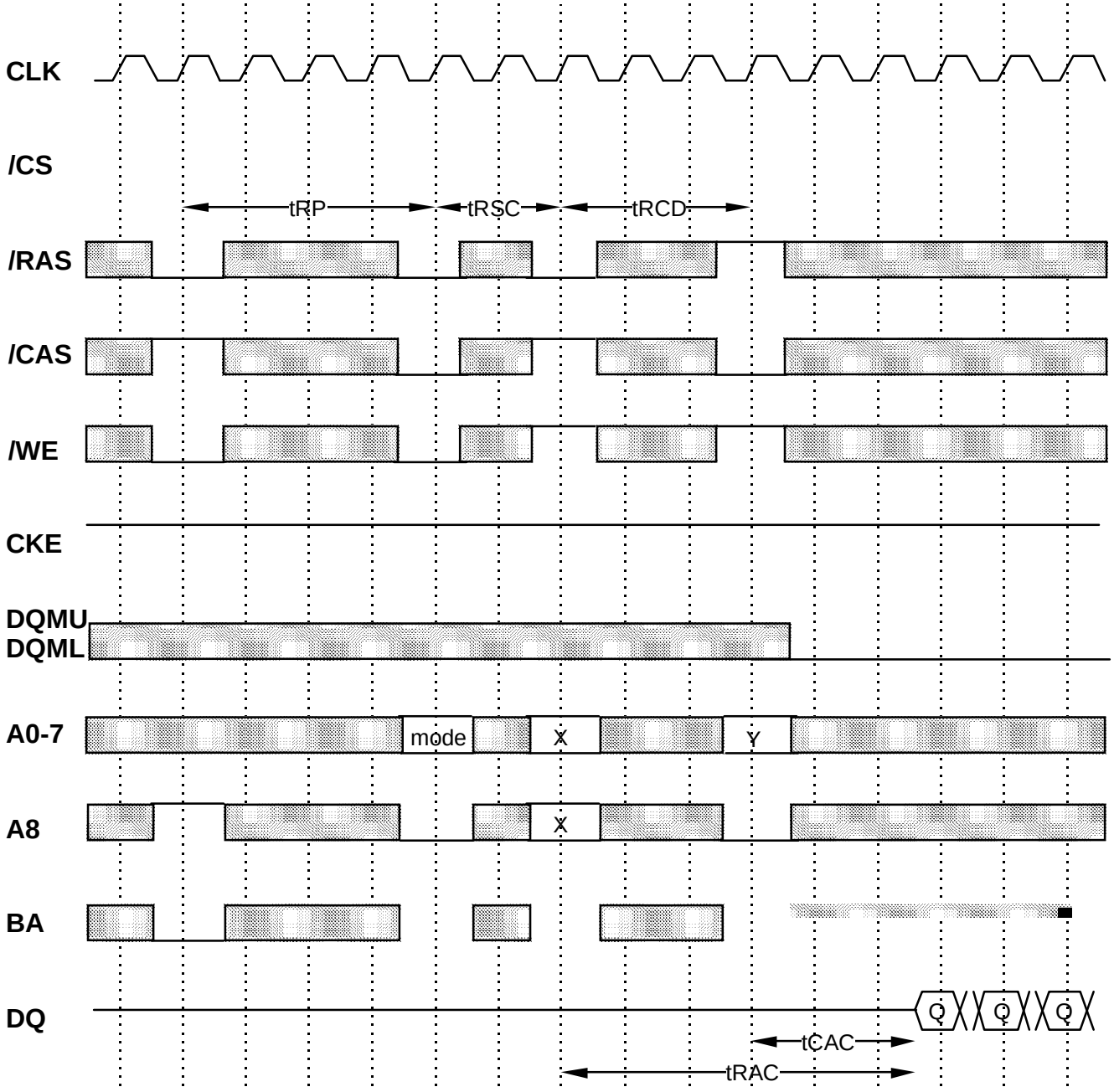


SELF-REFRESH EXIT



MODE REGISTER SET

BL=4, CL=3



if any bank is active, it must be precharged