1998.11.30 Ver.B

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M54R16AJ,ATP-10,-12,-15

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M54R16A is a family of 262144-word by 16-bit static RAMs, fabricated with the high performance CMOS process and designed for high speed application. These devices operate on a single 3.3V supply, and are directly TTL compatible.

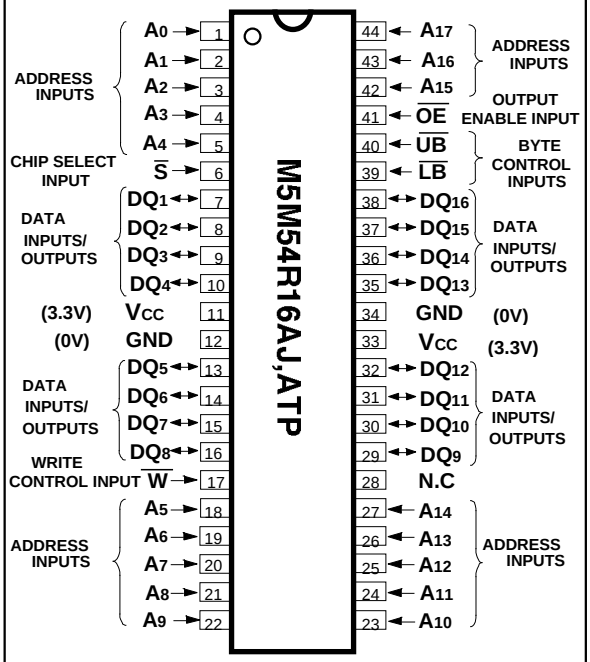
They include a power down feature as well. In write and read cycles, the lower and upper bytes are able to be controled either togethe or separately by $\overline{LB}$ and $\overline{UB}$.

FEATURES

•Fast access time M5M54R16AJ,ATP-10 ... 10ns(max)
M5M54R16AJ,ATP-12 ... 12ns(max)
M5M54R16AJ,ATP-15 ... 15ns(max)

•Single +3.3V power supply
•Fully static operation : No clocks, No refresh
•Common data I/O
•Easy memory expansion by $\overline{S}$
•Three-state outputs : OR-tie capability
•$\overline{OE}$ prevents data contention in the I/O bus
•Directly TTL compatible : All inputs and outputs
•Separate control of lower and upper bytes by LB and UB

PIN CONFIGURATION (TOP VIEW)



Outline 44P0K

APPLICATION

High-speed memory system

PACKAGE

M5M54R16AJ ..... 44pin 400mil SOJ
M5M54R16ATP ..... 44pin 400mil TSOP(II)

FUNCTION

The operation mode of the M5M54R16A is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$, $\overline{OE}$, $\overline{LB}$, and $\overline{UB}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with low level $\overline{LB}$ and/or low level $\overline{UB}$ and low level $\overline{S}$. The address must be set-up before write cycle and must be stable during the entire cycle.

The data is latched into a cell on the traling edge of $\overline{W}$, $\overline{LB}$, $\overline{UB}$ or $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is excuted by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{LB}$ and/or $\overline{UB}$ and $\overline{S}$ are in an active state. ($\overline{LB}$ and/or $\overline{UB}$=L, $\overline{S}$=L)

When setting $\overline{LB}$ at a high level and other pins are in an active state, upper-Byte are in a selectable mode in which both reading and writing are enable, and lower-Byte are in a non-selectable mode. And when setting $\overline{UB}$ at a high level and other pins are in an active state, lower-Byte are in a selectable mode in which both reading and writing are enable, and upper-Byte are in a non-selectable mode.

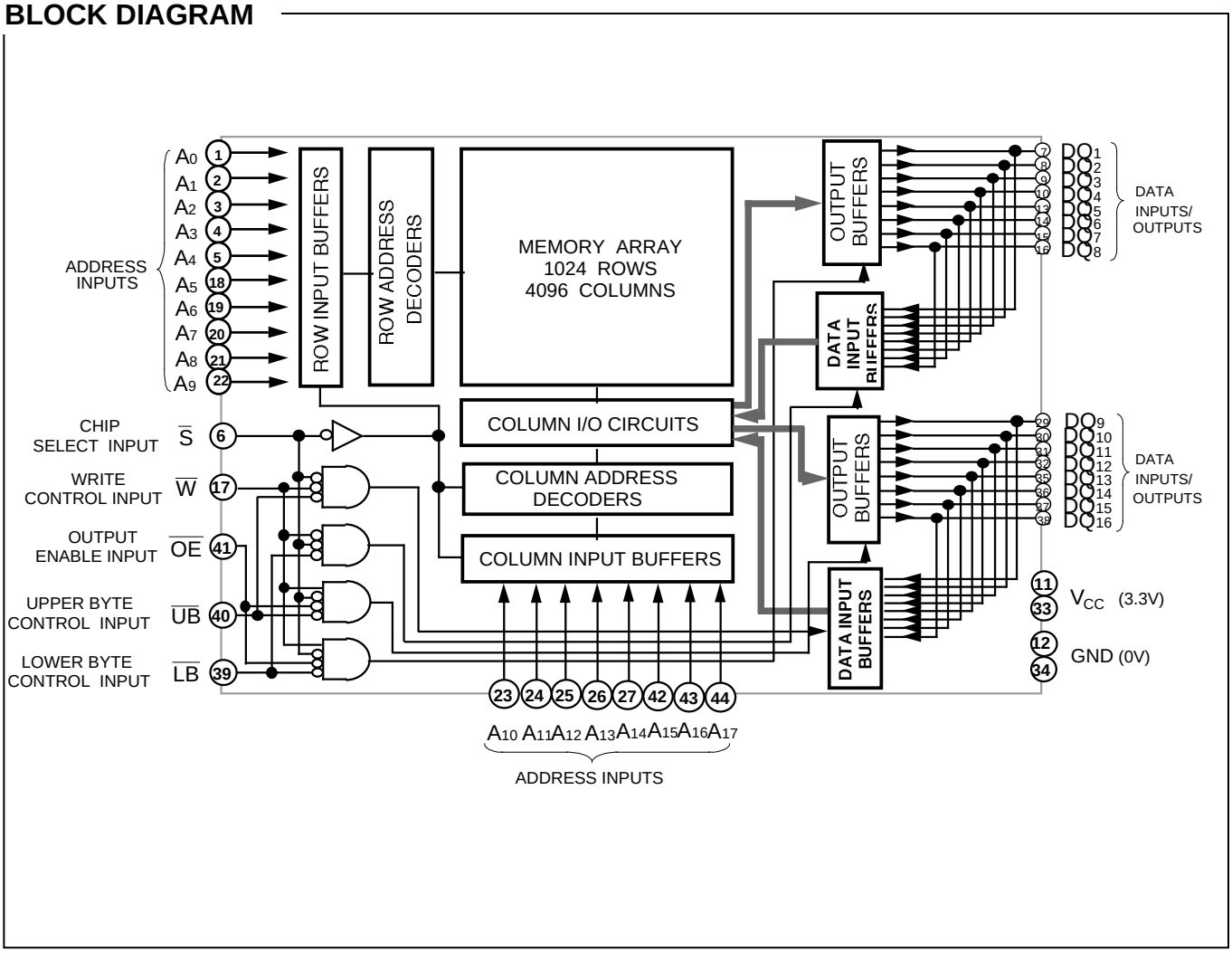
When setting $\overline{LB}$ and $\overline{UB}$ at a high level or $\overline{S}$ at high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{LB}$, $\overline{UB}$ and $\overline{S}$.

Signal-$\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissapation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	DQ1~8	DQ9~16	Icc
L	H	L	L	L	Read cycle All Bytes	D_{OUT}	D_{OUT}	Active
L	H	L	H	L	Read cycle Upper Bytes	High-impedance	D_{OUT}	Active
L	H	L	L	H	Read cycle Lower Bytes	D_{OUT}	High-impedance	Active
L	L	X	L	L	Write cycle All Bytes	D_{IN}	D_{IN}	Active
L	L	X	H	L	Write cycle Upper Bytes	High-impedance	D_{IN}	Active
L	L	X	L	H	Write cycle Lower Bytes	D_{IN}	High-impedance	Active
L	H	H	X	X	Output disable	High-impedance	High-impedance	Active
L	X	X	H	H				
H	X	X	X	X	Non selection	High-impedance	High-impedance	Stand by

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{cc}	Supply voltage	With respect to GND	- 2.0*~ 4.6	V
V_I	Input voltage		- 2.0*~ Vcc+0.5	V
V_O	Output voltage		- 2.0*~ Vcc	V
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
$T_{stg(bias)}$	Storage temperature(bias)		- 10 ~ 85	°C
T_{stg}	Storage temperature		- 65 ~ 150	°C

*Pulse width ≦3ns, In case of DC: - 0.5V

DC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V $^{+10\%}_{-5\%}$,unless otherwise noted)

Symbol	Parameter	Condition		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	I_{OH} = - 4mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL}= 8mA				0.4	V
I_I	Input current	V_I = 0 ~ Vcc				2	uA
$\lvert I_{OZ} \rvert$	Output current in off-state	$V_{I(\overline{S})}$= V_{IH} V_O= 0 ~ Vcc				2	uA
I_{CC1}	Active supply current (TTL level)	$V_{I(\overline{S})}$= V_{IL} other inputs V_{IH} or V_{IL} Output-open(duty 100%)	AC(10ns cycle)			260	mA
			AC(12ns cycle)			250	
			AC(15ns cycle)			230	
			DC			120	
I_{CC2}	Stand-by supply current (TTL level)	$V_{I(\overline{S})}$= V_{IH}	AC(10ns cycle)			90	mA
			AC(12ns cycle)			70	
			AC(15ns cycle)			60	
			DC			40	
I_{CC3}	Stand-by current (MOS level)	$V_{I(\overline{S})}$= Vcc - 0.2V other inputs $V_I \leqq 0.2V$ or $V_I \geqq$ Vcc - 0.2V				10	mA

Note 1: Direction for current flowing into an IC is positive (no mark).

CAPACITANCE (Ta=0~70°C , Vcc=3.3V $^{+10\%}_{-5\%}$,unless otherwise noted)

Symbol	Parameter	Test Condition	Limit Min	Limit Typ	Limit Max	Unit
C_I	Input capacitance	V_I =GND,V_i =25mVrms,f=1MHz			7	pF
C_O	Output capacitance	V_o =GND,V_o =25mVrms,f=1MHz			8	pF

Note 2: C_I,C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta= 0~70 °C ,Vcc=3.3V $^{+10\%}_{-5\%}$,unless otherwise noted)

(1) MEASUREMENT CONDITION

Input pulse levels ..... V_{IH}=3.0V,V_{IL}=0.0V
Input rise and fall time 3ns
Input timing reference levels ..... V_{IH}=1.5V,V_{IL}=1.5V
Output timing reference levels ..... V_{OH}=1.5V, V_{OL}=1.5V
Output loads ..... Fig1 ,Fig2

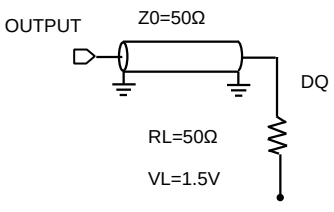


Fig.1 Output load

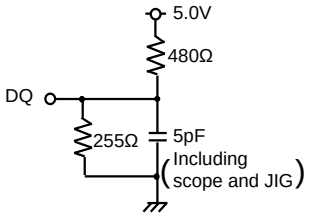


Fig.2 Output load for t_{en}, t_{dis}

READ CYCLE

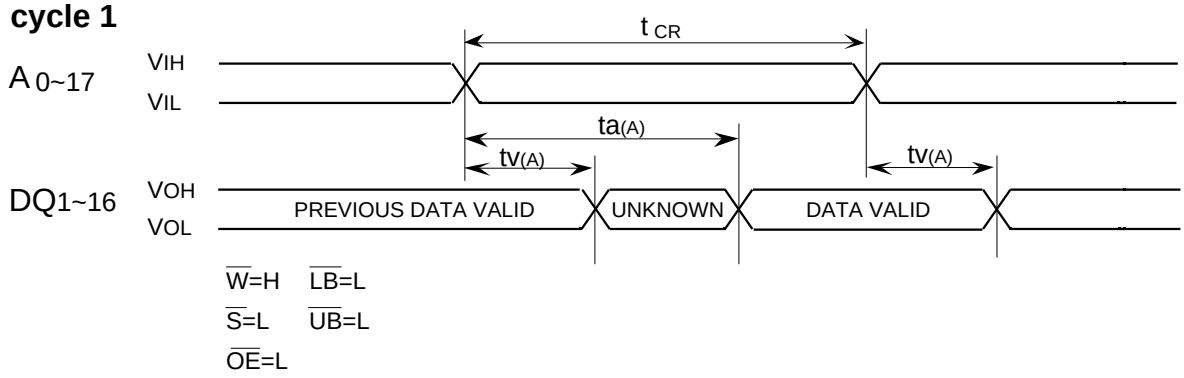
Symbol	Parameter	Limits						Unit
		M5M54R16AJ,ATP-10		M5M54R16AJ,ATP-12		M5M54R16AJ,ATP-15		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	10		12		15		ns
ta(A)	Address access time		10		12		15	ns
ta(S)	Chip select access time		10		12		15	ns
ta(OE)	Output enable access time		5		6		7	ns
ta(B)	$\overline{LB}$,$\overline{UB}$ access time		5		6		7	ns
tdis(S)	Output disable time after $\overline{S}$ high	0	5	0	6	0	7	ns
tdis(OE)	Output disable time after $\overline{OE}$ high	0	5	0	6	0	7	ns
tdis(B)	Output disable time after $\overline{LB}$,$\overline{UB}$ high	0	5	0	6	0	7	ns
ten(S)	Output enable time after $\overline{S}$ low	2		3		3		ns
ten(OE)	Output enable time after $\overline{OE}$ low	0		1		1		ns
ten(B)	Output enable time after $\overline{LB}$,$\overline{UB}$ low	0		1		1		ns
tv(A)	Data valid time after address change	2		3		3		ns
tPU	Power-up time after chip selection	0		0		0		ns
tPD	Power-down time after chip selection		10		12		15	ns

Write cycle

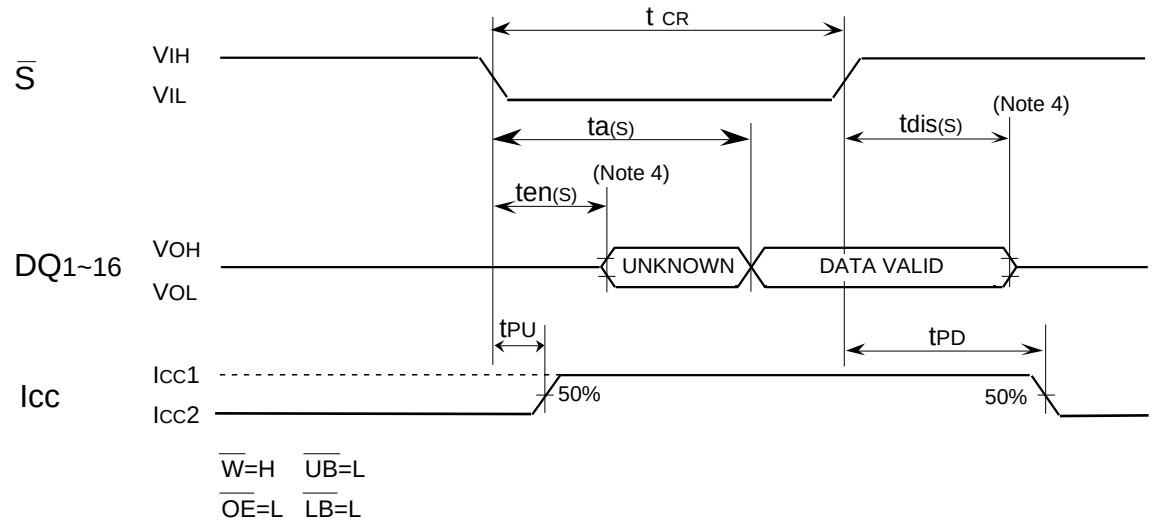
Symbol	Parameter	Limits						Unit
		M5M54R16AJ,ATP-10		M5M54R16AJ,ATP-12		M5M54R16AJ,ATP-15		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	10		12		15		ns
tw(W)	Write pulse width ($\overline{OE}$ low)	10		12		15		ns
tw(W)	Write pulse width($\overline{OE}$ high)	8		10		10		ns
tsu(B)	$\overline{LB}$,$\overline{UB}$ setup time	8		10		10		ns
tsu(A)1	Address setup time($\overline{W}$)	0		0		0		ns
tsu(A)2	Address setup time($\overline{S}$)	0		0		0		ns
tsu(S)	Chip select setup time	8		10		10		ns
tsu(D)	Data setup time	5		6		7		ns
th(D)	Data hold time	0		0		0		ns
trec(W)	Write recovery time	1		1		1		ns
tdis(W)	Output disable time after $\overline{W}$ low	0	5	0	6	0	7	ns
tdis(OE)	Output disable time after $\overline{OE}$ high	0	5	0	6	0	7	ns
ten(W)	Output enable time after $\overline{W}$ high	0		0		0		ns
ten(OE)	Output enable time after $\overline{OE}$ low	0		0		0		ns
ten(B)	Output enable time after $\overline{LB}$,$\overline{UB}$ low	0		0		0		ns
tsu(A-$\overline{W}$H)	Address to $\overline{W}$ High	8		10		10		ns
tsu(A-$\overline{S}$H)	Address to $\overline{S}$ High	8		10		10		ns
tsu(A-$\overline{B}$H)	Address to $\overline{LB}$,$\overline{UB}$ High	8		10		10		ns

(4)TIMING DIAGRAMS

Read cycle 1

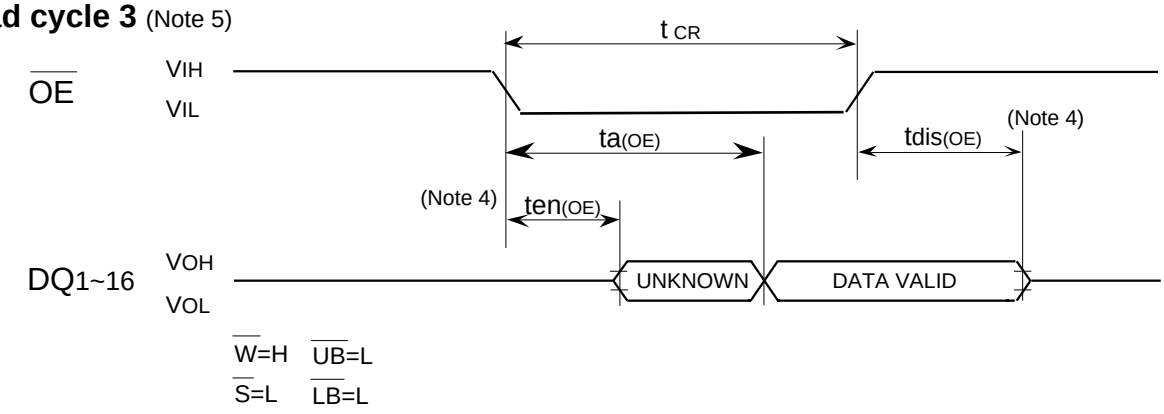


Read cycle 2 (Note 3)



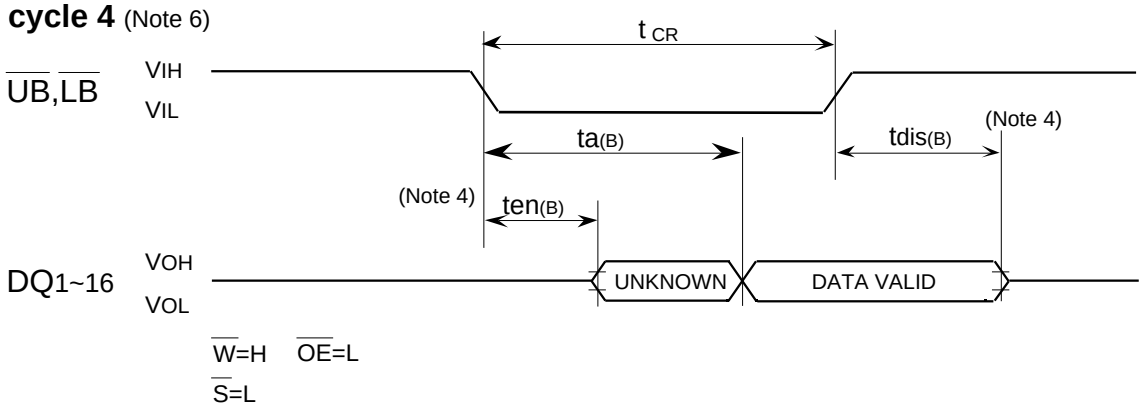
Note 3. Addresses valid prior to or coincident with S transition low.
4. Transition is measured ±500mv from steady state voltage with specified loading in Figure 2.

Read cycle 3 (Note 5)



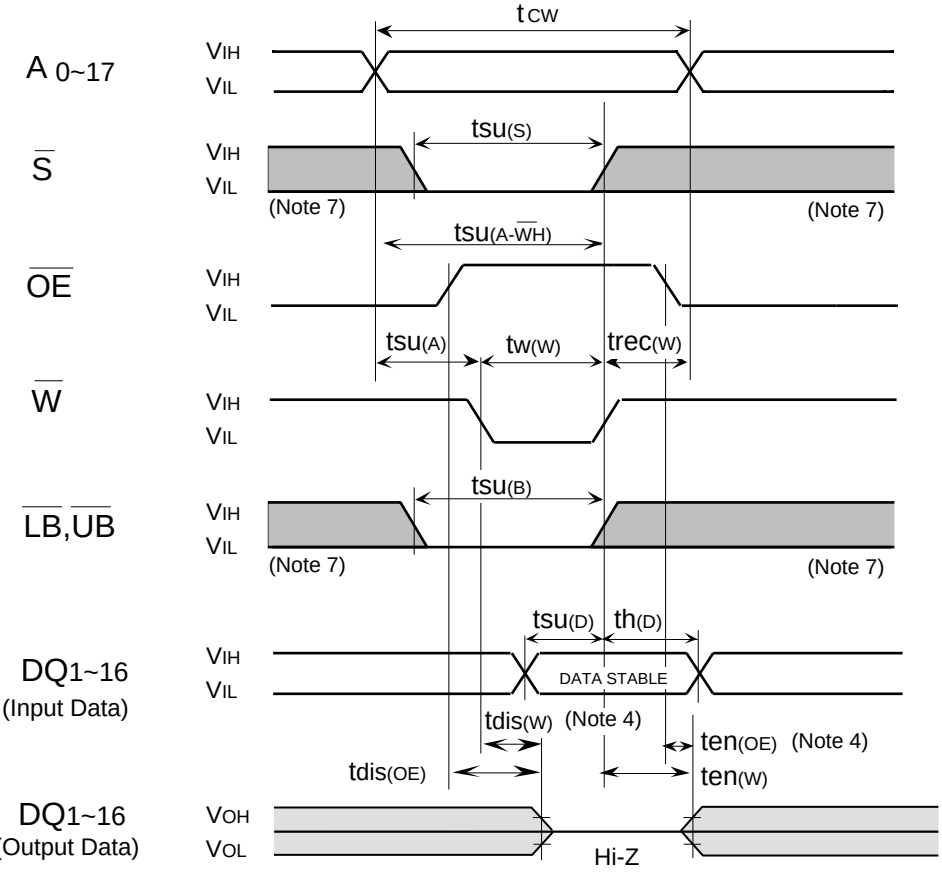
Note 5. Addresses and S valid prior to OE transition low by (ta(A)-ta(OE)), (ta(S)-ta(OE))

Read cycle 4 (Note 6)



Note 6. Addresses , S and OE valid prior to LB,UB transition low by (ta(A)-ta(B)), (ta(S)-ta(B)), (ta(OE)-ta(B)).

Write cycle (W control mode)

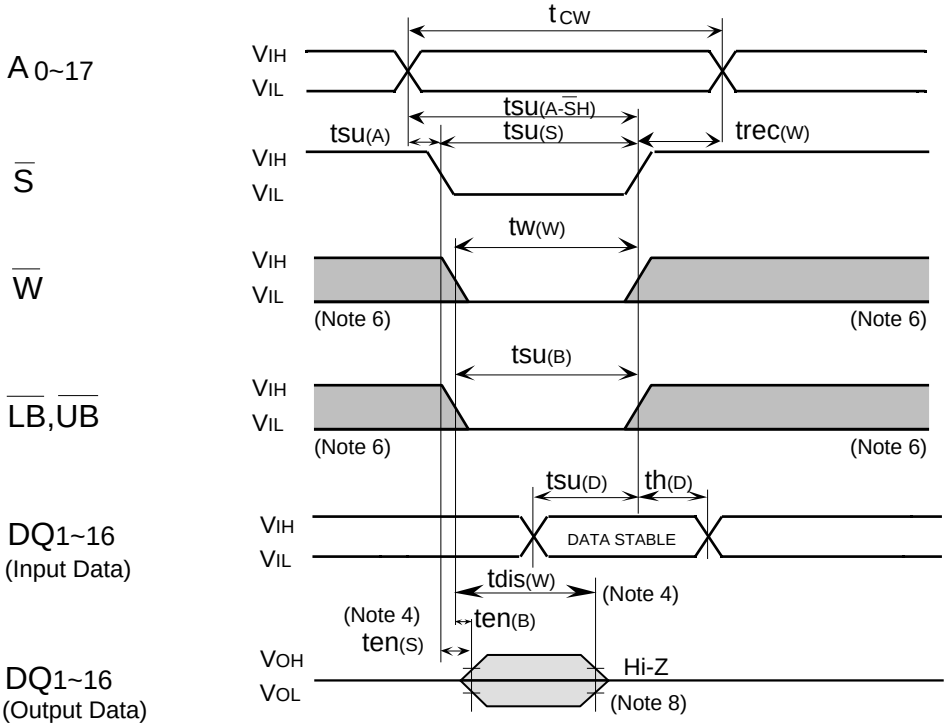


Note 7: Hatching indicates the state is don't care.

8: When the falling edge of W is simultaneous or prior to the falling edge of S, the output is maintained in the high impedance.

9: ten,tdis are periodically sampled and are not 100% tested.

Write cycle($\overline{S}$ control)



Write cycle($\overline{LB}$,$\overline{UB}$ control)