Preliminary

M69897VP

16:1 2.488 Gbps Multiplexer

DESCRIPTION

The M69897VP multiplexer chip is an integrated serialization SONET OC-48 (2.488 Gbps) interface device. The chip performs parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based ATM applications.
The merits of SOI (Silicon-On-Insulator) technology, such as low voltage operation, low substrate noise and good compatibility with standard CMOS technology, are fully utilized in the chip design to achieve low jitter and low power operation and small package outline of 64-pin PQFP.

FEATURES

- Single 1.8 V power supply
- Supports 2.488 Gbps (OC-48, STM-16)
- 16-bit single-ended PECL interface
- On-chip high-frequency PLL for clock generation
- 155.52 MHz reference frequency
- Low power consumption
- Available in 64 PQFP
- Parity check function

APPLICATIONS

- SONET/SDH systems
- Fiber optic systems
- High-speed back plane interconnect and point-to-point data links

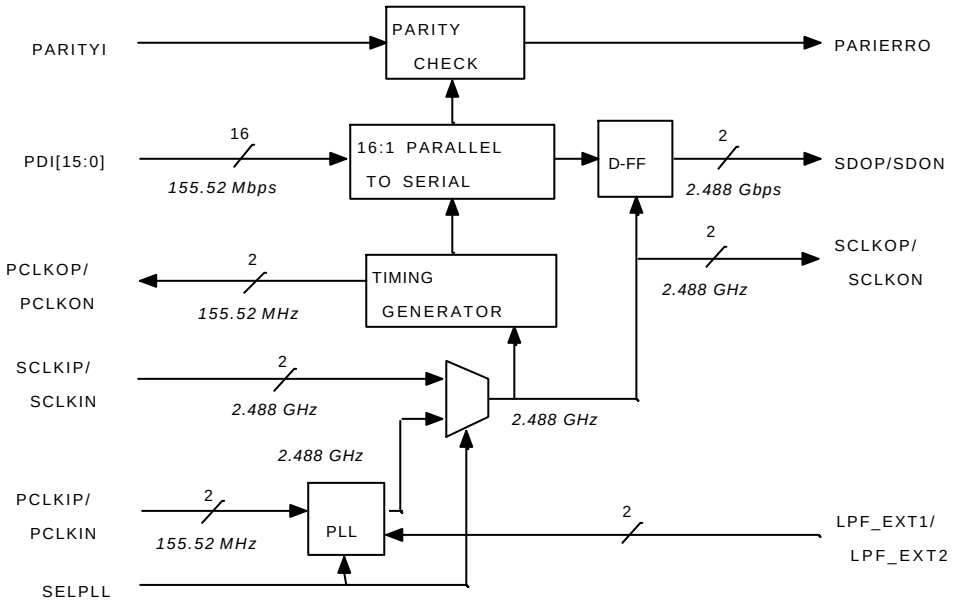


Figure 1 Functional Block Diagram

Table 1 Absolute Maximum Ratings

PARAMETER	MIN	TYP	MAX	UNITS
Storage Temperature	-65		150	ûC
Voltage on V_{DD} with Respect to GND	-0.5		2.2	V
Voltage on any PECL Pin	0		2.2	V
ESD Rating (HBM model)	1000			V

Table 2 Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Ambient Temperature Under Bias	0		70	ûC	
Junction Temperature Under Bias			110	ûC	
Voltage on V_{DD} with Respect to GND	1.71	1.8	1.89	V	
Power Consumption		260	310	mW	All Outputs Unterminated.
		320	420	mW	All Outputs Terminated.

Table 3 Differential PECL Input DC Characteristics

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	GND		V_{DD} -1.4	V	
V_{IH}	Input High Voltage	V_{DD} -1.2		V_{DD} -0.8	V	
$ÆV_{INDIFF}$	Differential Input Voltage Swing	0.2		1.1	V	See Figure 12.

Table 4 Single-Ended PECL Input DC Characteristics

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	GND		V_{DD} -1.5	V	
V_{IH}	Input High Voltage	V_{DD} -1.1		V_{DD} -0.8	V	
$ÆV_{IN}$	Input Voltage Swing	0.4		1.1	V	See Figure 12.

Table 5 CMOS Input DC Characteristics

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	GND		V_{DD} -1.3	V	
V_{IH}	Input High Voltage	V_{DD} -0.5		V_{DD}	V	

Table 6 Differential PECL Output DC Characteristics

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	CONDITIONS
V_{OL}	Output Low Voltage	GND		0.1	V	
V_{OH}	Output High Voltage	V_{DD} -0.9		V_{DD} -0.8	V	
$ÆV_{OUTDIFF}$	Differential Output Voltage Swing	0.7		1.1	V	See Figure 12.

Table 7 Single-Ended PECL Output DC Characteristics

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	CONDITIONS
V_{OL}	Output Low Voltage	GND		0.1	V	
V_{OH}	Output High Voltage	V_{DD} -0.9		V_{DD} -0.8	V	
$ÆV_{OUT}$	Output Voltage Swing	0.7		1.1	V	See Figure 12.

Table 8 Clock Jitter Characteristics

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	CONDITIONS
T_{jitter}	Output Jitter			0.01	UIrms	
F_{-3dB}	Jitter Transfer (12K-20MHz)			10	MHz	
F_{peak}	Jitter Transfer Peaking		0.1		dB	

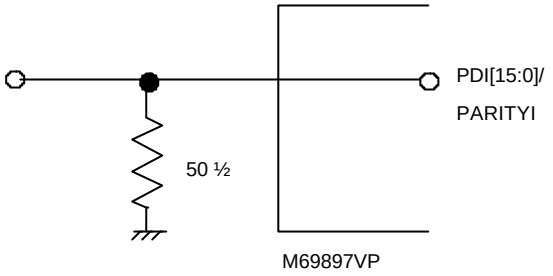


Figure 2 Single-Ended PECL Input DC Termination

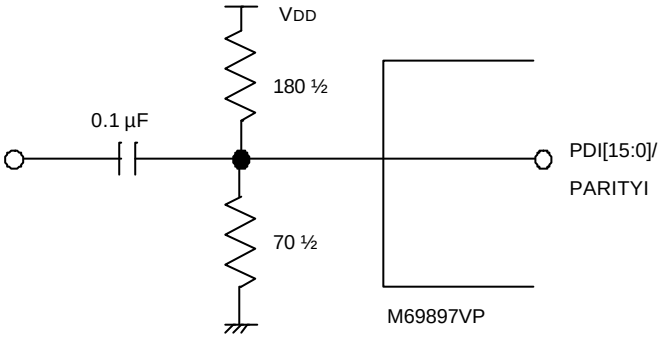


Figure 3 Single-Ended PECL Input AC Termination

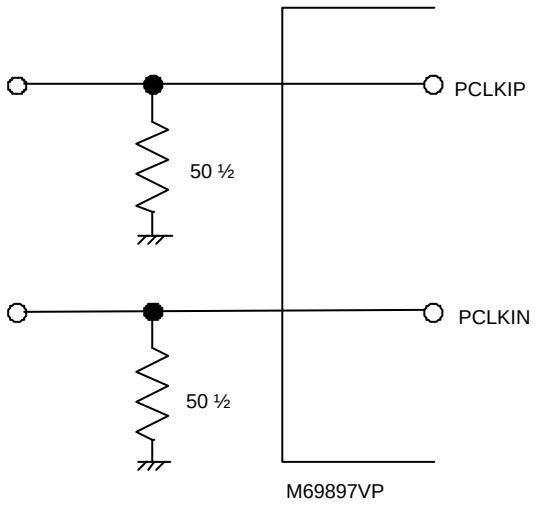


Figure 4 Differential PECL Input DC Termination for 155.52 MHz Clock.

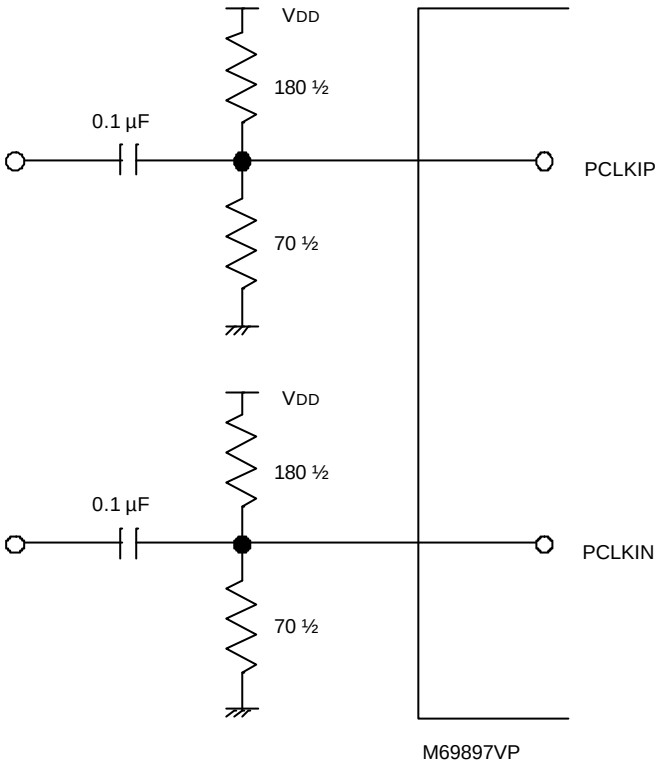


Figure 5 Differential PECL Input AC Termination for 155.52 MHz Clock.

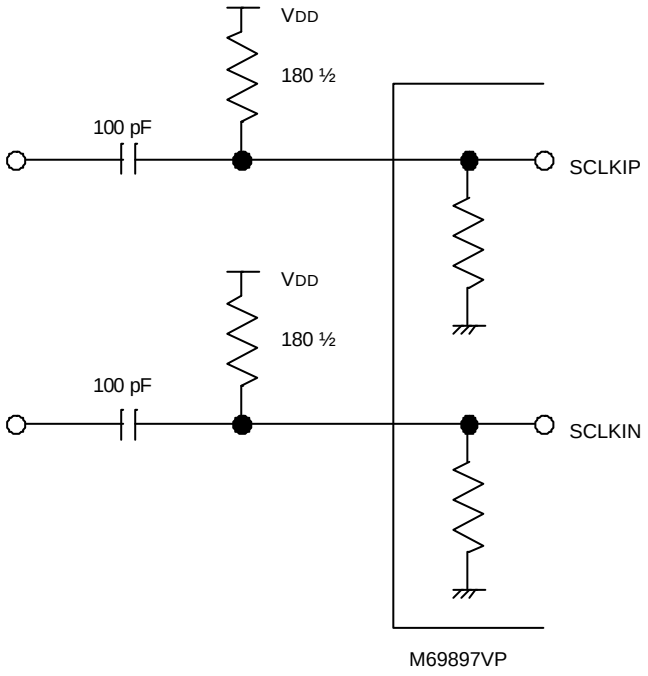


Figure 6 Differential PECL Input AC Termination for 2.488 GHz Clock
(Used for Internal PLL off-state mode).

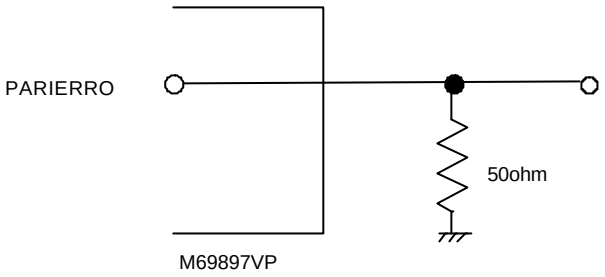
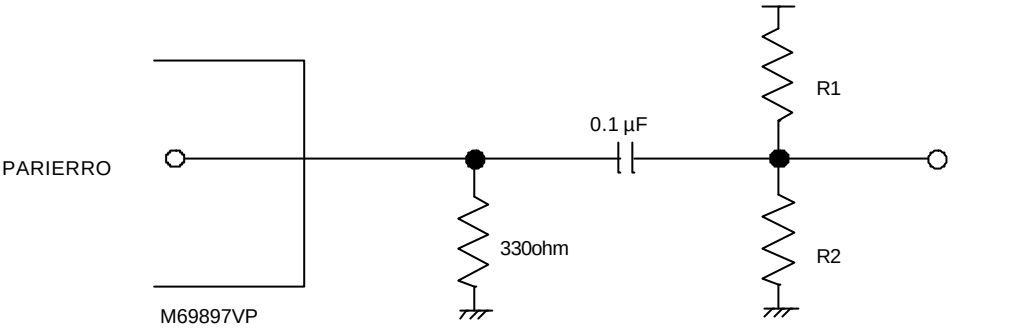


Figure 7 Single-Ended PECL Output DC Termination



R1xR2/(R1+R2) = 50ohm

Figure 8 Single-Ended PECL Output AC Termination

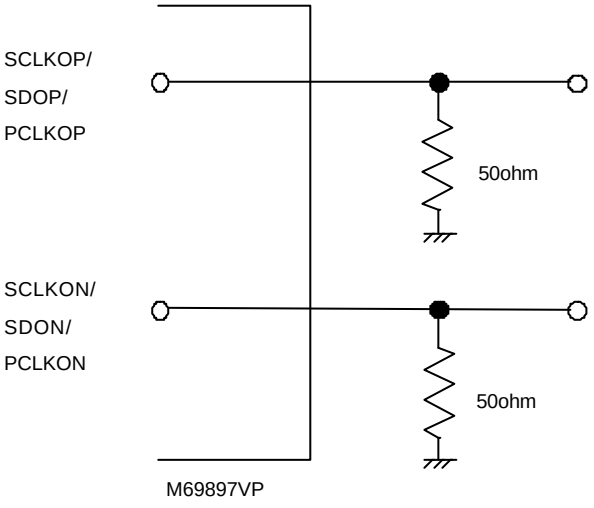


Figure 9 Differential PECL Output DC Termination

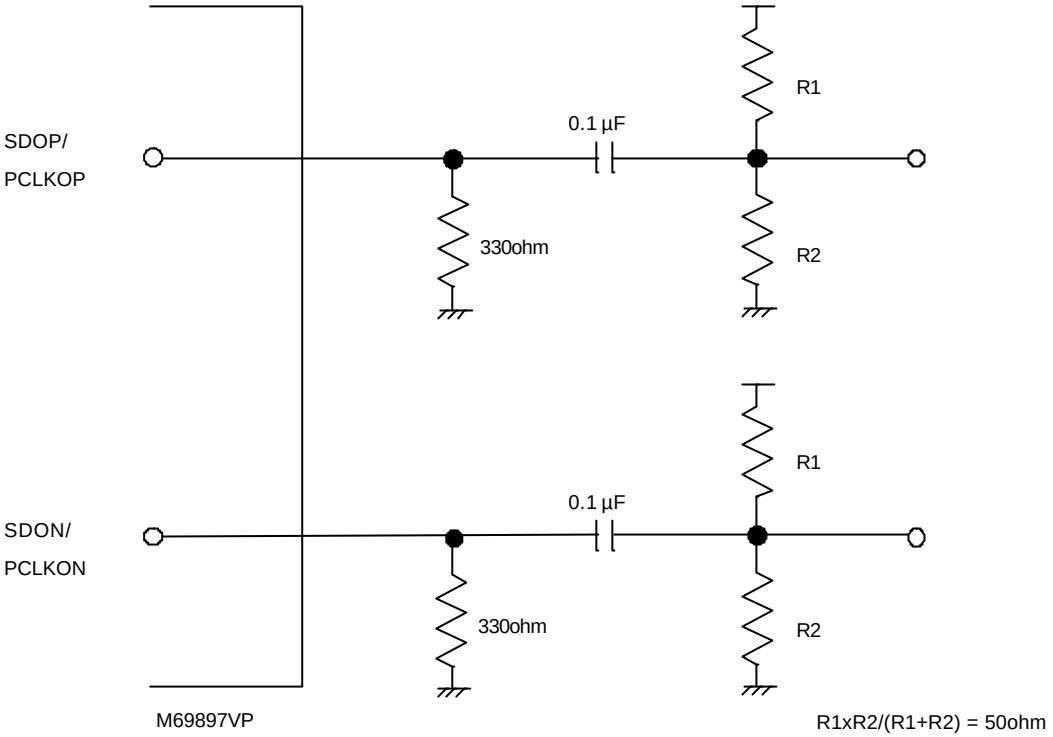


Figure 10 Differential PECL Output AC Termination

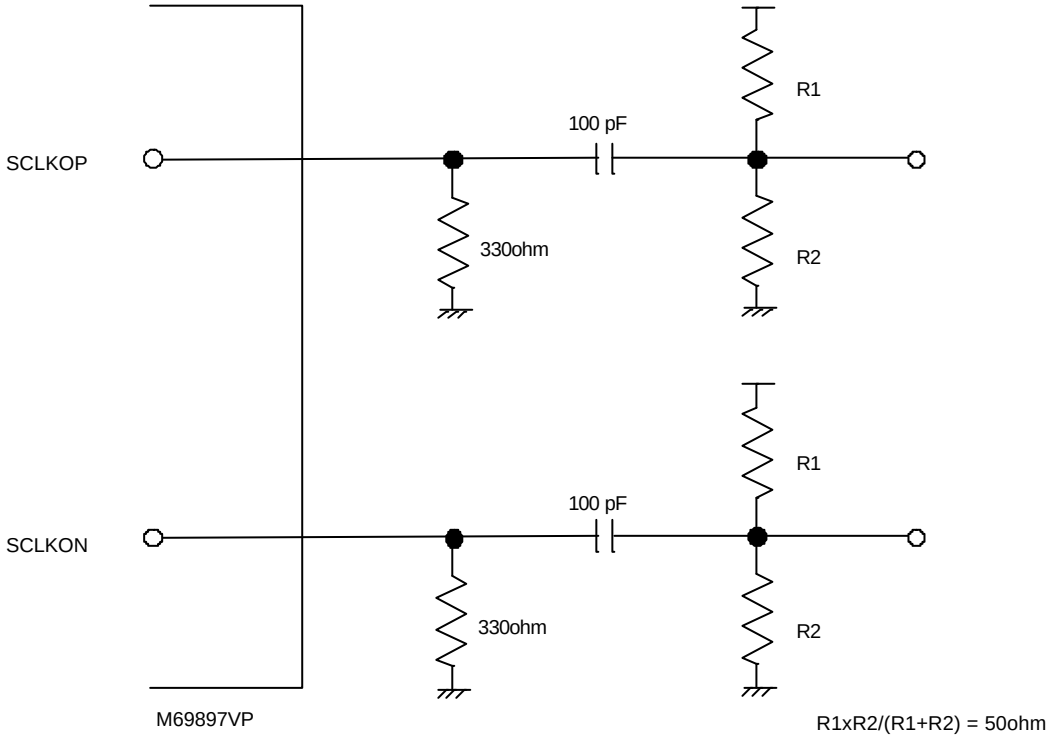


Figure 11 Differential PECL Output AC Termination for 2.488 GHz Clock Output

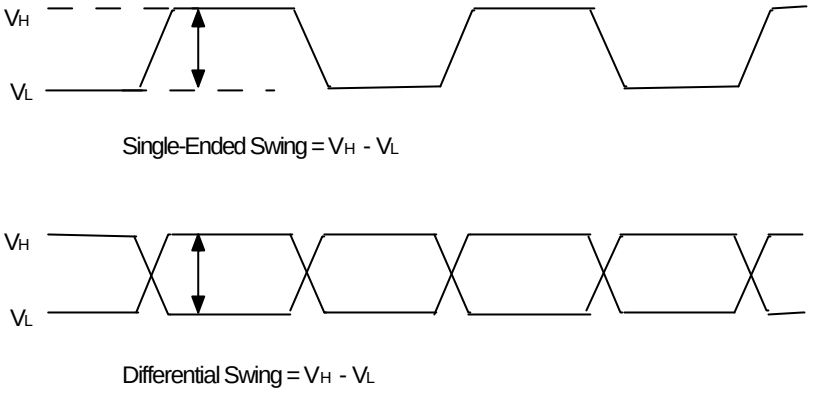


Figure 12 Voltage Swing

Table 9 AC Characteristics

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
	Serial Clock Rate		2.488		GHz
T_{DS}	Parallel Data Setup Time wrt PCLKIP	1.0			ns
T_{DH}	Parallel Data Hold Time wrt PCLKIP	1.0			ns
T_{DS2}	Parallel Data Setup Time wrt PCLKOP	1.0			ns
T_{DH2}	Parallel Data Hold Time wrt PCLKOP	1.0			ns
	Parallel Clock Input Duty Cycle	40		60	%
	Parallel Clock Output Duty Cycle	45		55	%
	Serial Clock Output to Serial Data Output Delay	-50		50	ps
	Serial Clock Output Rise and Fall Time [1]		100		ps
	Serial Data Output Rise and Fall Time [1]		120		ps
	Parallel Clock Input Rise and Fall Time [1]			1.0	ns
	Parallel Data Input Rise and Fall Time [1]			2.0	ns
	Parallel Data Input and Parity Input Skew			1.5	ns

1. 20% - 80%

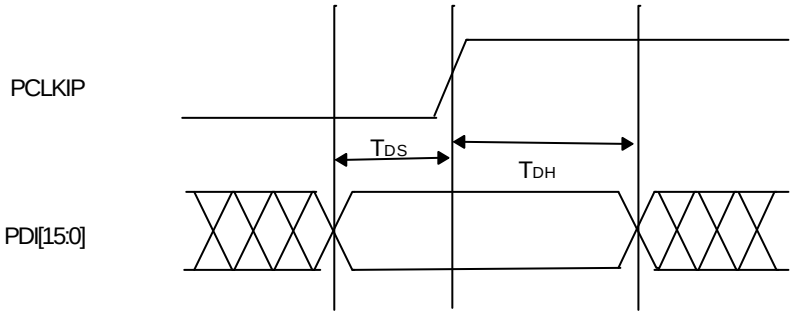


Figure 13 Input Timing (SELPLL = "H")

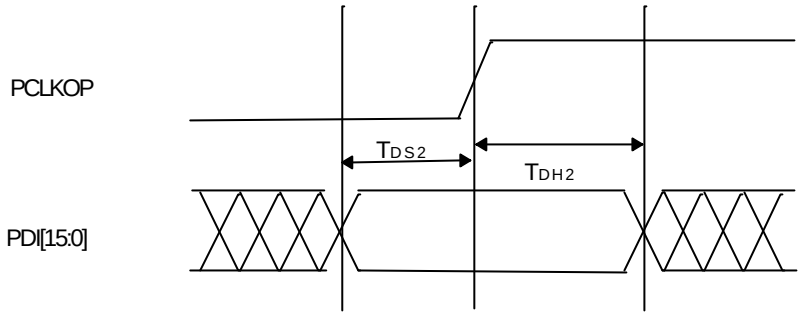


Figure 14 Input Timing (SELPLL = "L")

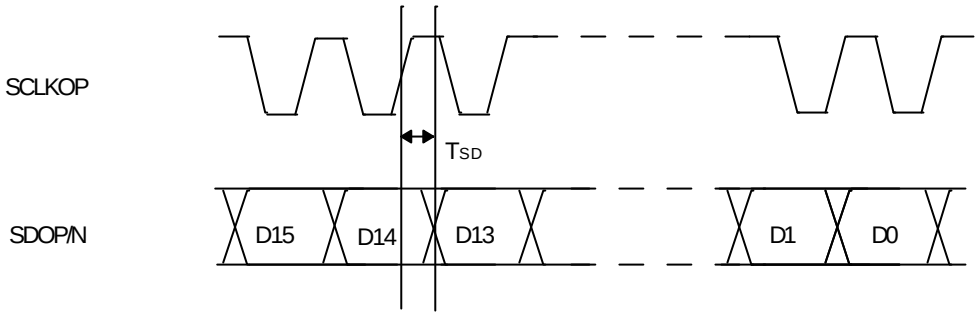


Figure 15 Output Timing

Table 10 Input/Output Pin Assignment

PIN NAME	LEVEL	I/O	PIN #	DESCRIPTION
LPF_EXT1 LPF_EXT2	-	-	22 21	Loop filter pins. (See Figure 16.)
PDI[15:0]	Single-Ended PECL	I	Table 11	Received parallel data input.
SCLKIP SCLKIN	Differential PECL	I	29 30	Serial reference clock input. (Used for Internal PLL off-state mode only.)
PCLKIP PCLKIN	Differential PECL	I	12 13	Reference clock input.
PARITYI	Single-Ended PECL	I	11	Used for parity check.
SDOP SDON	Differential PECL	O	38 37	Differential serial data output.
SCLKOP SCLKON	Differential PECL	O	41 40	Differential serial clock output.
PCLKOP PCLKON	Differential PECL	O	52 51	Differential parallel clock output.
PARIERRO	Single-Ended PECL	O	53	Parity error output.
SELPLL	CMOS	I	20	High: Internal PLL operating mode.
NC	-	-	26,47,54	No connect. Leave open.

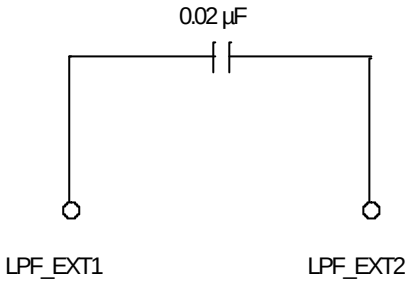


Figure 16 External Loop Filte

Table 11 Parity Check Condition

PARITYI	# of "High"s in PDI[15:0]	PARIERRO
High	Even	High
High	Odd	Low
Low	Even	Low
Low	Odd	High

Table 12 PDI Pin Assignment

PIN NAME	PIN #	PIN NAME	PIN #
PDI0	55	PDI8	3
PDI1	56	PDI9	4
PDI2	57	PDI10	5
PDI3	58	PDI11	6
PDI4	59	PDI12	7
PDI5	60	PDI13	8
PDI6	61	PDI14	9
PDI7	62	PDI15	10

Table 13 Common Pin Assignment

PIN NAME	LEVEL	PIN #	DESCRIPTION
V_{DD} 1	1.8 V	1, 14, 15, 17, 63	Core power supply.
V_{DD} 2	1.8 V	28, 31, 33, 36, 42, 44, 46, 50	I/O power supply.
$ANAV_{DD}$	1.8 V	25	Analog power supply.
GND	GND	2, 16, 18, 19, 27, 32, 34, 35, 39, 43, 45, 48, 49, 64	Ground.
ANAGND	GND	23, 24	Analog ground.

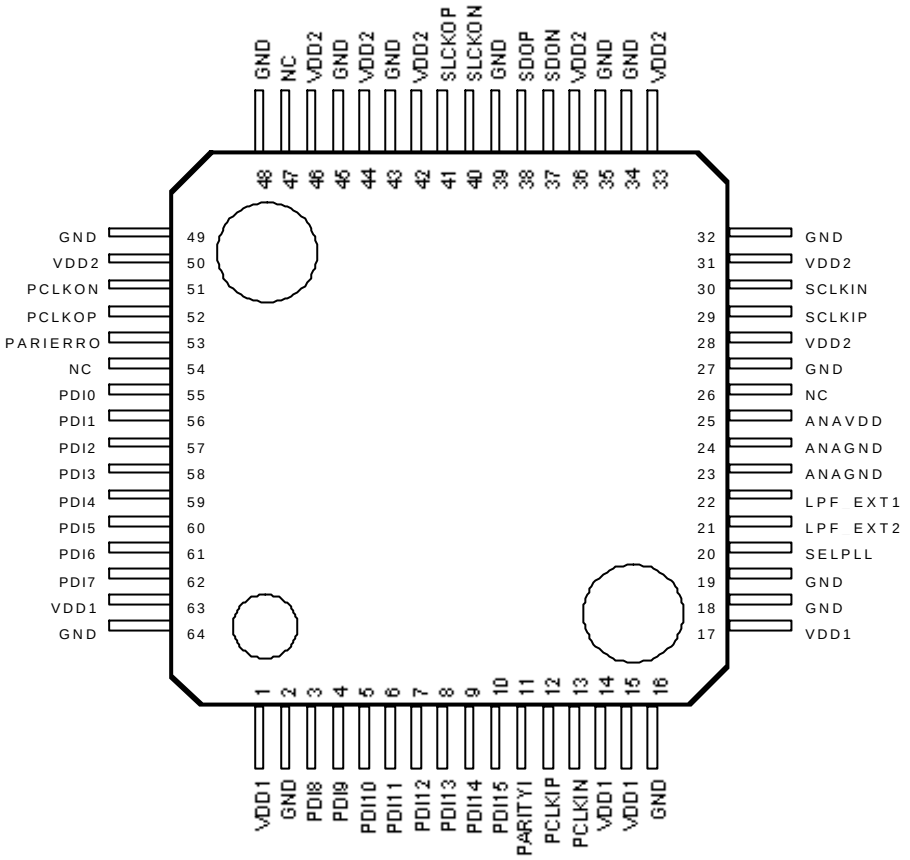


Figure 17 Pin Diagrams

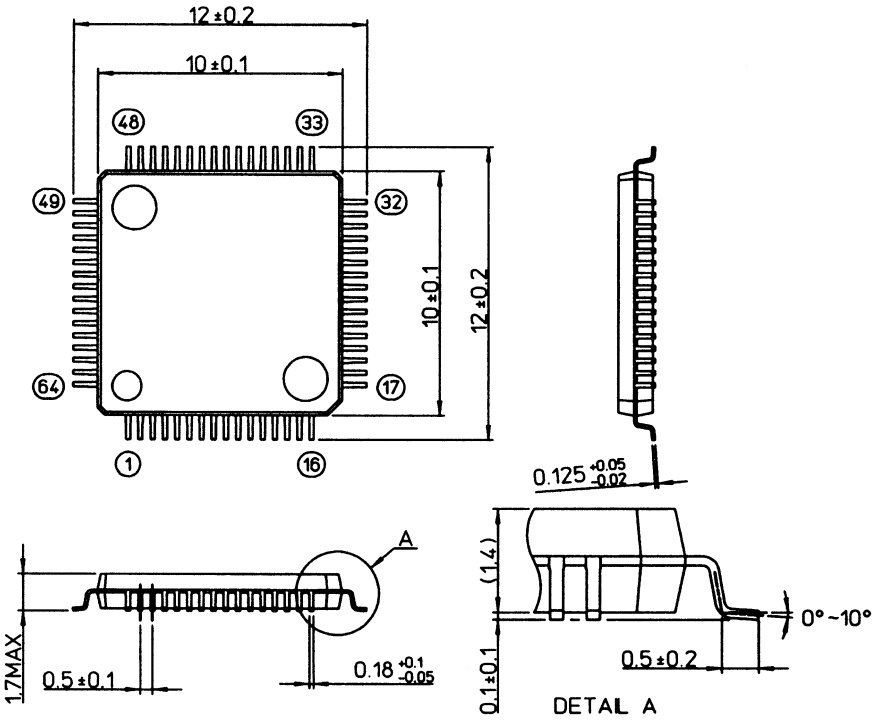


Figure 18 Package Information