

MH16V7245BATJ -5, -6

HYPER PAGE MODE 1207959552 - BIT (16777216 - WORD BY 72 - BIT) DYNAMIC RAM

DESCRIPTION

The MH16V7245BATJ is 16777216-word x 72-bit dynamic ram module. This consist of eighteen industry standard 16M x 4 dynamic RAMs in TSOP and three industry standard input buffer in TSSOP.

The mounting of TSOP on a card edge dual in-line package provides any application where high densities and large of quantities memory are required.

This is a socket-type memory module ,suitable for easy interchange or addition of module.

FEATURES

| Type name | /RAS access time (max.ns) | /CAS access time (max.ns) | Address access time (max.ns) | /OE access time (max.ns) | Cycle time (min.ns) | Power dissipation (typ.W) |
|-----------------|---------------------------|---------------------------|------------------------------|--------------------------|---------------------|---------------------------|
| MH16V7245BATJ-5 | 50 | 18 | 30 | 18 | 84 | 7.12 |
| MH16V7245BATJ-6 | 60 | 20 | 35 | 20 | 104 | 5.95 |

- Utilizes industry standard 16M x 4 RAMs TSOP and industry standard input buffer in TSSOP
- 168-pin (84-pin dual in-line pacement)
- Single 3.3V(+/-0.3V) supply operation
- Low stand-by power dissipation 121mW(Max)
- Low operation power dissipation
 MH16V7245BATJ -5 8.53W(Max)
 MH16V7245BATJ -6 7.88W(Max)
- All input,output LVTTTL compatible
- Includes(0.22uF x 20) decoupling capacitors
- 4096 refresh cycle every 64ms (A0~A11)
- JEDEC standard pin configuration & Buffered PD pin
 Buffered input except /RAS and DQ
- Gold plating contact pads

APPLICATION

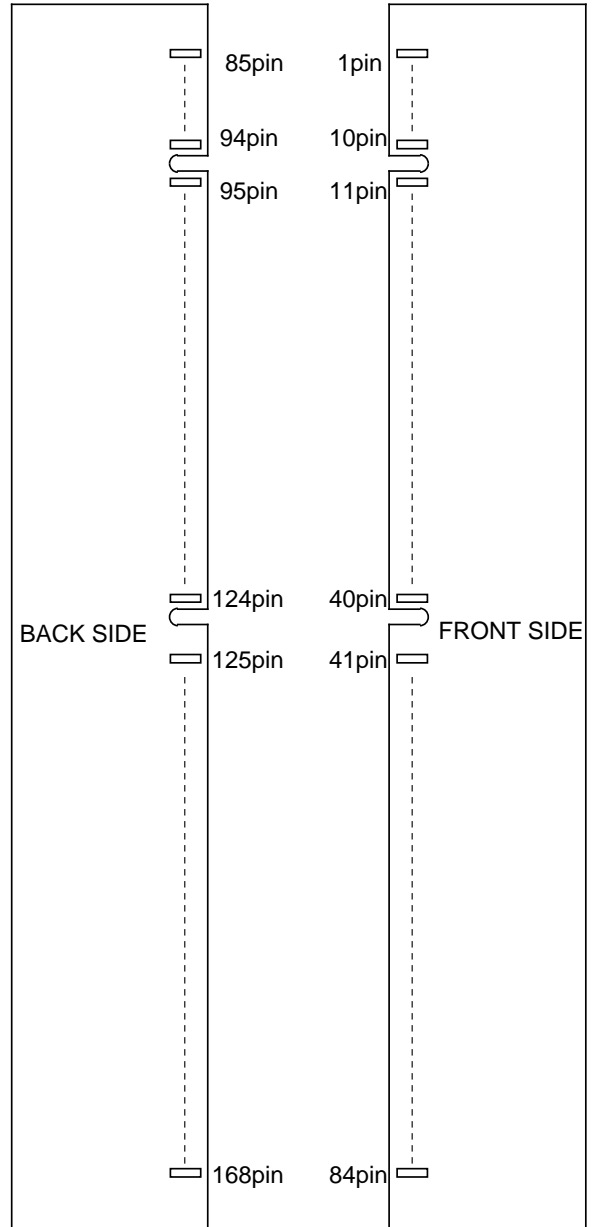
Main memory unit for computers , Microcomputer memory

PD&ID TABLE

| | PD1 | PD2 | PD3 | PD4 | PD5 | PD6 | PD7 | PD8 | ID0 | ID1 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| - 5 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| - 6 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

1 = NC , 0 = drive to VOL
 PD pin . . . buffered. When /PDE is low, PD information can be read
 ID pin . . . non-buffered

PIN CONFIGURATION



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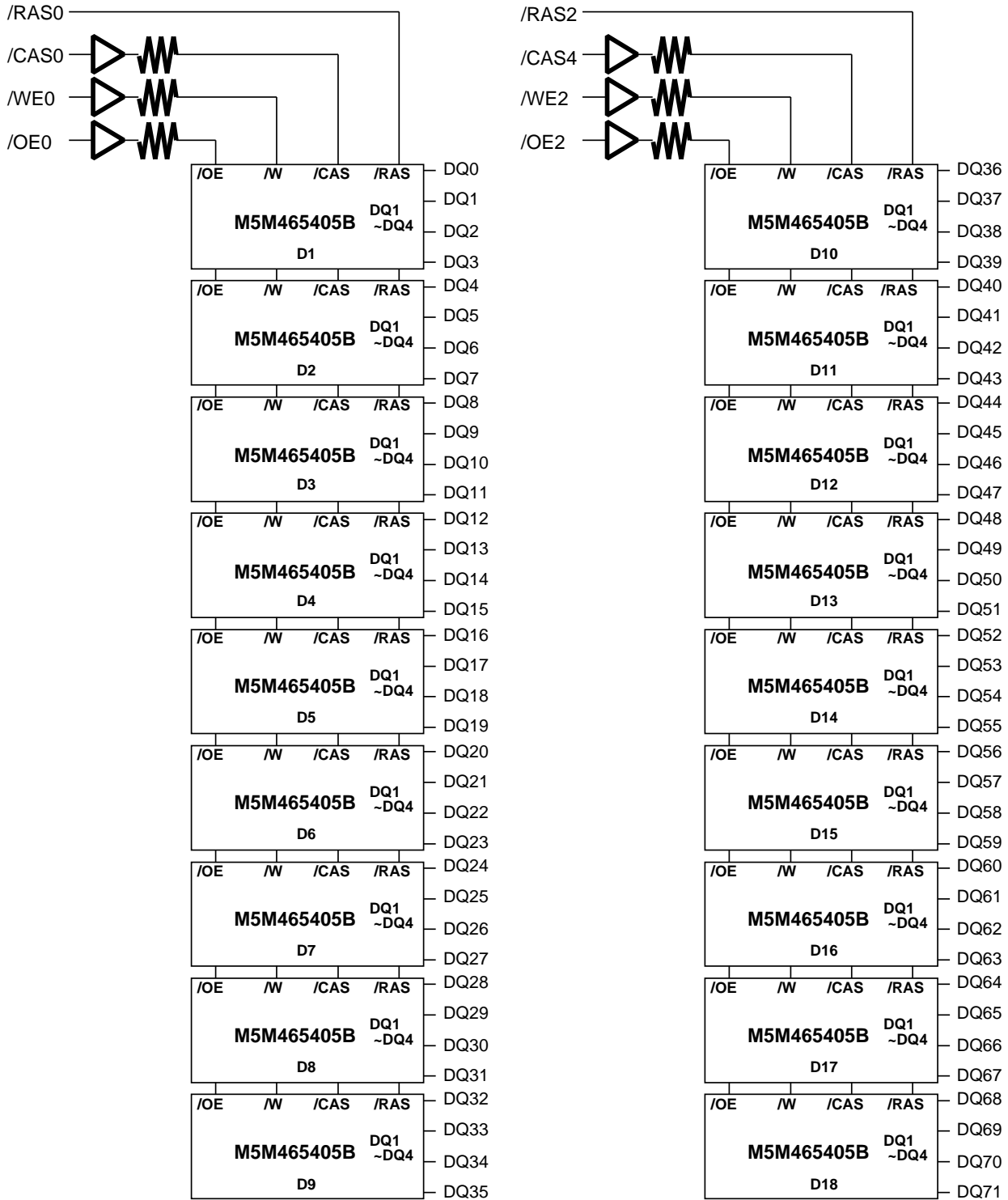
| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 1 | Vss | 43 | Vss | 85 | Vss | 127 | Vss |
| 2 | DQ0 | 44 | /OE2 | 86 | DQ36 | 128 | RFU |
| 3 | DQ1 | 45 | /RAS2 | 87 | DQ37 | 129 | Reserved |
| 4 | DQ2 | 46 | /CAS4 | 88 | DQ38 | 130 | Reserved |
| 5 | DQ3 | 47 | Reserved | 89 | DQ39 | 131 | Reserved |
| 6 | Vcc | 48 | /WE2 | 90 | Vcc | 132 | /PDE |
| 7 | DQ4 | 49 | Vcc | 91 | DQ40 | 133 | Vcc |
| 8 | DQ5 | 50 | Reserved | 92 | DQ41 | 134 | Reserved |
| 9 | DQ6 | 51 | Reserved | 93 | DQ42 | 135 | Reserved |
| 10 | DQ7 | 52 | DQ18 | 94 | DQ43 | 136 | DQ54 |
| 11 | DQ8 | 53 | DQ19 | 95 | DQ44 | 137 | DQ55 |
| 12 | Vss | 54 | Vss | 96 | Vss | 138 | Vss |
| 13 | DQ9 | 55 | DQ20 | 97 | DQ45 | 139 | DQ56 |
| 14 | DQ10 | 56 | DQ21 | 98 | DQ46 | 140 | DQ57 |
| 15 | DQ11 | 57 | DQ22 | 99 | DQ47 | 141 | DQ58 |
| 16 | DQ12 | 58 | DQ23 | 100 | DQ48 | 142 | DQ59 |
| 17 | DQ13 | 59 | Vcc | 101 | DQ49 | 143 | Vcc |
| 18 | Vcc | 60 | DQ24 | 102 | Vcc | 144 | DQ60 |
| 19 | DQ14 | 61 | RFU | 103 | DQ50 | 145 | RFU |
| 20 | DQ15 | 62 | RFU | 104 | DQ51 | 146 | RFU |
| 21 | DQ16 | 63 | RFU | 105 | DQ52 | 147 | RFU |
| 22 | DQ17 | 64 | RFU | 106 | DQ53 | 148 | RFU |
| 23 | Vss | 65 | DQ25 | 107 | Vss | 149 | DQ61 |
| 24 | Reserved | 66 | DQ26 | 108 | Reserved | 150 | DQ62 |
| 25 | Reserved | 67 | DQ27 | 109 | Reserved | 151 | DQ63 |
| 26 | Vcc | 68 | Vss | 110 | Vcc | 152 | Vss |
| 27 | /WE0 | 69 | DQ28 | 111 | RFU | 153 | DQ64 |
| 28 | /CAS0 | 70 | DQ29 | 112 | Reserved | 154 | DQ65 |
| 29 | Reserved | 71 | DQ30 | 113 | Reserved | 155 | DQ66 |
| 30 | /RAS0 | 72 | DQ31 | 114 | Reserved | 156 | DQ67 |
| 31 | /OE0 | 73 | Vcc | 115 | RFU | 157 | Vcc |
| 32 | Vss | 74 | DQ32 | 116 | Vss | 158 | DQ68 |
| 33 | A0 | 75 | DQ33 | 117 | A1 | 159 | DQ69 |
| 34 | A2 | 76 | DQ34 | 118 | A3 | 160 | DQ70 |
| 35 | A4 | 77 | DQ35 | 119 | A5 | 161 | DQ71 |
| 36 | A6 | 78 | Vss | 120 | A7 | 162 | Vss |
| 37 | A8 | 79 | PD1 | 121 | A9 | 163 | PD2 |
| 38 | A10 | 80 | PD3 | 122 | A11 | 164 | PD4 |
| 39 | NC | 81 | PD5 | 123 | Reserved | 165 | PD6 |
| 40 | Vcc | 82 | PD7 | 124 | Vcc | 166 | PD8 |
| 41 | RFU | 83 | ID0 | 125 | RFU | 167 | ID1 |
| 42 | RFU | 84 | Vcc | 126 | B0 | 168 | Vcc |

Reserved: Reserved use
RFU: Reserved for future use

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BLOCK DIAGRAM



| PIN NAME | FUNCTION |
|--------------|-----------------------------|
| /RAS0, /RAS2 | ROW ADDRESS STROBE INPUT |
| /CAS0, /CAS2 | COLUMN ADDRESS STROBE INPUT |
| /WE0, /WE2 | WRITE CONTROL INPUT |
| /OE0, /OE2 | OUTPUT ENABLE INPUT |
| A0~A11, B0 | ADDRESS INPUT |
| DQ0~DQ71 | DATA I/O |
| Vcc | POWER SUPPLY |
| Vss | GROUND |

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FUNCTION

The MH16V7245BATJ provide, in addition to normal read, write, and read-modify-write operations,

a number of other functions, e.g., Hyper page mode, /CAS before /RAS refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

| Operation | Inputs | | | | | | Input/Output | | Refresh | Remark |
|--------------------------|--------|------|-----|-----|-------------|----------------|--------------|--------|---------|---------------------------|
| | /RAS | /CAS | /W | /OE | Row address | Column address | Input | Output | | |
| Read | ACT | ACT | NAC | ACT | APD | APD | OPN | VLD | NO | Hyper page mode identical |
| Write (Early write) | ACT | ACT | ACT | DNC | APD | APD | VLD | OPN | NO | |
| Write (Delayed write) | ACT | ACT | ACT | DNC | APD | APD | VLD | IVD | NO | |
| Read-modify-write | ACT | ACT | ACT | ACT | APD | APD | VLD | VLD | NO | |
| Hidden refresh | ACT | ACT | DNC | ACT | DNC | DNC | OPN | VLD | YES | |
| /CAS before /RAS refresh | ACT | ACT | NAC | DNC | DNC | DNC | DNC | OPN | YES | |
| Standby | NAC | DNC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

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ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|--------|-----------------------|---------------------|-----------|------|
| Vcc | Supply voltage | With respect to Vss | -0.5~4.6 | V |
| VI | Input voltage | | -0.5~ 4.6 | |
| VO | Output voltage | | -0.5~ 4.6 | |
| IO | Output current | | 50 | mA |
| Pd | Power dissipation | Ta=25°C | 21.6 | W |
| Topr | Operating temperature | | 0~70 | °C |
| Tstg | Storage temperature | | -40~100 | °C |

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|--------|--------------------------------------|--------|-----|---------|------|
| | | Min | Nom | Max | |
| Vcc | Supply voltage | 3.0 | 3.3 | 3.6 | V |
| Vss | Supply voltage | 0 | 0 | 0 | V |
| VIH | High-level input voltage, all inputs | 2.0 | | Vcc+0.3 | V |
| VIL | Low-level input voltage | -0.3 | | 0.8 | v |

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V+/-0.3V, Vss=0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-----------|--|--|--------|-----|------|------|
| | | | Min | Typ | Max | |
| VOH | High-level output voltage | IOH=-2mA | 2.4 | | Vcc | V |
| VOL | Low-level output voltage | IOL=2mA | 0 | | 0.4 | V |
| IOZ | Off-state output current | Q floating 0V VOUT Vcc | -10 | | 10 | uA |
| II | Input current (except /RAS) | 0V VIN Vcc+0.3, Other input pins=0V | -10 | | 10 | uA |
| II (RAS) | Input current (/RAS) | 0V VIN Vcc+0.3, Other input pins=0V | -90 | | 90 | uA |
| ICC1 (AV) | Average supply current from Vcc operating (Note 3,4,5) | -5 /RAS, /CAS cycling tRC=tWC=min. output open | | | 2360 | mA |
| | | | -6 | | 2180 | |
| ICC2 | Supply current from Vcc , stand-by | /RAS=/CAS =VIH, output open | | | 38 | mA |
| | | /RAS=/CAS=/WE Vcc -0.2, output open | | | 29 | |
| ICC4(AV) | Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5) | -5 /RAS=VIL, /CAS cycling tPC=min. output open | | | 1820 | mA |
| | | | -6 | | 1640 | |
| ICC6(AV) | Average supply current from Vcc /CAS before /RAS refresh mode (Note 3) | -5 /CAS before /RAS refresh cycling tRC=min. output open | | | 2360 | mA |
| | | | -6 | | 2180 | |

Note 2: Current flowing into an IC is positive, out is negative.

3: Icc1 (AV), Icc3 (AV), Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Under condition of column address being changed once or less while /RAS=VIL and /CAS=VIH

CAPACITANCE (Ta = 0~70°C, Vcc = 3.3V+/-0.3V, Vss = 0V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-----------|--------------------------------------|-----------------|--------|-----|-----|------|
| | | | Min | Typ | Max | |
| CI (/RAS) | Input capacitance, /RAS input | VI=Vss | | | 80 | pF |
| CI | Input capacitance, except /RAS input | f=1MHZ | | | 15 | pF |
| C(DQ) | Input/Output capacitance, DATA | Vi=25mVrms | | | 18 | pF |

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SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V+/-0.3V, Vss=0V, unless otherwise noted, see notes 6,14,15)

| Symbol | Parameter | Limits | | | | Unit |
|--------|--|--------|-----|-----|-----|------|
| | | -5 | | -6 | | |
| | | Min | Max | Min | Max | |
| tCAC | Access time from /CAS (Note 7,8) | | 18 | | 20 | ns |
| tRAC | Access time from /RAS (Note 7,9) | | 50 | | 60 | ns |
| tAA | Column address access time (Note 7,10) | | 30 | | 35 | ns |
| tCPA | Access time from /CAS precharge (Note 7,11) | | 33 | | 38 | ns |
| tOEA | Access time from /OE (Note 7) | | 18 | | 20 | ns |
| tOHC | Output hold time /CAS high | 10 | | 10 | | ns |
| tOHR | Output hold time /RAS high (Note 13) | 5 | | 5 | | ns |
| tCLZ | Output low impedance time from /CAS low (Note 7) | 10 | | 10 | | ns |
| tOEZ | Output disable time after /OE high (Note 12) | | 18 | | 20 | ns |
| tWEZ | Output disable time after /WE high (Note 12) | | 18 | | 20 | ns |
| tOFF | Output disable time after /CAS high (Note 12,13) | | 18 | | 20 | ns |
| tREZ | Output disable time after /RAS high (Note 12,13) | | 13 | | 15 | ns |

Note 6: An initial pause of 500us is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a /RAS-Only refresh or /CAS before /RAS refresh).

Note the /RAS may be cycled during the initial pause. And any 8 /RAS or /RAS /CAS cycles are required after prolonged periods (greater than 64 ms) of /RAS inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to 1TTL loads and 50pF, VOH=2.4V (IOH=-2mA) and VOL=0.4V (IOL=-2mA).

The reference levels for measuring of output signals are 2.0V (VOH) and 0.8V (VOL).

8: Assumes that tRCD tRCD(max), tASC tASC(max) and tCP tCP(max).

9: Assumes that tRCD tRCD(max) and tRAD tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.

10: Assumes that tRAD tRAD(max) and tASC tASC(max).

11: Assumes that tCP tCP(max) and tASC tASC(max).

12: tOEZ (max), tWEZ(max), tOFF(max) and tREZ(max) defines the time at which the output achieves the high impedance state (IOUT 1+/-10uA) and is not reference to VOH(min) or VOL(max).

13: Output is disable after both /RAS and /CAS go to high

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Hyper-Page Mode Cycles)

(Ta=0~70°C, Vcc=3.3V+/-0.3V, Vss=0V, unless otherwise noted, see notes 14,15)

| Symbol | Parameter | Limits | | | | Unit |
|--------|--|--------|-----|-----|-----|------|
| | | -5 | | -6 | | |
| | | Min | Max | Min | Max | |
| tREF | Refresh cycle time | | 64 | | 64 | ms |
| tRP | /RAS high pulse width | 30 | | 40 | | ns |
| tRCD | Delay time, /RAS low to /CAS low (Note16) | 9 | 32 | 9 | 40 | ns |
| tCRP | Delay time, /CAS high to /RAS low | 10 | | 10 | | ns |
| tRPC | Delay time, /RAS high to /CAS low | 0 | | 0 | | ns |
| tCPN | /CAS high pulse width | 8 | | 10 | | ns |
| tRAD | Column address delay time from /RAS low (Note17) | 5 | 20 | 7 | 25 | ns |
| tASR | Row address setup time before /RAS low | 5 | | 5 | | ns |
| tASC | Column address setup time before /CAS low (Note18) | 0 | 10 | 0 | 13 | ns |
| tRAH | Row address hold time after /RAS low | 3 | | 5 | | ns |
| tCAH | Column address hold time after /CAS low | 8 | | 10 | | ns |
| tDZC | Delay time, data to /CAS low (Note19) | 0 | | 0 | | ns |
| tDZO | Delay time, data to /OE low (Note19) | 0 | | 0 | | ns |
| tRDD | Delay time, /RAS high to data (Note20) | 13 | | 15 | | ns |
| tCDD | Delay time, /CAS high to data (Note20) | 18 | | 20 | | ns |
| tODD | Delay time, /OE high to data (Note20) | 18 | | 20 | | ns |
| tT | Transition time (Note21) | 1 | 50 | 1 | 50 | ns |

Note 14: The timing requirements are assumed tT =2ns.

15: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

16: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

17: tRAD(max) is specified as a reference point only. If tRAD tRAD(max) and tASC tASC(max), access time is controlled exclusively by tAA.

18: tASC(max) is specified as a reference point only. If tRCD tRCD(max) and tASC tASC(max), access time is controlled exclusively by tCAC.

19: Either tDZC or tDZO must be satisfied.

20: Either tRDD or tCDD or tODD must be satisfied.

21: tT is measured between VIH(min) and VIL(max).

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Read and Refresh Cycles

| Symbol | Parameter | Limits | | | | Unit |
|--------|---|--------|-------|-----|-------|------|
| | | -5 | | -6 | | |
| | | Min | Max | Min | Max | |
| tRC | Read cycle time | 84 | | 104 | | ns |
| tRAS | /RAS iow pulse width | 50 | 10000 | 60 | 10000 | ns |
| tCAS | /CAS iow pulse width | 8 | 10000 | 10 | 10000 | ns |
| tCSH | /CAS hold time after /RAS iow | 30 | | 43 | | ns |
| tRSH | /RAS hold time after /CAS iow | 18 | | 20 | | ns |
| tRCS | Read Setup time after /CAS high | 0 | | 0 | | ns |
| tRCH | Read hold time after /CAS iow (Note 22) | 0 | | 0 | | ns |
| tRRH | Read hold time after /RAS iow (Note 22) | 0 | | 0 | | ns |
| tRAL | Column address to /RAS hold time | 30 | | 35 | | ns |
| tCAL | Column address to /CAS hold time | 13 | | 18 | | ns |
| tORH | /RAS hold time after /OE iow | 18 | | 20 | | ns |
| tOCH | /CAS hold time after /OE iow | 13 | | 15 | | ns |

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

| Symbol | Parameter | Limits | | | | Unit |
|--------|--|--------|-------|-----|-------|------|
| | | -5 | | -6 | | |
| | | Min | Max | Min | Max | |
| tWC | Write cycle time | 84 | | 104 | | ns |
| tRAS | /RAS iow pulse width | 50 | 10000 | 60 | 10000 | ns |
| tCAS | /CAS iow pulse width | 8 | 10000 | 10 | 10000 | ns |
| tCSH | /CAS hold time after /RAS iow | 30 | | 35 | | ns |
| tRSH | /RAS hold time after /CAS iow | 18 | | 20 | | ns |
| tWCS | Write setup time before /CAS low (Note 24) | 0 | | 0 | | ns |
| tWCH | Write hold time after /CAS iow | 8 | | 10 | | ns |
| tCWL | /CAS hold time after /W iow | 8 | | 10 | | ns |
| tRWL | /RAS hold time after W iow | 13 | | 15 | | ns |
| tWP | Write pulse width | 8 | | 10 | | ns |
| tDS | Data setup time before /CAS iow or W iow | -5 | | -5 | | ns |
| tDH | Data hold time after /CAS iow or W iow | 13 | | 15 | | ns |

Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | Limits | | | | Unit |
|--------|--|--------|-------|-----|-------|------|
| | | -5 | | -6 | | |
| | | Min | Max | Min | Max | |
| tRWC | Read write/read modify write cycle time (Note23) | 109 | | 133 | | ns |
| tRAS | RAS iow pulse width | 75 | 10000 | 89 | 10000 | ns |
| tCAS | CAS iow pulse width | 38 | 10000 | 44 | 10000 | ns |
| tCSH | CAS hold time after RAS low | 65 | | 77 | | ns |
| tRSH | RAS hold time after CAS low | 43 | | 49 | | ns |
| tRCS | Read setup time before CAS low | 0 | | 0 | | ns |
| tCWD | Delay time, CAS iow to W iow (Note24) | 28 | | 32 | | ns |
| tRWD | Delay time, RAS iow to W iow (Note24) | 60 | | 72 | | ns |
| tAWD | Delay time, address to W iow (Note24) | 40 | | 47 | | ns |
| tOEH | OE hold time after W iow | 13 | | 15 | | ns |

Note 23: tRWC is specified as $tRWC(\min)=tRAC(\max)+tODD(\min)+tRWL(\min)+tRP(\min)+4tT$.

24: tWCS, tCWD, tRWD, tAWD and tCPWD are specified as reference points only. If tWCS tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD tCWD(min), tRWD tRWD (min), tAWD tAWD(min) and tCPWD tCPWD(min) (for Hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until /CAS or /OE goes back to VIH) is indeterminate.

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**Hyper Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle,
Read Write Mix Cycle,Hi-Z control by /OE or /WE) (Note 25)**

| Symbol | Parameter | Limits | | | | Unit |
|--------|--|--------|---------------|-----|---------------|------|
| | | -5 | | -6 | | |
| | | Min | Max | Min | Max | |
| tHPC | Hyper page mode read/write cycle time | 20 | | 25 | | ns |
| tHPRWC | Hyper page mode read write/read modify write cycle time | 55 | | 66 | | ns |
| tRAS | /RAS low pulse width for read write cycle (Note26) | 65 | 100000 | 77 | 100000 | ns |
| tCP | /CAS high pulse width (Note27) | 8 | 15 | 10 | 18 | ns |
| tCPRH | /RAS hold time after /CAS precharge | 33 | | 38 | | ns |
| tCPWD | Delay time, /CAS precharge to W low (Note24) | 43 | | 50 | | ns |
| tCHOL | Hold time to maintain the data Hi-Z until /CAS access | 7 | | 7 | | ns |
| tOEPE | /OE Pulse Width (Hi-Z control) | 7 | | 7 | | ns |
| tWPE | /W Pulse Width (Hi-Z control) | 7 | | 7 | | ns |
| tHCWD | Delay time, /CAS low to /W low after read | 28 | | 32 | | ns |
| tHAWD | Delay time, Address to /W low after read | 40 | | 47 | | ns |
| tHPWD | Delay time, /CAS precharge to /W low after read | 43 | | 50 | | ns |
| tHCOD | Delay time, /CAS low to /OE high after read | 13 | | 15 | | ns |
| tHAOD | Delay time, Address to /OE high after read | 25 | | 30 | | ns |
| tHPOD | Delay time, /CAS precharge to /OE high after read | 28 | | 33 | | ns |

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

26: tRAS(min) is specified as two cycles of CAS input are performed.

27: tCP(max) is specified as a reference point only.

/CAS before /RAS Refresh Cycle (Note 28)

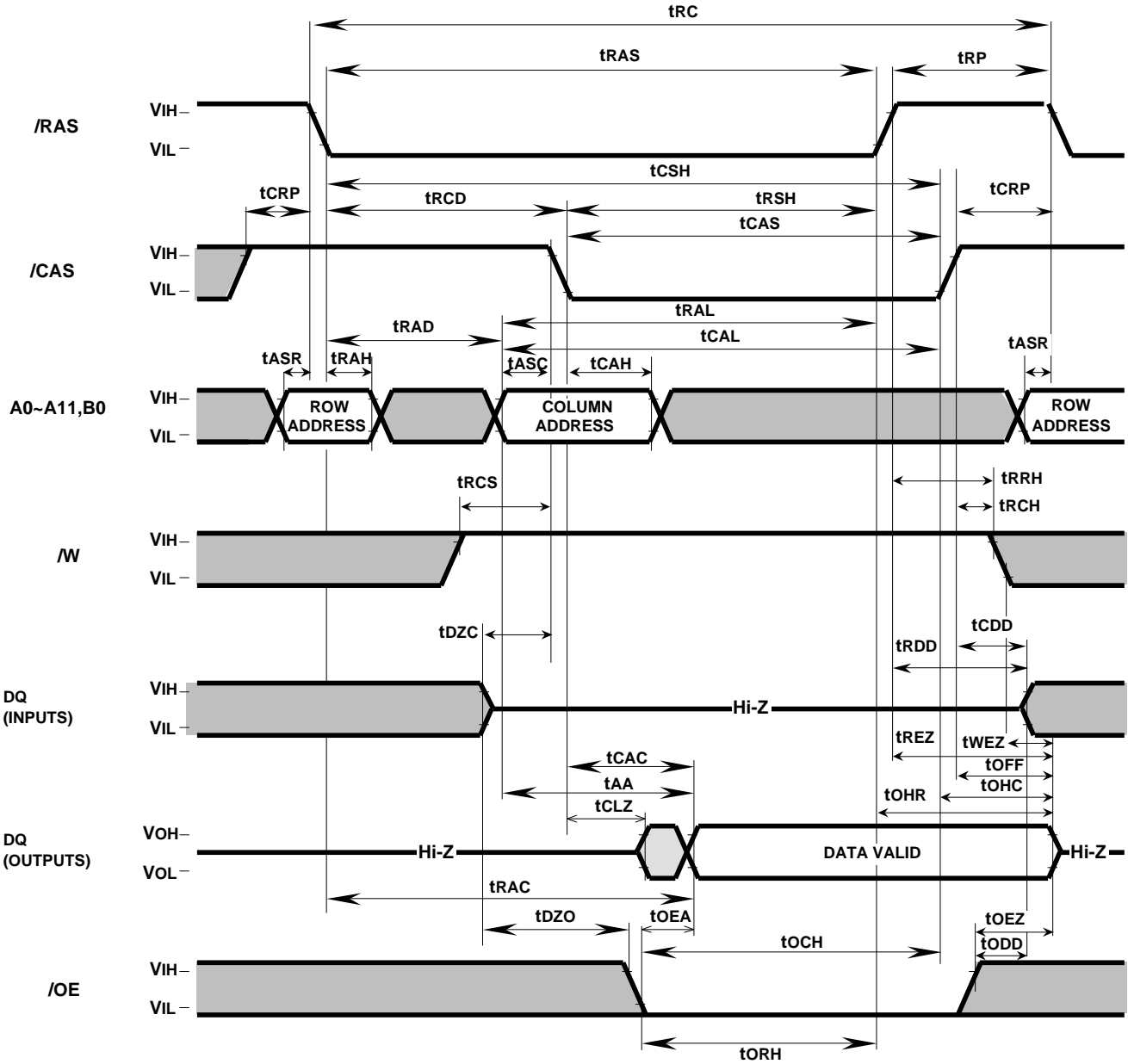
| Symbol | Parameter | Limits | | | | Unit |
|--------|---------------------------------|--------|-----|-----|-----|------|
| | | -5 | | -6 | | |
| | | Min | Max | Min | Max | |
| tCSR | /CAS setup time before /RAS low | 10 | | 10 | | ns |
| tCHR | /CAS hold time after /RAS low | 5 | | 5 | | ns |
| tRSR | Read setup time before /RAS low | 15 | | 15 | | ns |
| tRHR | Read hold time after /RAS low | 5 | | 5 | | ns |



Note 28: Eight or more /CAS before /RAS cycles instead of eight /RAS cycles are necessary for proper operation of /CAS before /RAS refresh mode.

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Timing Diagrams (Note 29) Read Cycle

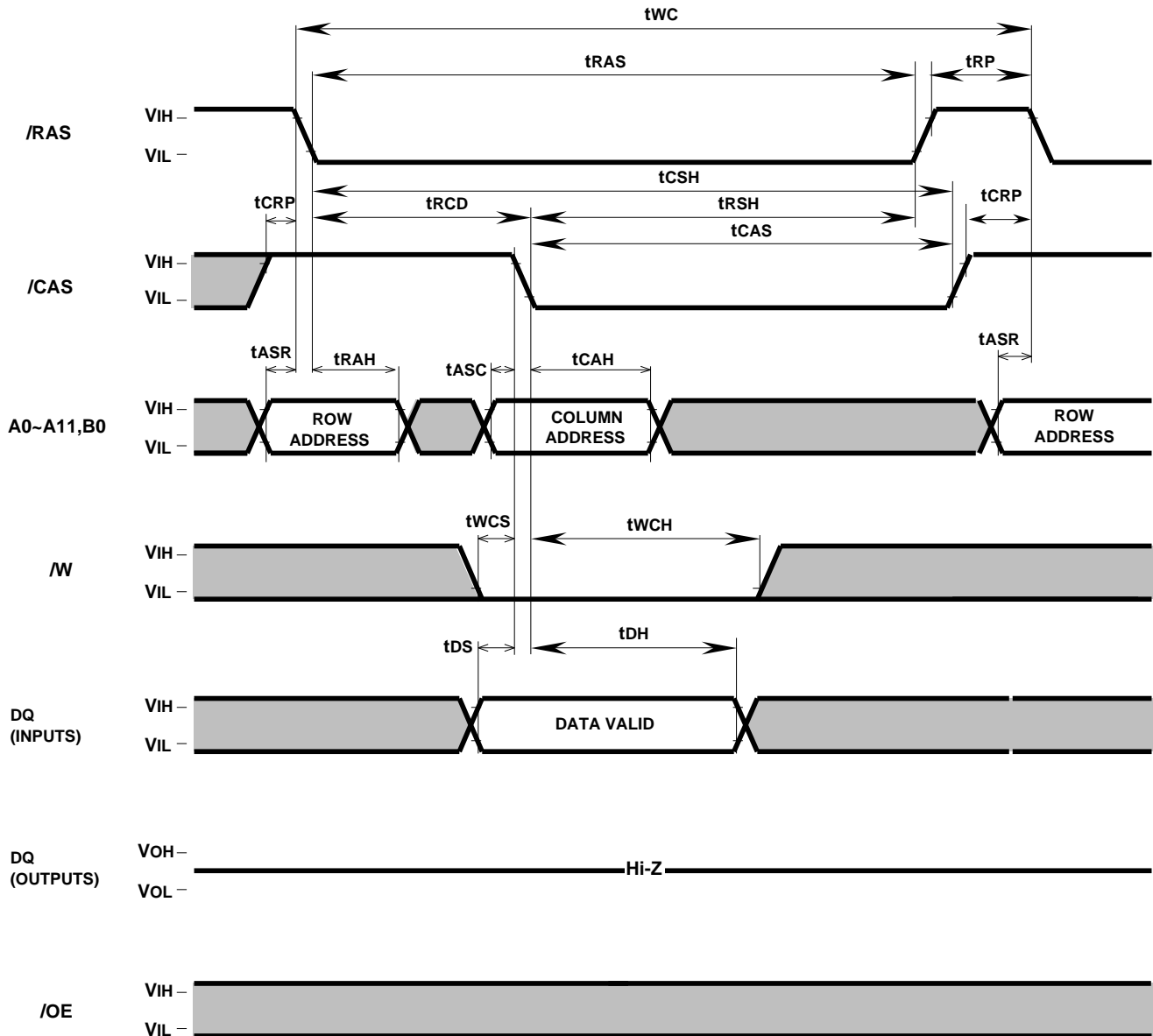


Note 29  Indicates the don't care input.
 VIH(min) VIN VIH(max) or VIL(min) VIN VIL(max)
 Indicates the invalid output.

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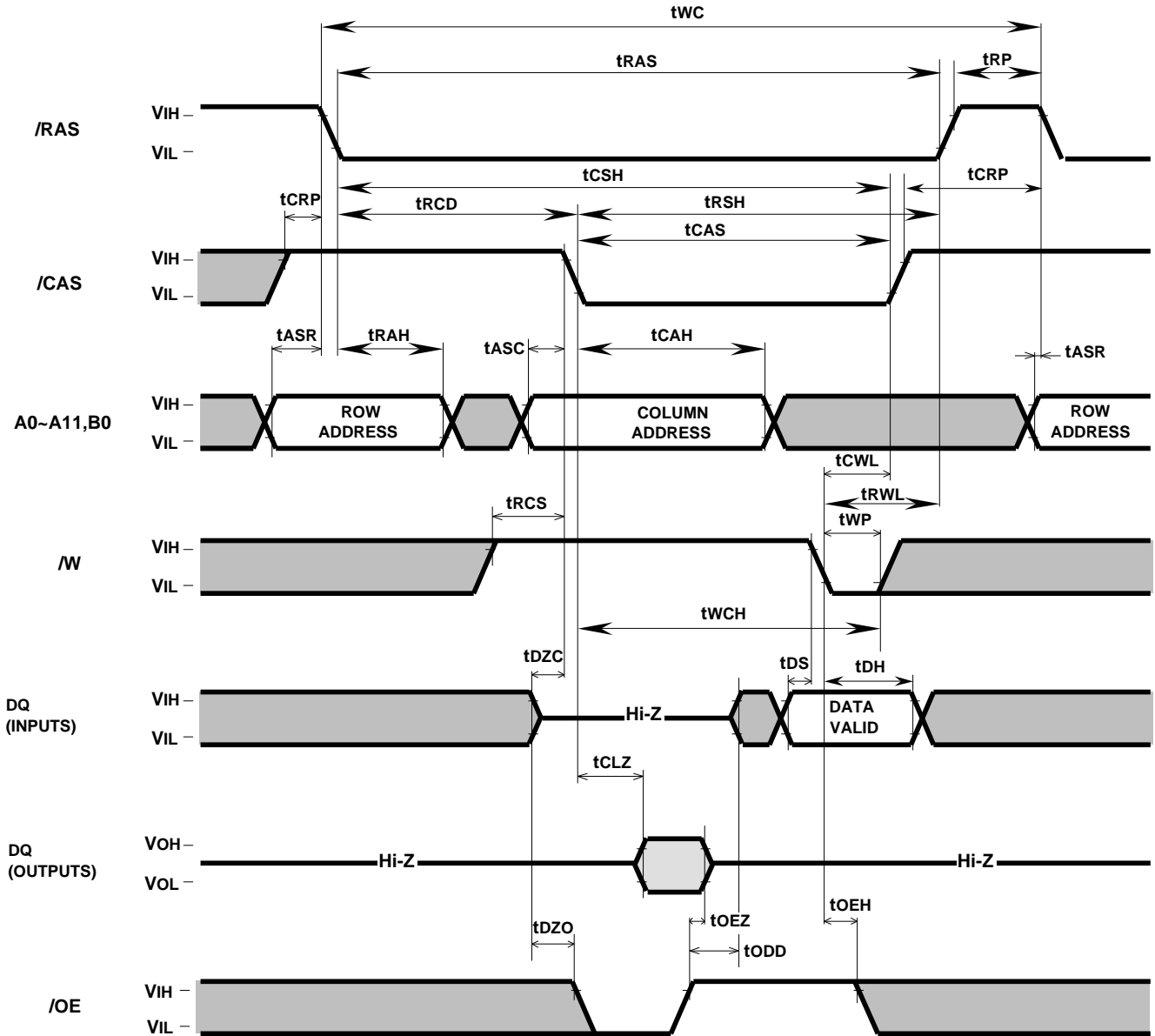
Early Write Cycle



MH16V7245BATJ -5, -6

HYPER PAGE MODE 1207959552 - BIT (16777216 - WORD BY 72 - BIT) DYNAMIC RAM

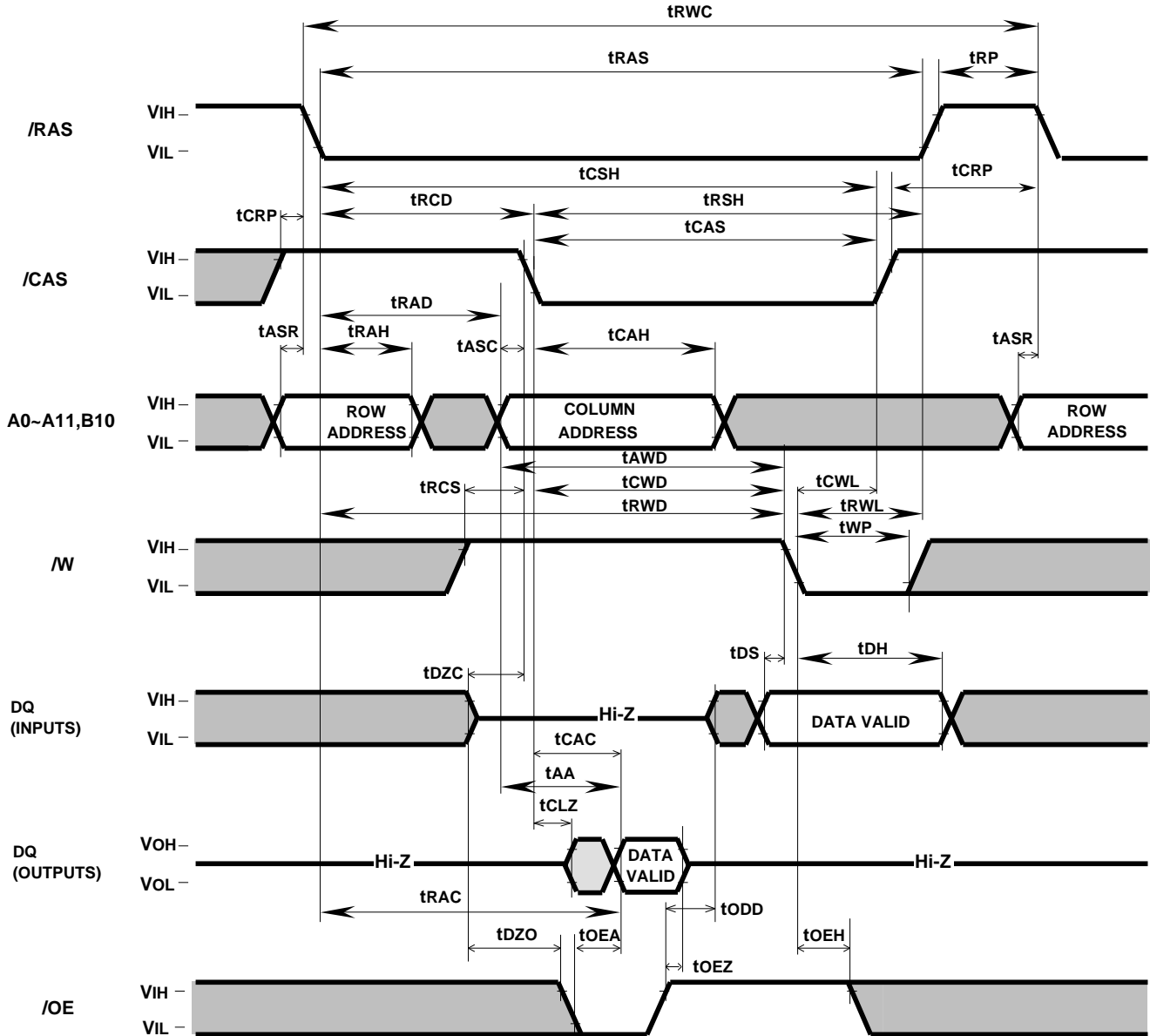
Delayed Write Cycle



MH16V7245BATJ -5, -6

HYPER PAGE MODE 1207959552 - BIT (16777216 - WORD BY 72 - BIT) DYNAMIC RAM

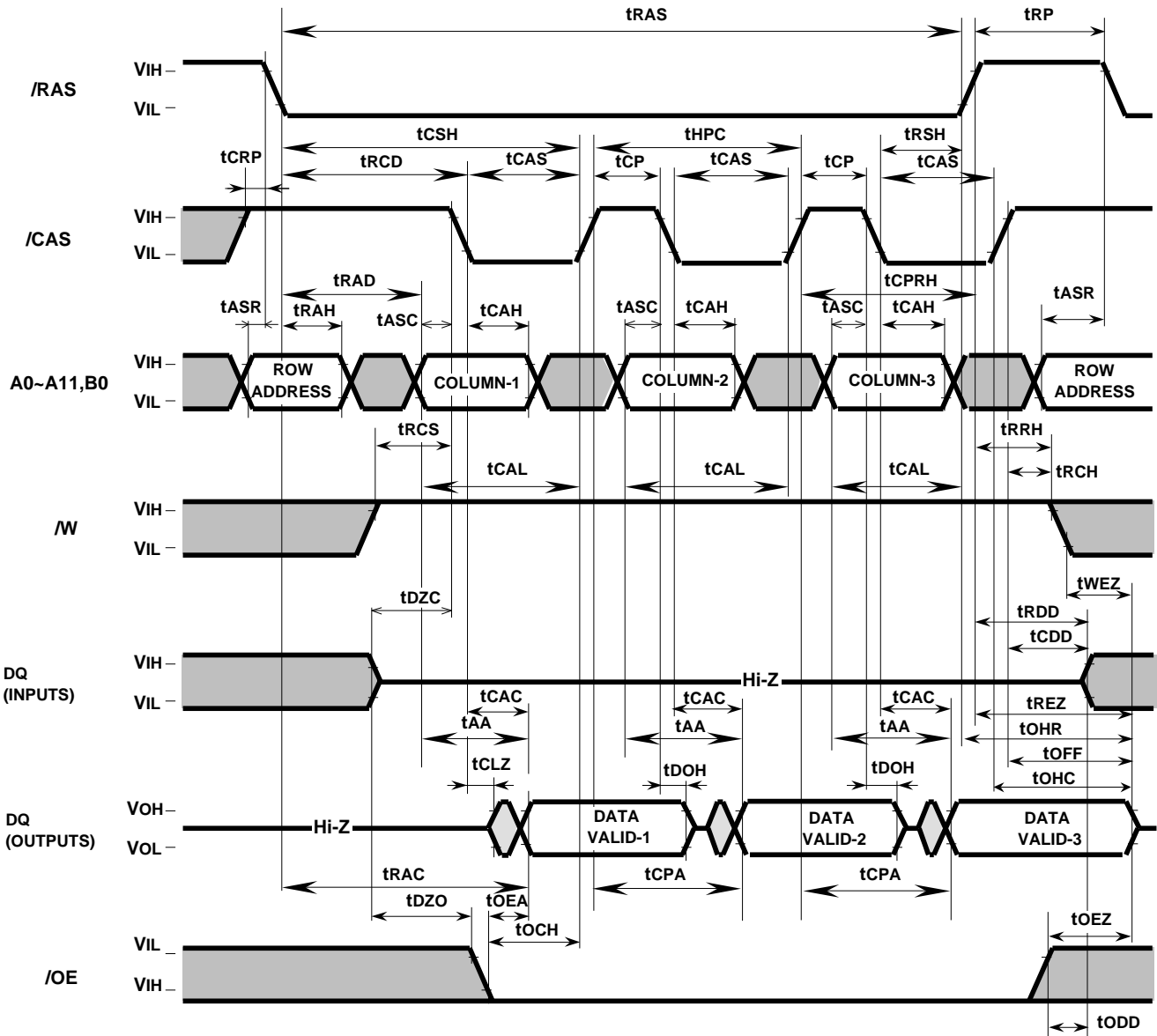
Read-Write, Read-Modify-Write Cycle



MH16V7245BATJ -5, -6

HYPER PAGE MODE 1207959552 - BIT (16777216 - WORD BY 72 - BIT) DYNAMIC RAM

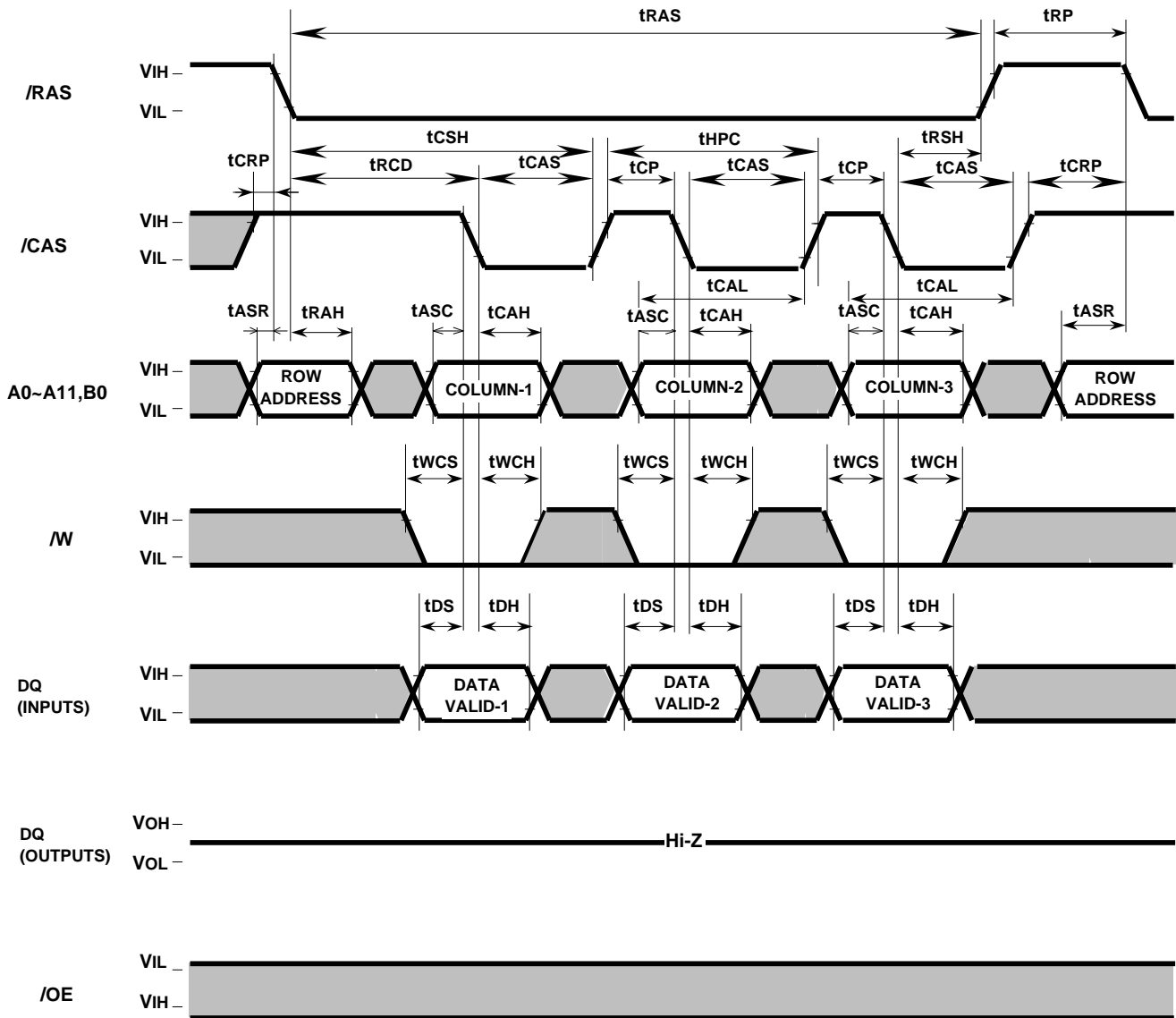
Hyper Page Mode Read Cycle



MH16V7245BATJ -5, -6

HYPER PAGE MODE 1207959552 - BIT (16777216 - WORD BY 72 - BIT) DYNAMIC RAM

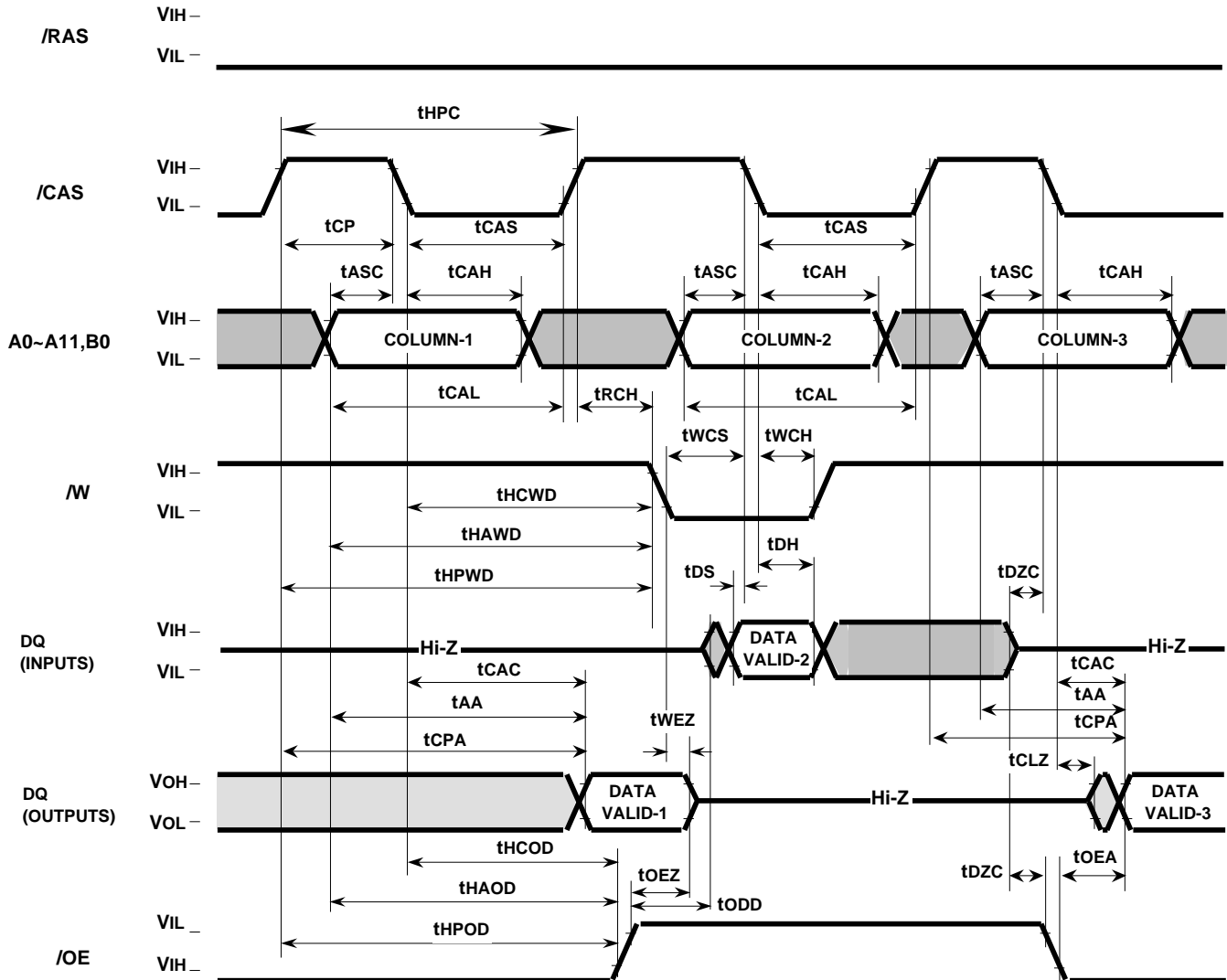
Hyper Page Mode Early Write Cycle



MH16V7245BATJ -5, -6

HYPER PAGE MODE 1207959552 - BIT (16777216 - WORD BY 72 - BIT) DYNAMIC RAM

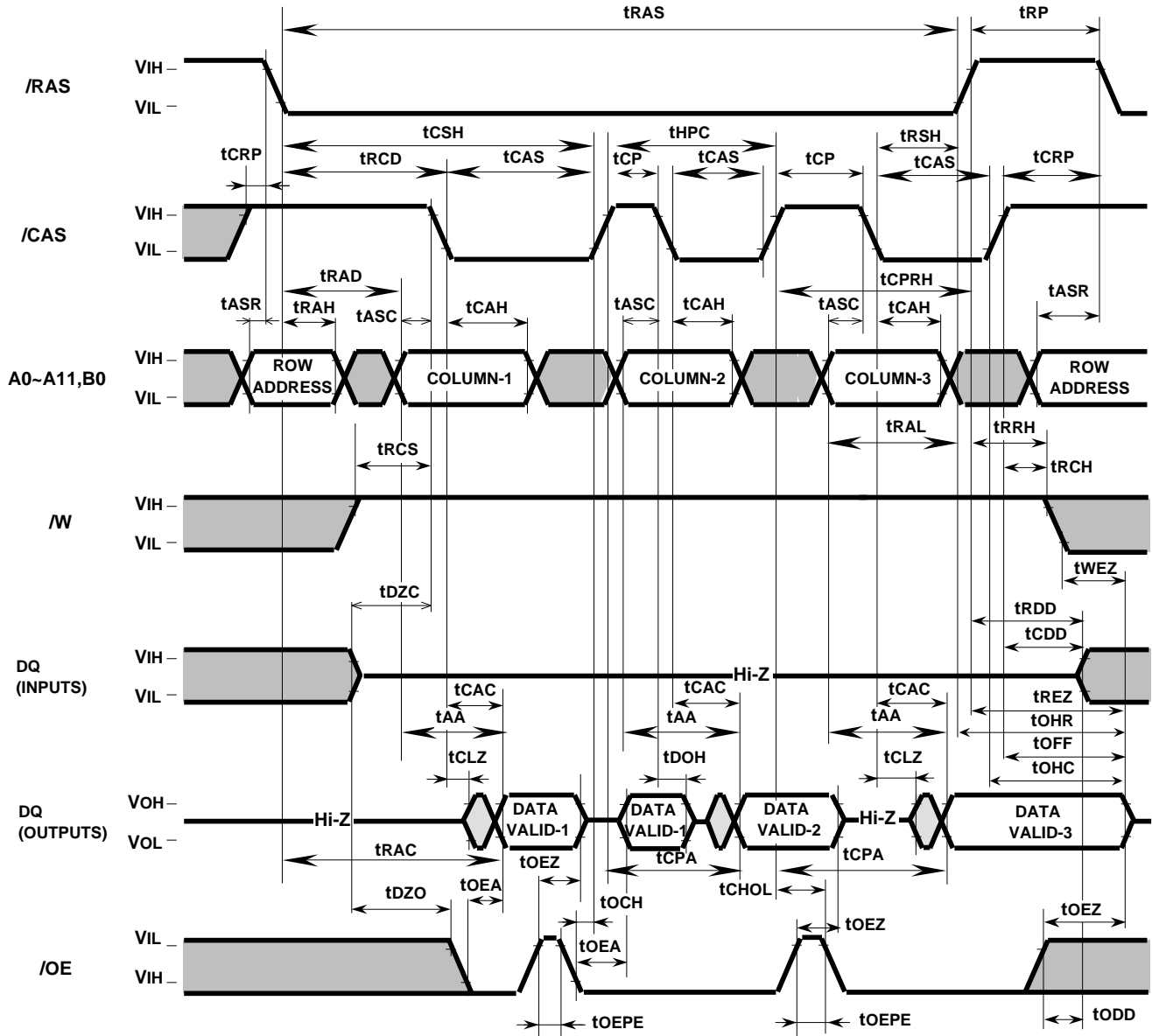
Hyper Page Mode Mix Cycle (2)



MH16V7245BATJ -5, -6

HYPER PAGE MODE 1207959552 - BIT (16777216 - WORD BY 72 - BIT) DYNAMIC RAM

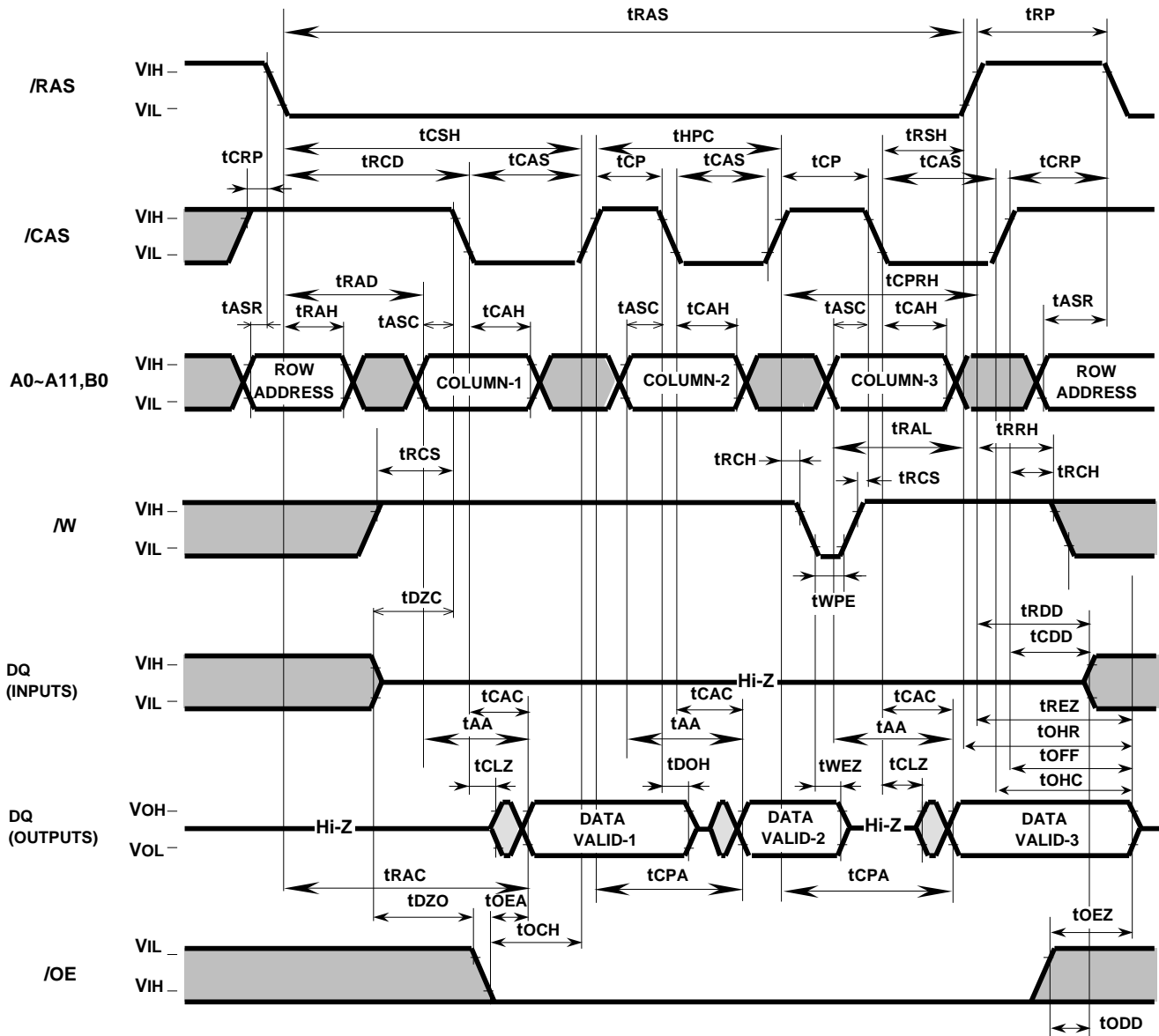
Hyper Page Mode Read Cycle (Hi-Z control by OE)



MH16V7245BATJ -5, -6

HYPER PAGE MODE 1207959552 - BIT (16777216 - WORD BY 72 - BIT) DYNAMIC RAM

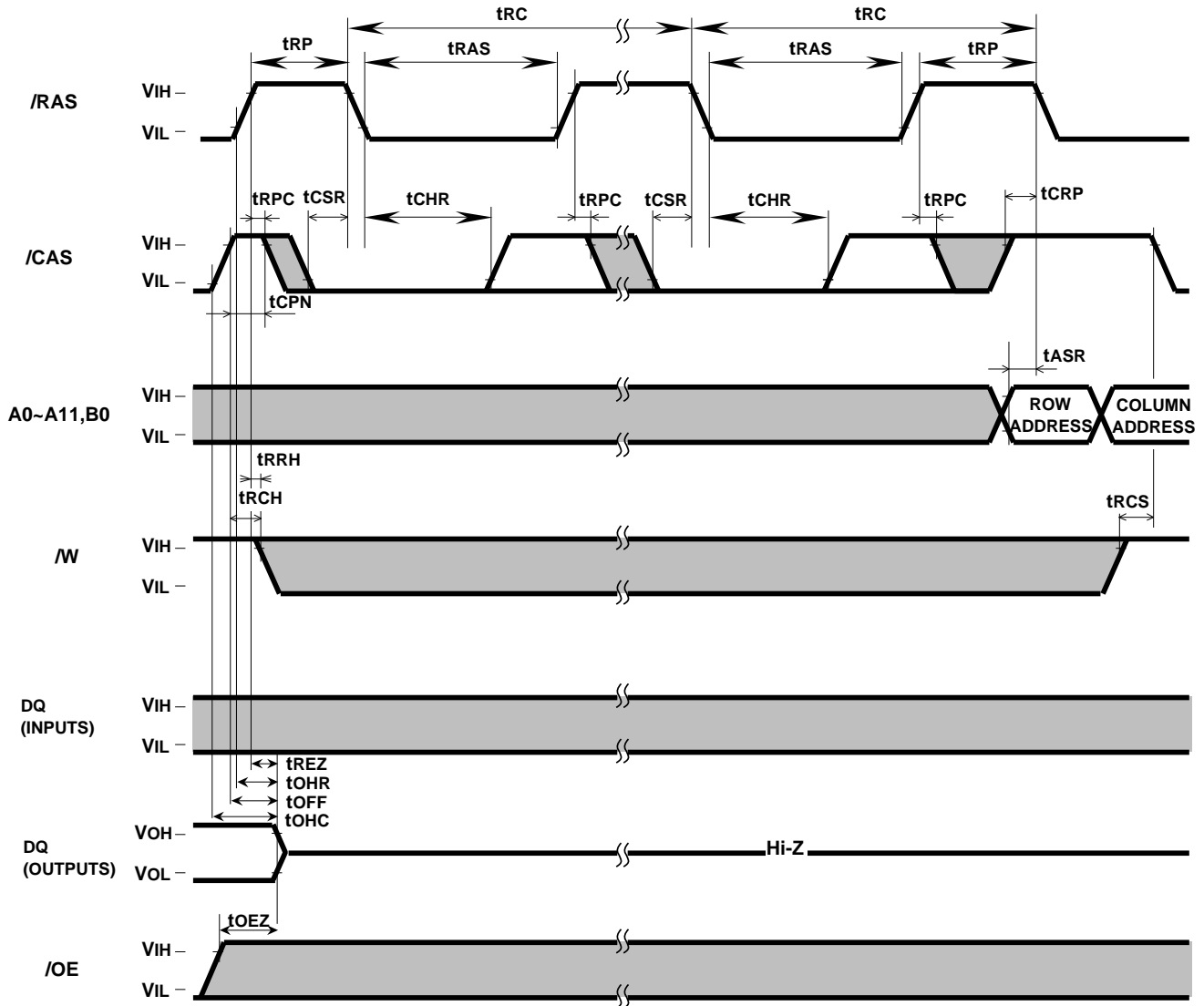
Hyper Page Mode Read Cycle (Hi-Z control by \overline{W})



MH16V7245BATJ -5, -6

HYPER PAGE MODE 1207959552 - BIT (16777216 - WORD BY 72 - BIT) DYNAMIC RAM

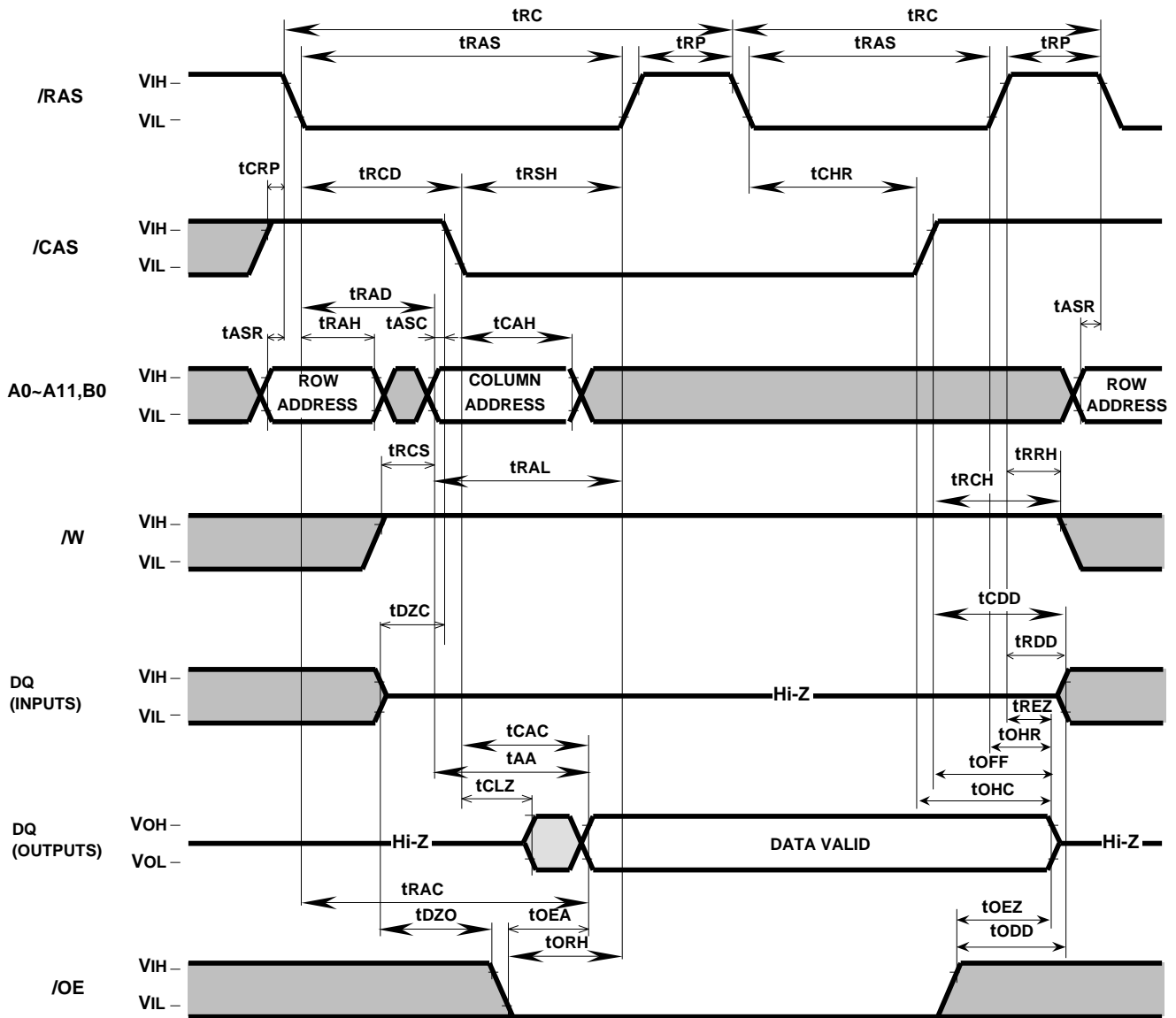
/CAS before /RAS Refresh Cycle



MH16V7245BATJ -5, -6

HYPER PAGE MODE 1207959552 - BIT (16777216 - WORD BY 72 - BIT) DYNAMIC RAM

Hidden Refresh Cycle (Read) (Note 31)



Note 31: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

MH16V7245BATJ -5, -6

HYPER PAGE MODE 1207959552 - BIT (16777216 - WORD BY 72 - BIT) DYNAMIC RAM

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