MH32S64APHB -6,-7,-8

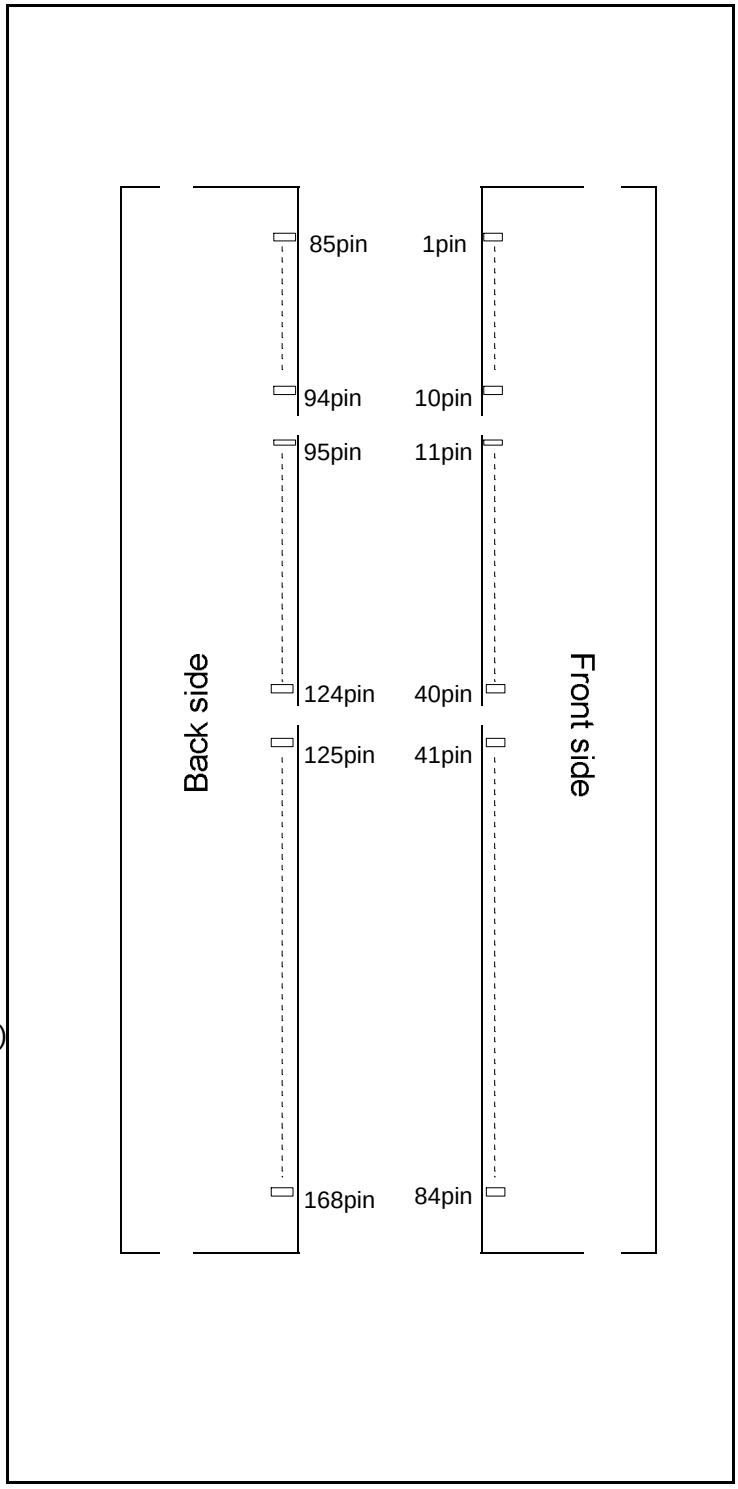
2,147,483,648-BIT (33,554,432 - WORD BY 64-BIT)Synchronous DRAM

DESCRIPTION

The MH32S64APHB is 33554432 - word by 64-bit Synchronous DRAM module. This consists of sixteen industry standard 16Mx8 Synchronous DRAMs in TSOP and one industory standard EEPROM in TSSOP.

The mounting of TSOP on a card edge Dual Inline package provides any application where high densities and large quantities of memory are required.

This is a socket type - memory modules, suitable for easy interchange or addition of modules.



FEATURES

	Frequency	CLK Access Time (Component SDRAM)
-6	133MHz	5.4ns(CL=3)
-7	100MHz	6.0ns(CL=2)
-8	100MHz	6.0ns(CL=3)

- Utilizes industry standard 16M x 8 Synchronous DRAMs TSOP and industry standard EEPROM in TSSOP
- 168-pin (84-pin dual in-line package)
- single 3.3V±0.3V power supply
- Max. Clock frequency -6:133MHz,-7,8:100MHz
- Fully synchronous operation referenced to clock rising edge
- 4 bank operation controlled by BA0,1(Bank Address)
- /CAS latency- 2/3(programmable)
- Burst length- 1/2/4/8/Full Page(programmable)
- Burst type- sequential / interleave(programmable)
- Column access - random
- Auto precharge / All bank precharge controlled by A10
- Auto refresh and Self refresh
- 4096 refresh cycle /64ms
- LVTTL Interface
- Discrete IC and module design conform to PC100/PC133 specification.

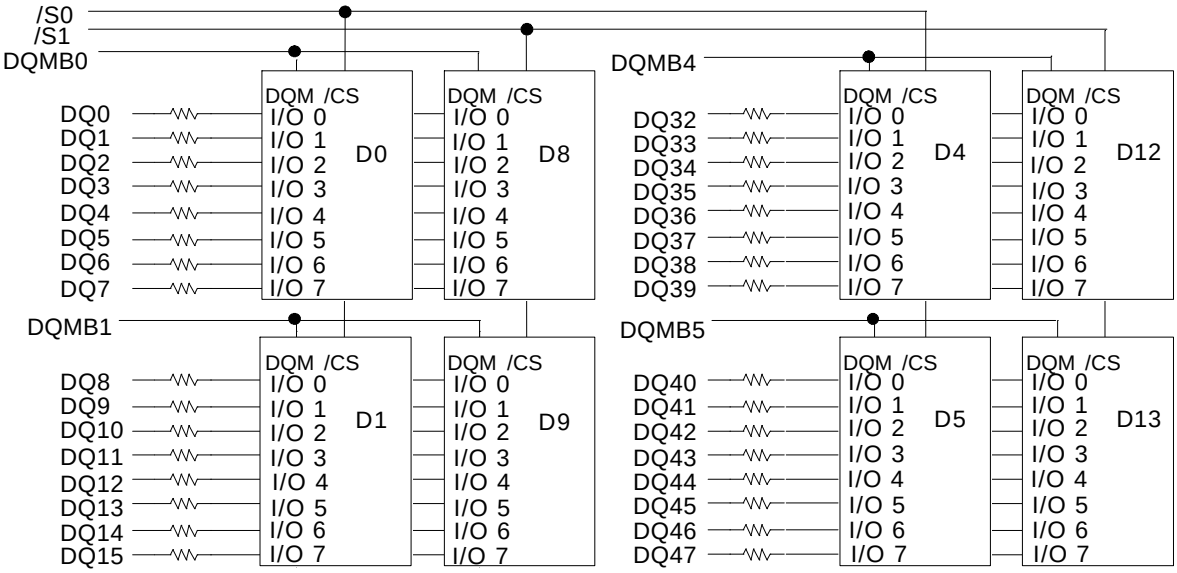
APPLICATION

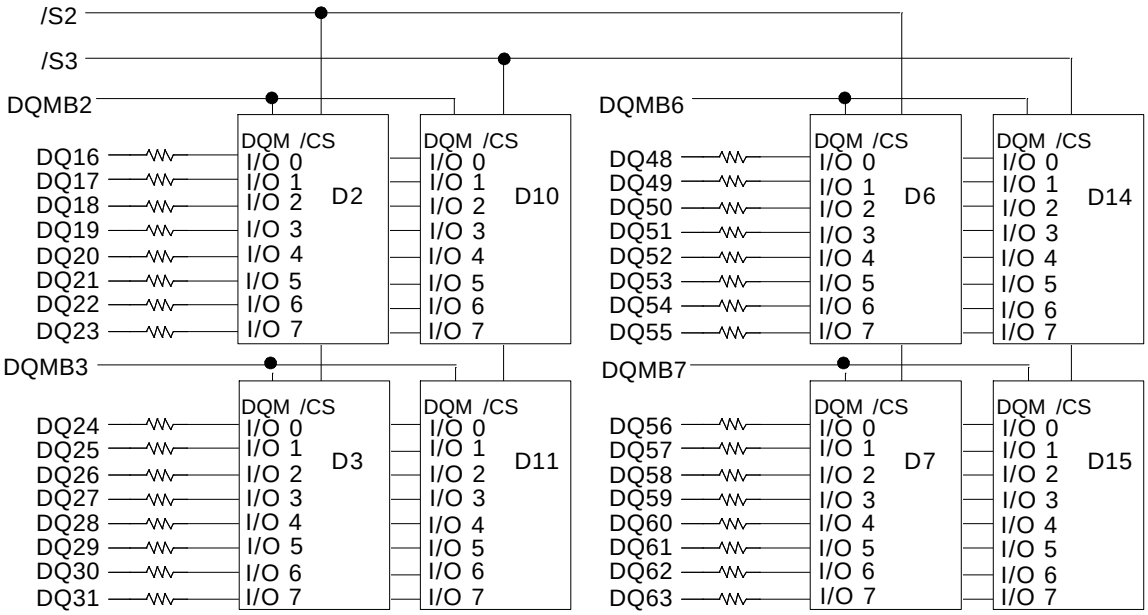
PC main memory

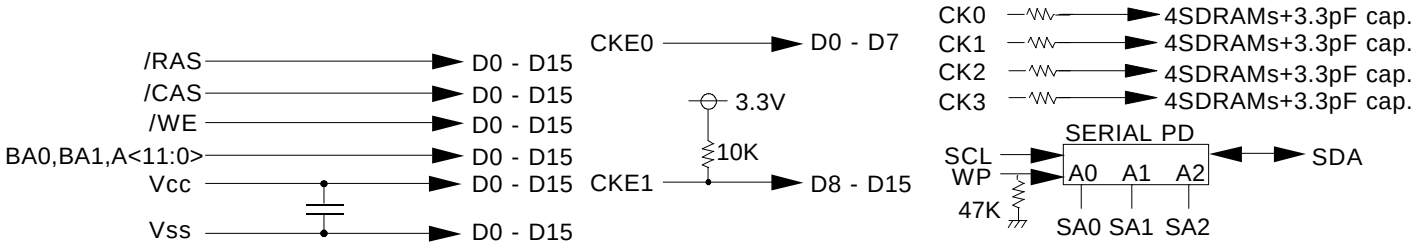
PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	/S2	87	DQ33	129	/S3
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VDD	48	NC	90	VDD	132	NC
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	CKE1	105	NC	147	NC
22	NC	64	VSS	106	NC	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	VSS	110	VDD	152	VSS
27	/WE0	69	DQ24	111	/CAS	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	/S0	72	DQ27	114	/S1	156	DQ59
31	NC	73	VDD	115	/RAS	157	VDD
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	CK1	167	SA2
42	CK0	84	VDD	126	NC	168	VDD

NC = No Connection

Block Diagram







Serial Presence Detect Table I

Byte	Function described		SPD enrty data	SPD DATA(hex)
0	Defines # bytes written into serial memory at module mfgr		128	80
1	Total # bytes of SPD memory device		256 Bytes	08
2	Fundamental memory type		SDRAM	04
3	# Row Addresses on this assembly		A0-A11	0C
4	# Column Addresses on this assembly		A0-A9	0A
5	# Module Banks on this assembly		2BANK	02
6	Data Width of this assembly...		x64	40
7	... Data Width continuation		0	00
8	Voltage interface standard of this assembly		LVTTL	01
9	SDRAM Cycletime at Max. Supported CAS Latency (CL). Cycle time for CL=3	-6	7.5ns	75
		-7,-8	10ns	A0
10	SDRAM Access from Clock tAC for CL=3	-6	5.4ns	54
		-7,-8	6ns	60
11	DIMM Configuration type (Non-parity,Parity,ECC)		Non-PARITY	00
12	Refresh Rate/Type		self refresh(15.625uS)	80
13	SDRAM width,Primary DRAM		x8	08
14	Error Checking SDRAM data width		N/A	00
15	Minimum Clock Delay,Back to Back Random Column Addresses		1	01
16	Burst Lengths Supported		1/2/4/8/Full page	8F
17	# Banks on Each SDRAM device		4bank	04
18	CAS# Latency		2/3	06
19	CS# Latency		0	01
20	Write Latency		0	01
21	SDRAM Module Attributes		non-buffered,non-registered	00
22	SDRAM Device Attributes:General		Precharge All,Auto precharge	0E
23	SDRAM Cycle time(2nd highest CAS latency) Cycle time for CL=2	-6	10ns	A0
		-7	10ns	A0
		-8	13ns	D0
24	SDRAM Access form Clock(2nd highest CAS latency) tAC for CL=2	-6	6ns	60
		-7	6ns	60
		-8	7ns	70
25	SDRAM Cycle time(3rd highest CAS latency)		N/A	00
26	SDRAM Access form Clock(3rd highest CAS latency)		N/A	00
27	Precharge to Active Minimum	-6	22.5ns	17
		-7,-8	20ns	14
28	Row Active to Row Active Min.	-6	15ns	0F
		-7,-8	20ns	14
29	RAS to CAS Delay Min	-6	22.5ns	17
		-7,-8	20ns	14
30	Active to Precharge Min	-6	45ns	2D
		-7,-8	50ns	32

Serial Presence Detect Table II

31	Density of each bank on module		128MByte	20
32	Command and Address signal input setup time	-6	1.5ns	15
		-7,-8	2ns	20
33	Command and Address signal input hold time	-6	0.8ns	08
		-7,-8	1ns	10
34	Data signal input setup time	-6	1.5ns	15
		-7,-8	2ns	20
35	Data signal input hold time	-6	0.8ns	08
		-7,-8	1ns	10
36-61	Superset Information (may be used in future)		option	00
62	SPD Revision		rev 1.2B	12
63	Checksum for bytes 0-62		Check sum for -6	B6
			Check sum for -7	17
			Check sum for -8	57
64-71	Manufactures Jedec ID code per JEP-108E		MITSUBISHI	1CFFFFFFFFFFFFFF
72	Manufacturing location		Miyoshi,Japan	01
			Tajima,Japan	02
			NC,USA	03
			Germany	04
73-90	Manufactures Part Number		MH32S64APHB-6	4D48333253363441504842 2D362020202020
			MH32S64APHB-7	4D48333253363441504842 2D372020202020
			MH32S64APHB-8	4D48333253363441504842 2D382020202020
91-92	Revision Code		PCB revision	rrrr
93-94	Manufacturing date		year/week code	yyww
95-98	Assembly Serial Number		serial number	ssssssss
99-125	Manufacture Specific Data		option	00
126	Intetl specification frequency		100MHz	64
127	Intel specification CAS# Latency support	-6,-7	CL=2/3,AP,CK0,2	FF
		-8	CL=3,AP,CK0,2	FD
128+	Unused storage locations		open	00

PIN FUNCTION

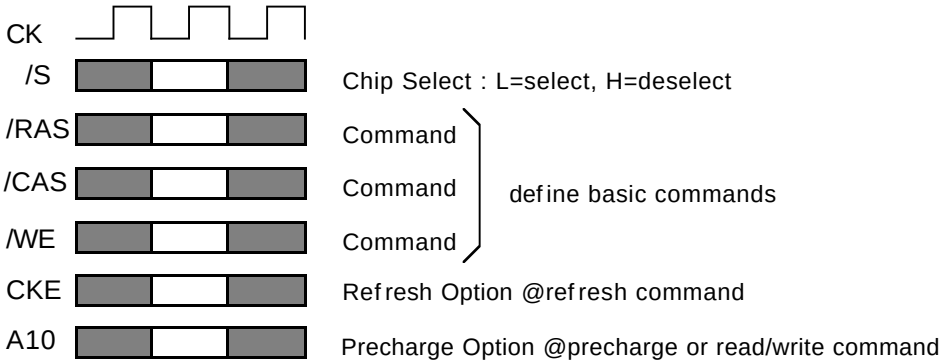
CK (CK0 ~ CK3)	Input	Master Clock:All other inputs are referenced to the rising edge of CK
CKE0,1	Input	Clock Enable:CKE controls internal clock.When CKE is low,internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE becomes asynchronous input.Self refresh is maintained as long as CKE is low.
/S (/S0~3)	Input	Chip Select: When /S is high,any command means No Operation.
/RAS,/CAS,/WE	Input	Combination of /RAS,/CAS,/WE defines basic commands.
A0-11	Input	A0-11 specify the Row/Column Address in conjunction with BA.The Row Address is specified by A0-11.The Column Address is specified by A0-9.A10 is also used to indicate precharge option.When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, all banks are precharged.
BA0,1	Input	Bank Address:BA0,1 is not simply BA.BA specifies the bank to which a command is applied.BA0,1 must be set with ACT,PRE,READ,WRITE commands
DQ0-63	Input/Output	Data In and Data out are referenced to the rising edge of CK
DQMB0-7	Input	Din Mask/Output Disable:When DQMB is high in burst write.Din for the current cycle is masked.When DQMB is high in burst read,Dout is disabled at the next but one cycle.
Vdd,Vss	Power Supply	Power Supply for the memory mounted module.
SCL	Input	Serial clock for serial PD
SDA	Output	Serial data for serial PD
SA0-3	Input	Address input for serial PD

BASIC FUNCTIONS

The MH32S64APHB provides basic functions,bank(row)activate,burst read / write, bank(row)precharge,and auto / self refresh.

Each command is defined by control signals of /RAS,/CAS and /WE at CK rising edge. In addition to 3 signals,/S,CKE and A10 are used as chip select,refresh option,and precharge option,respectively.

To know the detailed definition of commands please see the command truth table.



Activate(ACT) [/RAS =L, /CAS = /WE =H]

ACT command activates a row in an idle bank indicated by BA.

Read(READ) [/RAS =H,/CAS =L, /WE =H]

READ command starts burst read from the active bank indicated by BA.First output data appears after /CAS latency. When A10 =H at this command,the bank is deactivated after the burst read(auto-precharge,**READA**).

Write(WRITE) [/RAS =H, /CAS = /WE =L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 =H at this command, the bank is deactivated after the burst write(auto-precharge,**WRITEA**).

Precharge(PRE) [/RAS =L, /CAS =H,/WE =L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read / write operation. When A10 =H at this command, both banks are deactivated(precharge all, **PREA**).

Auto-Refresh(REFA) [/RAS =/CAS =L, /WE =CKE =H]

REFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

COMMAND TRUTH TABLE

COMMAND	MNEMONIC	CKE n-1	CKE n	/S	/RAS	/CAS	/WE	BA0,1	A11	A10	A0-9
Deselect	DESEL	H	X	H	X	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X	X
Row Adress Entry & Bank Activate	ACT	H	X	L	L	H	H	V	V	V	V
Single Bank Precharge	PRE	H	X	L	L	H	L	V	X	L	X
Precharge All Bank	PREA	H	X	L	L	H	L	X	X	H	X
Column Address Entry & Write	WRITE	H	X	L	H	L	L	V	V	L	V
Column Address Entry & Write with Auto-Precharge	WRITEA	H	X	L	H	L	L	V	V	H	V
Column Address Entry & Read	READ	H	X	L	H	L	H	V	V	L	V
Column Address Entry & Read with Auto Precharge	READA	H	X	L	H	L	H	V	V	H	V
Auto-Refresh	REFA	H	H	L	L	L	H	X	X	X	X
Self-Refresh Entry	REFS	H	L	L	L	L	H	X	X	X	X
Self-Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X	X
		L	H	L	H	H	H	X	X	X	X
Burst Terminate	TERM	H	X	L	H	H	L	X	X	X	X
Mode Register Set	MRS	H	X	L	L	L	L	L	L	L	V*1

H =High Level, L = Low Level, V = Valid, X = Don't Care, n = CK cycle number

NOTE:
1.A7-9 = 0, A0-6 = Mode Address

FUNCTION TRUTH TABLE

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action
IDLE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA,RA	ACT	Bank Active,Latch RA
	L	L	H	L	BA,A10	PRE/PREA	NOP*4
	L	L	L	H	X	REFA	Auto-Refresh*5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	NOP
	L	H	L	H	BA,CA,A10	READ/READA	Begin Read,Latch CA, Determine Auto-Precharge
	L	H	L	L	BA,CA,A10	WRITE/ WRITEA	Begin Write,Latch CA, Determine Auto-Precharge
	L	L	H	H	BA,RA	ACT	Bank Active/ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	Precharge/Precharge All
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst
	L	H	L	H	BA,CA,A10	READ/READA	Terminate Burst,Latch CA, Begin New Read,Determine Auto-Precharge*3
	L	H	L	L	BA,CA,A10	WRITE/WRITEA	Terminate Burst,Latch CA, Begin Write,Determine Auto-Precharge*3
	L	L	H	H	BA,RA	ACT	Bank Active/ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	Terminate Burst,Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action
WRITE	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst
	L	H	L	H	BA,CA,A10	READ/READA	Terminate Burst,Latch CA, Begin Read,Determine Auto-Precharge*3
	L	H	L	L	BA,CA,A10	WRITE/ WRITEA	Terminate Burst,Latch CA, Begin Write,Determine Auto-Precharge*3
	L	L	H	H	BA,RA	ACT	Bank Active/ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	Terminate Burst,Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL
	L	H	L	L	BA,CA,A10	WRITE/ WRITEA	ILLEGAL
	L	L	H	H	BA,RA	ACT	Bank Active/ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL
	L	H	L	L	BA,CA,A10	WRITE/ WRITEA	ILLEGAL
	L	L	H	H	BA,RA	ACT	Bank Active/ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action
PRE - CHARGING	H	X	X	X	X	DESEL	NOP(Idle after tRP)
	L	H	H	H	X	NOP	NOP(Idle after tRP)
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA,RA	ACT	ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	NOP*4(Idle after tRP)
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP(Row Active after tRCD
	L	H	H	H	X	NOP	NOP(Row Active after tRCD
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA,RA	ACT	ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RE-COVERING	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA,RA	ACT	ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action
RE-FRESHING	H	X	X	X	X	DESEL	NOP(Idle after tRC)
	L	H	H	H	X	NOP	NOP(Idle after tRC)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA,RA	ACT	ILLEGAL
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP(Idle after tRSC)
	L	H	H	H	X	NOP	NOP(Idle after tRSC)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA,RA	ACT	ILLEGAL
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

ABBREVIATIONS:
H = Hige Level, L = Low Level, X = Don't Care
BA = Bank Address, RA = Row Address, CA = Column Address, NOP = No Operation

NOTES:
1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state.May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and / or date-integrity are not guaranteed.

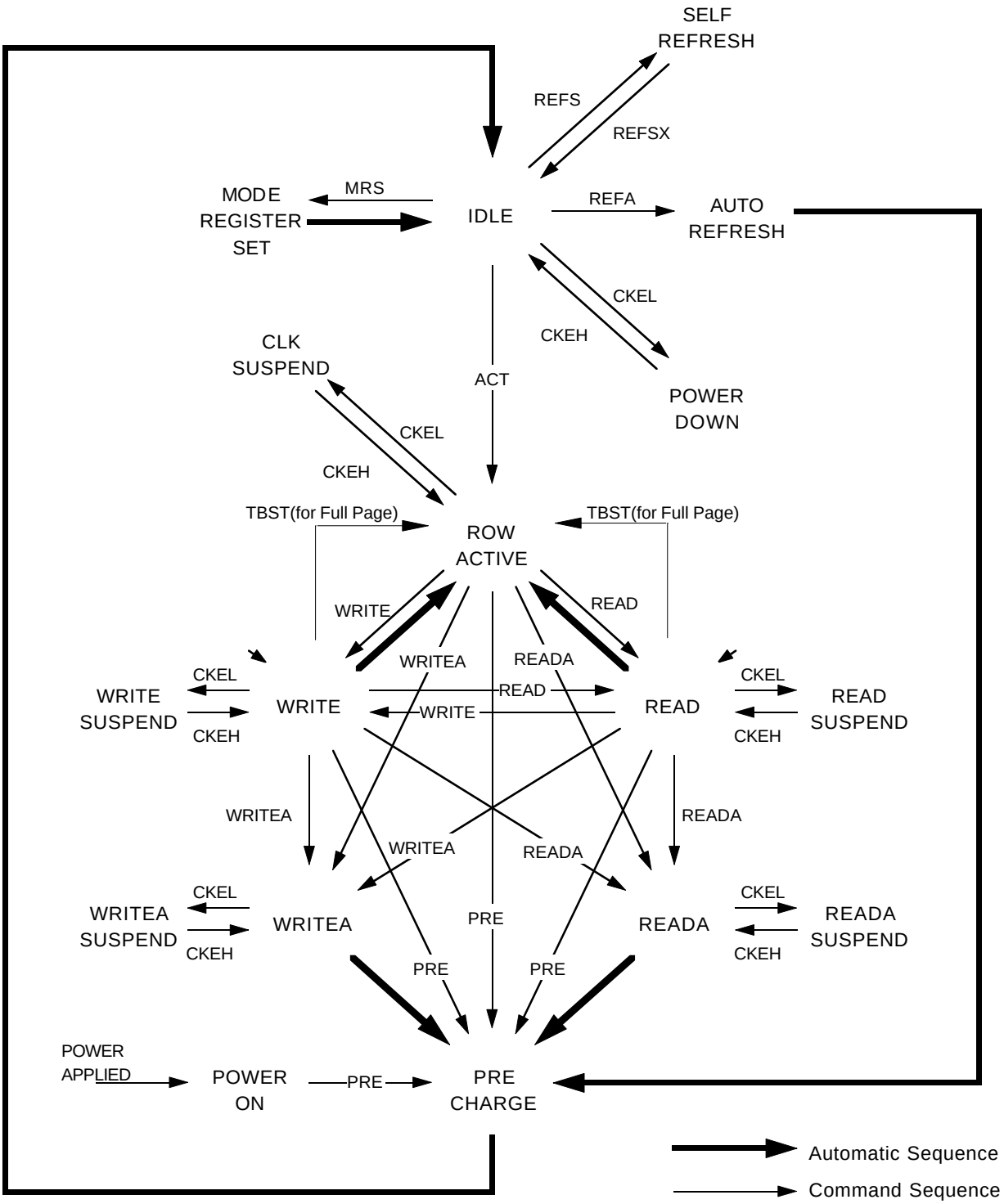
FUNCTION TRUTH TABLE FOR CKE

Current State	CKE n-1	CKE n	/S	/RAS	/CAS	/WE	Add	Action
SELF - REFRESH*1	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self-Refresh(Idle after tRC)
	L	H	L	H	H	H	X	Exit Self-Refresh(Idle after tRC)
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain Self-Refresh)
POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Power Down to Idle
	L	L	X	X	X	X	X	NOP(Maintain Self-Refresh)
ALL BANKS IDLE*2	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State = Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	X	X	X	X	X	Begin CK0 Suspend at Next Cycle*3
	L	H	X	X	X	X	X	Exit CK0 Suspend at Next Cycle*3
	L	L	X	X	X	X	X	Maintain CK0 Suspend

ABBREVIATIONS:
H = High Level, L = Low Level, X = Don't Care

NOTES:
1. CKE Low to High transition will re-enable CK and other inputs **asynchronously**.
   A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from the All banks idle State.
3. Must be legal command.

SIMPLIFIED STATE DIAGRAM



POWER ON SEQUENCE

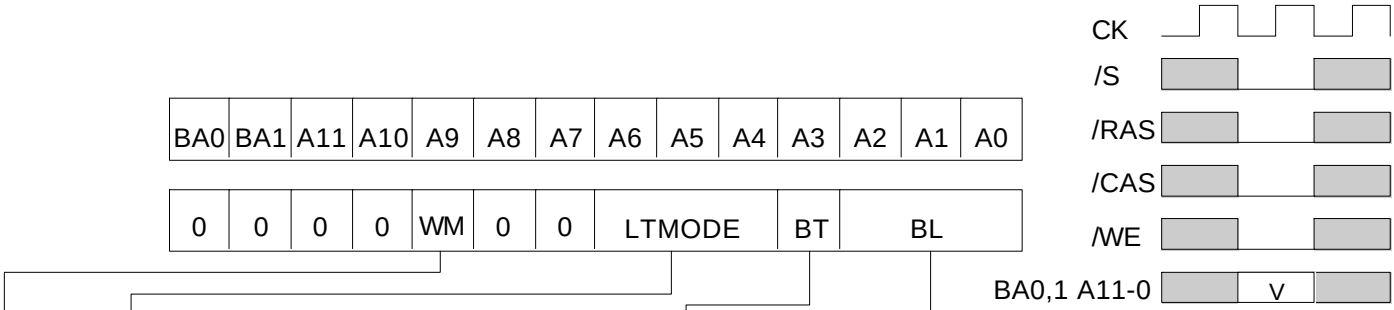
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high, DQMB0-7 high and NOP condition at the inputs.
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200us.
3. Issue precharge commands for all banks. (PRE or PREA)
4. After all banks become idle state (after tRP), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

After these sequence, the SDRAM is idle state and ready for normal operation.

MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register(MRS). The mode register stores these date until the next MRS command, which may be issue when both banks are in idle state. After tRSC from a MRS command, the SDRAM is ready for new command.



BA0	BA1	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

0	0	0	0	WM	0	0	LTMODE		BT	BL			

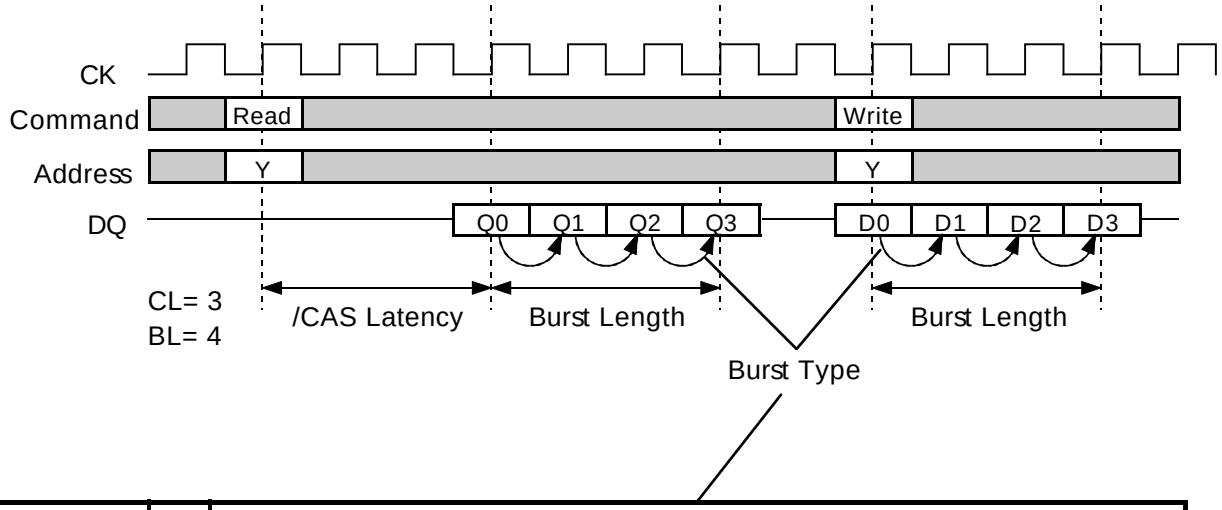
	CL	/CAS LATENCY
LATENCY MODE	0 0 0	R
	0 0 1	R
	0 1 0	2
	0 1 1	3
	1 0 0	R
	1 0 1	R
	1 1 0	R
	1 1 1	R

	BL	BT= 0	BT= 1
BURST LENGTH	0 0 0	1	1
	0 0 1	2	2
	0 1 0	4	4
	0 1 1	8	8
	1 0 0	R	R
	1 0 1	R	R
	1 1 0	R	R
	1 1 1	FP	R

WRITE MODE	0	BURST
	1	SINGLE BIT

BURST TYPE	0	SEQUENTIAL
	1	INTERLEAVED

R:Reserved for Future Use
FP: Full Page



Initial Address			BL	Column Addressing															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

OPERATION DESCRIPTION

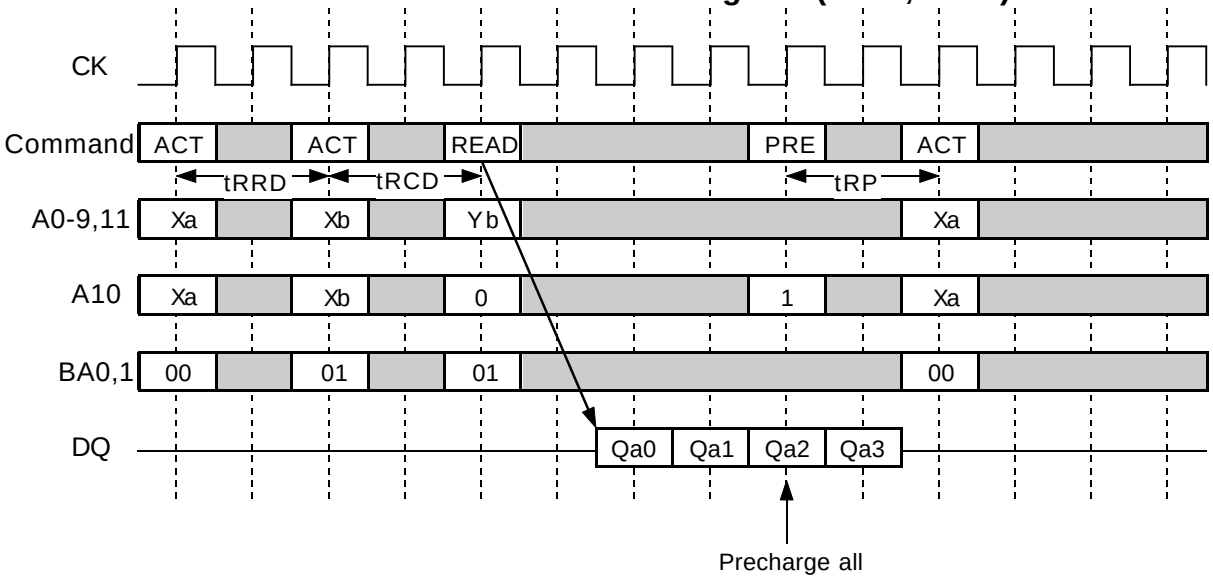
BANK ACTIVATE

One of four banks is activated by an ACT command.
An bank is selected by BA0-1. A row is selected by A0-11.
Multiple banks can be active state concurrently by issuing multiple ACT commands.
Minimum activation interval between one bank and another bank is tRRD.

PRECHARGE

An open bank is deactivated by a PRE command.
A bank to be deactivated is designated by BA0-1.
When multiple banks are active, a precharge all command (PREA, PRE + A10=H) deactivates all of open banks at the same time. BA0-1 are "Don't Care" in this case.
Minimum delay time of an ACT command after a PRE command to the same bank is tRP.

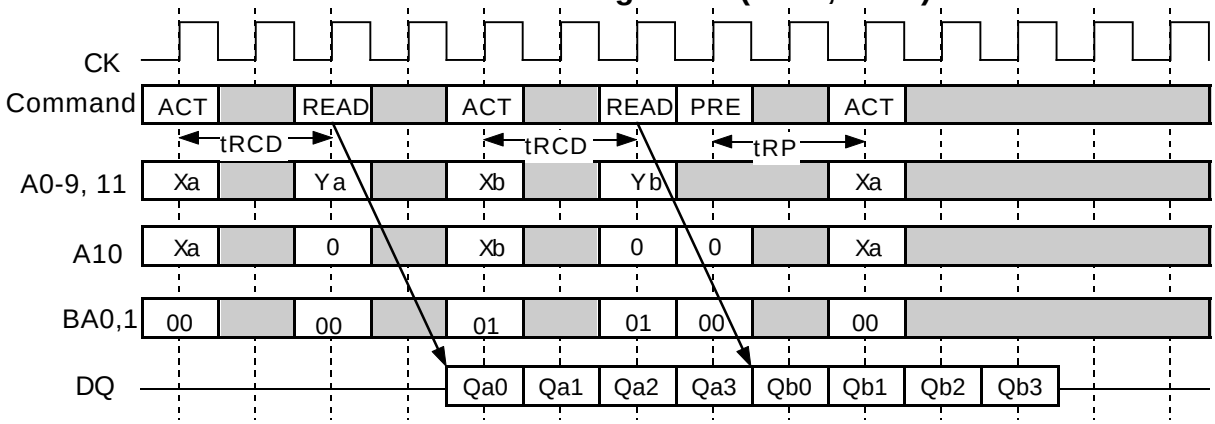
Bank Activation and Precharge All (BL=4, CL=2)



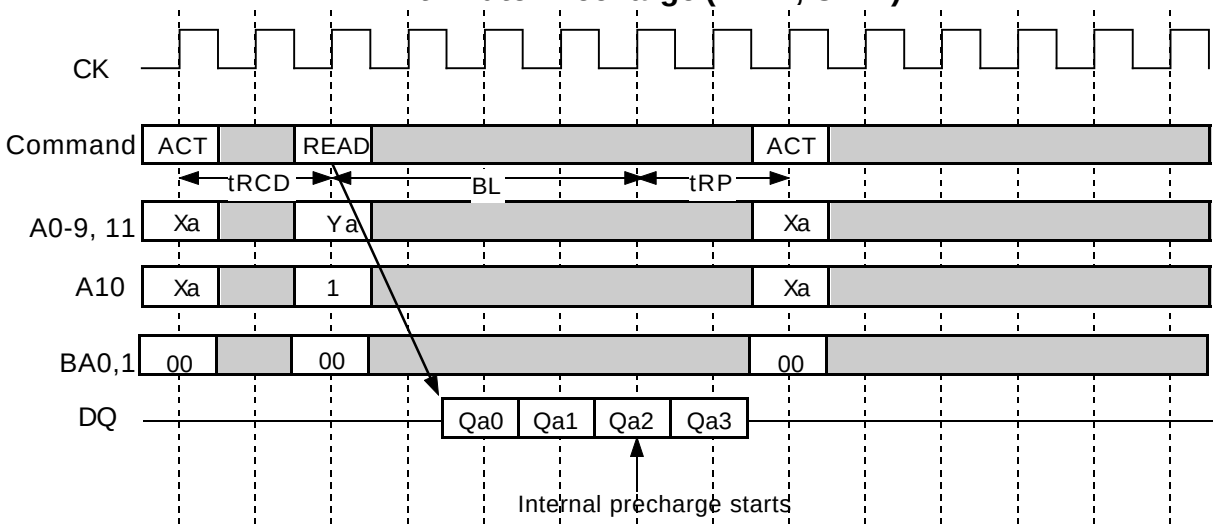
READ

A READ command can be issued to any active bank. The start address is specified by A0-9 (x8) . 1st output data is available after the /CAS Latency from the READ. The consecutive data length is defined by the Burst Length. The address sequence of the burst data is defined by the Burst Type. Minimum delay time of a READ command after an ACT command to the same bank is tRCD.
When A10 is high at a READ command, auto-precharge (READA) is performed. Any command (READ, WRITE, PRE, ACT, TBST) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at the BL after READA. The next ACT command can be issued after (BL + tRP) from the previous READA. In any case, tRCD+BL $\geq$ tRASmin must be met.

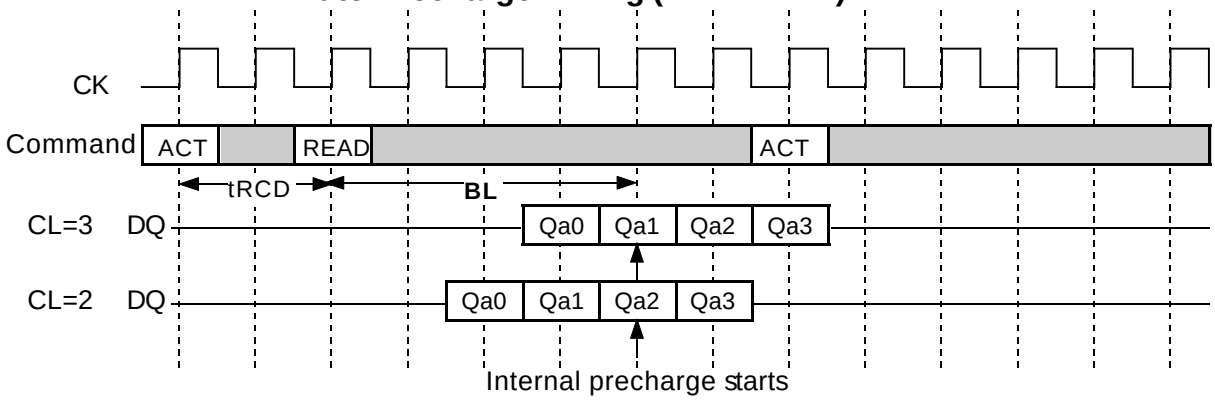
Multi Bank Interleaving READ (BL=4, CL=2)



READ with Auto-Precharge (BL=4, CL=2)



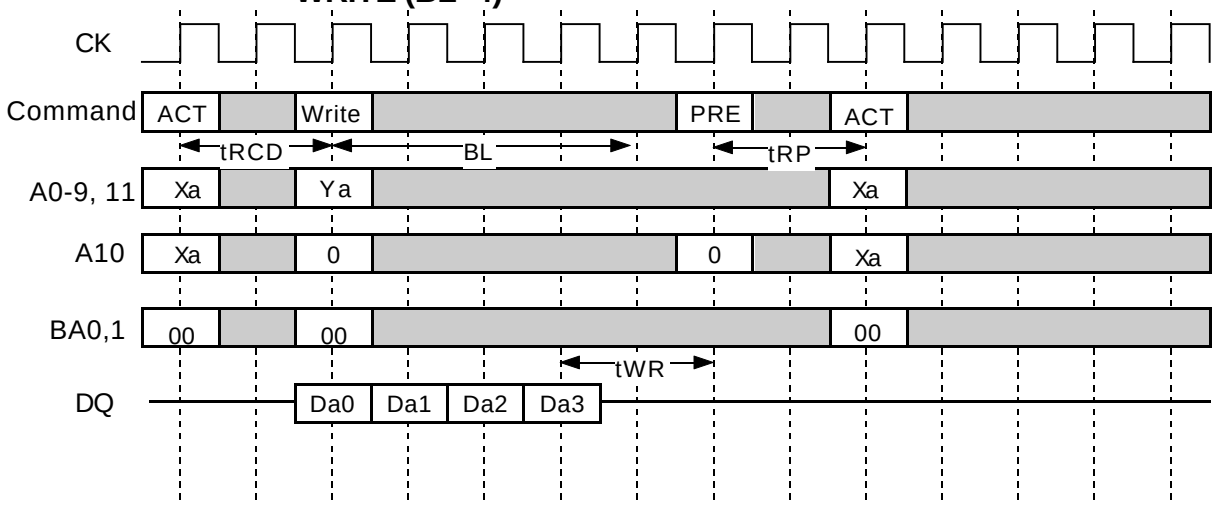
Auto-Precharge Timing (READ BL=4)



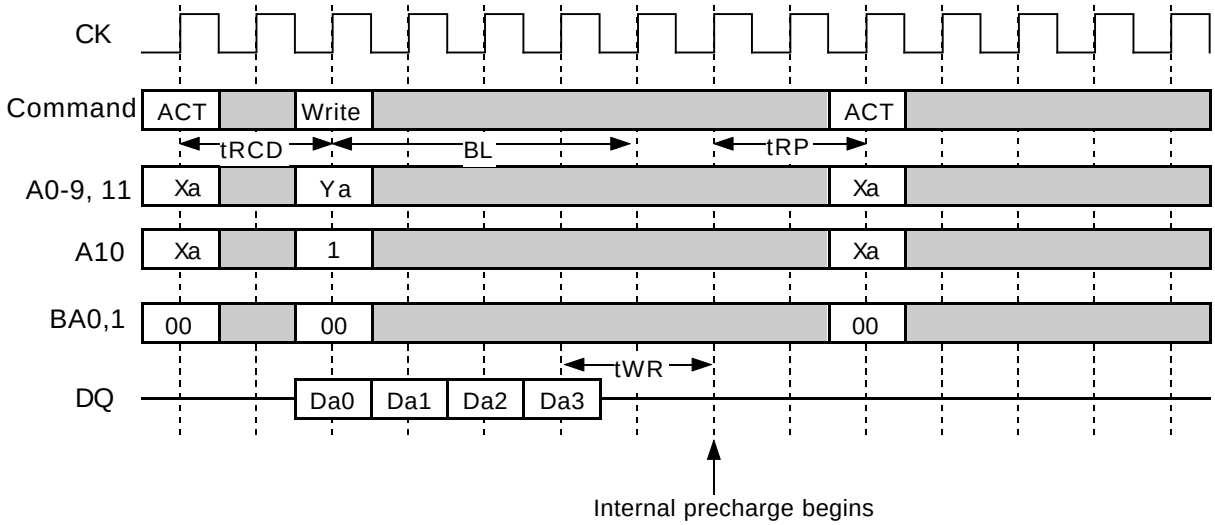
WRITE

A WRITE command can be issued to any active bank. The start address is specified by A0-9 (x8). 1st input data is set at the same cycle as the WRITE. The consecutive data length to be written is defined by the Burst Length. The address sequence of burst data is defined by the Burst Type. Minimum delay time of a WRITE command after an ACT command to the same bank is tRCD. From the last input data to the PRE command, the write recovery time (tWR) is required. When A10 is high at a WRITE command, auto-precharge (WRITEA) is performed. Any command (READ, WRITE, PRE, ACT, TBST) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at tWR after the last input data cycle. The next ACT command can be issued after (BL + tWR -1 + tRP) from the previous WRITEA. In any case, tRCD + BL + tWR -1 ≥ tRASmin must be met.

WRITE (BL=4)



WRITE with Auto-Precharge (BL=4)

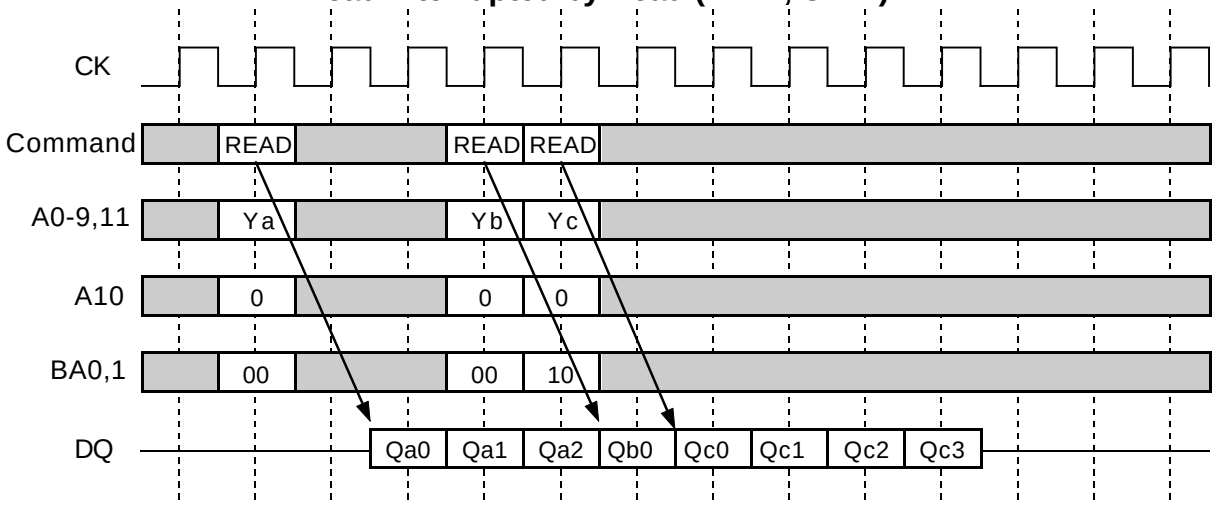


BURST INTERRUPTION

[Read Interrupted by Read]

Burst read oparation can be interrupted by new read of the same or the other bank. Random column access is allowed READ to READ interval is minimum 1 CK

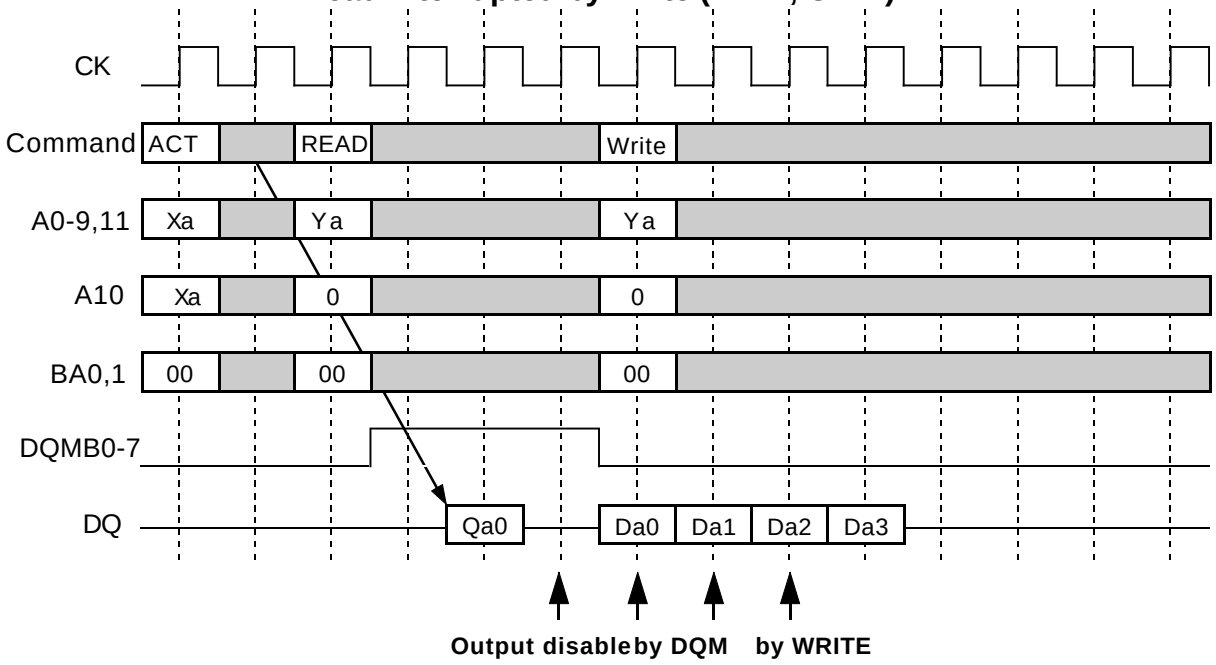
Read Interrupted by Read (BL=4, CL=2)



[Read Interrupted by Write]

Burst read operation can be interrupted by write of any active bank. Random column access is allowed. In this case, the DQ should be controlled adequately by using the DQMB0-7 to prevent the bus contention. The output is disabled automatically 1 cycle after WRITE assertion.

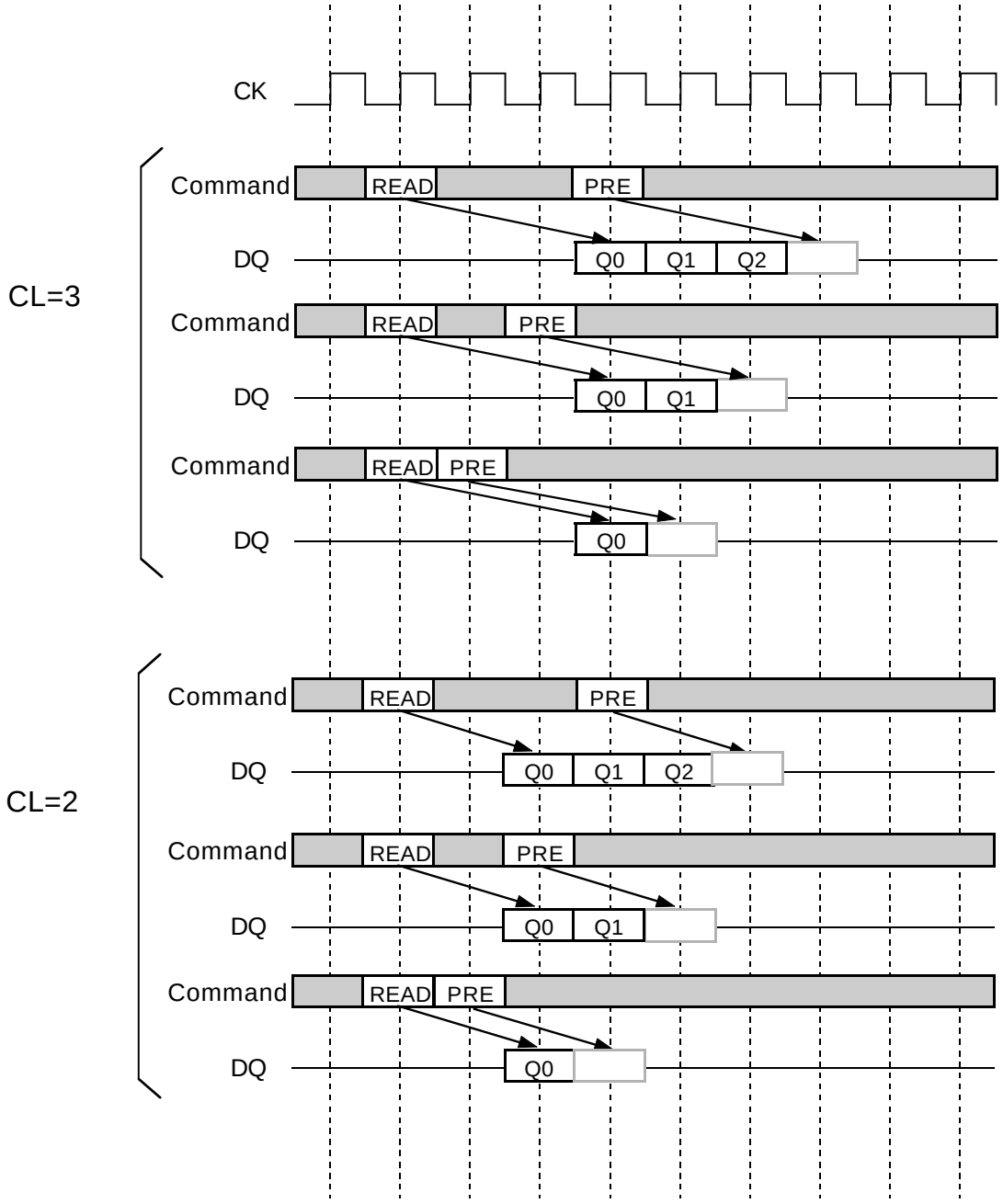
Read Interrupted by Write (BL=4, CL=2)



[Read Interrupted by Precharge]

A burst read operation can be interrupted by precharge of *the same bank*. Read to PRE interval is minimum 1 CK. A PRE command output disable latency is equivalent to the /CAS Latency.

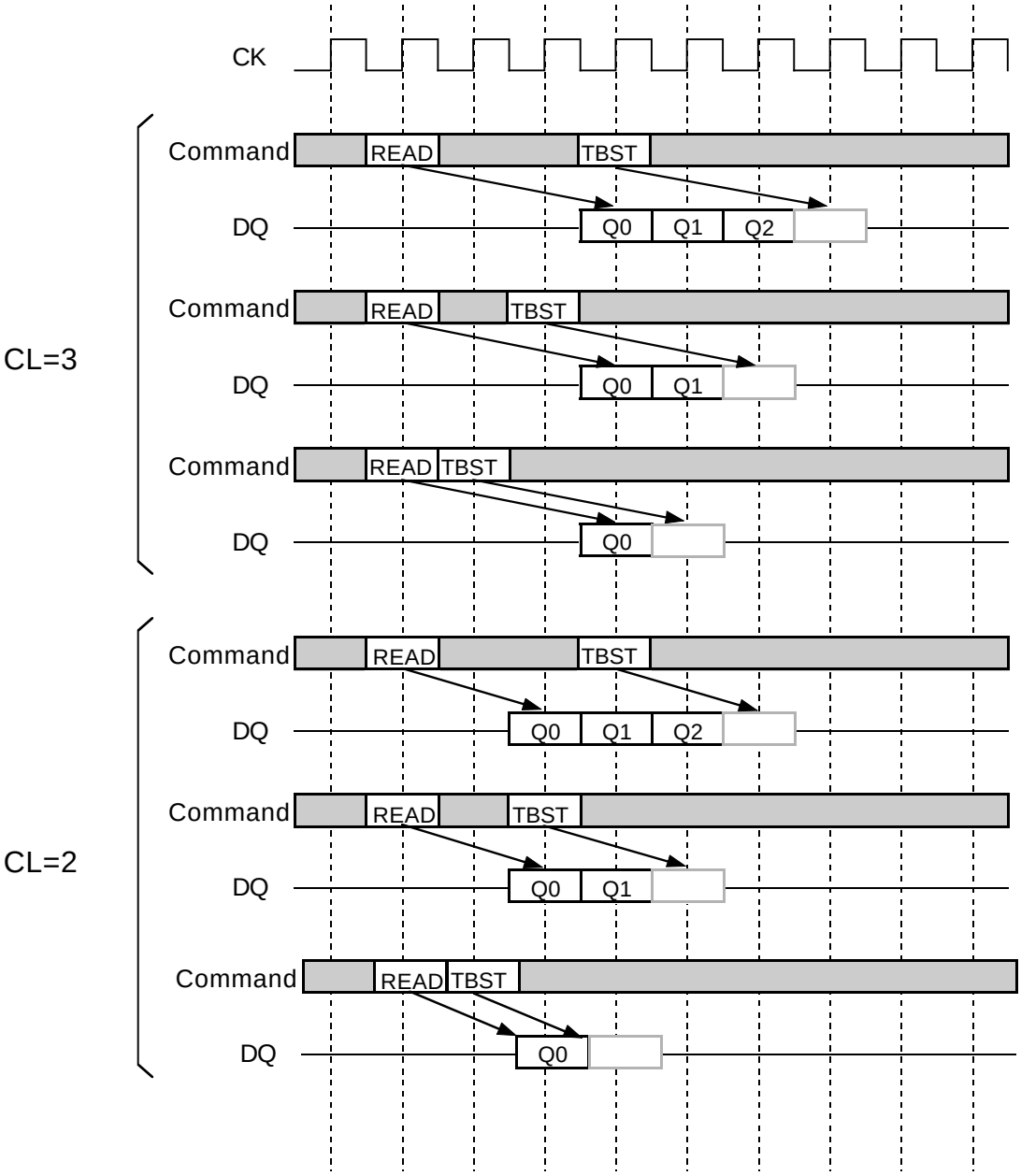
Read Interrupted by Precharge (BL=4)



[Read Interrupted by Burst Terminate]

Similarly to the precharge, burst terminate command can interrupt burst read operation and disable the data output. The terminated bank remains active,READ to TBST interval is minimum of 1 CK. A TBSTcommand to output disable latency is equivalent to the /CAS Latency.

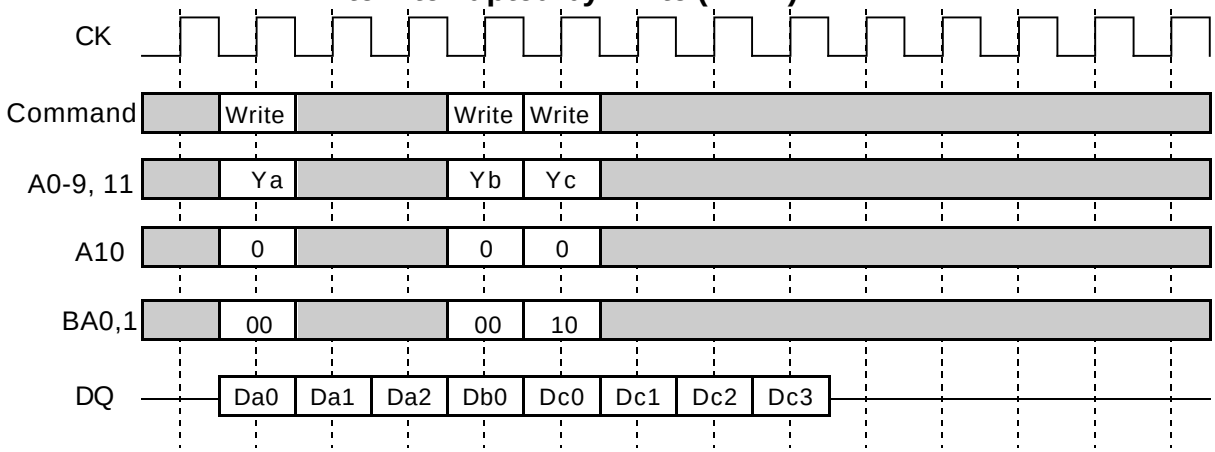
Read Interrupted by Terminate (BL=4)



[Write Interrupted by Write]

Burst write operation can be interrupted by new write of any active bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CK.

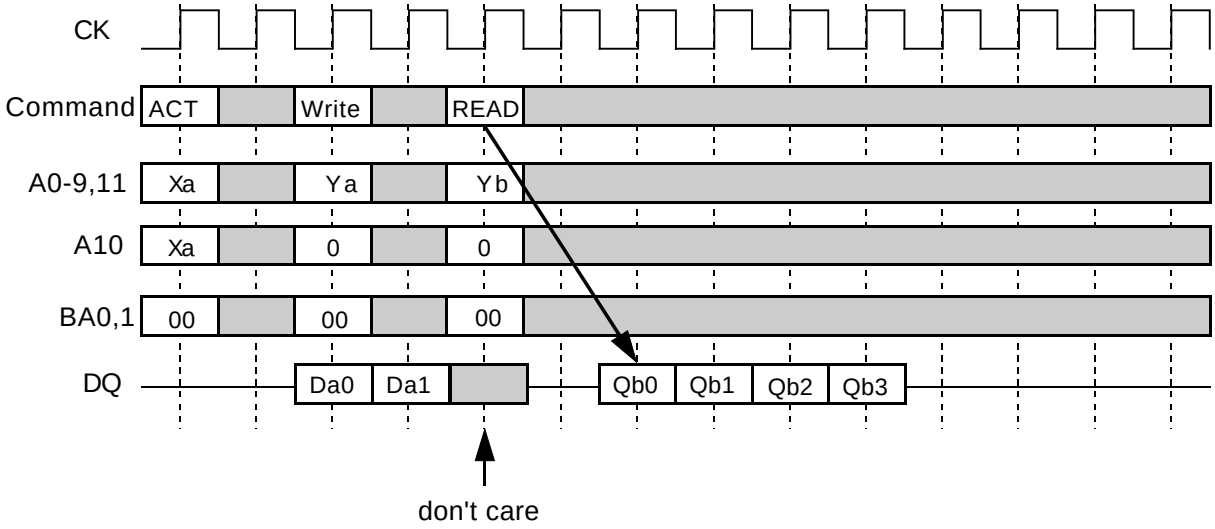
Write Interrupted by Write (BL=4)



[Write Interrupted by Read]

Burst write operation can be interrupted by read of any active bank. Random column access is allowed. WRITE to READ interval is minimum 1 CK. The input data on DQ at the interrupting READ cycle is "don't care".

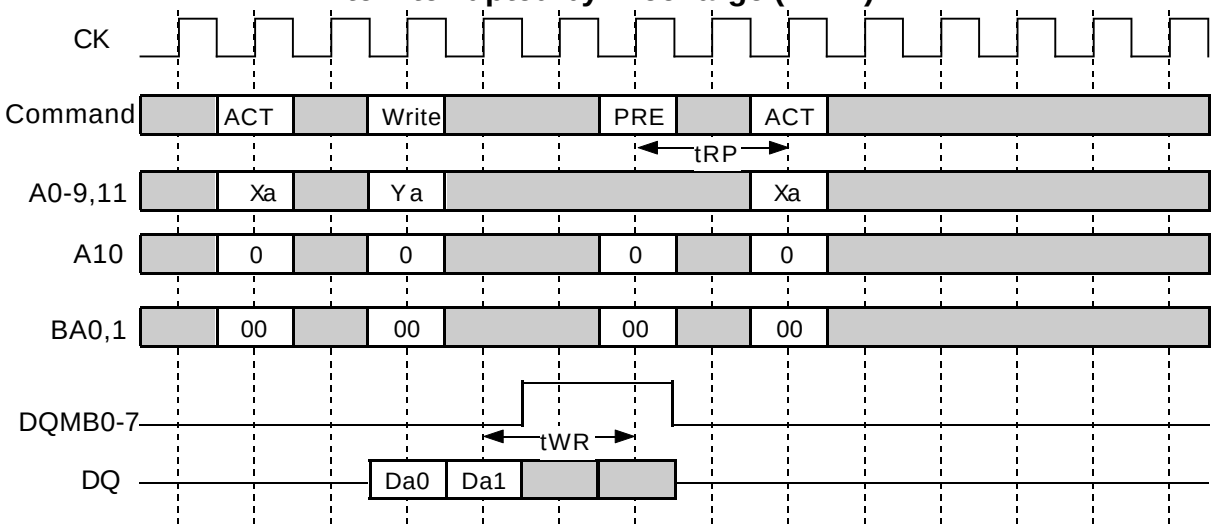
Write Interrupted by Read (BL=4, CL=2)



[Write Interrupted by Precharge]

Burst write operation can be interrupted by precharge of *the same bank*. Write recovery time(tWR) is required from the last data to PRE command. During write recovery, data inputs must be masked by DQM.

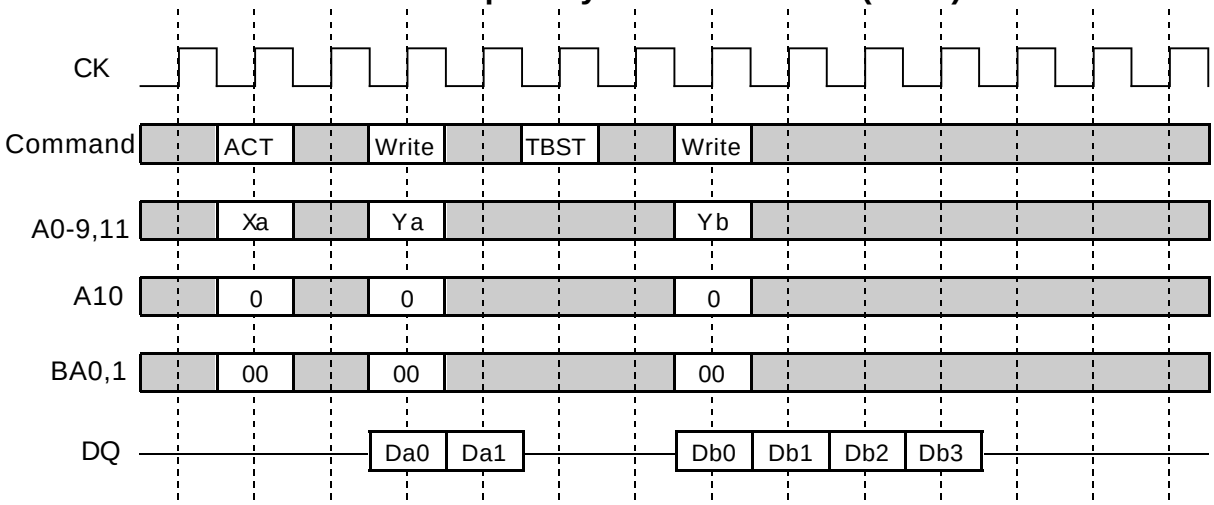
Write Interrupted by Precharge (BL=4)



[Write Interrupted by Burst Terminate]

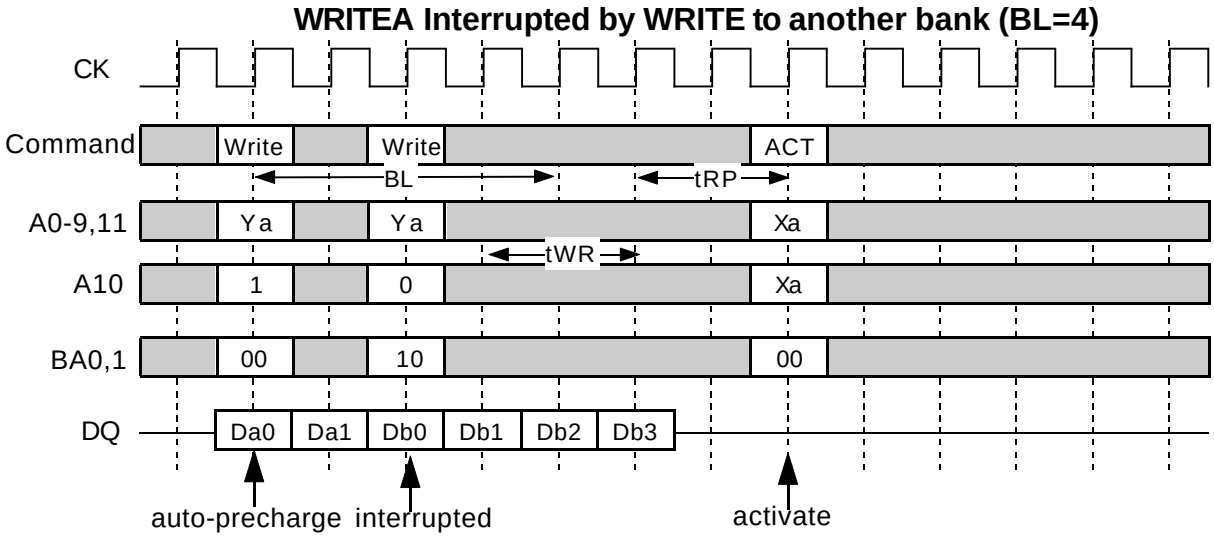
Burst terminate command can terminate burst write operation. In this case, the write recovery time is not required and the bank remains active.The WRITE to TBST minimum interval is 1CK.

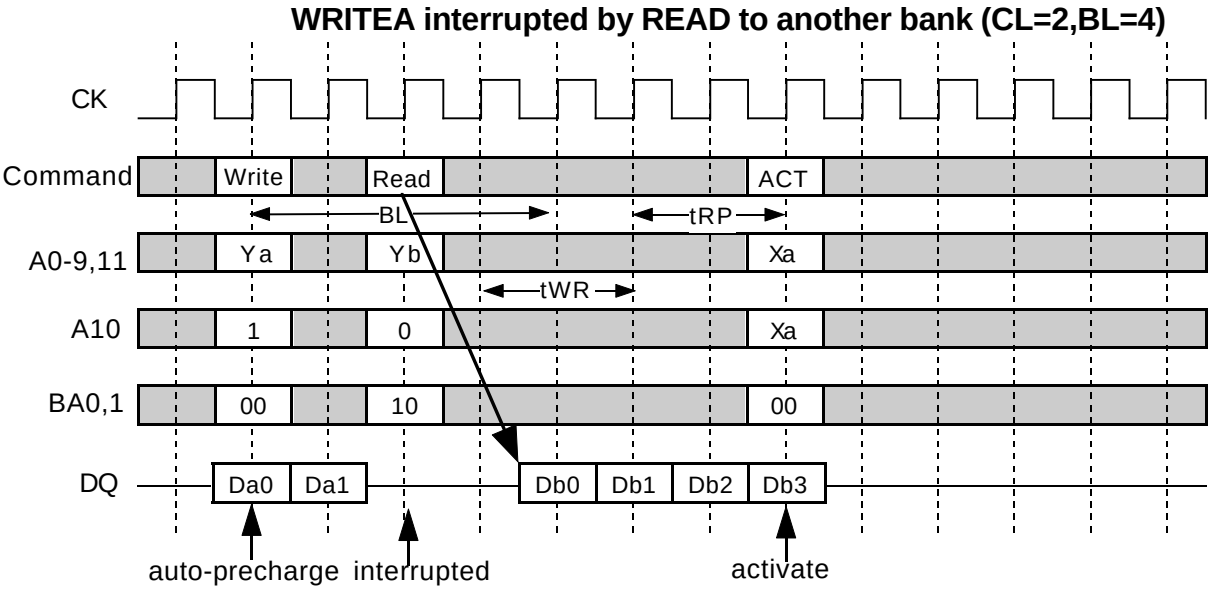
Write Interrupted by Burst Terminate (BL=4)



[Write with Auto-Precharge interrupted by Write or Read to anotehr Bank]

Burst write with auto-precharge can be interrupted by write or read to*another bank*. Next ACT command can be issued after (BL+tWR-1+tRP) from the WRITEA. Auto-precharge interrrupted by a command to the same bank is inhibited.

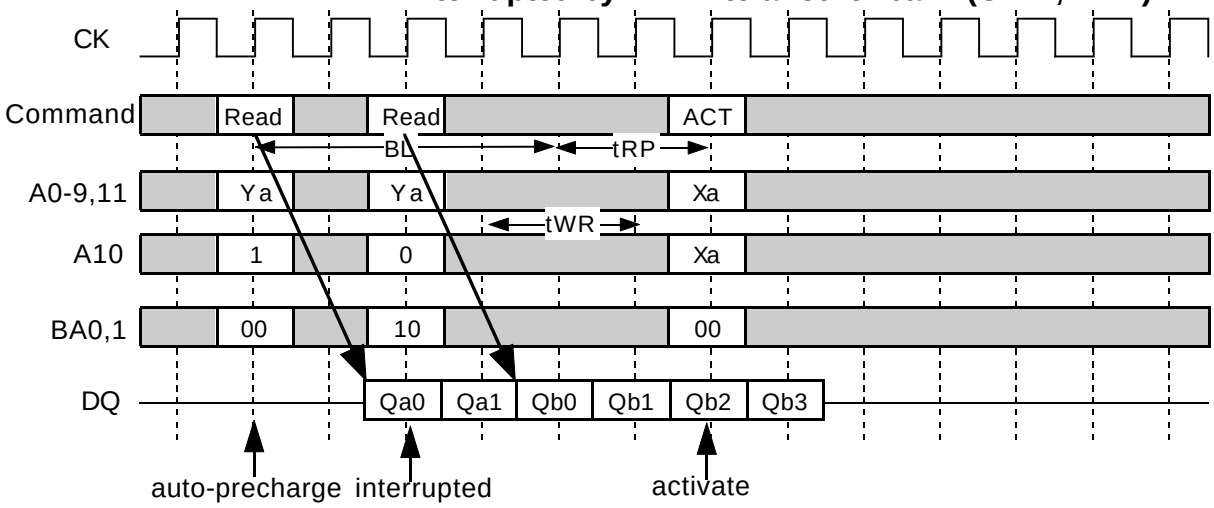




[Read with Auto-Precharge interrupted by Read to anotehr Bank]

Burst read with auto-precharge can be interrupted by read to*another bank*. Next ACT command can be issued after (BL+tRP) from the READA. Auto-precharge interrrupted by a command to the same bank is inhibited.

READA Interrupted by READ to another bank (CL=2,BL=4)



Full Page Burst

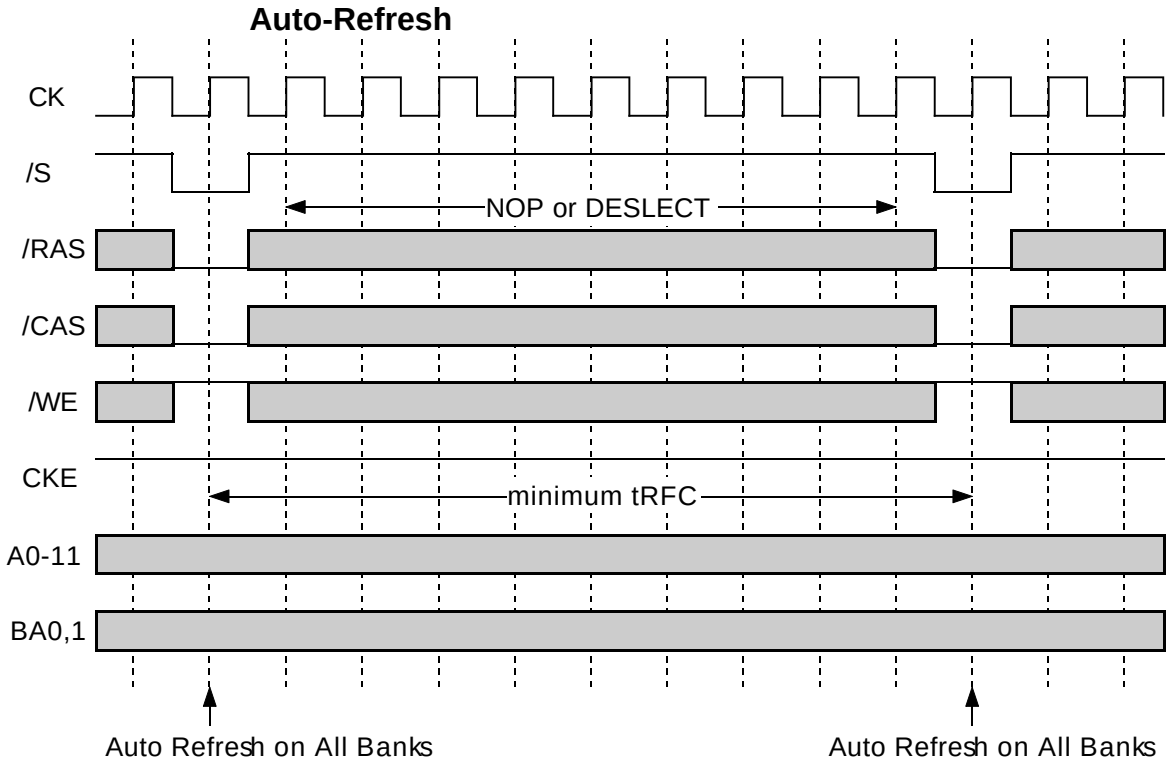
Full page burst length is available for only the sequential burst type. Full page burst read or write is repeated untill aPrecharge or a Burst Terminate command is issued. In case of the full page burst , a read or write with auto-precharge command is illegal.

Single Write

When single write mode is set, burst length for write is always one, independently of Burst Length defined by (A2-0).

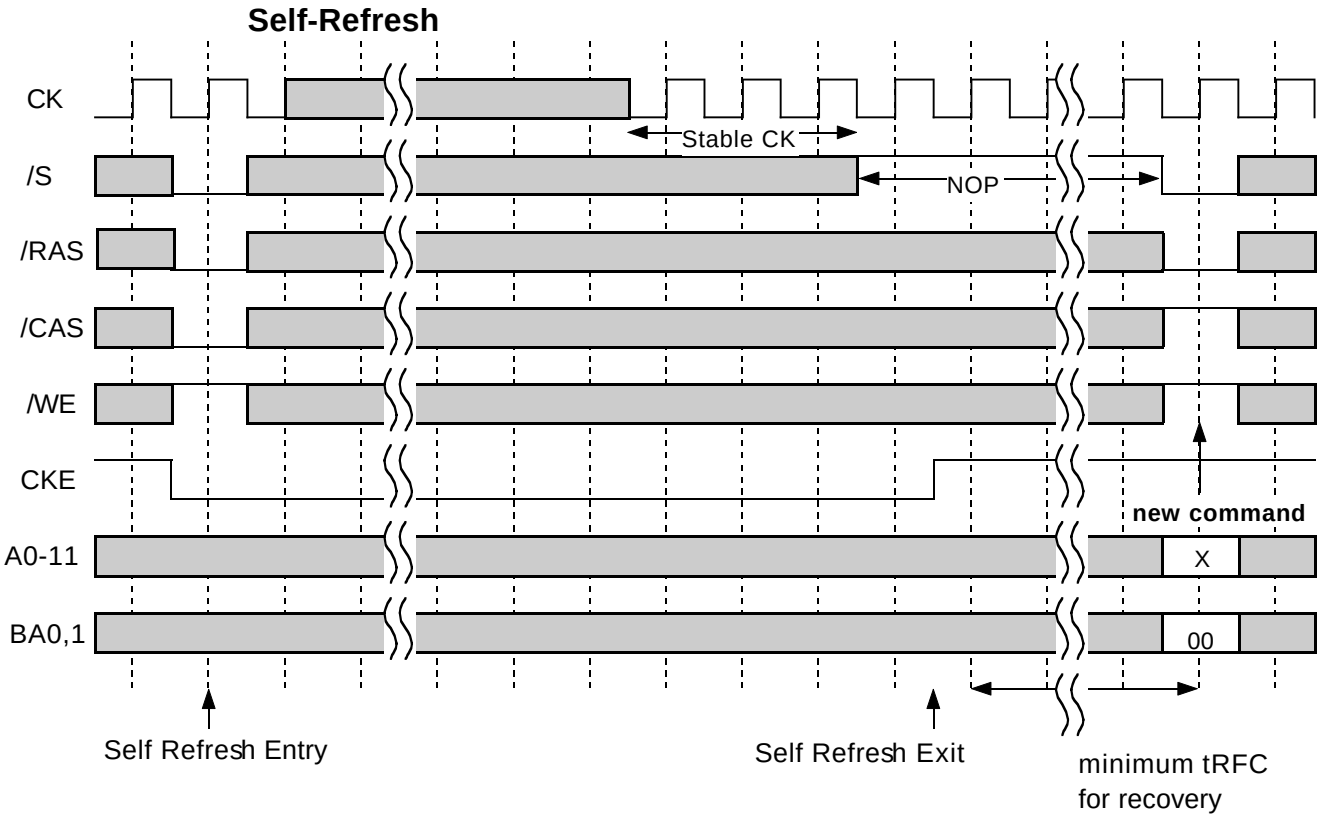
AUTO REFRESH

Single cycle of auto-refresh is initiated with a REFA(/CS=/RAS=/CAS=L, /WE=/CKE=H) command. The refresh address is generated internally. 4096 REFA cycle within 64ms refresh 128Mbit memory cells. The auto-refresh is performed on 4banks concurrently. Before performing an auto-refresh, all banks must be in the idle state. Auto-refresh to auto-refresh interval is minimum tRFC. Any command must not be issued before tRFC from the REFA command.



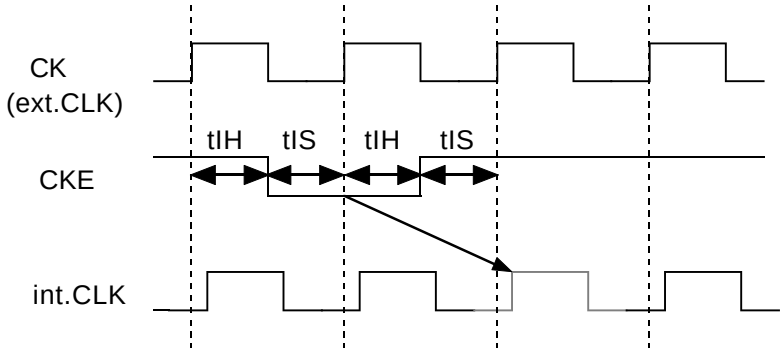
SELF REFRESH

Self-refresh mode is entered by issuing a REFS command (/CS=/RAS=/CAS=L, /WE=H, CKE=L). Once the self-refresh is initiated, it is maintained as log as CKE is kept low.During the self-refresh mode, CKE is asynchronous and the only enabled input , all other inputs including CK are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CK inputs, asserting DESEL or NOP command and then asserting CKE=H. After tRFC from the 1st CK edge follwing CKE=H, all banks are in the idle state and a new command can be issued after, but DESEL or NOP commands must be asserted till then.

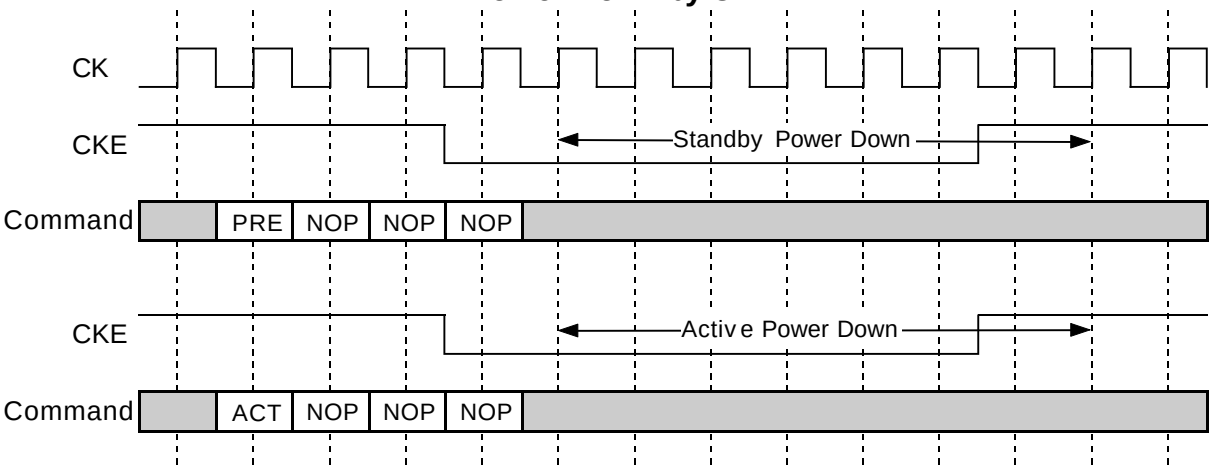


CLK SUSPEND and POWER DOWN

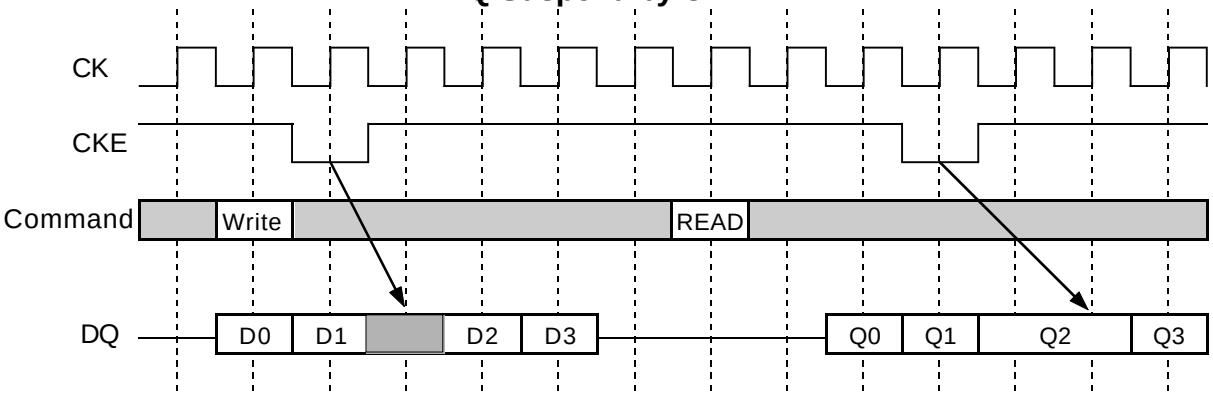
CKE controls the internal CLK at the following cycle. Figure below shows how CKE works. By negating CKE, the next internal CLK is suspended. The purpose of CLK suspend is power down, output suspend or input suspend. CKE is a synchronous input except during the self-refresh mode. CLK suspend can be performed either when the banks are active or idle. A command at the suspended cycle is ignored.



Power Down by CKE



DQ Suspend by CKE

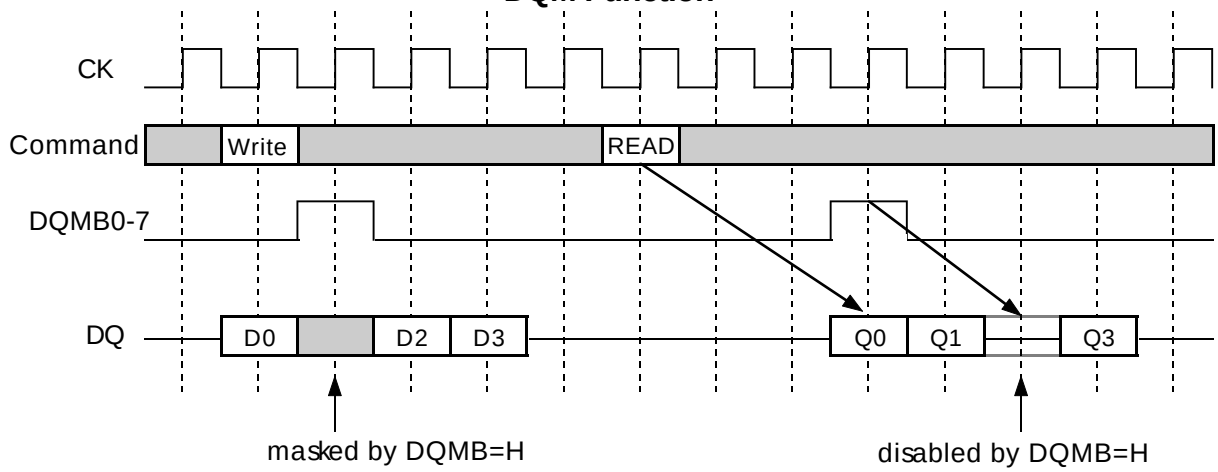


DQM CONTROL

DQMB0-7 is a dual function signal defined as the data mask for writes and the output disable for reads. During writes, DQMB0-7 masks input data word by word. DQMB0-7 to Data In latency is 0.

During reads, DQMB0-7 forces output to Hi-Z word by word. DQMB0-7 to output Hi-Z latency is 2.

DQM Function



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Ratings	Unit
Vdd	Supply Voltage	with respect to Vss	-0.5 ~ 4.6	V
VI	Input Voltage	with respect to Vss	-0.5 ~ Vdd+0.5	V
VO	Output Voltage	with respect to Vss	-0.5 ~ Vdd+0.5	V
IO	Output Current		50	mA
Pd	Power Dissipation	Ta=25°C	16	W
Topr	Operating Temperature		0 ~ 70	°C
Tstg	Storage Temperature		-40 ~ 100	°C

RECOMMENDED OPERATING CONDITION

(Ta=0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vdd	Supply Voltage	3.0	3.3	3.6	V
Vss	Supply Voltage	0	0	0	V
VIH	High-Level Input Voltage all inputs	2.0		Vdd+0.3	V
VIL	Low-Level Input Voltage all inputs	-0.3		0.8	V

Note)
1:VIH(max)=5.5V for pulse width less than 10ns.
2.VIL(min)=-1.0 for pulse width less than 10ns.

CAPACITANCE

(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits(max.)	Unit
CI(A)	Input Capacitance, address pin	@1MHz 1.4V bias 200mV swing	95	pF
CI(C)	Input Capacitance, /RAS,/CAS,/WE		95	pF
CI(K)	Input Capacitance, CK pin		31	pF
CI/O	Input Capacitance, I/O pin		22	pF

AVERAGE SUPPLY CURRENT from Vdd

(Ta=0 ~70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

Parameter	Symbol	Test Condition	Limits (max)		Unit
			-6	-7, -8	
operating current one bank active (discrete)	Icc1	tRC=min.tCLK=min, BL=1,CL=3	1120	1040	mA
precharge stanby current in power-down mode	Icc2P	CKE=L,tCLK=15ns, /CS>Vcc-0.2V	32	32	mA
	Icc2PS	CKE=CLK=L, /CS>Vcc-0.2V	16	16	mA
precharge stanby current in non power-down mode	Icc2N	CKE=H,tCLK=15ns,VIH>Vcc-0.2V,VIL<0.2V	400	400	mA
	Icc2NS	CKE=H,CLK=L,VIH>Vcc-0.2V,VIL<0.2V(fixed)	240	240	mA
active stanby current in non power-down mode one bank active (discrete)	Icc3N	CKE=H,tCLK=15ns	480	480	mA
	Icc3NS	CKE=H,CLK=L	320	320	mA
burst current	Icc4	tCLK=min, BL=4, CL=3,all banks active(discerte)	1440	1200	mA
auto-refresh current	Icc5	tRC=min, tCLK=min	2560	2560	mA
self-refresh current	Icc6	CKE <0.2V	32	32	mA

Note)
1:Icc(max) is specified at the output open condition.

AC OPERATING CONDITIONS AND CHARACTERISTICS

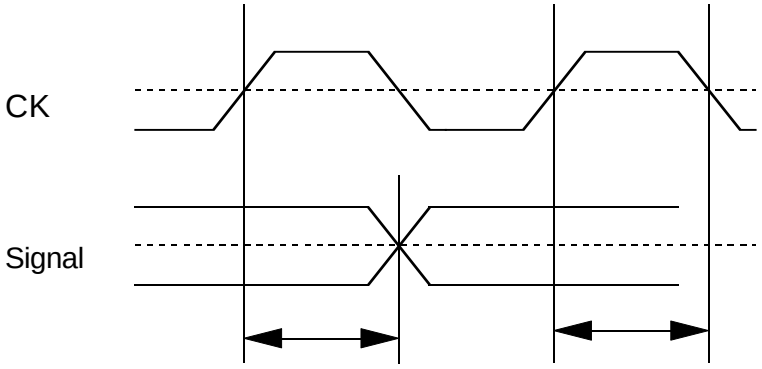
(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits		Unit
			Min.	Max.	
VOH(DC)	High-Level Output Voltage(DC)	IOH=-2mA	2.4		V
VOL(DC)	Low-Level Output Voltage(DC)	IOL=2mA		0.4	V
IOZ	Off-stare Output Current	Q floating VO=0 ~ Vdd	-20	20	uA
Ii	Input Current	VIH=0 ~ Vdd+0.3V	-160	160	uA

AC TIMING REQUIREMENTS (SDRAM Component)

(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)
Input Pulse Levels: 0.8V to 2.0V
Input Timing Measurement Level: 1.4V

Symbol	Parameter		Limits						Unit
			-6		-7		-8		
			Min.	Max.	Min.	Max.	Min.	Max.	
tCLK	CK cycle time	CL=2	10		10		13		ns
		CL=3	7.5		10		10		ns
tCH	CK High pulse width		2.5		3		3		ns
tCL	CK Low pilse width		2.5		3		3		ns
tT	Transition time of CK		1	10	1	10	1	10	ns
tIS	Input Setup time(all inputs)		1.5		2		2		ns
tIH	Input Hold time(all inputs)		0.8		1		1		ns
tRC	Row cycle time		67.5		70		70		ns
tRCD	Row to Column Delay		20		20		20		ns
tRAS	Row Active time		45	100K	50	100K	50	100K	ns
tRP	Row Precharge time		20		20		20		ns
tWR	Write Recovery time		15		20		20		ns
tRRD	Act to Act Deley time		15		20		20		ns
tRSC	Mode Register Set Cycle time		15		20		20		ns
tSRX	Self Refresh Exit time		7.5		10		10		ns
tPDE	Power Down Exit time		7.5		10		10		ns
tREF	Refresh Interval time			64		64		64	ms



Any AC timing is referenced to the input signal crossing through 1.4V.

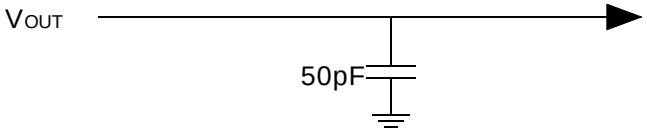
SWITCHING CHARACTERISTICS (SDRAM Component)

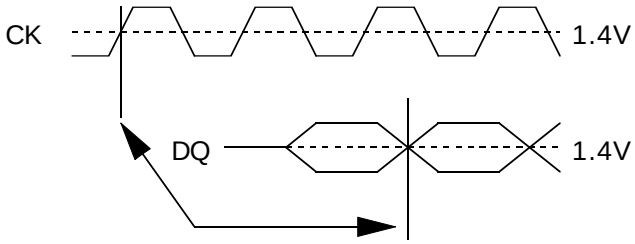
(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise note3)

Symbol	Parameter		Limits						Unit
			-6		-7		-8		
			Min.	Max.	Min.	Max.	Min.	Max.	
tAC	Access time from CK	CL=2		6		6		7	ns
		CL=3		5.4		6		6	ns
tOH	Output Hold time from CK	CL=2	3		3		3		ns
		CL=3	2.7		3		3		ns
tOLZ	Delay time, output low impedance from CK		0		0		0		ns
tOHZ	Delay time, output high impedance from CK		2.7	5.4	3	6	3	6	ns

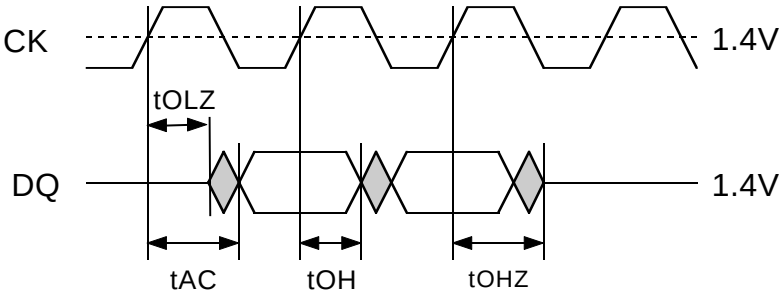
Note)
1 If clock rising time is longer than 1ns,(tT/2-0.5)ns should be added to parameter.

Output Load Condition

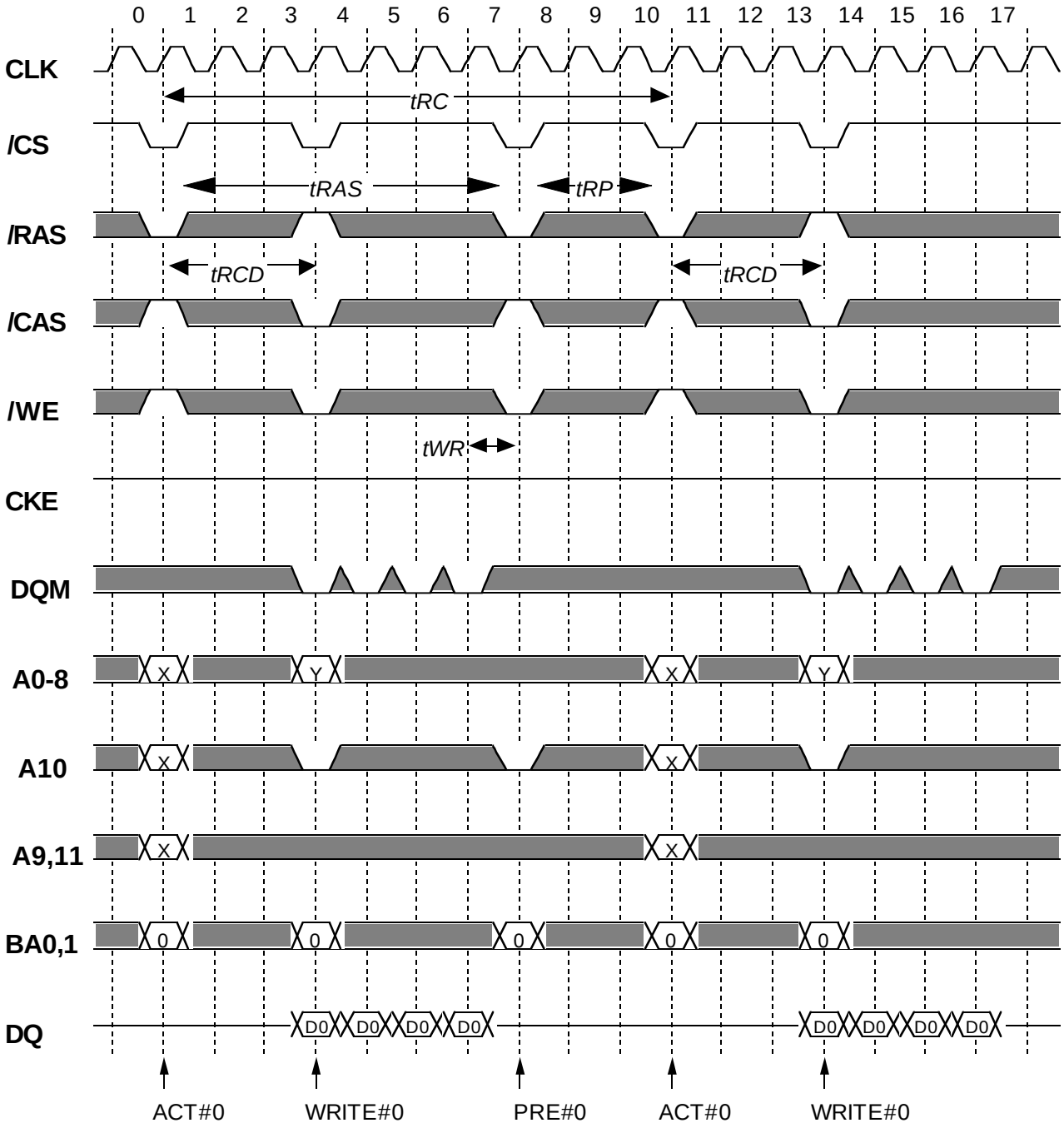




Output Timing Measurement Reference Point

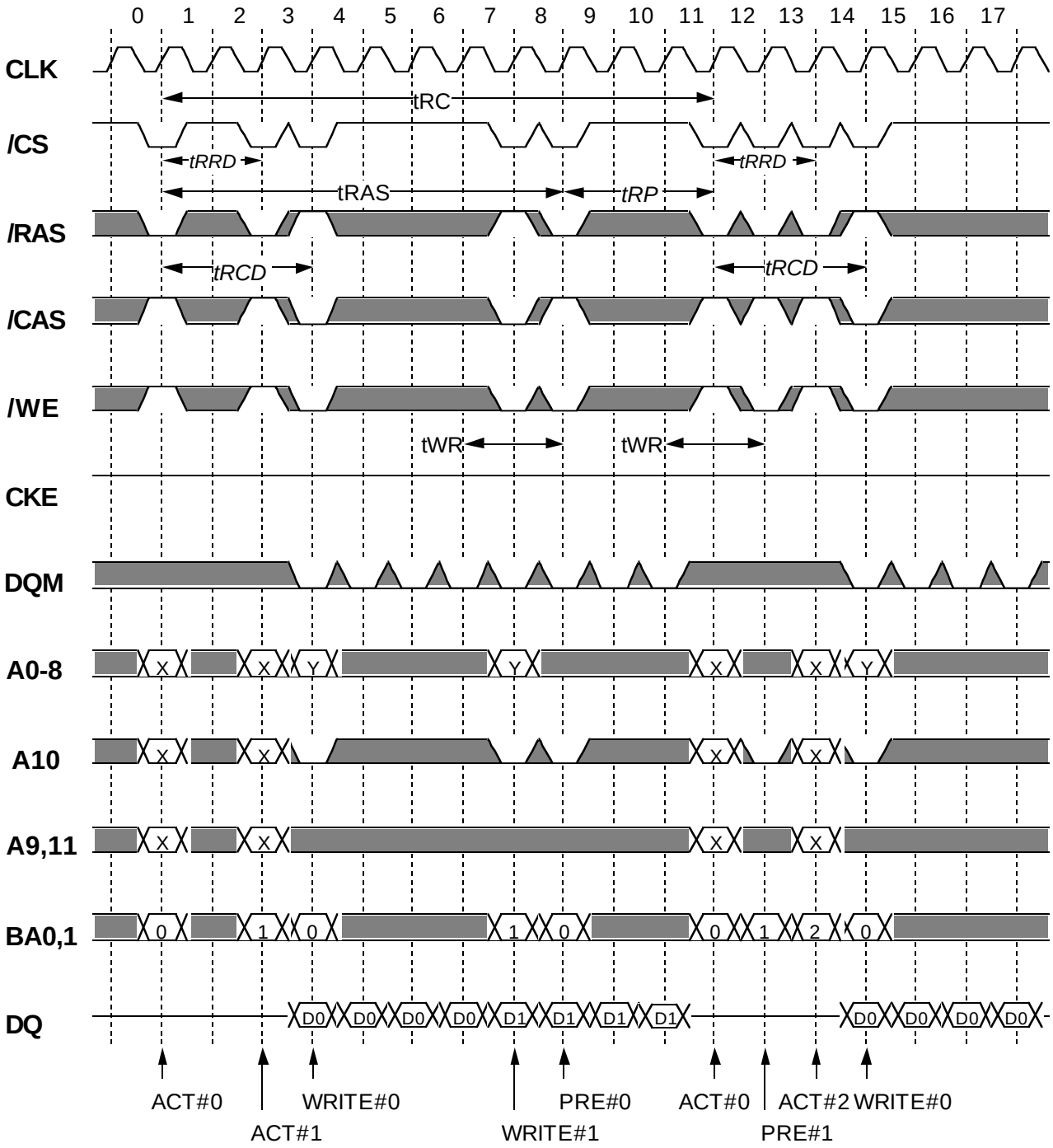


Burst Write (single bank) @BL=4



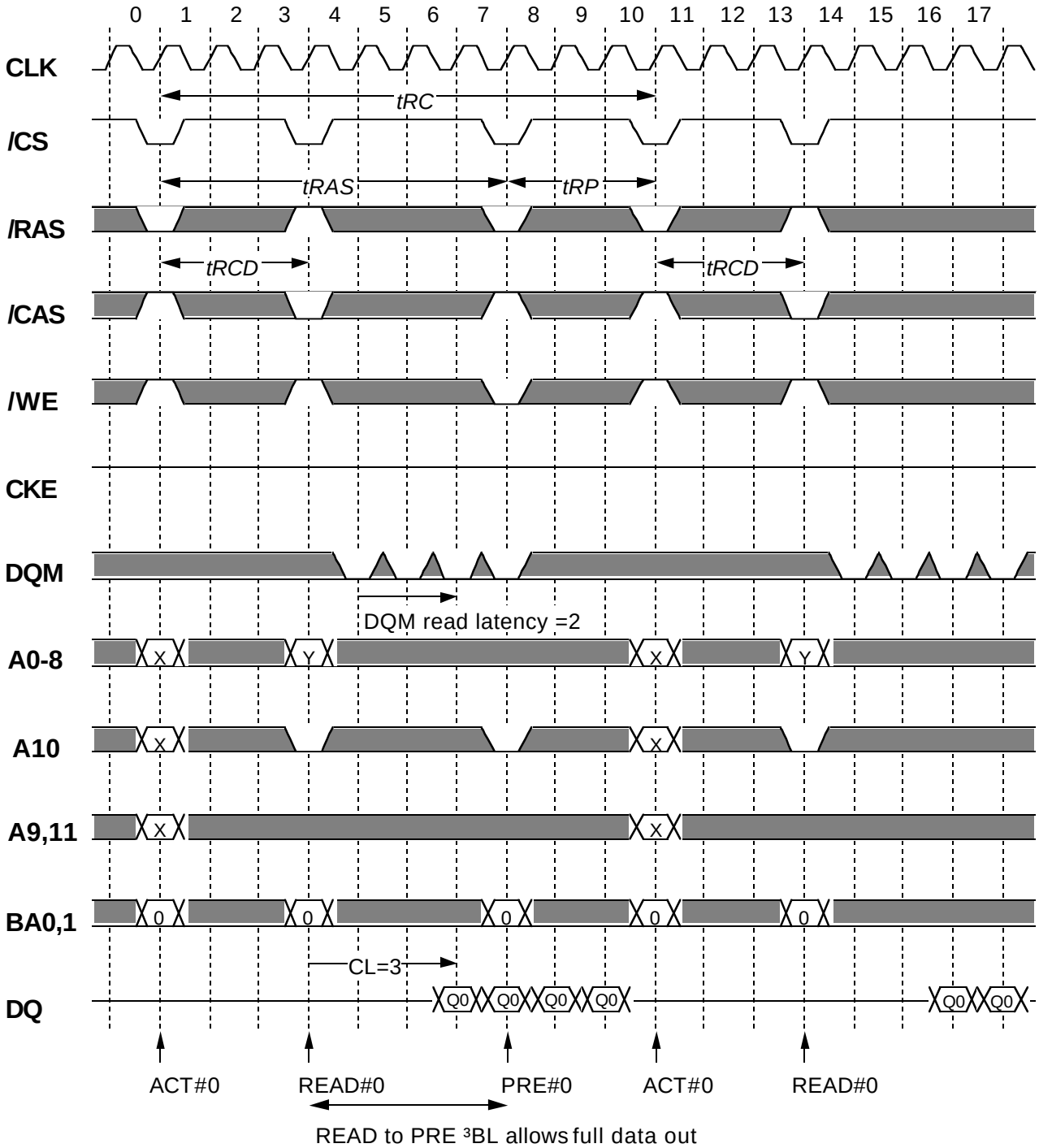
Italic parameter indicates minimum case

Burst Write (multi bank) @BL=4



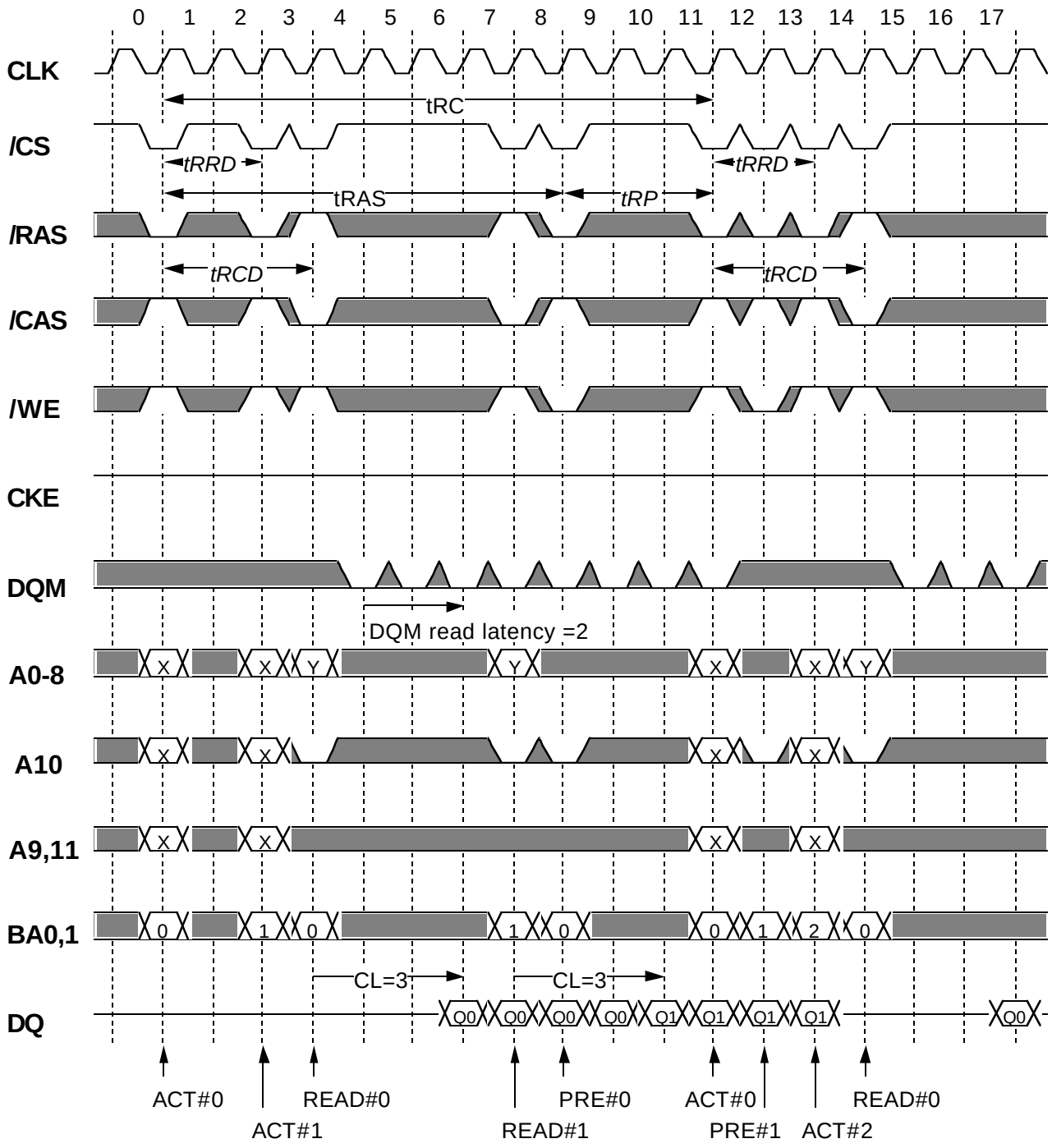
Italic parameter indicates minimum case

Burst Read (single bank) @BL=4 CL=3



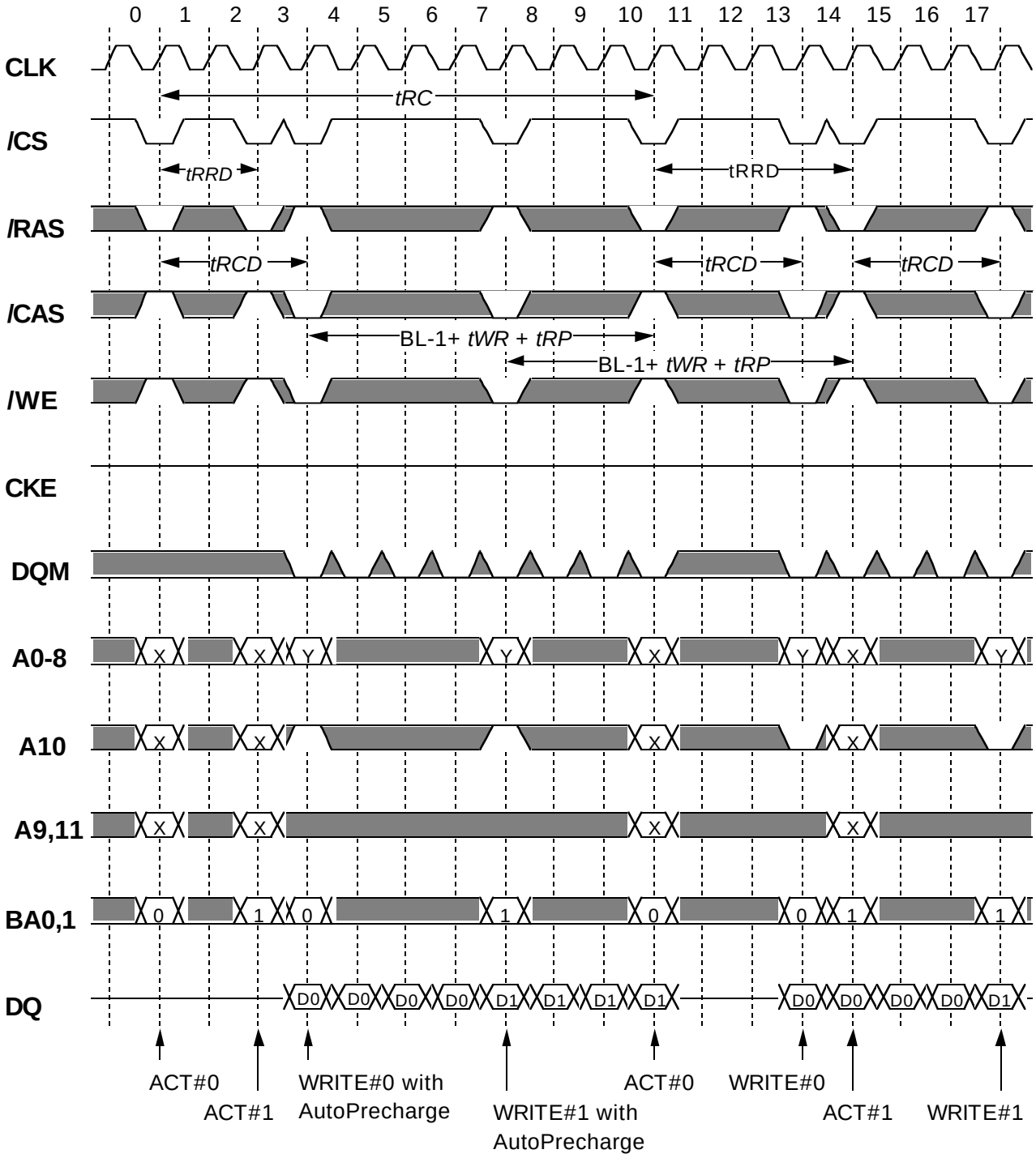
Italic parameter indicates minimum case

Burst Read (multiple bank) @BL=4 CL=3



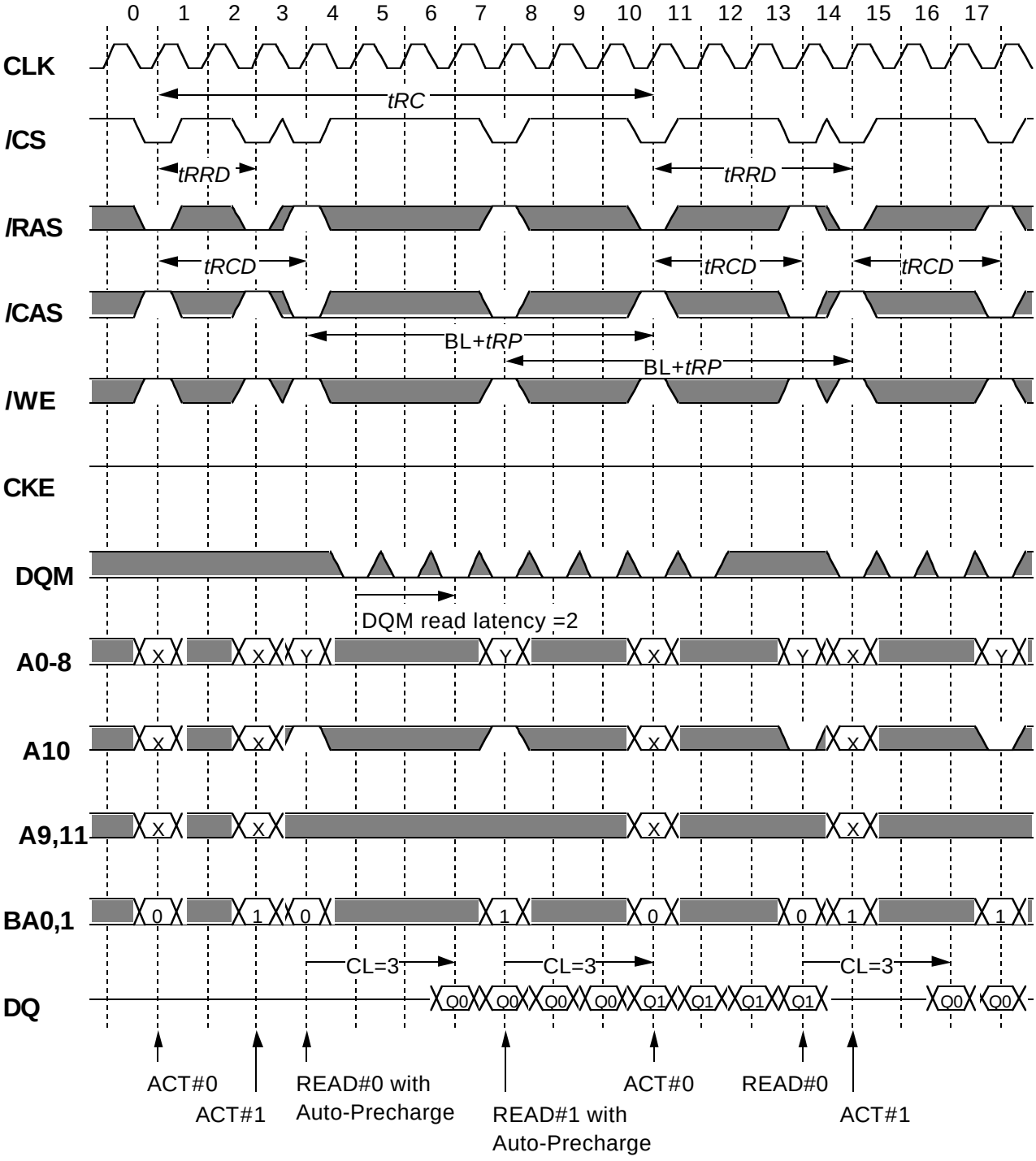
Italic parameter indicates minimum case

Burst Write (multi bank) with Auto-Precharge @BL=4



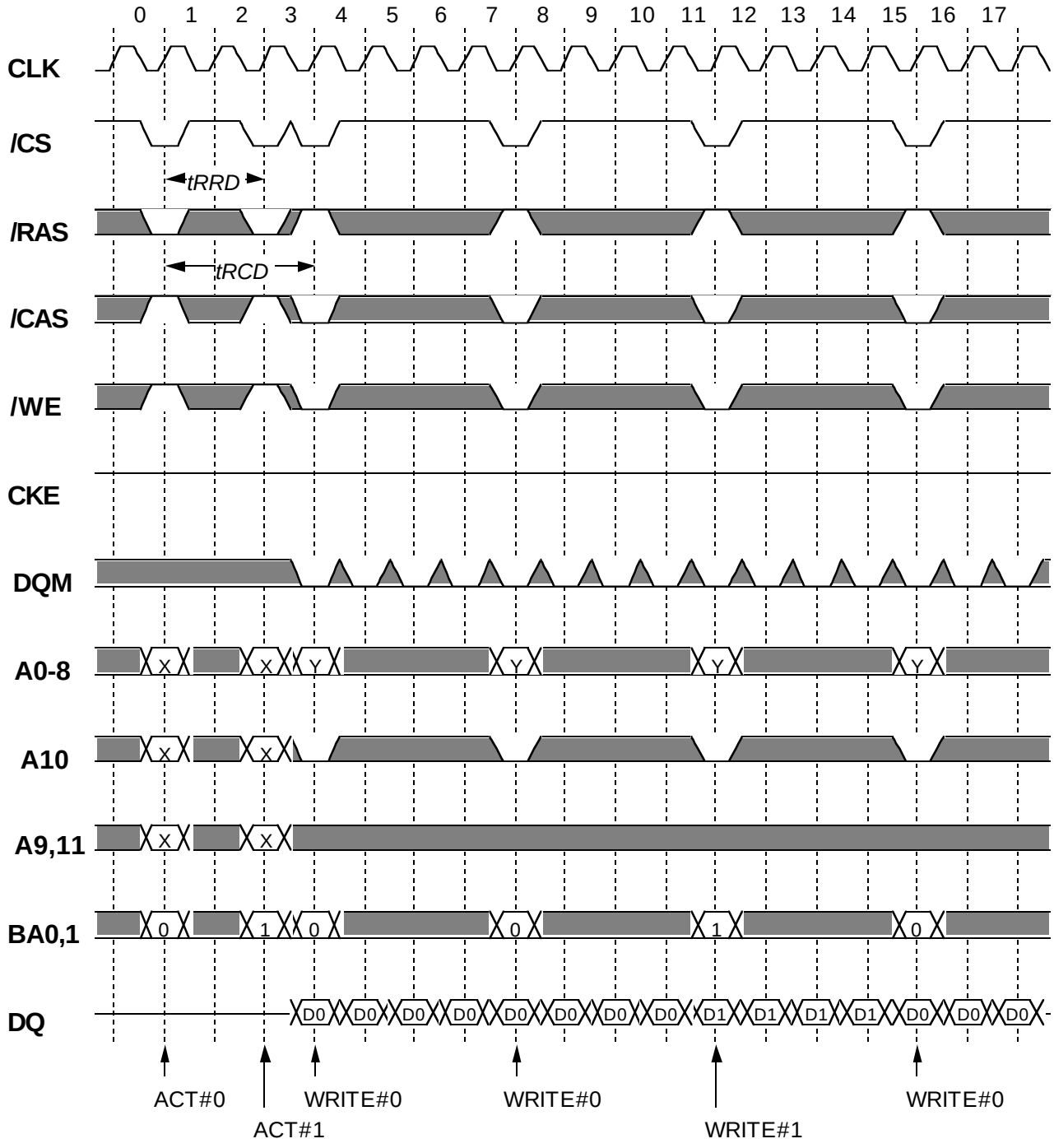
Italic parameter indicates minimum case

Burst Read (multiple bank) with Auto-Precharge @BL=4 CL=3



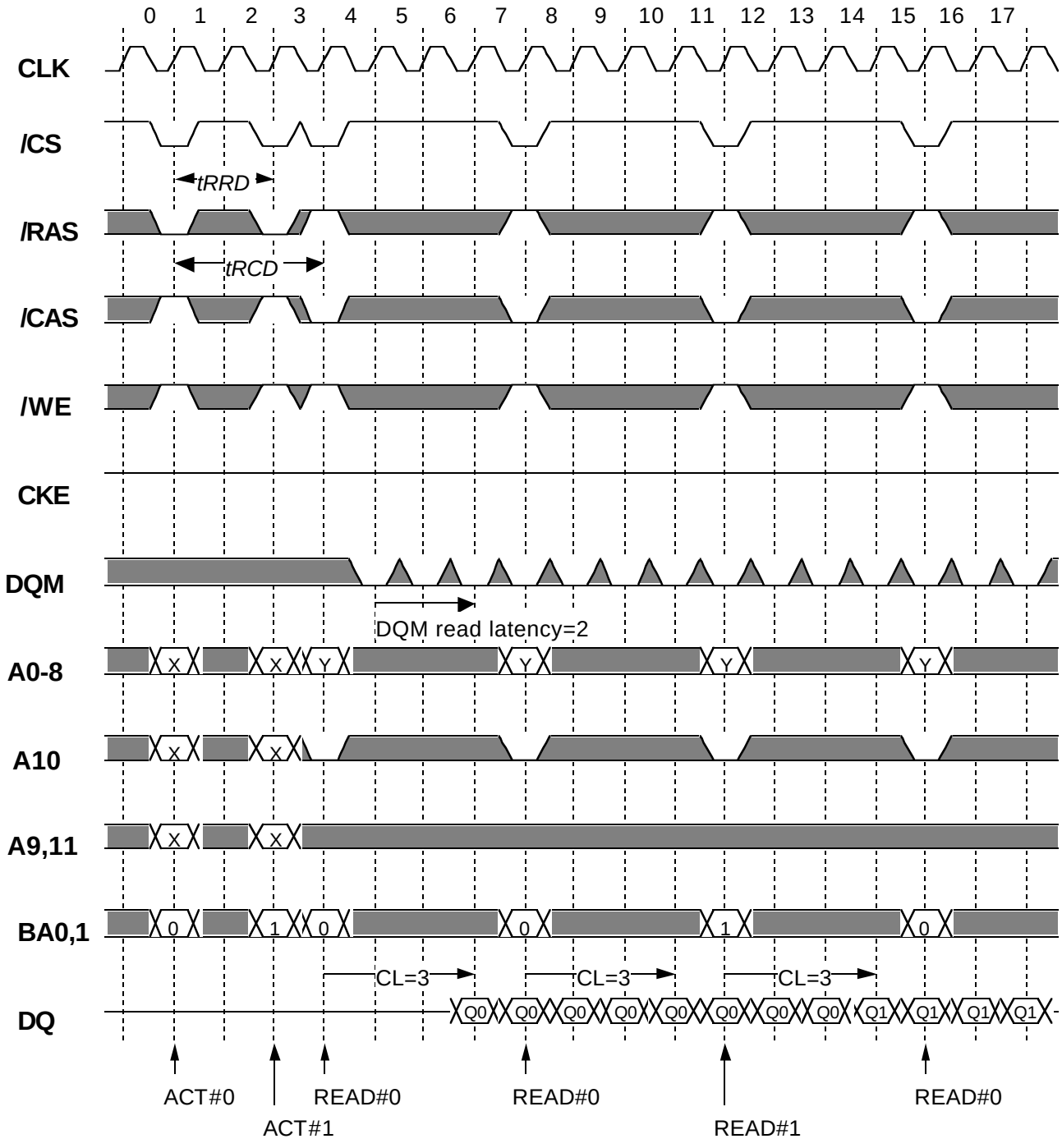
Italic parameter indicates minimum case

Page Mode Burst Write (multi bank) @BL=4



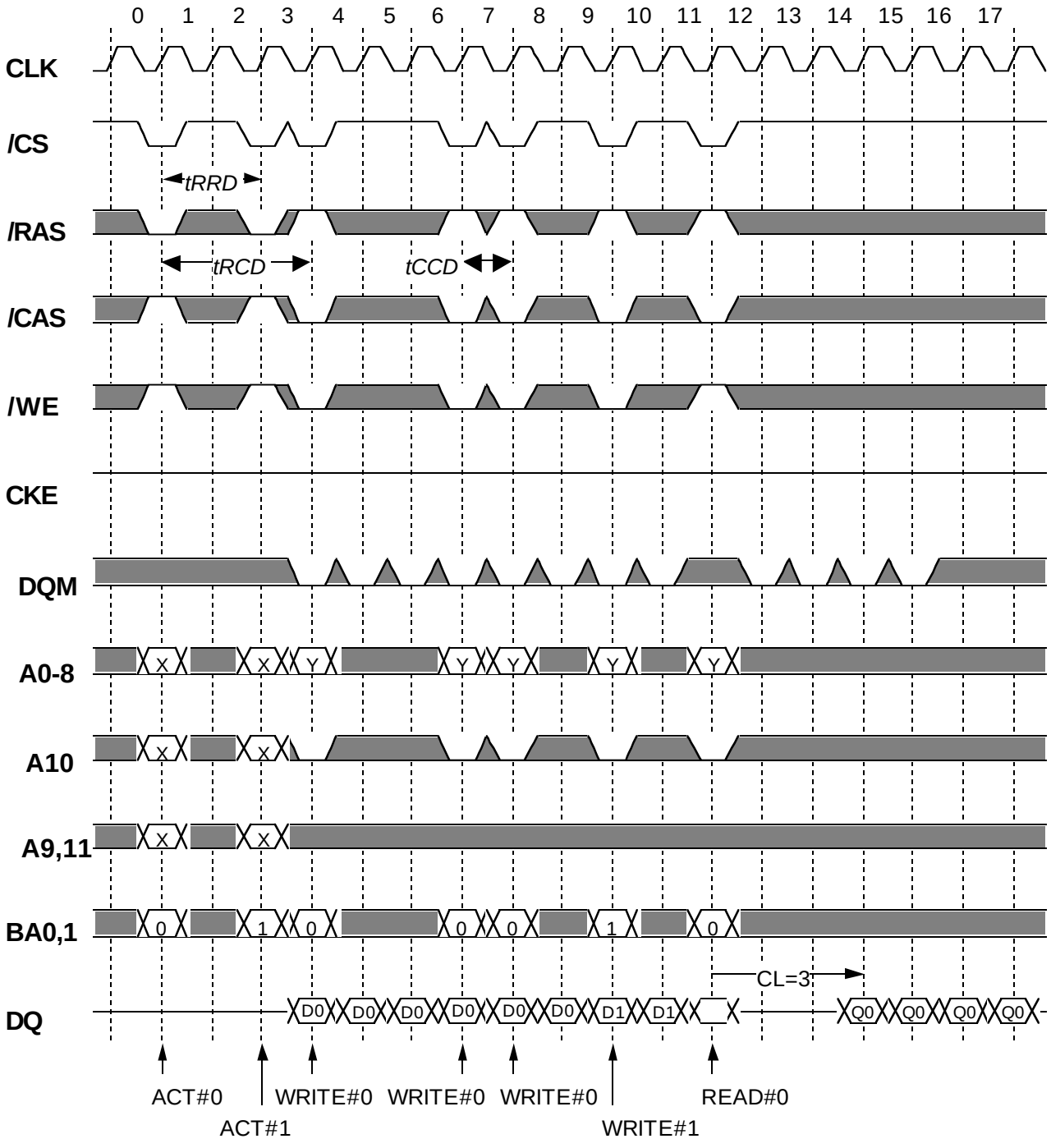
Italic parameter indicates minimum case

Page Mode Burst Read (multi bank) @BL=4 CL=3



Italic parameter indicates minimum case

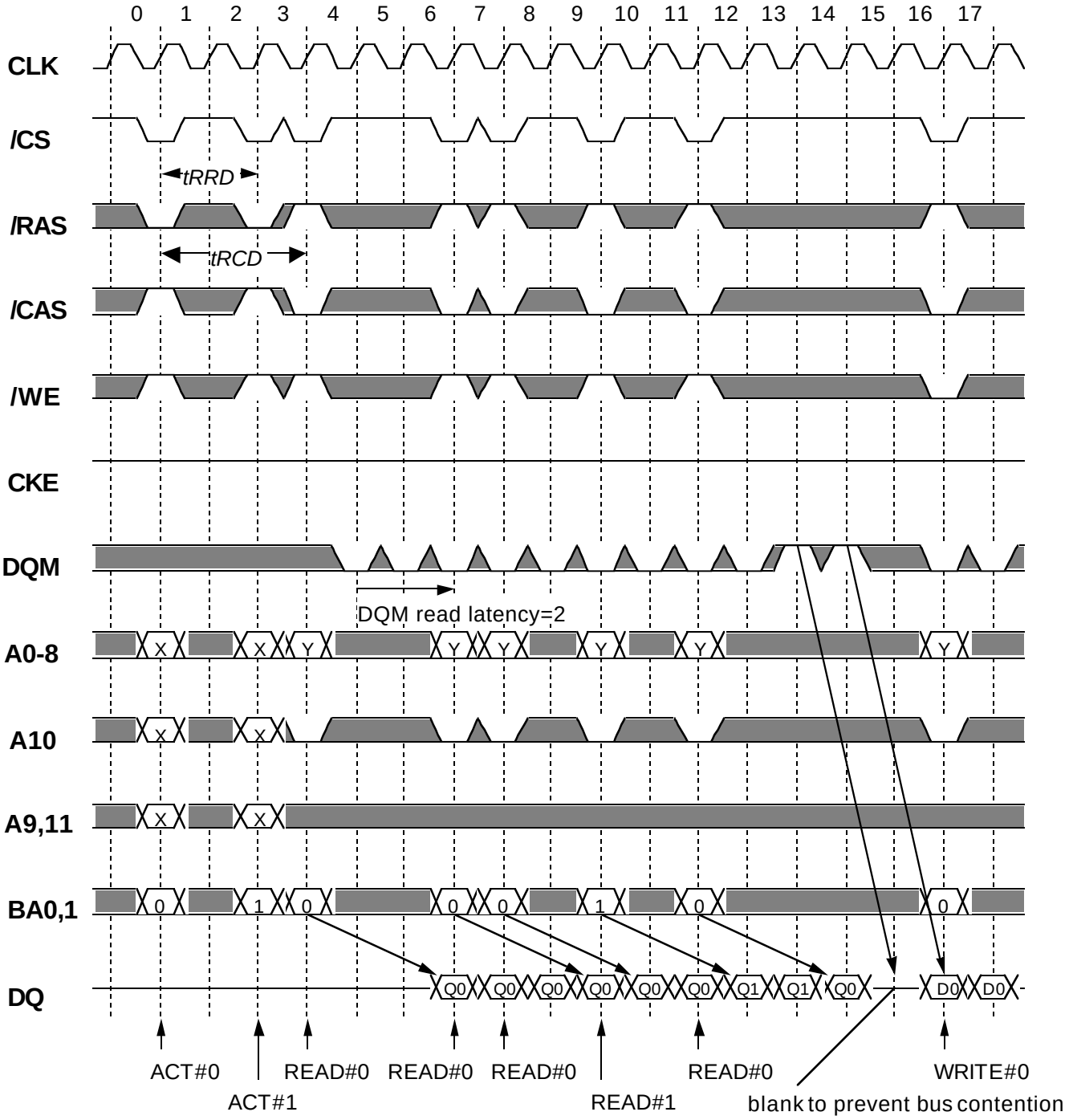
Write Interrupted by Write / Read @BL=4



Burst Write can be interrupted by Write or Read of any active bank.

Italic parameter indicates minimum case

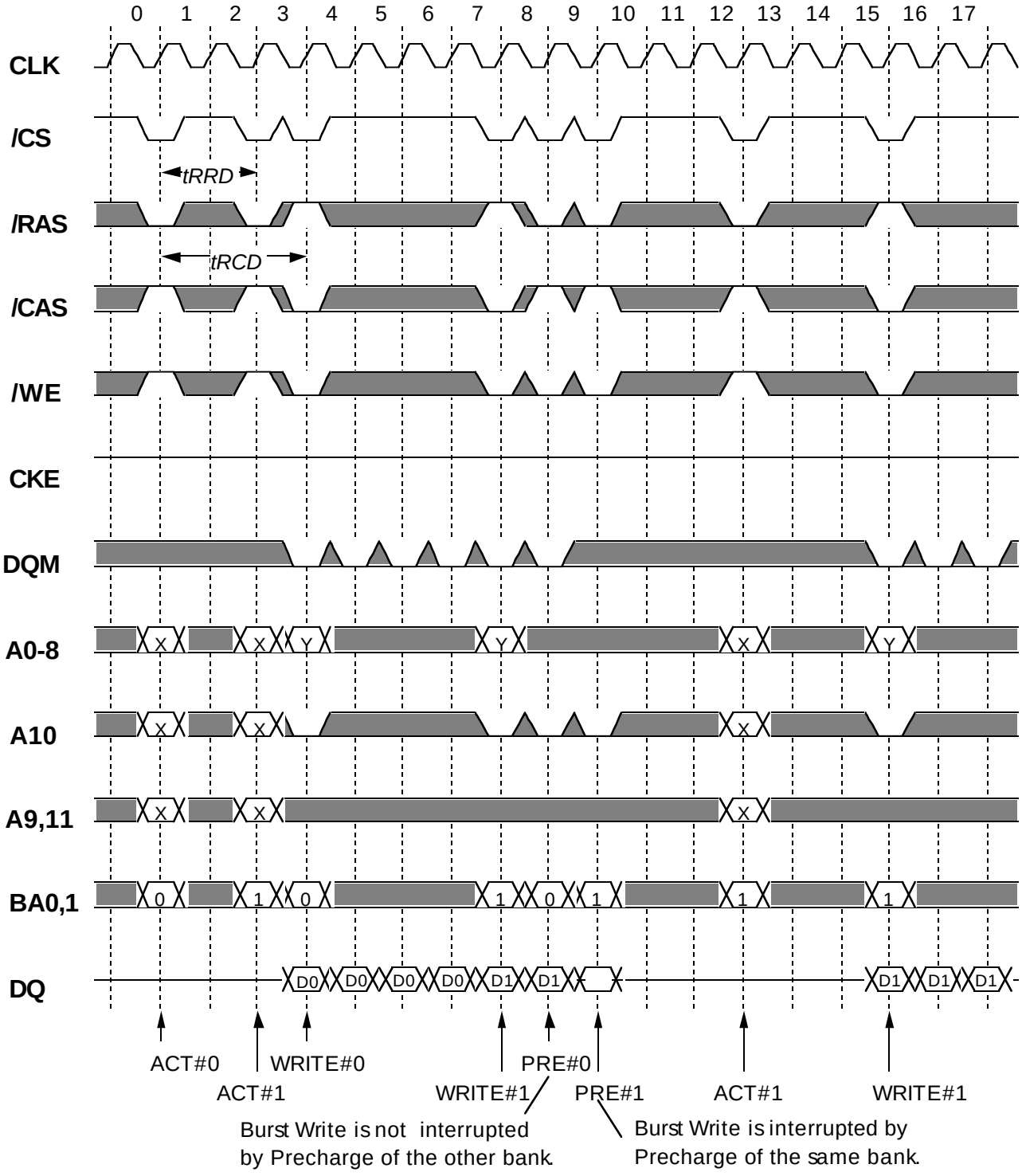
Read Interrupted by Read / Write @BL=4 CL=3



Burst Read can be interrupted by Read or Write of any active bank.

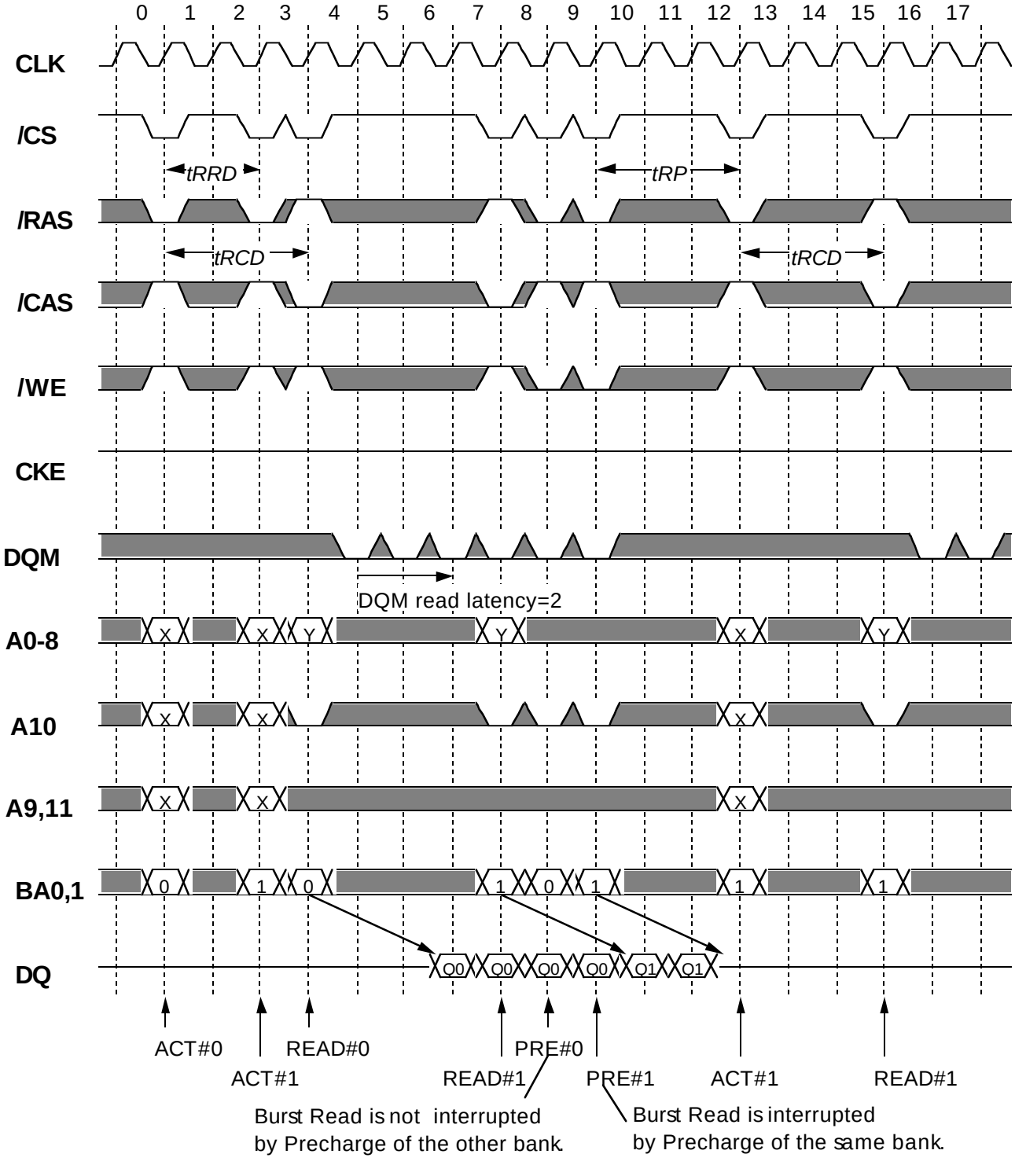
Italic parameter indicates minimum case

Write Interrupted by Precharge @BL=4



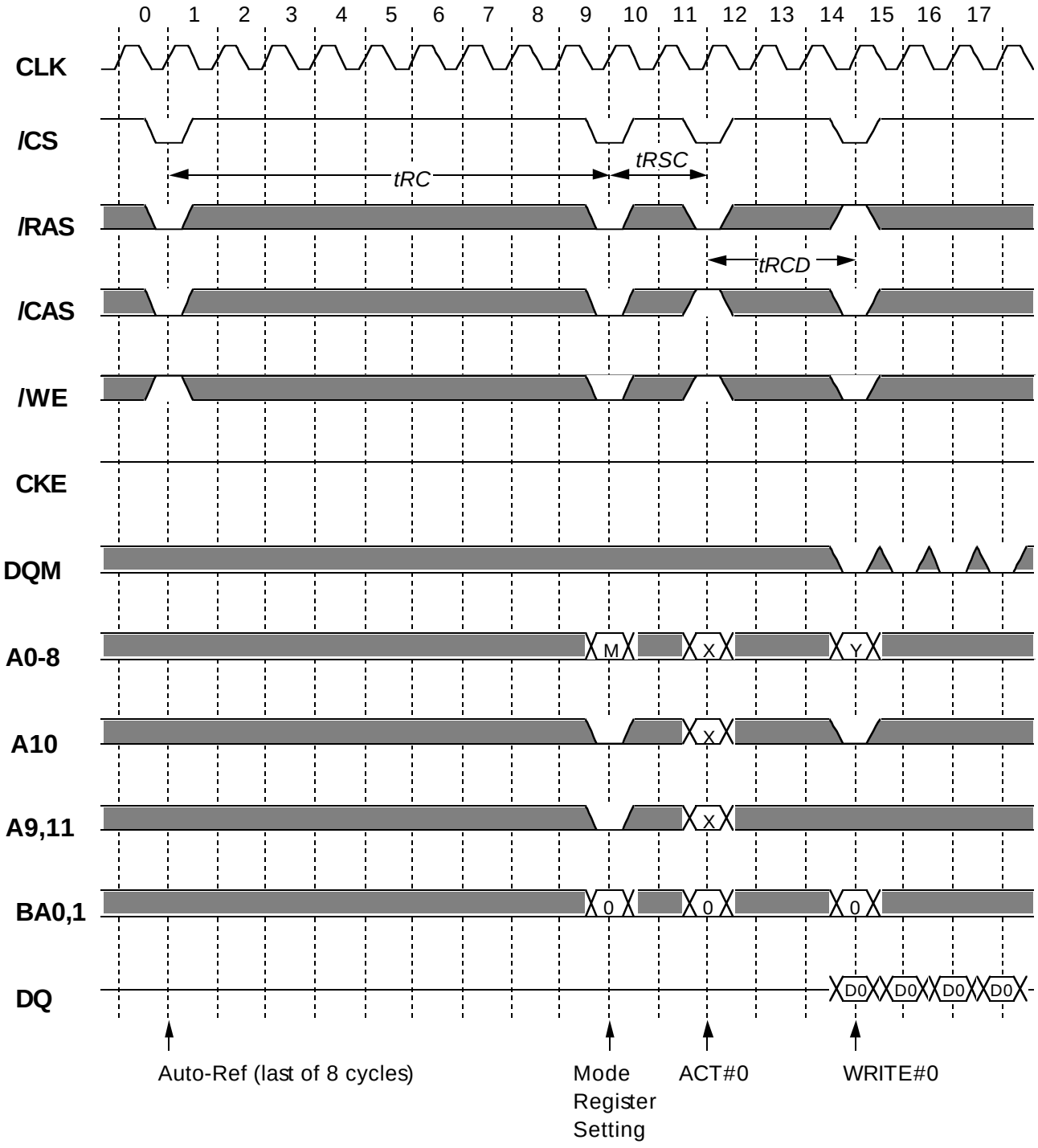
Italic parameter indicates minimum case

Read Interrupted by Precharge @BL=4 CL=3



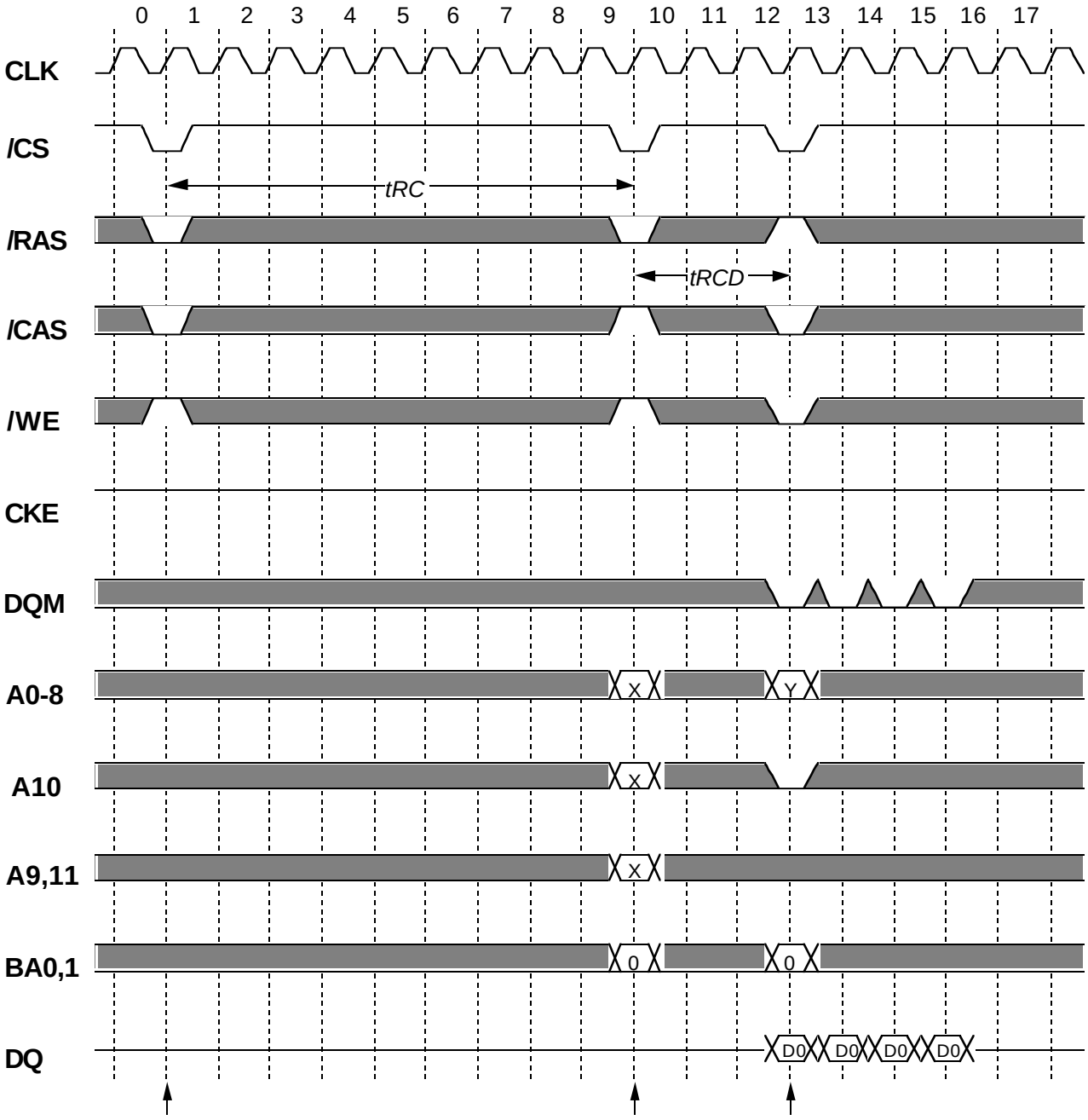
Italic parameter indicates minimum case

Mode Register Setting



Italic parameter indicates minimum case

Auto-Refresh @BL=4



Auto-Refresh

Before Auto-Refresh,
all banks must be idle state.

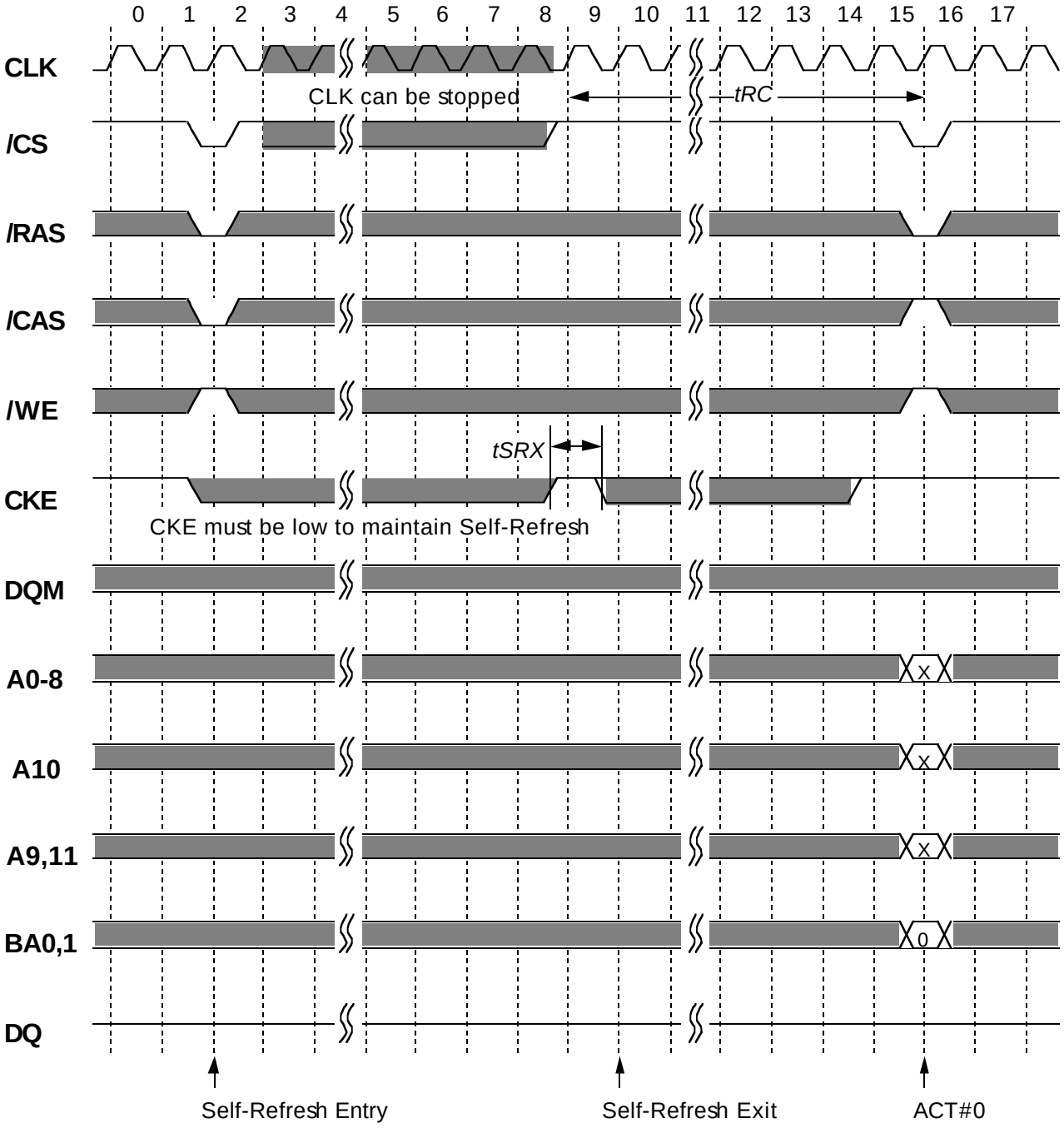
ACT#0

After tRC from Auto-Refresh,
all banks are idle state.

WRITE#0

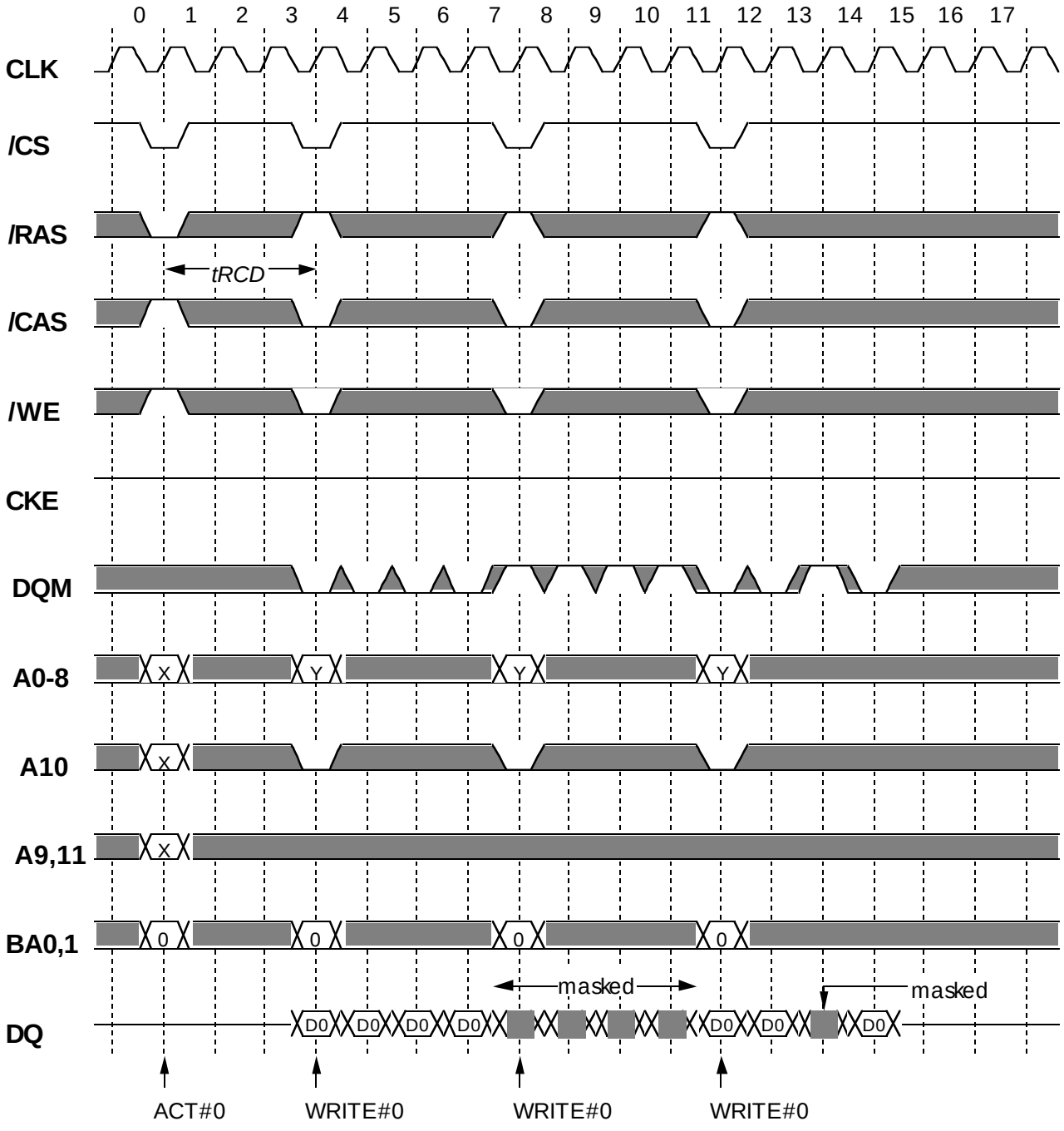
Italic parameter indicates minimum case

Self-Refresh



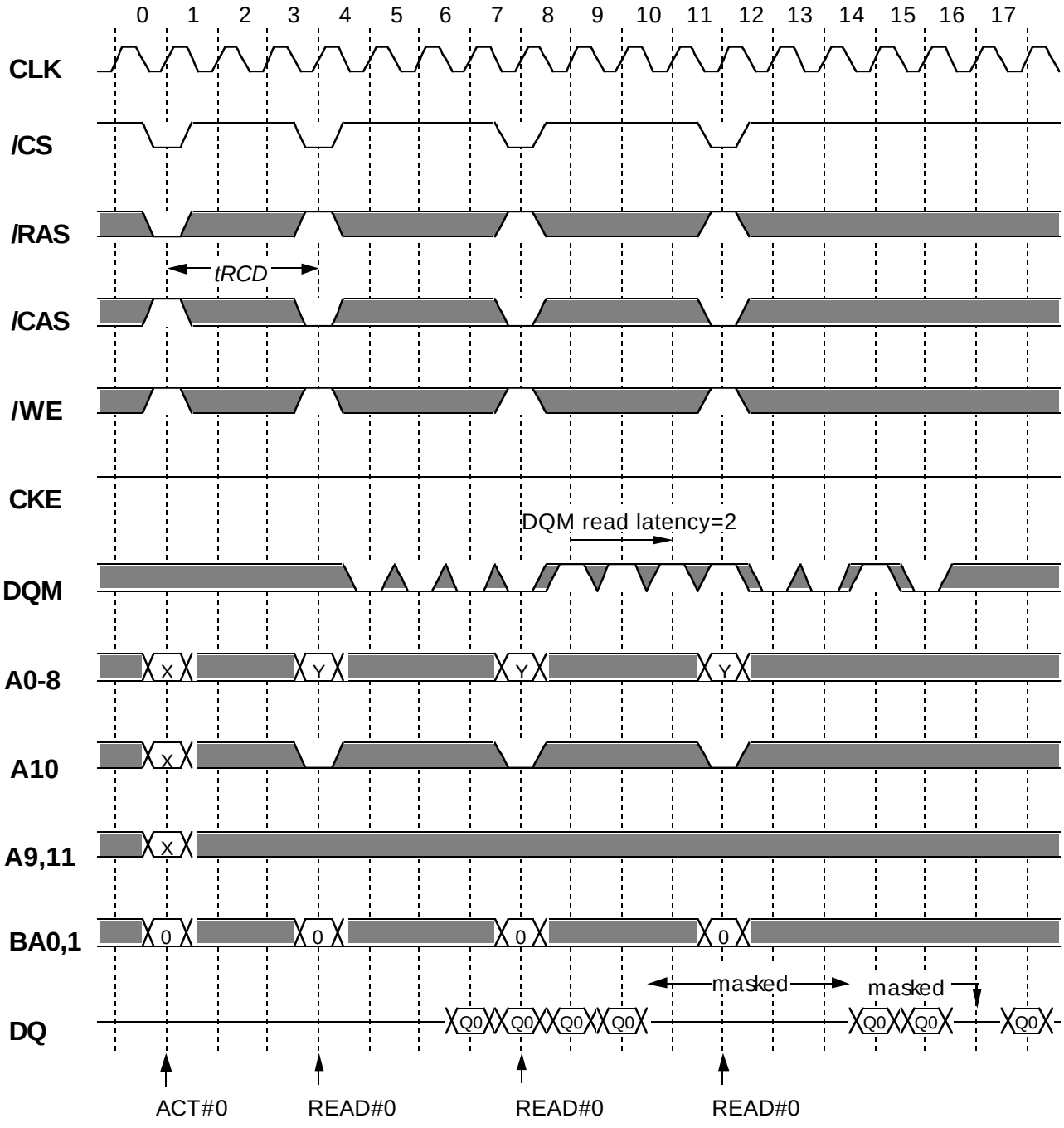
Italic parameter indicates minimum case

DQM Write Mask @BL=4



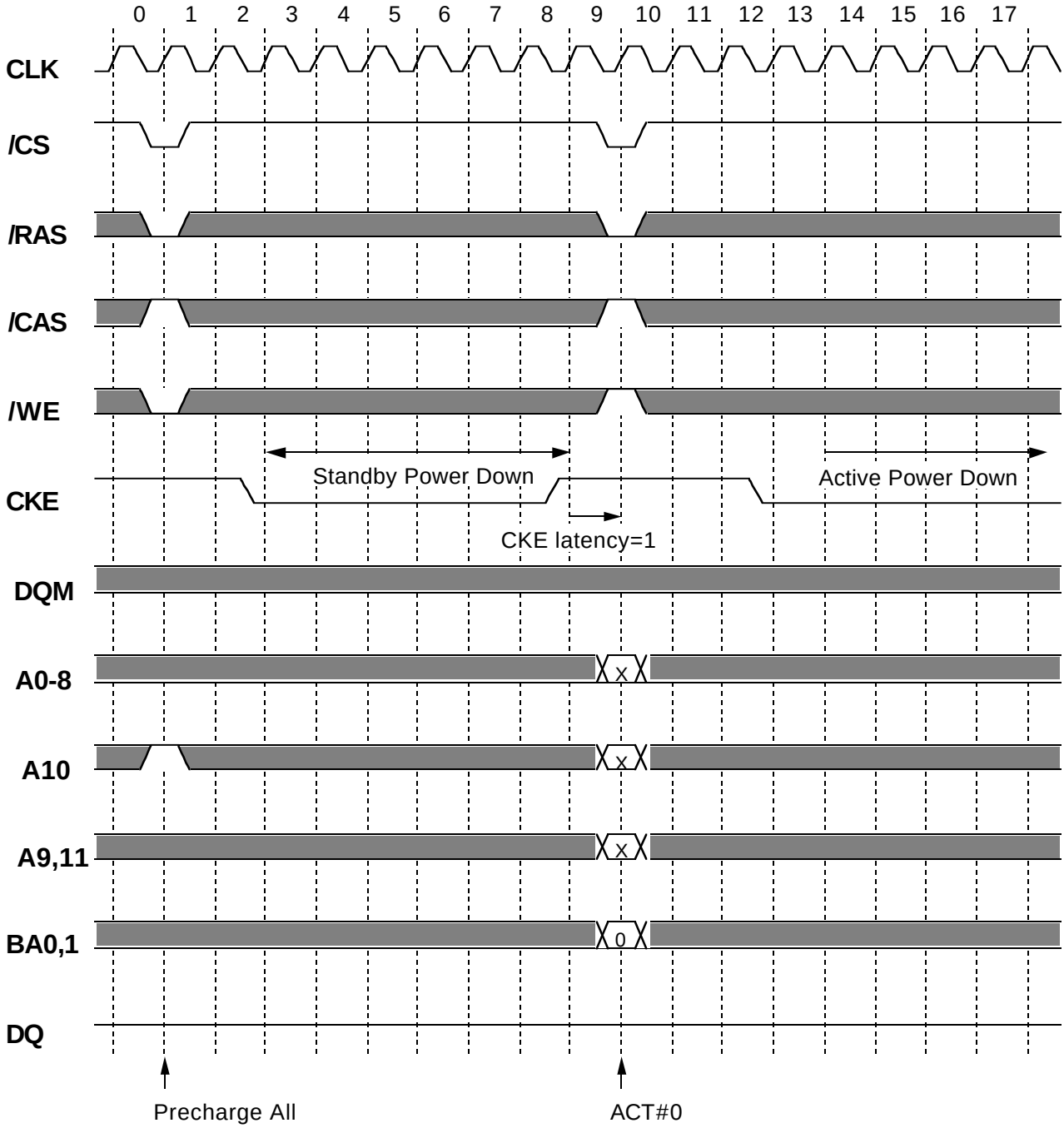
Italic parameter indicates minimum case

DQM Read Mask @BL=4 CL=3



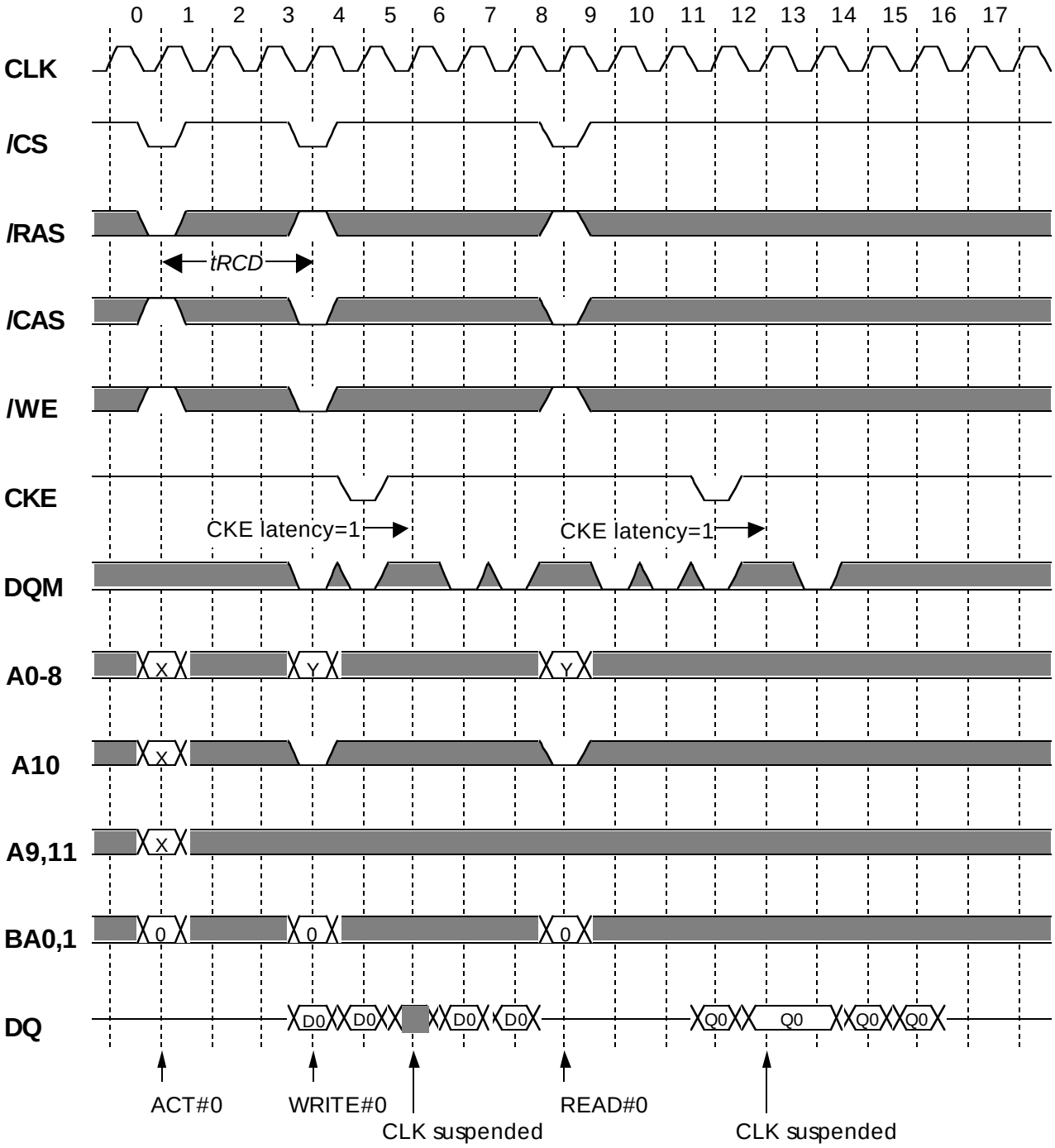
Italic parameter indicates minimum case

Power Down



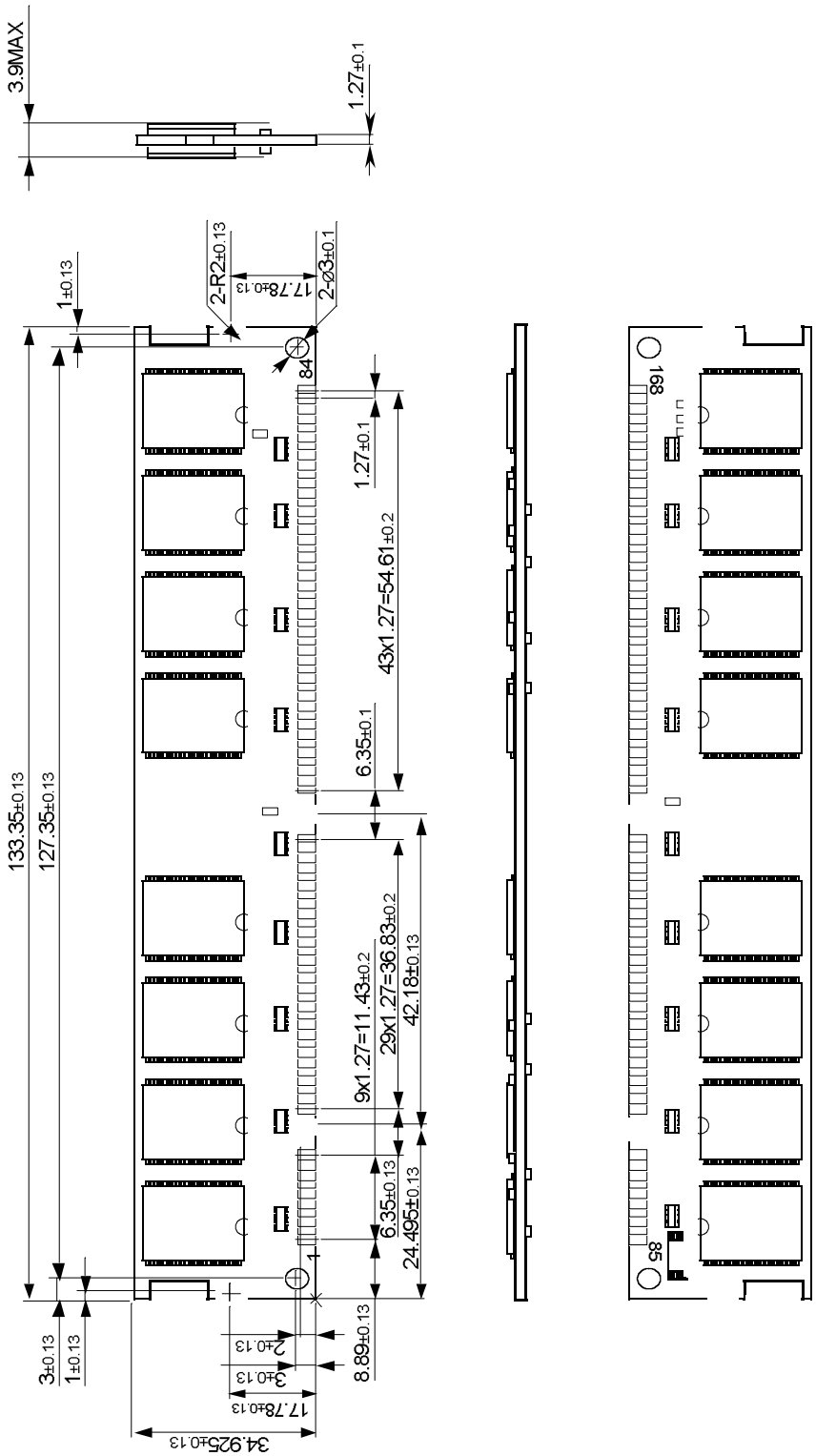
Italic parameter indicates minimum case

CLK Suspend @BL=4 CL=3



Italic parameter indicates minimum case

OUTLINE


3.9MAX
1.27±0.1
2-R2±0.13
17.78±0.13
2-Ø3±0.1
1±0.13
84
1.27±0.1
43x1.27=54.61±0.2
6.35±0.1
133.35±0.13
127.35±0.13
9x1.27=11.43±0.2
29x1.27=36.83±0.2
42.18±0.13
6.35±0.13
24.495±0.13
3±0.13
1±0.13
2±0.13
3±0.13
17.78±0.13
34.925±0.13
8.89±0.13
168
85

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