

Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

PRELIMINARY

Some of contents are subject to change without notice.

DESCRIPTION

The MH32S72QJA is 33554432 - word x 72-bit Synchronous DRAM module. This consist of eighteen industry standard 32M x 4 Synchronous DRAMs in TSOP.

The TSOP on a card edge dual in-line package provides any application where high densities and large of quantities memory are required.

This is a socket-type memory module ,suitable for easy interchange or addition of module.

FEATURES

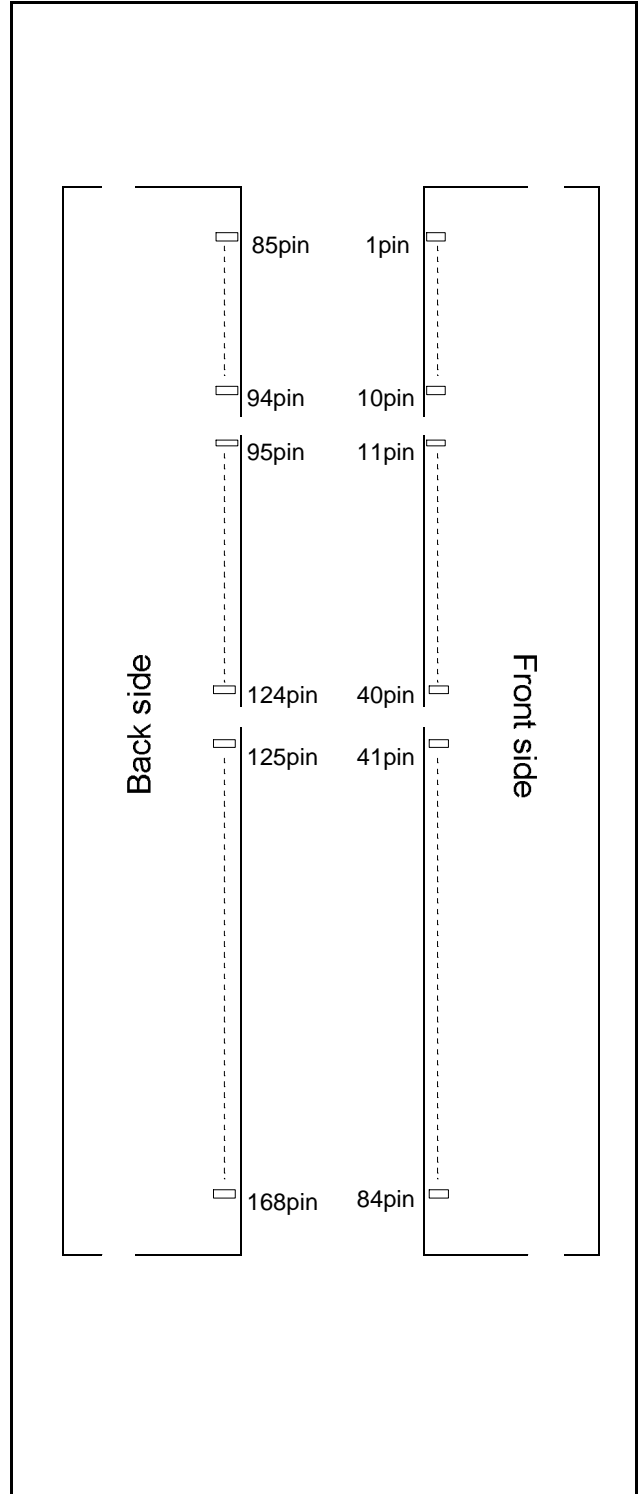
| Type name | Max. Frequency | CLK Access Time [component level] |
|--------------|----------------|-----------------------------------|
| MH32S72QJA-7 | 100MHz | 6ns (CL = 2, 3) |
| MH32S72QJA-8 | 100MHz | 6ns (CL = 3) |

- Utilizes industry standard 32M X 4 Synchronous DRAMs in TSOP package , industrystandard Resistered buffer in TSSOP package and industry standard PLL in TSSOP package
- Single 3.3V +/- 0.3V supply
- LVTTTL Interface
- Burst length 1/2/4/8/Full Page(programmable)
- Burst W rite / Single W rite(programmable)
- Auto precharge / All bank precharge controlled by A10
- Auto refresh and Self refresh
- 4096 refresh cycles every 64ms

Discrete IC and module design conform to PC/100 specification.
(module Spec. Rev. 1.2 and SPD 1.2A)

APPLICATION

Main memoryunit for computers, Microcomputer memory.



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| PIN NO. | PIN NAME | PIN NO. | PIN NAME | PIN NO. | PIN NAME | PIN NO. | PIN NAME |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 1 | VSS | 43 | VSS | 85 | VSS | 127 | VSS |
| 2 | DQ0 | 44 | NC | 86 | DQ32 | 128 | CKE0 |
| 3 | DQ1 | 45 | /S2 | 87 | DQ33 | 129 | NC |
| 4 | DQ2 | 46 | DQMB2 | 88 | DQ34 | 130 | DQMB6 |
| 5 | DQ3 | 47 | DQMB3 | 89 | DQ35 | 131 | DQMB7 |
| 6 | VDD | 48 | NC | 90 | VDD | 132 | NC |
| 7 | DQ4 | 49 | VDD | 91 | DQ36 | 133 | VDD |
| 8 | DQ5 | 50 | NC | 92 | DQ37 | 134 | NC |
| 9 | DQ6 | 51 | NC | 93 | DQ38 | 135 | NC |
| 10 | DQ7 | 52 | CB2 | 94 | DQ39 | 136 | CB6 |
| 11 | DQ8 | 53 | CB3 | 95 | DQ40 | 137 | CB7 |
| 12 | VSS | 54 | VSS | 96 | VSS | 138 | VSS |
| 13 | DQ9 | 55 | DQ16 | 97 | DQ41 | 139 | DQ48 |
| 14 | DQ10 | 56 | DQ17 | 98 | DQ42 | 140 | DQ49 |
| 15 | DQ11 | 57 | DQ18 | 99 | DQ43 | 141 | DQ50 |
| 16 | DQ12 | 58 | DQ19 | 100 | DQ44 | 142 | DQ51 |
| 17 | DQ13 | 59 | VDD | 101 | DQ45 | 143 | VDD |
| 18 | VDD | 60 | DQ20 | 102 | VDD | 144 | DQ52 |
| 19 | DQ14 | 61 | NC | 103 | DQ46 | 145 | NC |
| 20 | DQ15 | 62 | Vref.NC | 104 | DQ47 | 146 | Vref.NC |
| 21 | CB0 | 63 | CKE1 | 105 | CB4 | 147 | REGE |
| 22 | CB1 | 64 | VSS | 106 | CB5 | 148 | VSS |
| 23 | VSS | 65 | DQ21 | 107 | VSS | 149 | DQ53 |
| 24 | NC | 66 | DQ22 | 108 | NC | 150 | DQ54 |
| 25 | NC | 67 | DQ23 | 109 | NC | 151 | DQ55 |
| 26 | VDD | 68 | VSS | 110 | VDD | 152 | VSS |
| 27 | /WE | 69 | DQ24 | 111 | /CAS | 153 | DQ56 |
| 28 | DQMB0 | 70 | DQ25 | 112 | DQMB4 | 154 | DQ57 |
| 29 | DQMB1 | 71 | DQ26 | 113 | DQMB5 | 155 | DQ58 |
| 30 | /S0 | 72 | DQ27 | 114 | NC | 156 | DQ59 |
| 31 | NC | 73 | VDD | 115 | /RAS | 157 | VDD |
| 32 | VSS | 74 | DQ28 | 116 | VSS | 158 | DQ60 |
| 33 | A0 | 75 | DQ29 | 117 | A1 | 159 | DQ61 |
| 34 | A2 | 76 | DQ30 | 118 | A3 | 160 | DQ62 |
| 35 | A4 | 77 | DQ31 | 119 | A5 | 161 | DQ63 |
| 36 | A6 | 78 | VSS | 120 | A7 | 162 | VSS |
| 37 | A8 | 79 | CK2 | 121 | A9 | 163 | CK3 |
| 38 | A10 | 80 | NC | 122 | BA0 | 164 | NC |
| 39 | BA1 | 81 | WP | 123 | A11 | 165 | SA0 |
| 40 | VDD | 82 | SDA | 124 | VDD | 166 | SA1 |
| 41 | VDD | 83 | SCL | 125 | CK1 | 167 | SA2 |
| 42 | CK0 | 84 | VDD | 126 | NC | 168 | VDD |

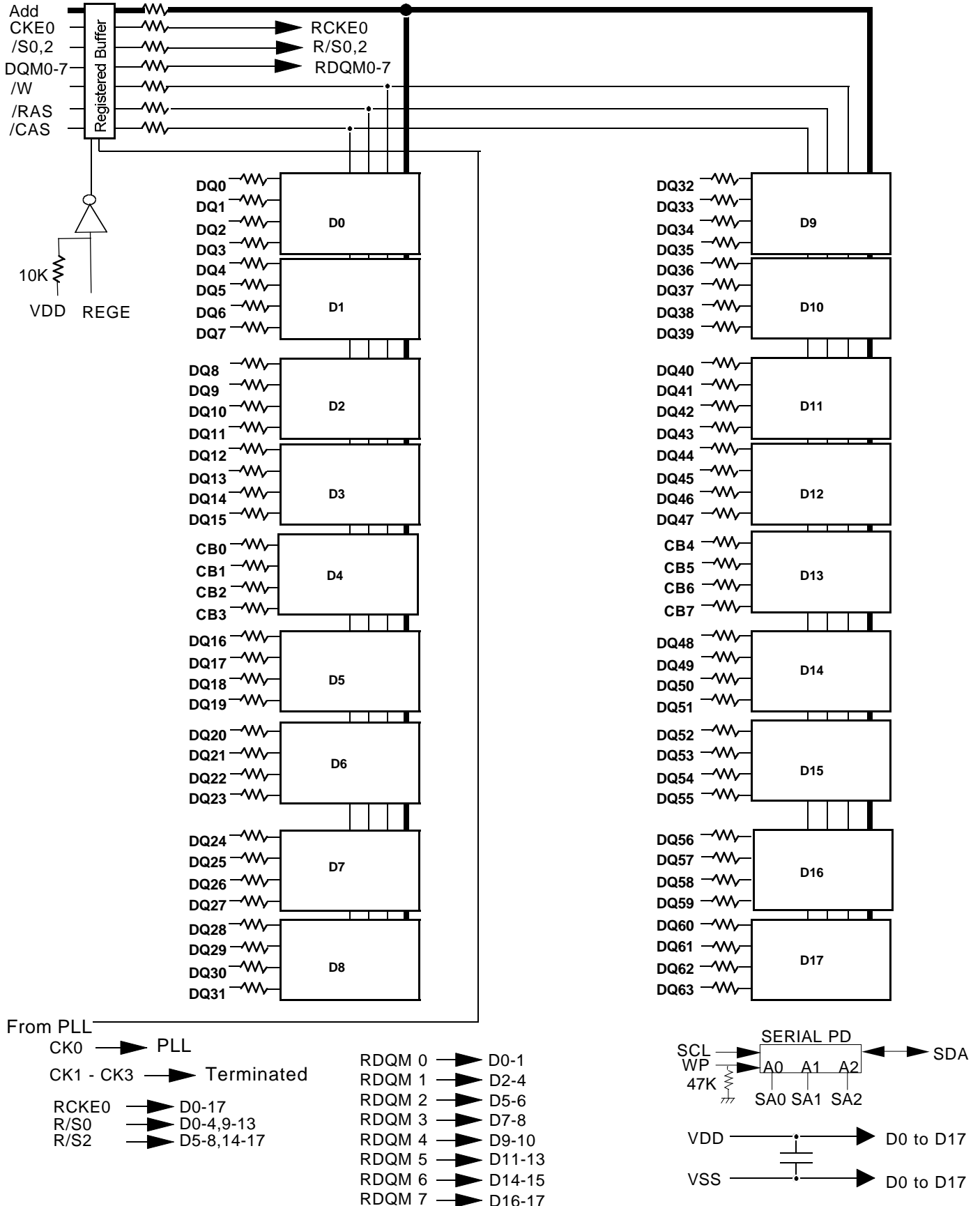
NC = No Connection

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PIN FUNCTION

| | | |
|-----------------|--------------|--|
| CK0 | Input | Master Clock:All other inputs are referenced to the rising edge of CK |
| CKE0 | Input | Clock Enable:CKE controls internal clock.When CKE is low,internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE E becomes asynchronous input.Self refresh is maintained as long as CKE is low. |
| /S0,2 | Input | Chip Select: When /S is high,any command means No Operation. |
| /RAS,/CAS,/W | Input | Combination of /RAS,/CAS,/W defines basic commands. |
| A0-11 | Input | A0-11 specify the Row/Column Address in conjunction with BA.The Row Address is specified by A0-11.The Column Address is specified by A0-10.A10 is also used to indicate precharge option.When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, both banks are precharged. |
| BA0-1 | Input | Bank Address:BA0,1 is not simply BA.BA0,1 specifies the bank to which a command is applied.BA must be set with ACT,PRE,READ,WRITE commands |
| DQ0-63 CB0-7 | Input/Output | Data In and Data out are referenced to the rising edge of CK |
| DQM0-7 | Input | Din Mask/Output Disable:When DQMB is high in burst write.Din for the current cycle is masked.When DQMB is high in burst read,Dout is disabled at the next but one cycle. |
| Vdd,Vss | Power Supply | Power Supply for the memory mounted module. |
| REGE | Output | Register enable:When REGE is low,All control signals and address are buffered. (Buffer mode) When REGE is high,All control and address are latched. (Latch mode) |

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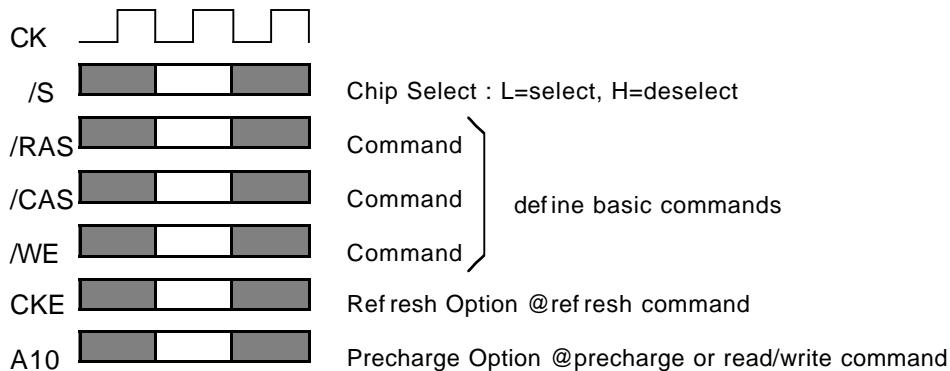
2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

BASIC FUNCTIONS

The MH32S72QJA provides basic functions, bank(row) activate, burst read / write, bank(row) precharge, and auto / self refresh.

Each command is defined by control signals of /RAS, /CAS and /WE at CK rising edge. In addition to 3 signals, /S, CKE and A10 are used as chip select, refresh option, and precharge option, respectively.

To know the detailed definition of commands please see the command truth table.



Activate(ACT) [/RAS =L, /CAS = /WE =H]

ACT command activates a row in an idle bank indicated by BA.

Read(READ) [/RAS =H, /CAS =L, /WE =H]

READ command starts burst read from the active bank indicated by BA. First output data appears after /CAS latency. When A10 =H at this command, the bank is deactivated after the burst read (auto-precharge, READA).

Write(WRITE) [/RAS =H, /CAS = /WE =L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 =H at this command, the bank is deactivated after the burst write (auto-precharge, WRITEA).

Precharge(PRE) [/RAS =L, /CAS =H, /WE =L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read / write operation. When A10 =H at this command, both banks are deactivated (precharge all, PREA).

Auto-Refresh(PEFA) [/RAS =/CAS =L, /WE =CKE =H]

PEFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

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COMMAND TRUTH TABLE

| COMMAND | MNEMONIC | CK _{n-1} | CK _n | /S | /RAS | /CAS | /WE | BA | A10 | A0-9 |
|--|----------|-------------------|-----------------|----|------|------|-----|----|-----|------|
| Deselect | DESEL | H | X | H | X | X | X | X | X | X |
| No Operation | NOP | H | X | L | H | H | H | X | X | X |
| Row Address Entry & Bank Activate | ACT | H | X | L | L | H | H | V | V | V |
| Single Bank Precharge | PRE | H | X | L | L | H | L | V | L | X |
| Precharge All Bank | PREA | H | X | L | L | H | L | V | H | X |
| Column Address Entry & Write | WRITE | H | X | L | LH | H | L | V | L | V |
| Column Address Entry & Write with Auto-Precharge | WRITEA | H | X | L | H | L | L | V | H | V |
| Column Address Entry & Read | READ | H | X | L | H | L | H | V | L | V |
| Column Address Entry & Read with Auto Precharge | READA | H | X | L | H | L | H | V | H | V |
| Auto-Refresh | REFA | H | H | L | HL | L | H | X | X | X |
| Self-Refresh Entry | REFS | H | L | L | L | L | H | X | X | X |
| Self-Refresh Exit | REFSX | L | H | H | LX | X | X | X | X | X |
| | | L | H | L | H | H | H | X | X | X |
| Burst Terminate | TERM | H | X | L | H | H | L | X | X | X |
| Mode Register Set | MRS | H | X | L | L | L | L | L | L | V*1 |

H = High Level, L = Low Level, V = Valid, X = Don't Care, n = CK cycle number

NOTE:

1.A7-9 = 0, A0-6 = Mode Address

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FUNCTION TRUTH TABLE

| Current State | /S | /RAS | /CAS | /WE | Address | Command | Action |
|---------------|----|------|------|-----|----------------------|------------------|---|
| IDLE | H | X | X | X | X | DESEL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | BA | TBST | ILLEGAL*2 |
| | L | H | L | X | BA,CA,A10 | READ/WRITE | ILLEGAL*2 |
| | L | L | H | H | BA,RA | ACT | Bank Active,Latch RA |
| | L | L | H | L | BA,A10 | PRE/PREA | NOP*4 |
| | L | L | L | H | X | REFA | Auto-Refresh*5 |
| | L | L | L | L | Op-Code, Mode-Add | MRS | Mode Register Set*5 |
| ROW ACTIVE | H | X | X | X | X | DESEL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | BA | TBST | NOP |
| | L | H | L | H | BA,CA,A10 | READ/READA | Begin Read,Latch CA, Determine Auto-Precharge |
| | L | H | L | L | BA,CA,A10 | WRITE/ WRITEA | Begin Write,Latch CA, Determine Auto-Precharge |
| | L | L | H | H | BA,RA | ACT | Bank Active/ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | Precharge/Precharge All |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| READ | H | X | X | X | X | DESEL | NOP(Continue Burst to END) |
| | L | H | H | H | X | NOP | NOP(Continue Burst to END) |
| | L | H | H | L | BA | TBST | Terminate Burst |
| | L | H | L | H | BA,CA,A10 | READ/READA | Terminate Burst,Latch CA, Begin New Read,Determine Auto-Precharge*3 |
| | L | H | L | L | BA,CA,A10 | WRITE/ WRITEA | Terminate Burst,Latch CA, Begin Write,Determine Auto- Precharge*3 |
| | L | L | H | H | BA,RA | ACT | Bank Active/ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | Terminate Burst,Precharge |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |

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FUNCTION TRUTH TABLE(continued)

| Current State | /S | /RAS | /CAS | /WE | Address | Command | Action |
|---------------------------------|----|------|------|-----|----------------------|------------------|---|
| WRITE | H | X | X | X | X | DESEL | NOP(Continue Burst to END) |
| | L | H | H | H | X | NOP | NOP(Continue Burst to END) |
| | L | H | H | L | BA | TBST | Terminate Burst |
| | L | H | L | H | BA,CA,A10 | READ/READA | Terminate Burst,Latch CA, Begin Read,Determine Auto-Precharge*3 |
| | L | H | L | L | BA,CA,A10 | WRITE/ WRITEA | Terminate Burst,Latch CA, Begin Write,Determine Auto-Precharge*3 |
| | L | L | H | H | BA,RA | ACT | Bank Active/ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | Terminate Burst,Precharge |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| READ with AUTO PRECHARGE | H | X | X | X | X | DESEL | NOP(Continue Burst to END) |
| | L | H | H | H | X | NOP | NOP(Continue Burst to END) |
| | L | H | H | L | BA | TBST | ILLEGAL |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL |
| | L | H | L | L | BA,CA,A10 | WRITE/ WRITEA | ILLEGAL |
| | L | L | H | H | BA,RA | ACT | Bank Active/ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL*2 |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| WRITE with AUTO PRECHARGE | H | X | X | X | X | DESEL | NOP(Continue Burst to END) |
| | L | H | H | H | X | NOP | NOP(Continue Burst to END) |
| | L | H | H | L | BA | TBST | ILLEGAL |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL |
| | L | H | L | L | BA,CA,A10 | WRITE/ WRITEA | ILLEGAL |
| | L | L | H | H | BA,RA | ACT | Bank Active/ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL*2 |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |

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FUNCTION TRUTH TABLE(continued)

| Current State | /S | /RAS | /CAS | /WE | Address | Command | Action |
|-----------------------|----|------|------|-----|----------------------|------------|----------------------------|
| PRE - CHARGING | H | X | X | X | X | DESEL | NOP(Idle after tRP) |
| | L | H | H | H | X | NOP | NOP(Idle after tRP) |
| | L | H | H | L | BA | TBST | ILLEGAL*2 |
| | L | H | L | X | BA,CA,A10 | READ/WRITE | ILLEGAL*2 |
| | L | L | H | H | BA,RA | ACT | ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | NOP*4(Idle after tRP) |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| ROW ACTIVATING | H | X | X | X | X | DESEL | NOP(Row Active after tRCD) |
| | L | H | H | H | X | NOP | NOP(Row Active after tRCD) |
| | L | H | H | L | BA | TBST | ILLEGAL*2 |
| | L | H | L | X | BA,CA,A10 | READ/WRITE | ILLEGAL*2 |
| | L | L | H | H | BA,RA | ACT | ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL*2 |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| WRITE RE- COVERING | H | X | X | X | X | DESEL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | BA | TBST | ILLEGAL*2 |
| | L | H | L | X | BA,CA,A10 | READ/WRITE | ILLEGAL*2 |
| | L | L | H | H | BA,RA | ACT | ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL*2 |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |

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FUNCTION TRUTH TABLE(continued)

| Current State | /S | /RAS | /CAS | /WE | Address | Command | Action |
|-----------------------|----|------|------|-----|-------------------|------------|----------------------|
| RE-FRESHING | H | X | X | X | X | DESEL | NOP(Idle after tRC) |
| | L | H | H | H | X | NOP | NOP(Idle after tRC) |
| | L | H | H | L | BA | TBST | ILLEGAL |
| | L | H | L | X | BA,CA,A10 | READ/WRITE | ILLEGAL |
| | L | L | H | H | BA,RA | ACT | ILLEGAL |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| MODE REGISTER SETTING | H | X | X | X | X | DESEL | NOP(Idle after tRSC) |
| | L | H | H | H | X | NOP | NOP(Idle after tRSC) |
| | L | H | H | L | BA | TBST | ILLEGAL |
| | L | H | L | X | BA,CA,A10 | READ/WRITE | ILLEGAL |
| | L | L | H | H | BA,RA | ACT | ILLEGAL |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |

ABBREVIATIONS:

H = High Level, L = Low Level, X = Don't Care

BA = Bank Address, RA = Row Address, CA = Column Address, NOP = No Operation

NOTES:

1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and / or data-integrity are not guaranteed.

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FUNCTION TRUTH TABLE FOR CKE

| Current State | CK _{n-1} | CK _n | /S | /RAS | /CAS | /WE | Add | Action |
|---|-------------------|-----------------|----|------|------|-----|-----|-------------------------------------|
| SELF - REFRESH*1 | H | X | X | X | X | X | X | INVALID |
| | L | H | H | X | X | X | X | Exit Self-Refresh(Idle after tRC) |
| | L | H | L | H | H | H | X | Exit Self-Refresh(Idle after tRC) |
| | L | H | L | H | H | L | X | ILLEGAL |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP(Maintain Self-Refresh) |
| POWER DOWN | H | X | X | X | X | X | X | INVALID |
| | L | H | X | X | X | X | X | Exit Power Down to Idle |
| | L | L | X | X | X | X | X | NOP(Maintain Self-Refresh) |
| ALL BANKS IDLE*2 | H | H | X | X | X | X | X | Refer to Function Truth Table |
| | H | L | L | L | L | H | X | Enter Self-Refresh |
| | H | L | H | X | X | X | X | Enter Power Down |
| | H | L | L | H | H | H | X | Enter Power Down |
| | H | L | L | H | H | L | X | ILLEGAL |
| | H | L | L | H | L | X | X | ILLEGAL |
| | H | L | L | L | X | X | X | ILLEGAL |
| | L | X | X | X | X | X | X | Refer to Current State = Power Down |
| ANY STATE other than listed above | H | H | X | X | X | X | X | Refer to Function Truth Table |
| | H | L | X | X | X | X | X | Begin CK0 Suspend at Next Cycle*3 |
| | L | H | X | X | X | X | X | Exit CK0 Suspend at Next Cycle*3 |
| | L | L | X | X | X | X | X | Maintain CK0 Suspend |

ABBREVIATIONS:

H = High Level, L = Low Level, X = Don't Care

NOTES:

1. CKE Low to High transition will re-enable CK and other inputs **asynchronously**.
A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from the All banks idle State.
3. Must be legal command.

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POWER ON SEQUENCE

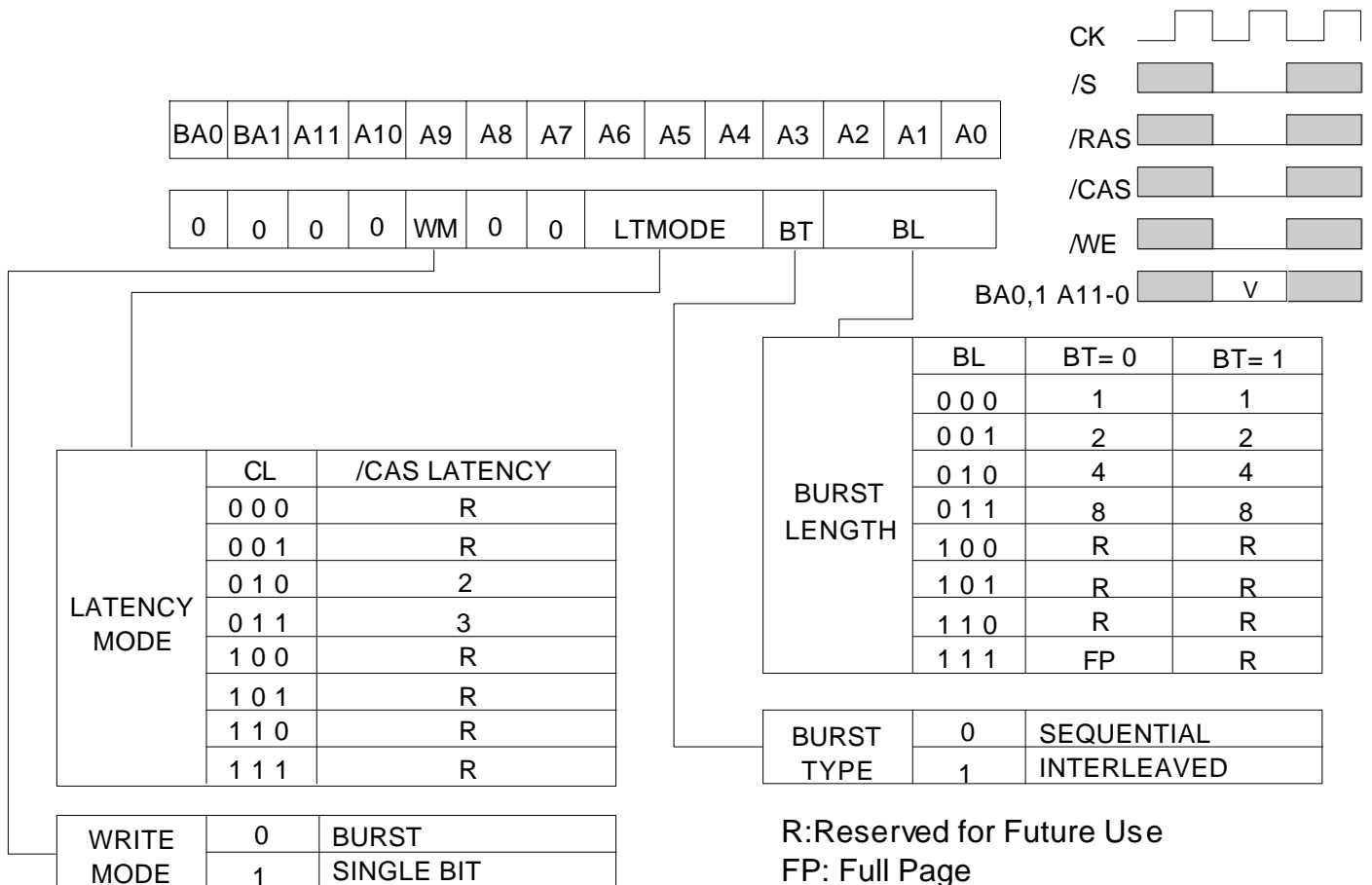
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high, DQMB high and NOP condition at the inputs.
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 500µs.
3. Issue precharge commands for all banks. (PRE or PREA)
4. After all banks become idle state (after tRP), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

After these sequence, the SDRAM is idle state and ready for normal operation.

MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register(MRS). The mode register stores these data until the next MRS command, which may be issue when both banks are in idle state. After tRSC from a MRS command, the SDRAM is ready for new command.

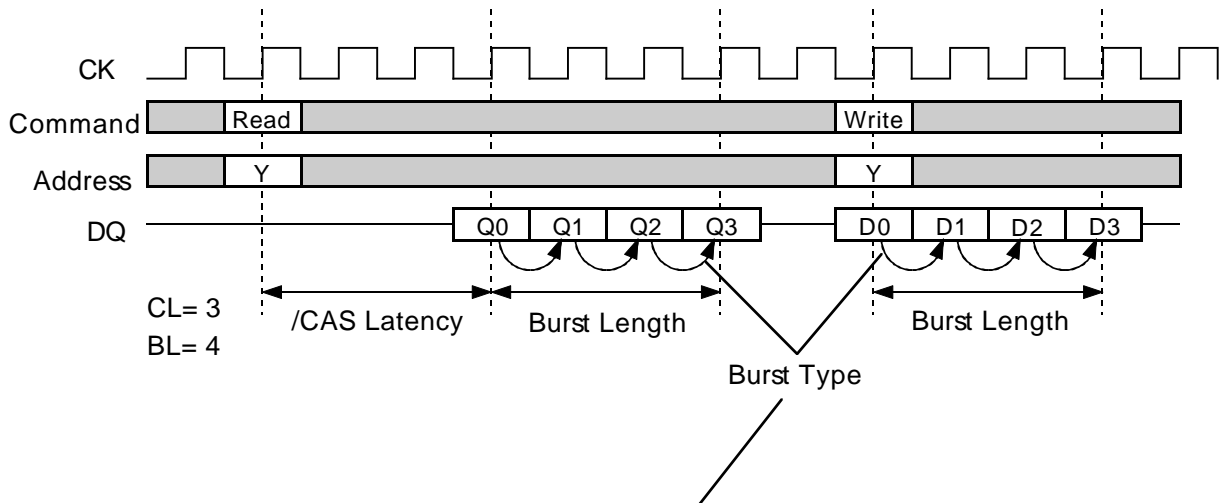


R:Reserved for Future Use
FP: Full Page

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| Initial Address | | | BL | Column Addressing | | | | | | | | | | | | | | | |
|-----------------|----|----|----|-------------------|---|---|---|---|---|---|---|-------------|---|---|---|---|---|---|---|
| A2 | A1 | A0 | | Sequential | | | | | | | | Interleaved | | | | | | | |
| 0 | 0 | 0 | 8 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 0 | 1 | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 0 | 3 | 2 | 5 | 4 | 7 | 6 |
| 0 | 1 | 0 | | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 0 | 1 | 6 | 7 | 4 | 5 |
| 0 | 1 | 1 | | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 |
| 1 | 0 | 0 | | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 |
| 1 | 0 | 1 | | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 4 | 7 | 6 | 1 | 0 | 3 | 2 |
| 1 | 1 | 0 | | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 4 | 5 | 2 | 3 | 0 | 1 |
| 1 | 1 | 1 | | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | 0 | 0 | 4 | 0 | 1 | 2 | 3 | | | | | 0 | 1 | 2 | 3 | | | | |
| - | 0 | 1 | | 1 | 2 | 3 | 0 | | | | | 1 | 0 | 3 | 2 | | | | |
| - | 1 | 0 | | 2 | 3 | 0 | 1 | | | | | 2 | 3 | 0 | 1 | | | | |
| - | 1 | 1 | | 3 | 0 | 1 | 2 | | | | | 3 | 2 | 1 | 0 | | | | |
| - | - | 0 | 2 | 0 | 1 | | | | | | | 0 | 1 | | | | | | |
| - | - | 1 | | 1 | 0 | | | | | | | 1 | 0 | | | | | | |

Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Condition | Ratings | Unit |
|--------|-----------------------|---------------------|------------|------|
| Vdd | Supply Voltage | with respect to Vss | -0.5 ~ 4.6 | V |
| VI | Input Voltage | with respect to Vss | -0.5 ~ 4.6 | V |
| VO | Output Voltage | with respect to Vss | -0.5 ~ 4.6 | V |
| IO | Output Current | | 50 | mA |
| Pd | Power Dissipation | Ta=25°C | 20.7 | W |
| Topr | Operating Temperature | | 0 ~ 70 | °C |
| Tstg | Storage Temperature | | -45 ~ 100 | °C |

RECOMMENDED OPERATING CONDITION

(Ta=0 ~ 70°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|--------|-------------------------------------|--------|------|---------|------|
| | | Min. | Typ. | Max. | |
| Vdd | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| Vss | Supply Voltage | 0 | 0 | 0 | V |
| VIH*1 | High-Level Input Voltage all inputs | 2.0 | | Vdd+0.3 | V |
| VIL*2 | Low-Level Input Voltage all inputs | -0.3 | | 0.8 | V |

NOTE)

1.VIH(max)=5.5V for pulse width less than 10ns.

2.VIL(min)=-1.0V for pulse width less than 10ns.

CAPACITANCE

(Ta=0 ~ 70°C, Vdd = 3.3 +/- 0.3V, Vss = 0V, unless otherwise noted)

| Symbol | Parameter | Test Condition | Limits(max.) | Unit |
|--------|--------------------------------|----------------------------------|--------------|------|
| CI(A) | Input Capacitance, address pin | VI = Vss f=1MHz Vi=25mVrms | 20 | pF |
| CI(C) | Input Capacitance, control pin | | 20 | pF |
| CI(K) | Input Capacitance, CK0 pin | | 20 | pF |
| CI/O | Input Capacitance, I/O pin | | 22 | pF |

Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

AVERAGE SUPPLY CURRENT from Vdd

(Ta=0 ~70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

| Parameter | Symbol | Test Condition | Limits (max) | Unit | Note |
|---|--------|---|--------------|------|------|
| | | | -7, -8 | | |
| operating current one bank active (discrete) | Icc1 | tRC=min.tCLK=min, BL=1, CL=3 | 2095 | mA | *1 |
| precharge standby current in non power-down mode /CS>Vcc-0.2V | Icc2N | tCLK=15ns, CKE = H, VIH > Vcc - 0.2V, VIL < 0.2V | 475 | mA | *1 |
| | Icc2NS | CLK=L & CKE=H, VIH > Vcc - 0.2V, VIL < 0.2V all input signals are fixed. | 295 | mA | *1 |
| precharge standby current in power-down mode /CS>Vcc-0.2V | Icc2P | tCLK = 15ns, CKE = L | 61 | mA | *1 |
| | Icc2PS | CLK = L, CKE = L | 43 | mA | *1 |
| active standby current | Icc3N | CKE=H, tCLK=15ns | 745 | mA | *1 |
| | Icc3NS | CKE=H, CLK=L | 655 | mA | *1 |
| burst current | Icc4 | tCLK=min, BL=4, CL=3 Aall banks active | 2545 | mA | *1 |
| auto-refresh current | Icc5 | tRC=min, tCLK=min | 3625 | mA | *1 |
| self-refresh current | Icc6 | CKE <0.2V | 61 | mA | *1,2 |
| | | | 39.4 | mA | |

Note1:Icc(max) is specified at the output open condition.

Note2:Low Power version

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

| Symbol | Parameter | Test Condition | Limits | | Unit |
|---------|-------------------------------|-----------------------|--------|------|------|
| | | | Min. | Max. | |
| VOH(DC) | High-Level Output Voltage(DC) | IOH=-2mA | 2.4 | | V |
| VOL(DC) | Low-Level Output Voltage(DC) | IOL=2mA | | 0.4 | V |
| IOZ | Off-state Output Current | Q floating VO=0 ~ Vdd | -10 | 10 | uA |
| Ii | Input Current | VIH=0 ~ Vdd+0.3V | -10 | -10 | uA |

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

AC TIMING REQUIREMENTS

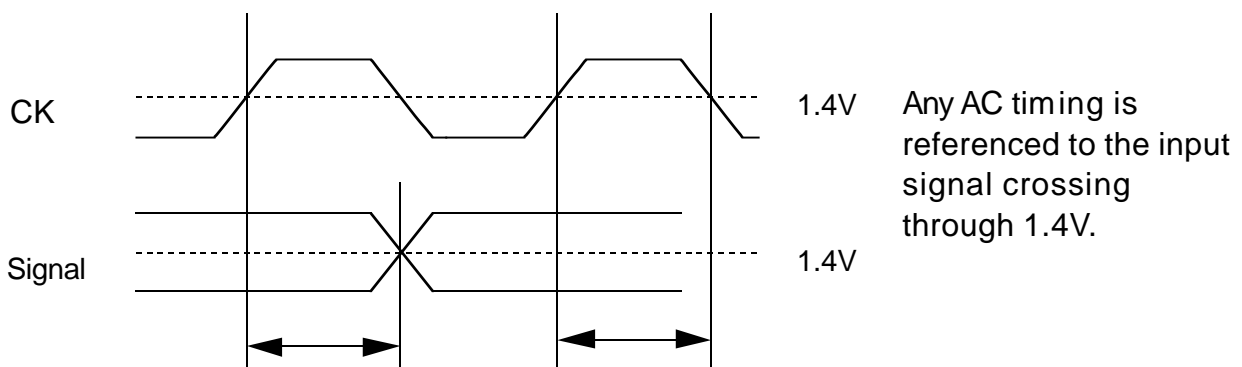
(Ta=0 ~ 70°C, Vdd = 3.3 +/- 0.3V, Vss = 0V, unless otherwise noted)

Input Pulse Levels: 0.8V to 2.0V

Input Timing Measurement Level: 1.4V

LATCH MODE

| Symbol | Parameter | Limits | | | | Unit |
|--------|------------------------------|--------|--------|------|--------|------|
| | | -7 | | -8 | | |
| | | Min. | Max. | Min. | Max. | |
| tCLK | CK cycle time | CL=3 | 10 | | 13 | ns |
| | | CL=4 | 10 | | 10 | ns |
| tCH | CK High pulse width | 3 | | 4 | | ns |
| tCL | CK Low pulse width | 3 | | 4 | | ns |
| tT | Transition time of CK | 1 | 10 | 1 | 10 | ns |
| tIS | Input Setup time(all inputs) | 2 | | 2 | | ns |
| tIH | Input Hold time(all inputs) | 1 | | 1 | | ns |
| tRC | Row cycle time | 70 | | 70 | | ns |
| tRCD | Row to Column Delay | 20 | | 20 | | ns |
| tRAS | Row Active time | 50 | 100000 | 50 | 100000 | ns |
| tRP | Row Precharge time | 20 | | 20 | | ns |
| tWR | Write Recovery time | 20 | | 20 | | ns |
| tRRD | Act to Act Deley time | 20 | | 20 | | ns |
| tRSC | Mode Register Set Cycle time | 20 | | 20 | | ns |
| tSRX | Self Refresh Exit time | 10 | | 10 | | ns |
| tPDE | Power Down Exit time | 10 | | 10 | | ns |
| tREF | Refresh Interval time | | 64 | | 64 | ms |



Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

BUFFER MODE

| Symbol | Parameter | Limits | | | | Unit | |
|--------|------------------------------|--------|------|--------|------|--------|----|
| | | -7 | | -8 | | | |
| | | Min. | Max. | Min. | Max. | | |
| tCLK | CK cycle time | CL=2 | 10 | | 13 | | ns |
| | | CL=3 | 10 | | 10 | | ns |
| tCH | CK High pulse width | | 3 | | 4 | | ns |
| tCL | CK Low pulse width | | 3 | | 4 | | ns |
| tT | Transition time of CK | | 1 | 10 | 1 | 10 | ns |
| tIS | Input Setup time(all inputs) | | 7 | | 7 | | ns |
| tIH | Input Hold time(all inputs) | | 1 | | 1 | | ns |
| tRC | Row cycle time | | 70 | | 70 | | ns |
| tRCD | Row to Column Delay | | 20 | | 20 | | ns |
| tRAS | Row Active time | | 50 | 100000 | 50 | 100000 | ns |
| tRP | Row Precharge time | | 20 | | 20 | | ns |
| tWR | Write Recovery time | | 20 | | 20 | | ns |
| tRRD | Act to Act Delay time | | 20 | | 20 | | ns |
| tRSC | Mode Register Set Cycle time | | 20 | | 20 | | ns |
| tSRX | Self Refresh Exit time | | 10 | | 10 | | ns |
| tPDE | Power Down Exit time | | 10 | | 10 | | ns |
| tREF | Refresh Interval time | | | 64 | | 64 | ms |

SWITCHING CHARACTERISTICS

(Ta=0 ~ 70°C, Vdd = 3.3 +/- 0.3V, Vss = 0V, unless otherwise noted)

LATCH MODE

| Symbol | Parameter | Limits | | | | Unit | Note |
|--------|---|--------|------|------|------|------|------|
| | | -7 | | -8 | | | |
| | | Min. | Max. | Min. | Max. | | |
| tAC | Access time from CK | CL=3 | | 6 | | 7 | *1 |
| | | CL=4 | | 6 | | 6 | |
| tOH | Output Hold time from CK | | 3 | | 3 | | |
| tOLZ | Delay time, output low impedance from CK | | 0 | | 0 | | |
| tOHZ | Delay time, output high impedance from CK | | 3 | 6 | 3 | 6 | |

NOTE)

1.If clock rising time is longer than 1ns, (tr /2-0.5ns) should be added to the paraneter.

Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

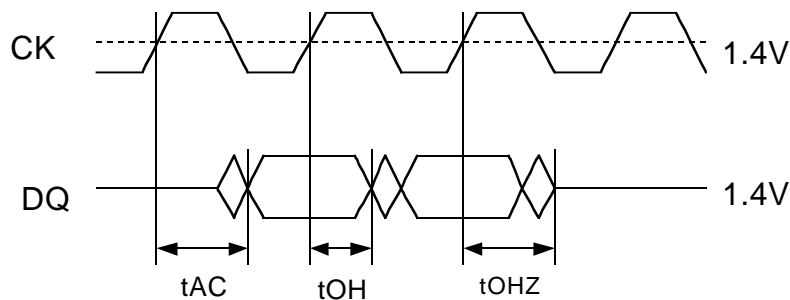
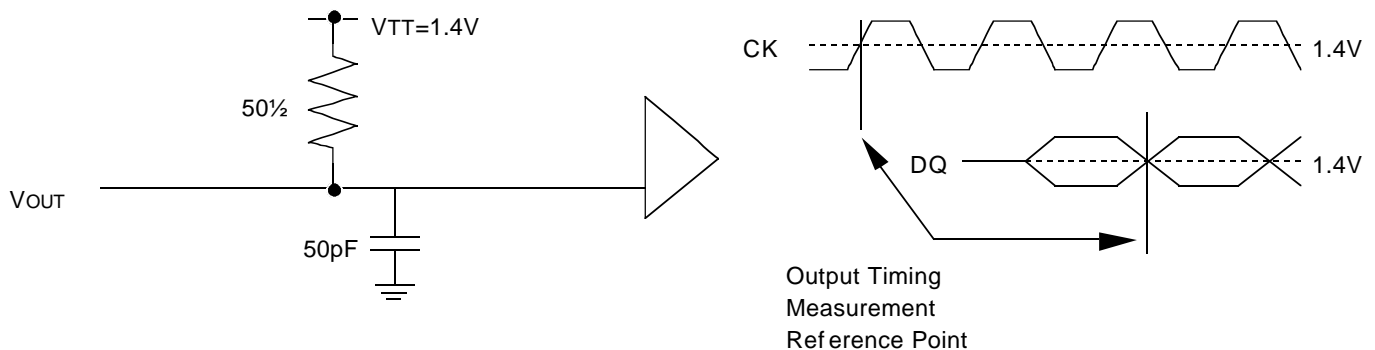
BUFFER MODE

| Symbol | Parameter | Limits | | | | Unit | Note | |
|--------|---|--------|------|------|------|------|------|----|
| | | -7 | | -8 | | | | |
| | | Min. | Max. | Min. | Max. | | | |
| tAC | Access time from CK | CL=2 | | 6 | | 7 | ns | *1 |
| | | CL=3 | | 6 | | 6 | | |
| tOH | Output Hold time from CK | 3 | | 3 | | ns | | |
| tOLZ | Delay time, output low impedance from CK | 0 | | 0 | | ns | | |
| tOHZ | Delay time, output high impedance from CK | 3 | 6 | 3 | 6 | ns | | |

NOTE)

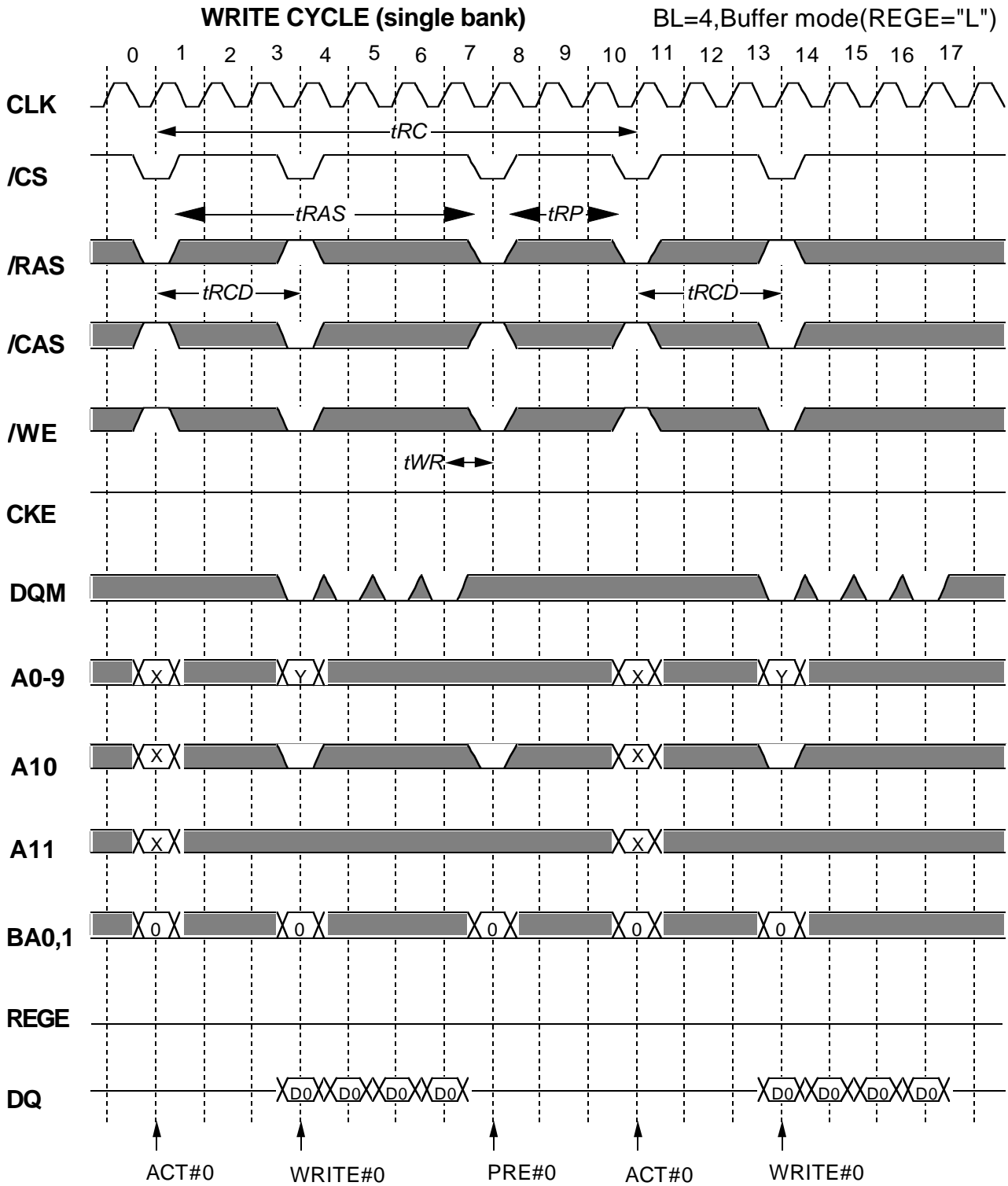
1.If clock rising time is longer than 1ns, (tr /2-0.5ns) should be added to the paraneter.

Output Load Condition



MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

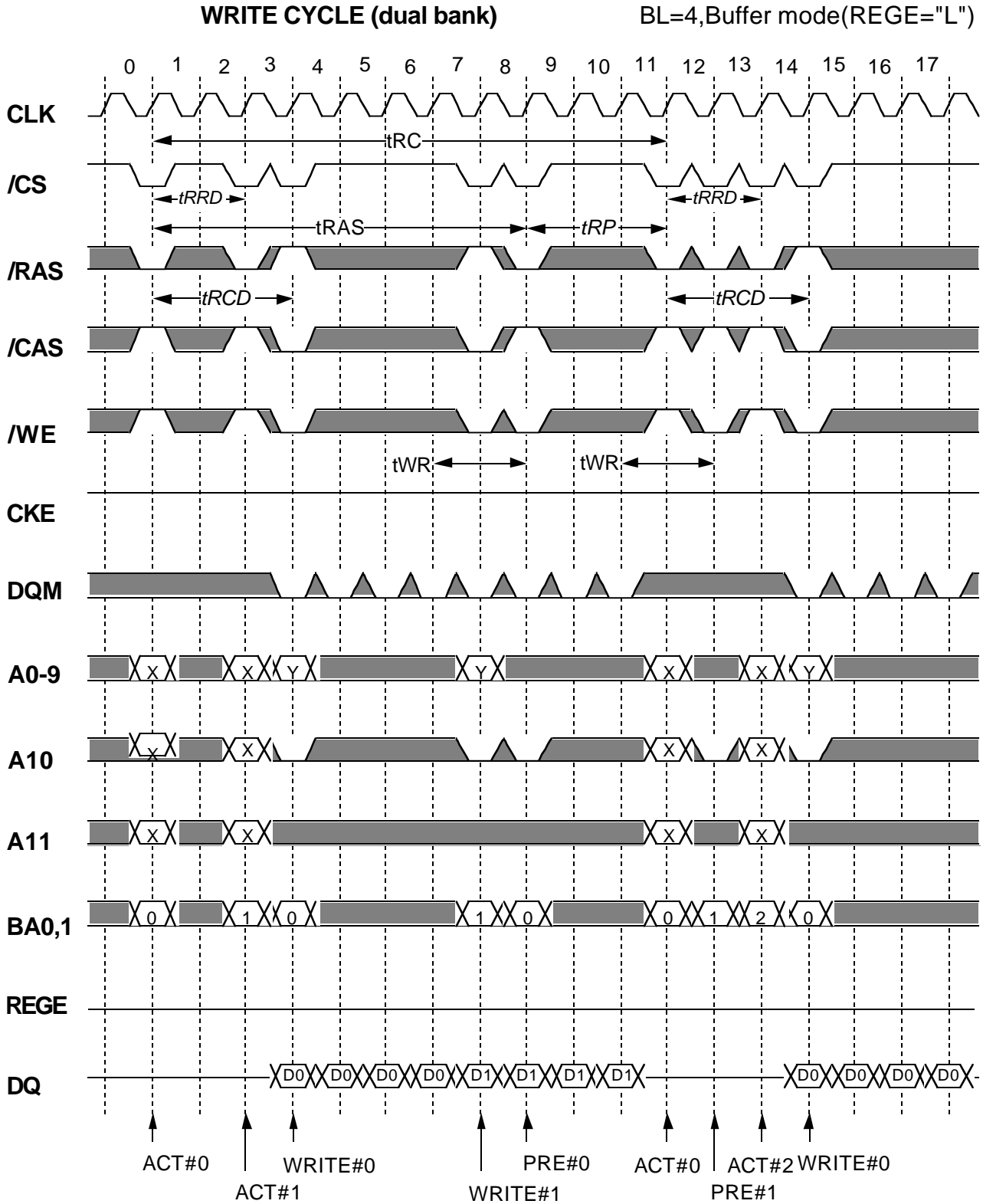


Italic parameter indicates minimum case

Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

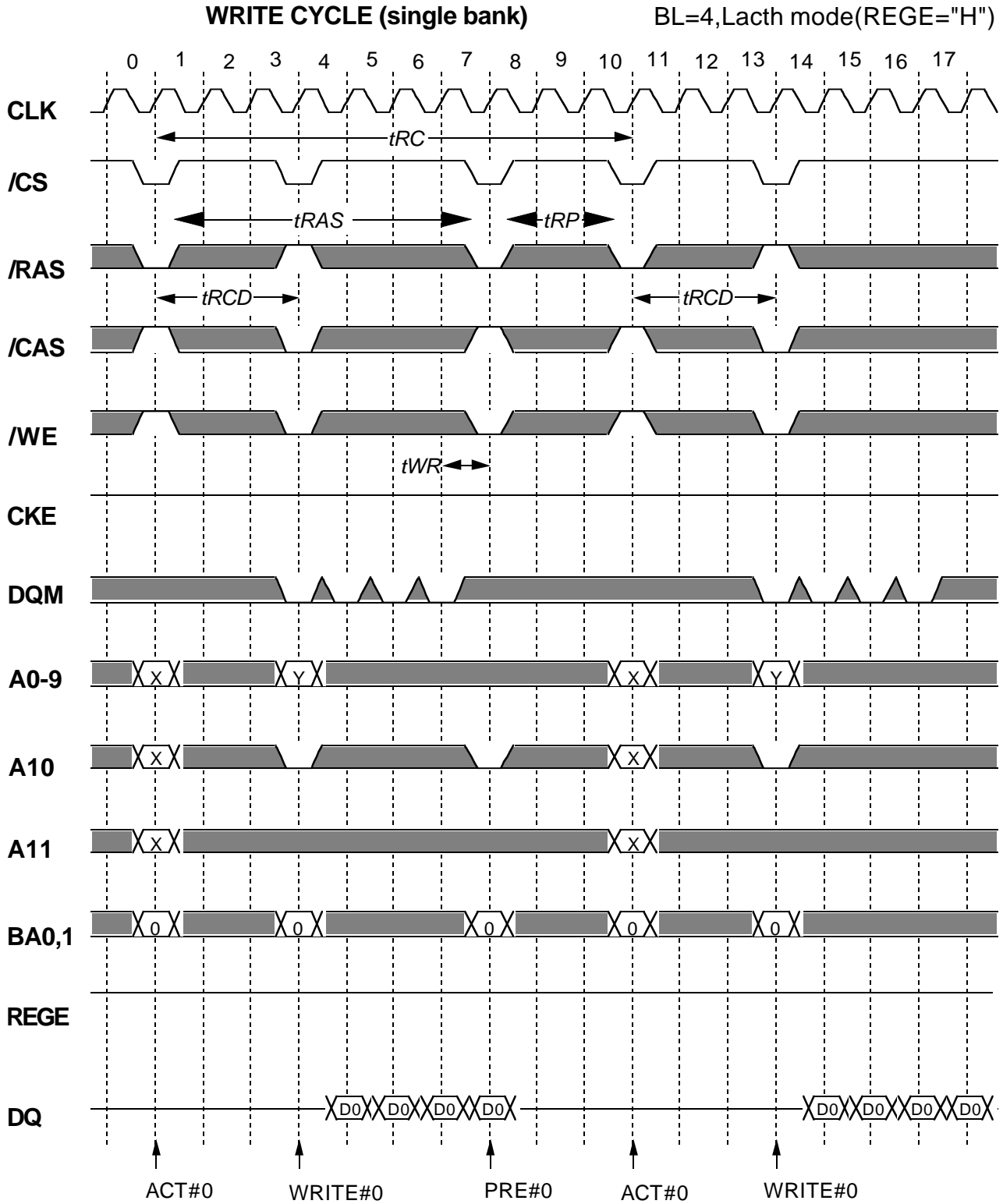


Italic parameter indicates minimum case

Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM



Italic parameter indicates minimum case

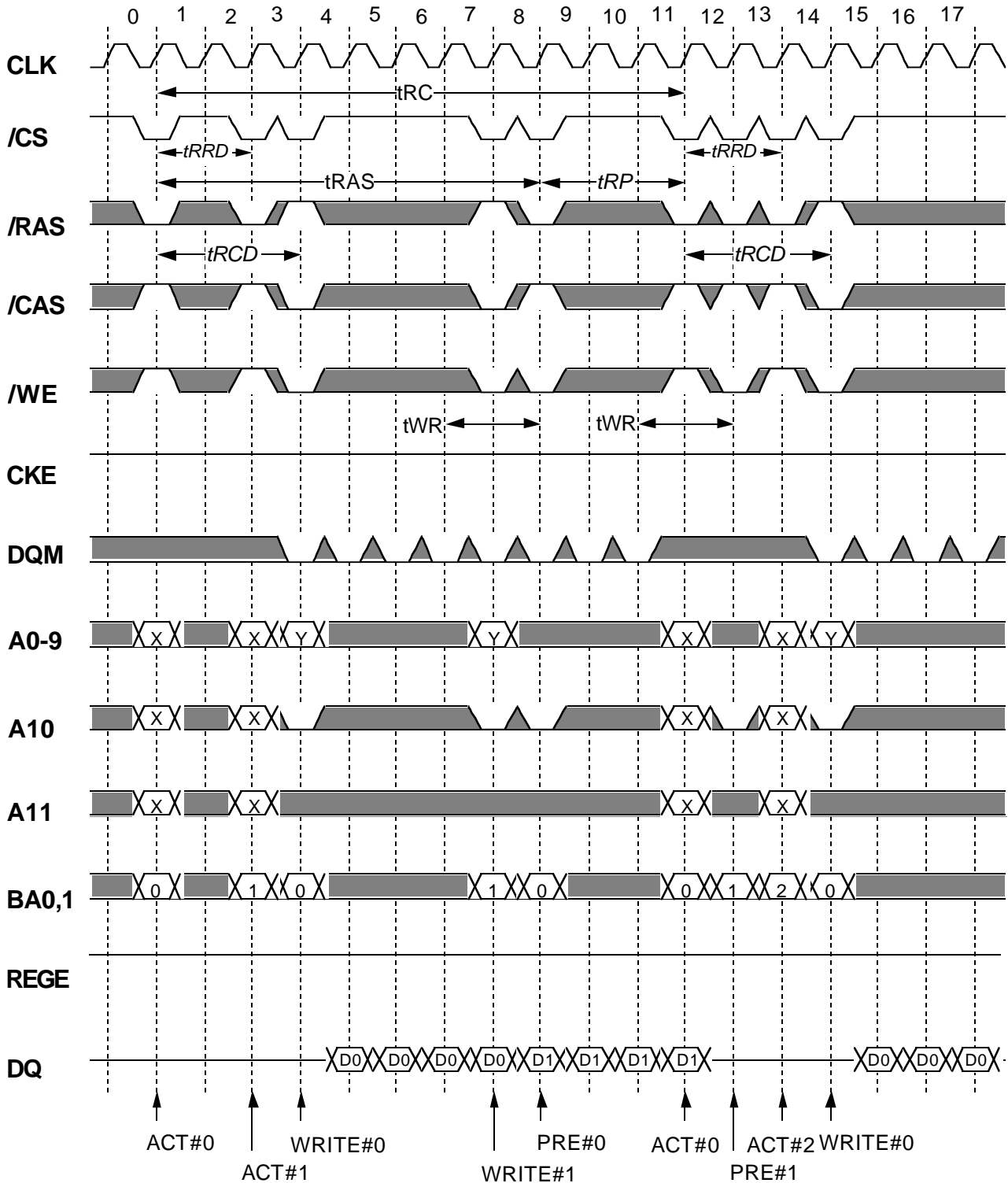
Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

WRITE CYCLE (dual bank)

BL=4, Latch mode (REGE="H")



Italic parameter indicates minimum case

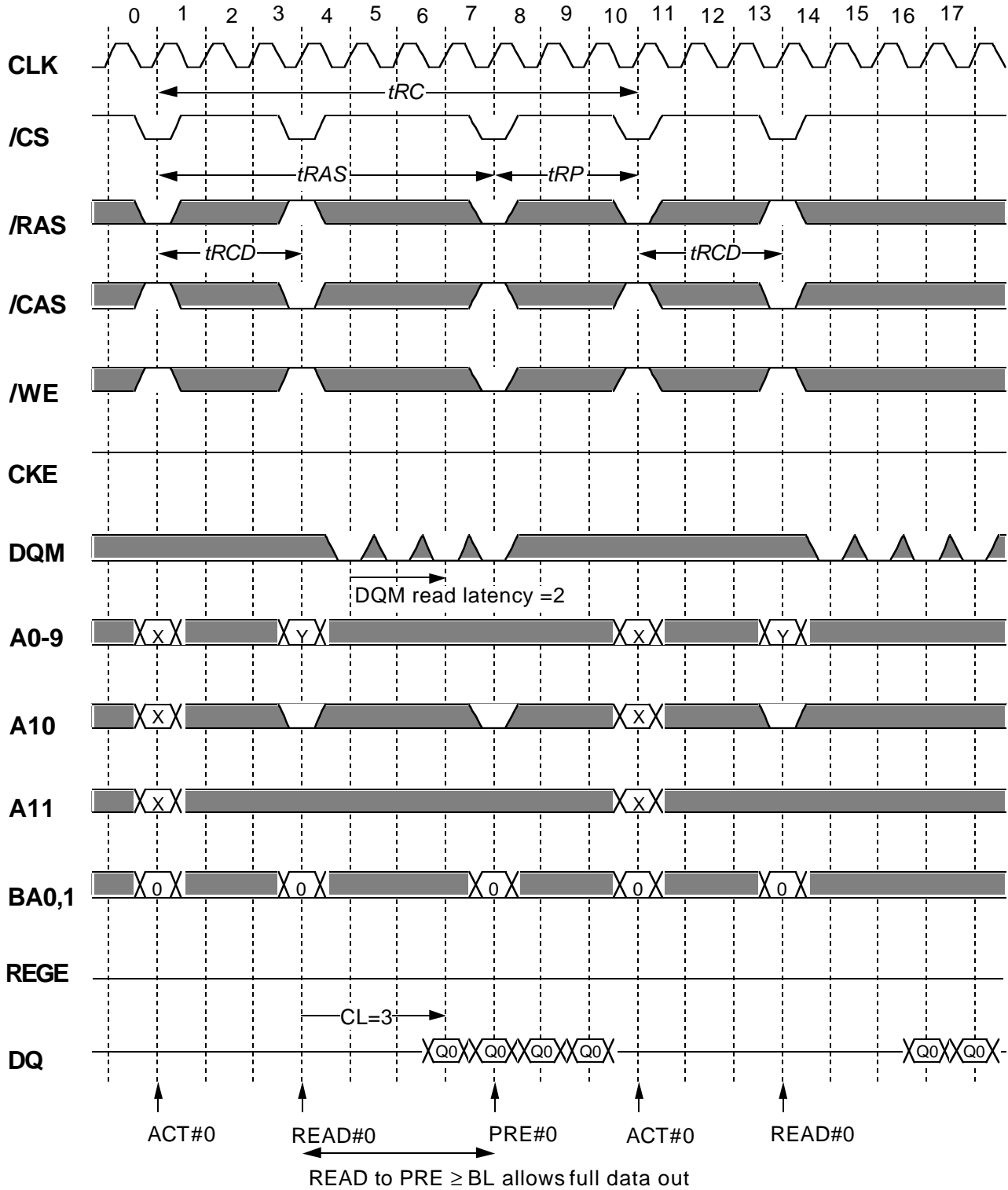
Preliminary Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

READ CYCLE (single bank)

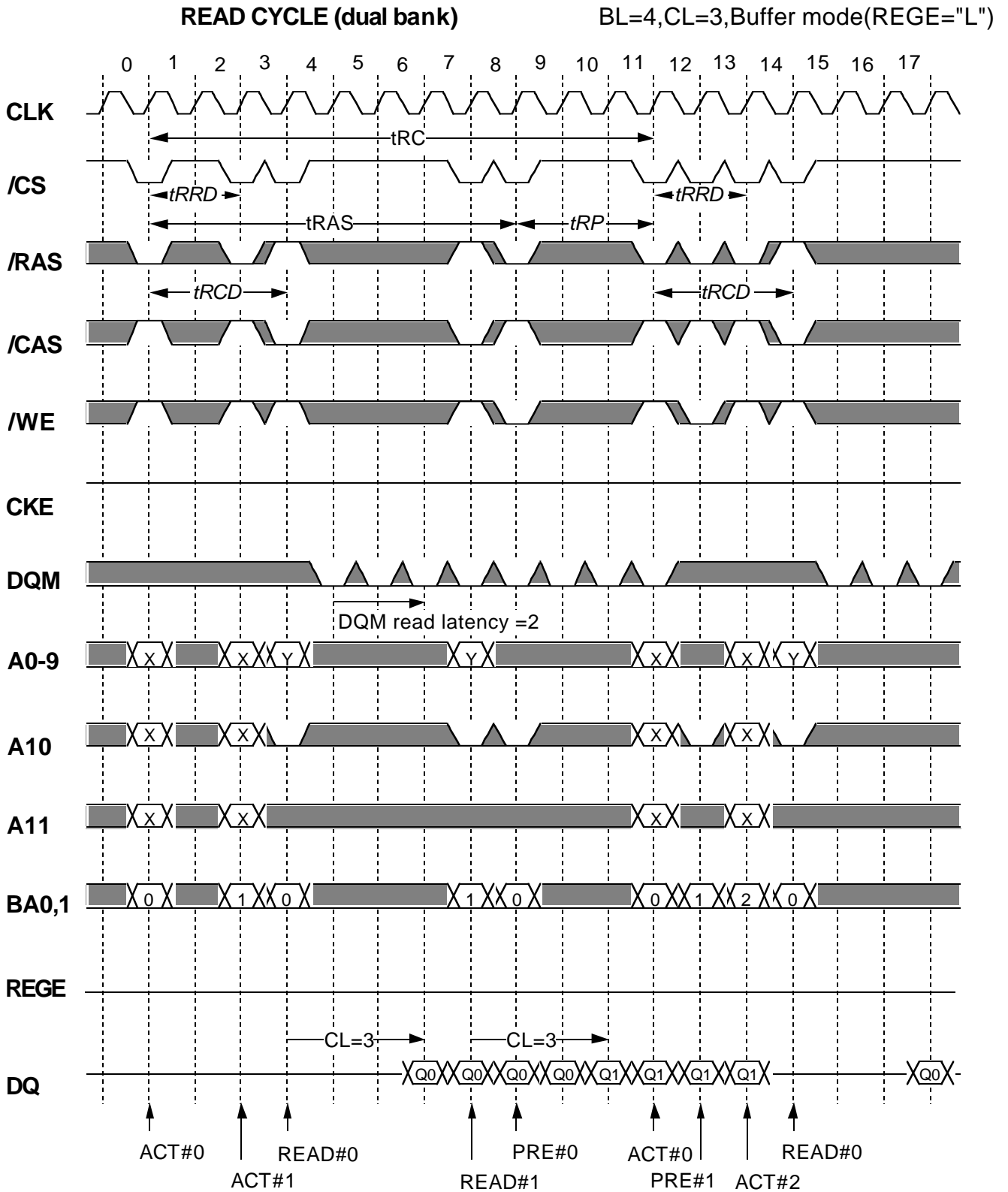
BL=4,CL=3,Buffer mode(REGE="L")



Italic parameter indicates minimum case

MH32S72QJA-7, -8

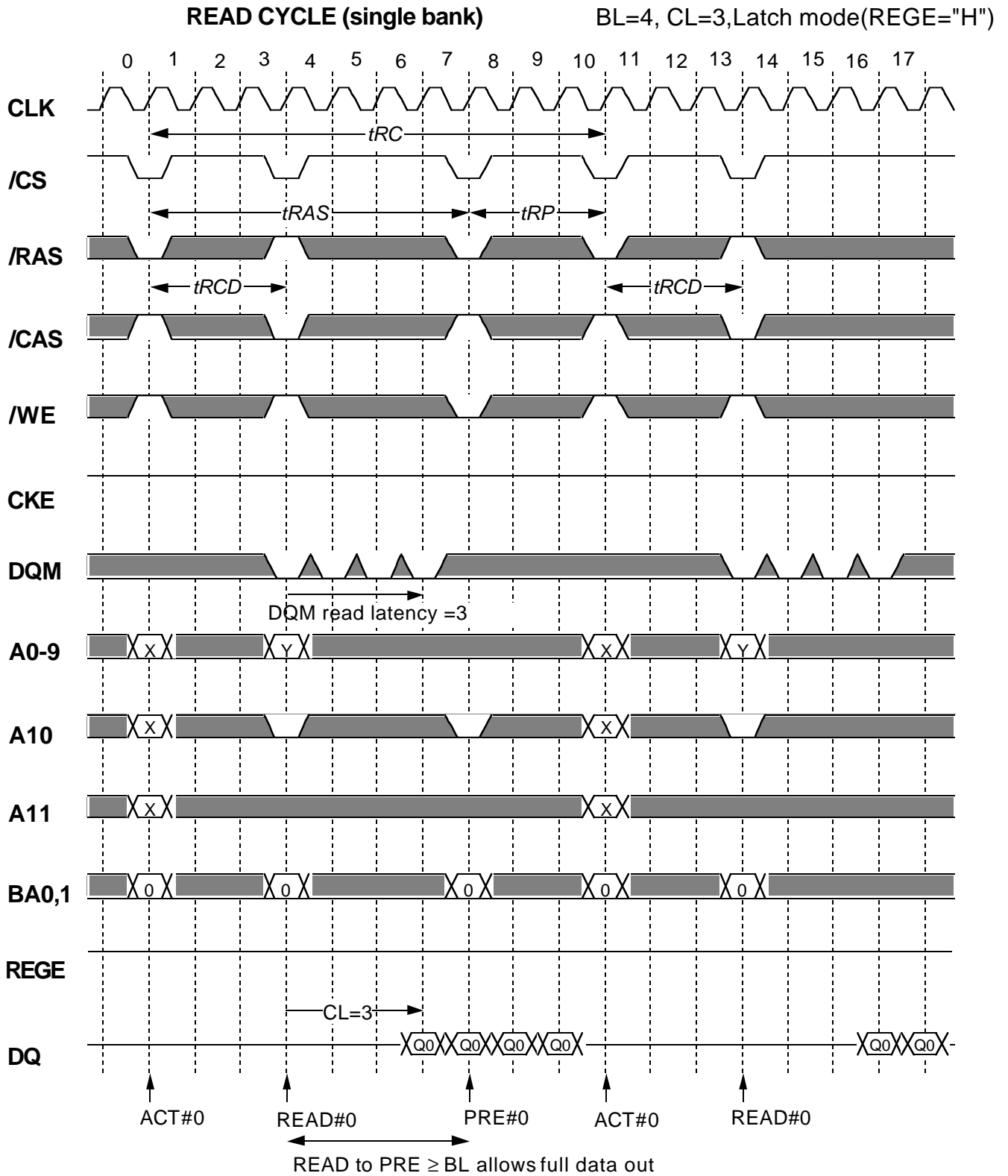
2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM



Italic parameter indicates minimum case

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM



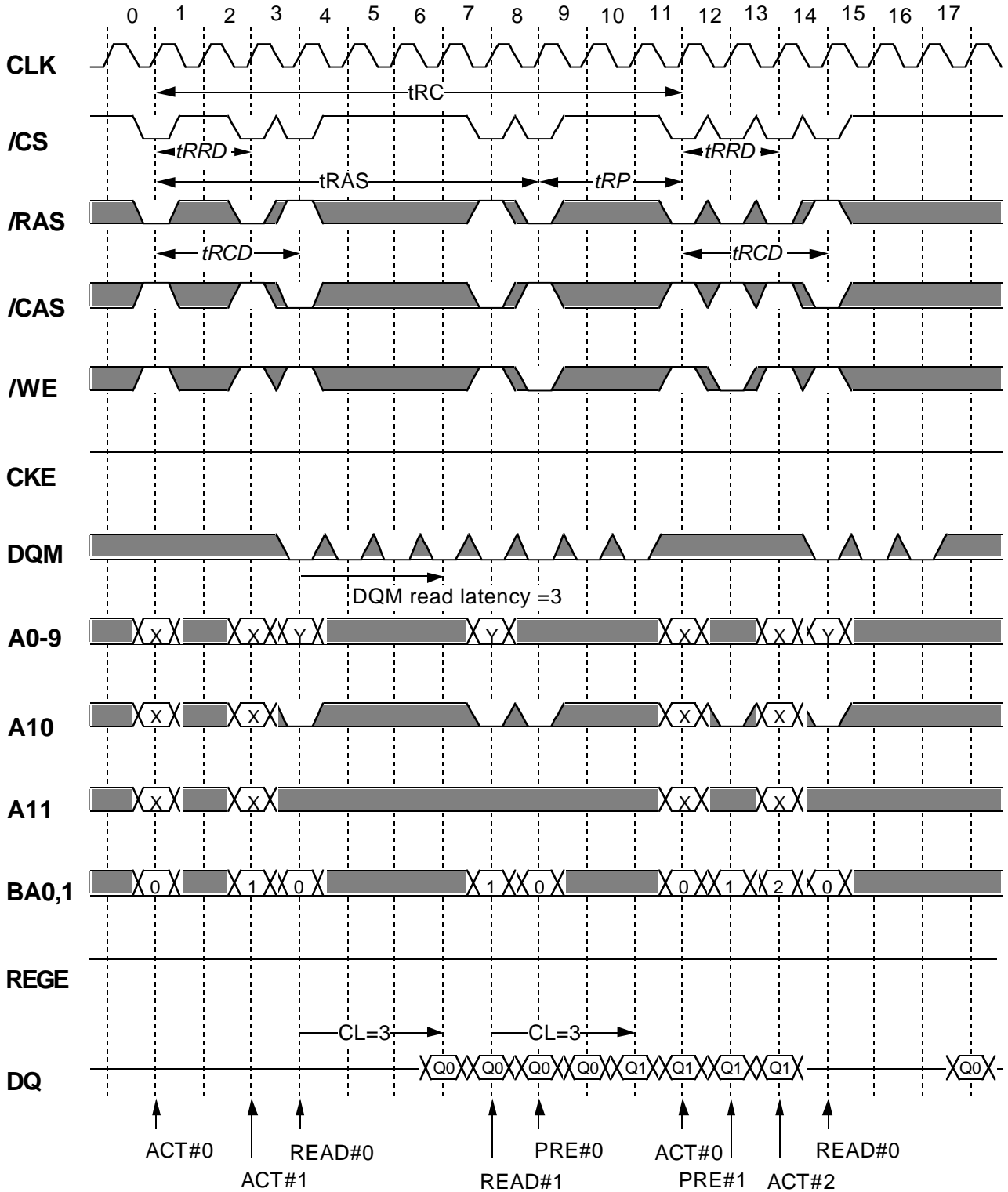
Italic parameter indicates minimum case

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

READ CYCLE (dual bank)

BL=4, CL=3, Latch mode (REGE="H")

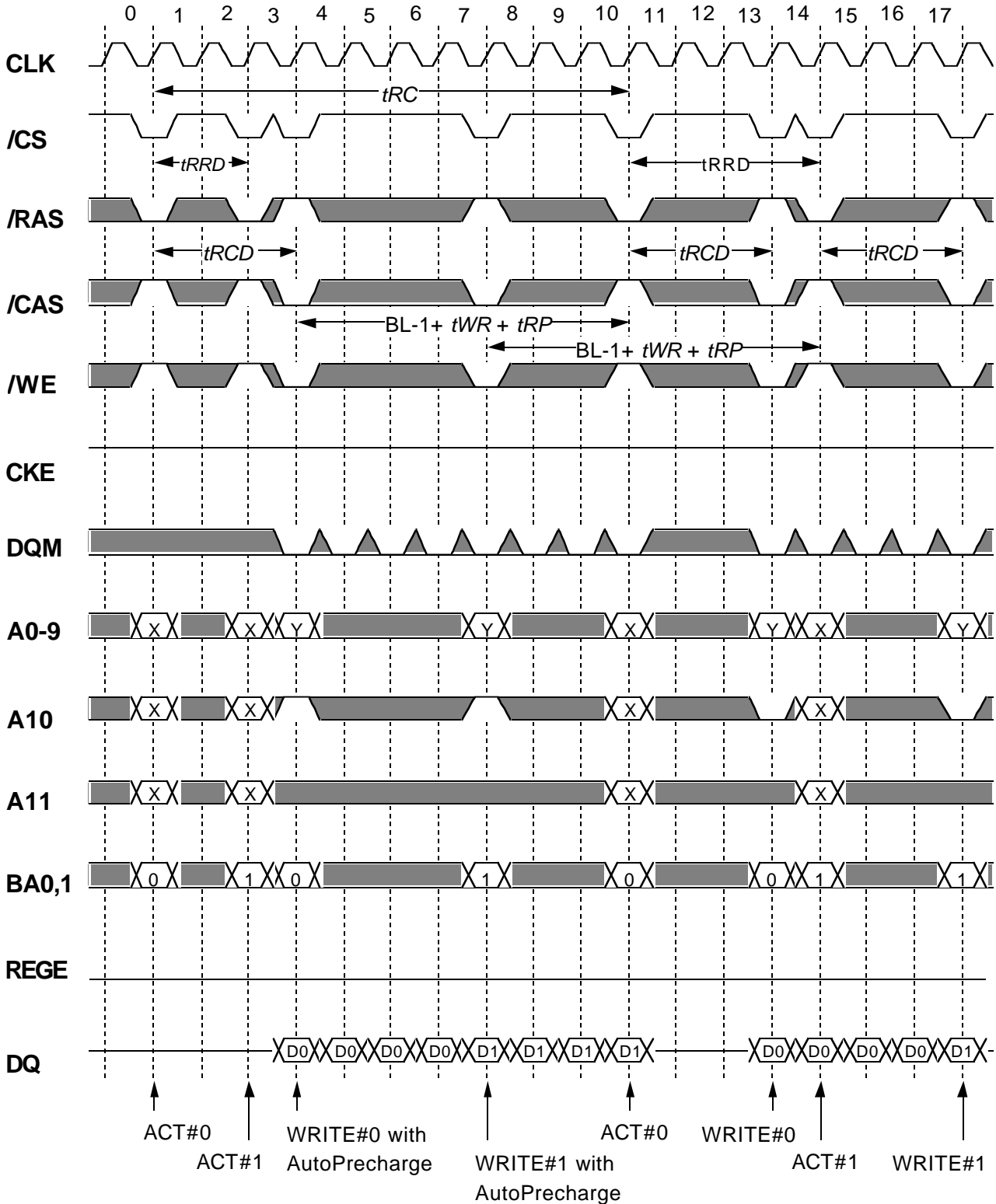


Italic parameter indicates minimum case

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Burst WRITE (multi bank) with AUTO-PRECHARGE BL=4, Buffer mode(REGE="L")

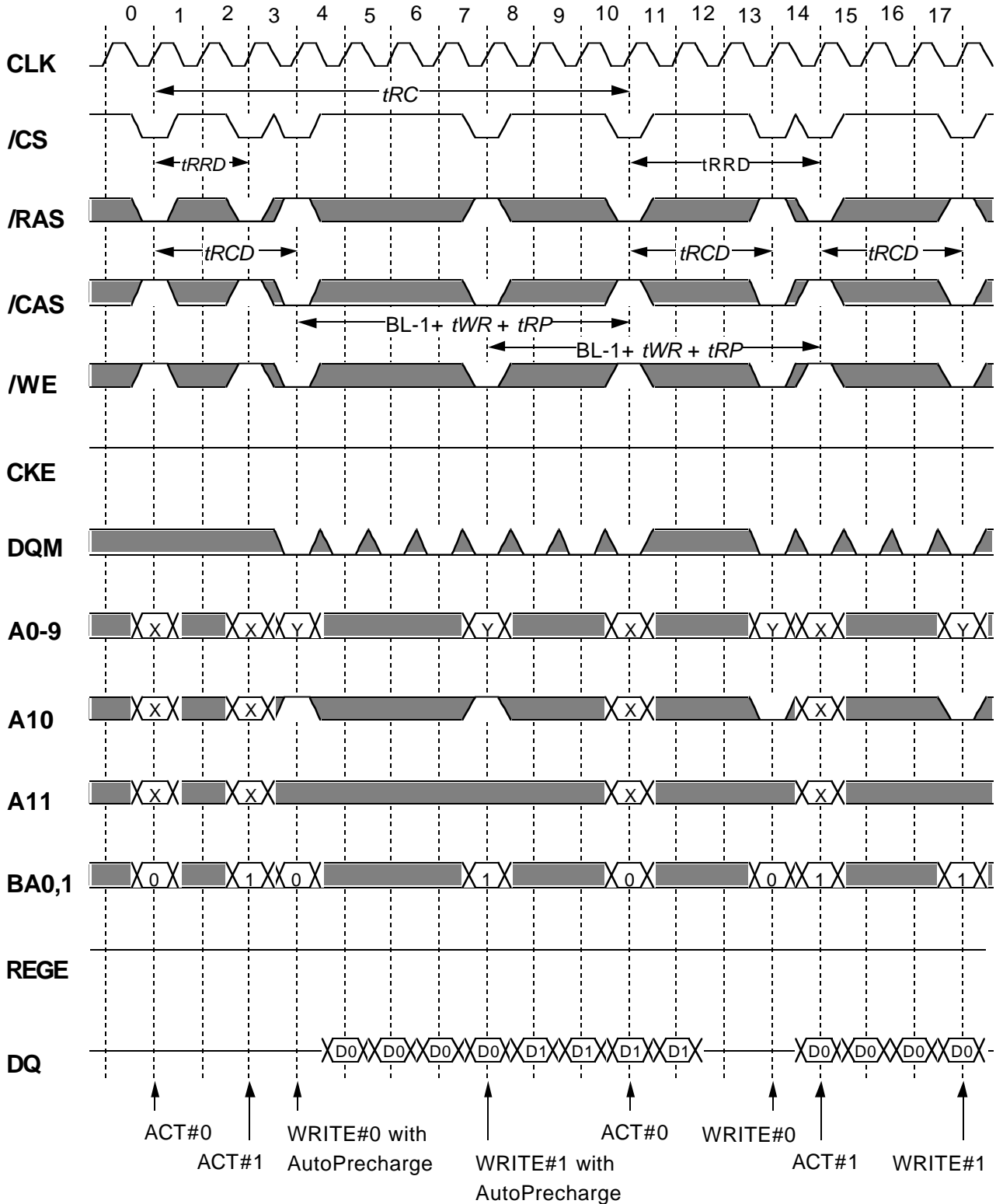


Italic parameter indicates minimum case

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Burst WRITE (multi bank) with AUTO-PRECHARGE BL=4,Latch mode(REGE="H")



Italic parameter indicates minimum case

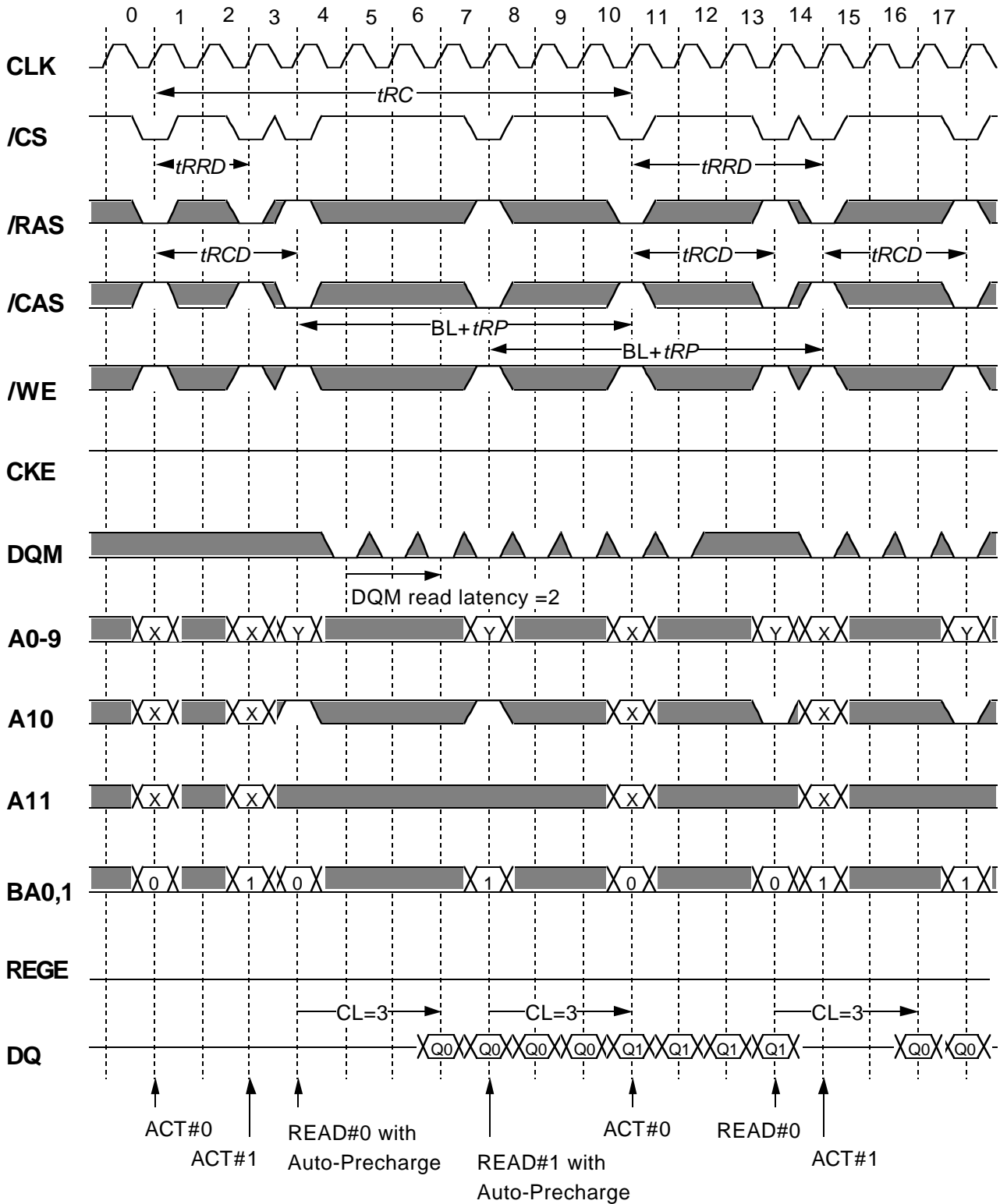
Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Burst READ (multi bank) with AUTO-PRECHARGE

BL=4, Buffer mode(REGE="L")



Italic parameter indicates minimum case

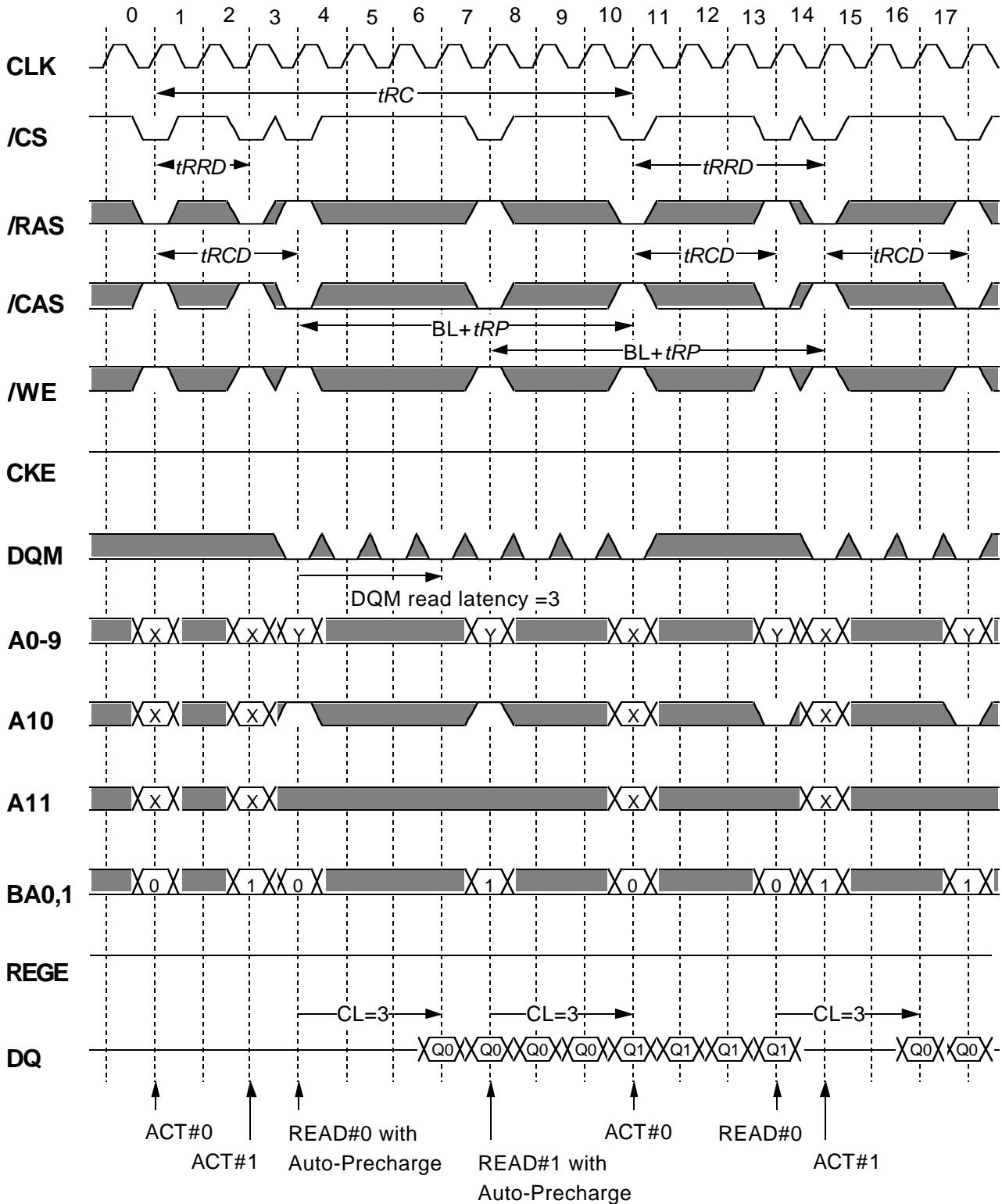
Preliminary Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Burst READ (multi bank) with AUTO-PRECHARGE

BL=4,Latch mode(REGE="H")



Italic parameter indicates minimum case

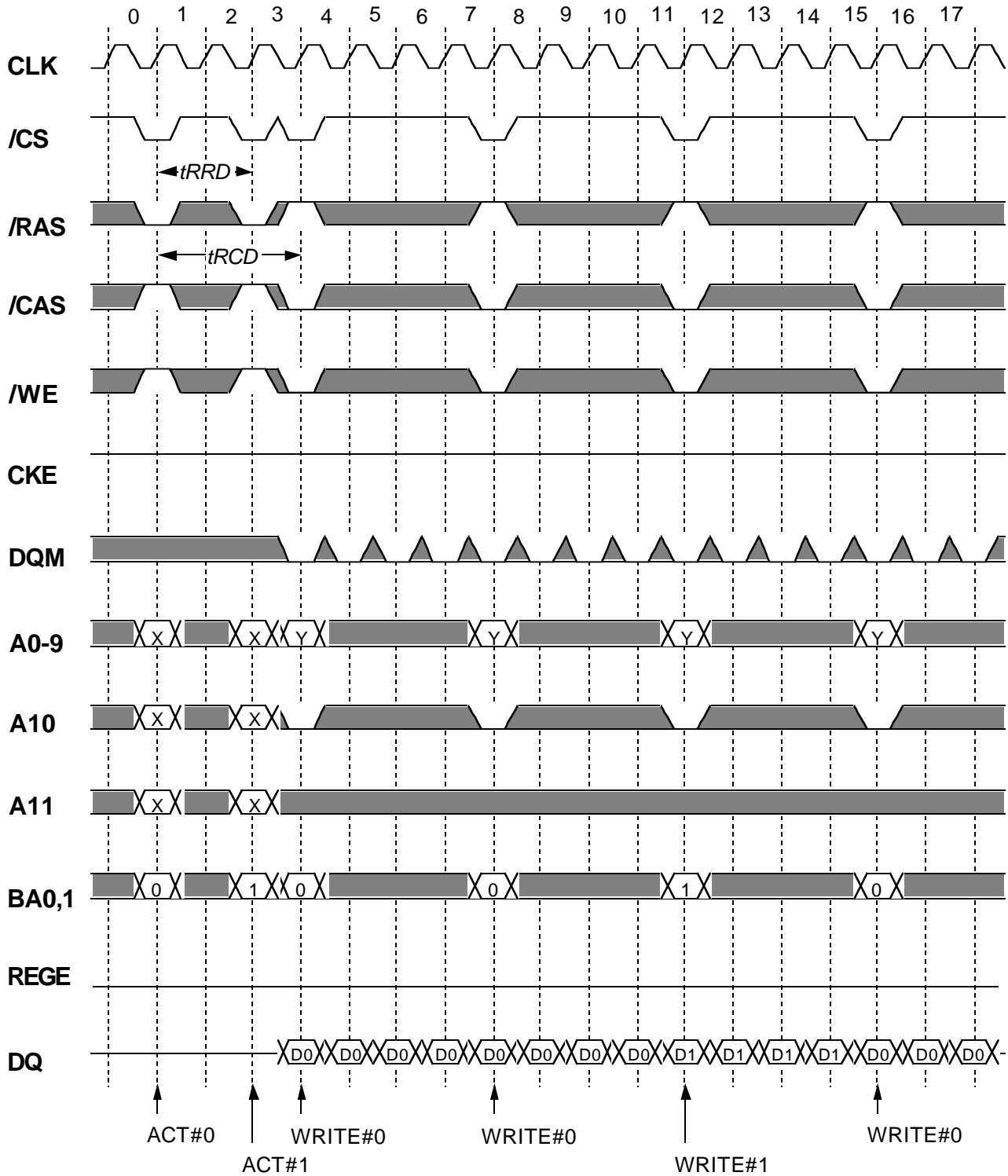
Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Page Mode Burst Write (multi bank)

BL=4, Buffer mode(REGE="L")



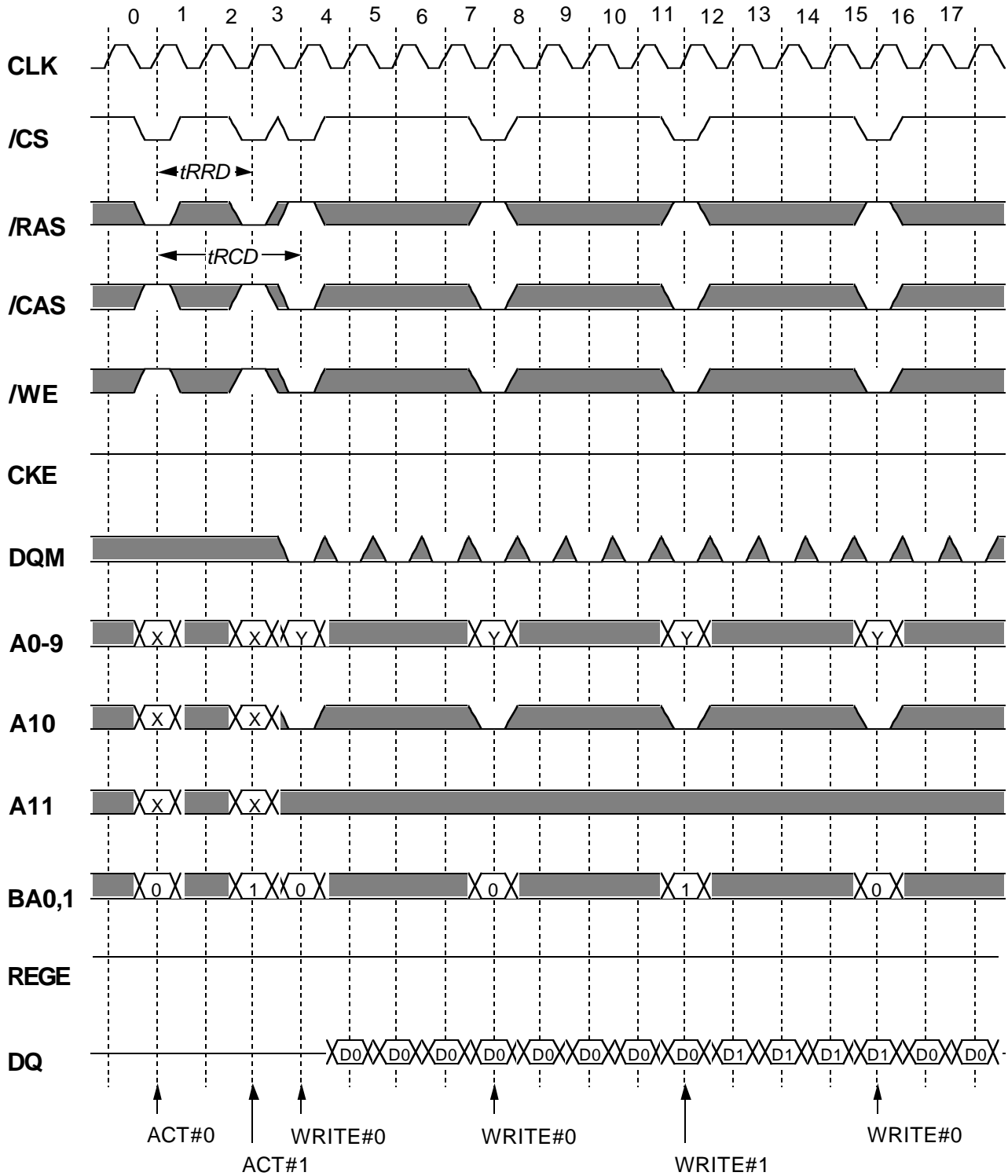
Italic parameter indicates minimum case

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Page Mode Burst Write (multi bank)

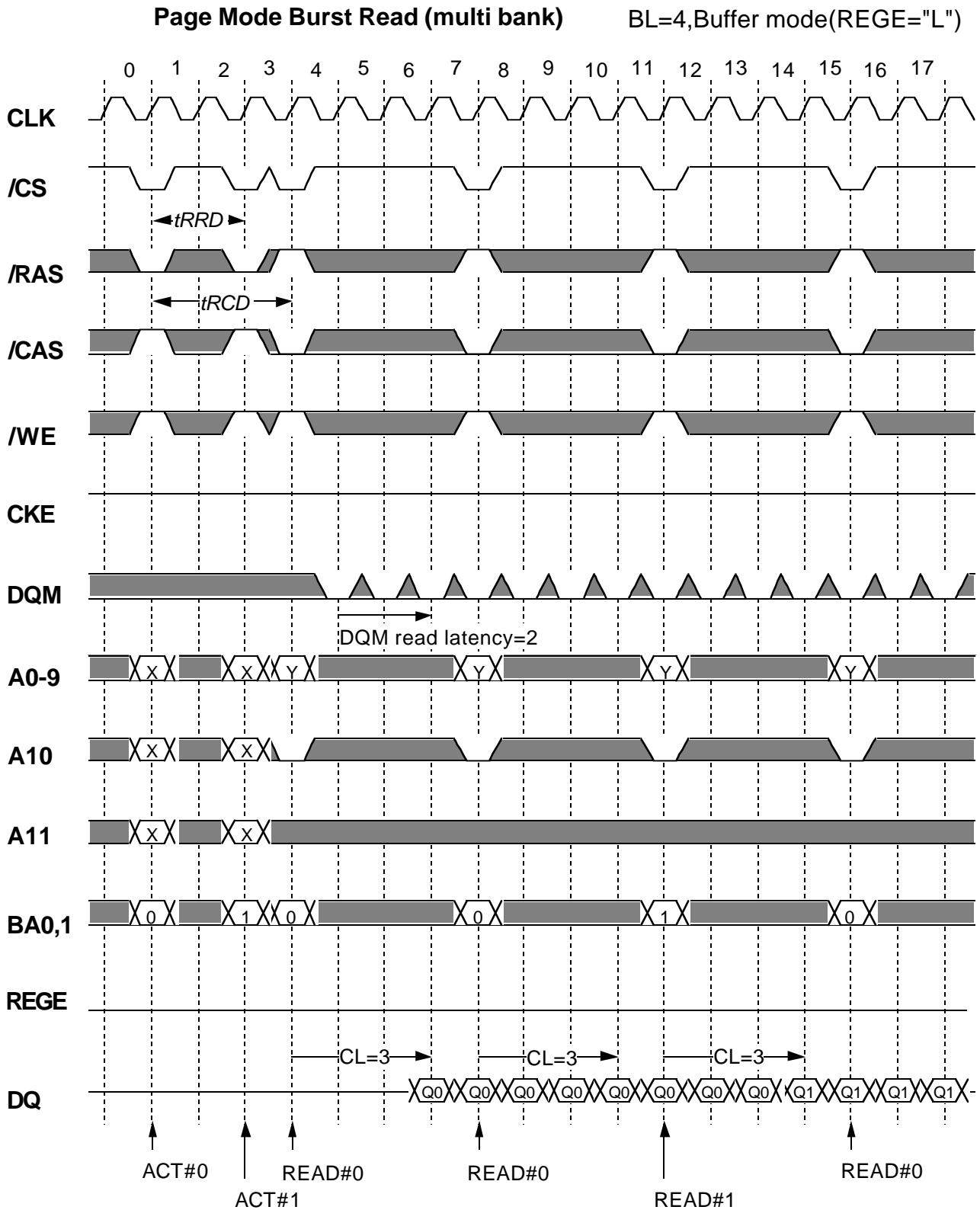
BL=4, Latch mode (REGE="H")



Italic parameter indicates minimum case

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM



Italic parameter indicates minimum case

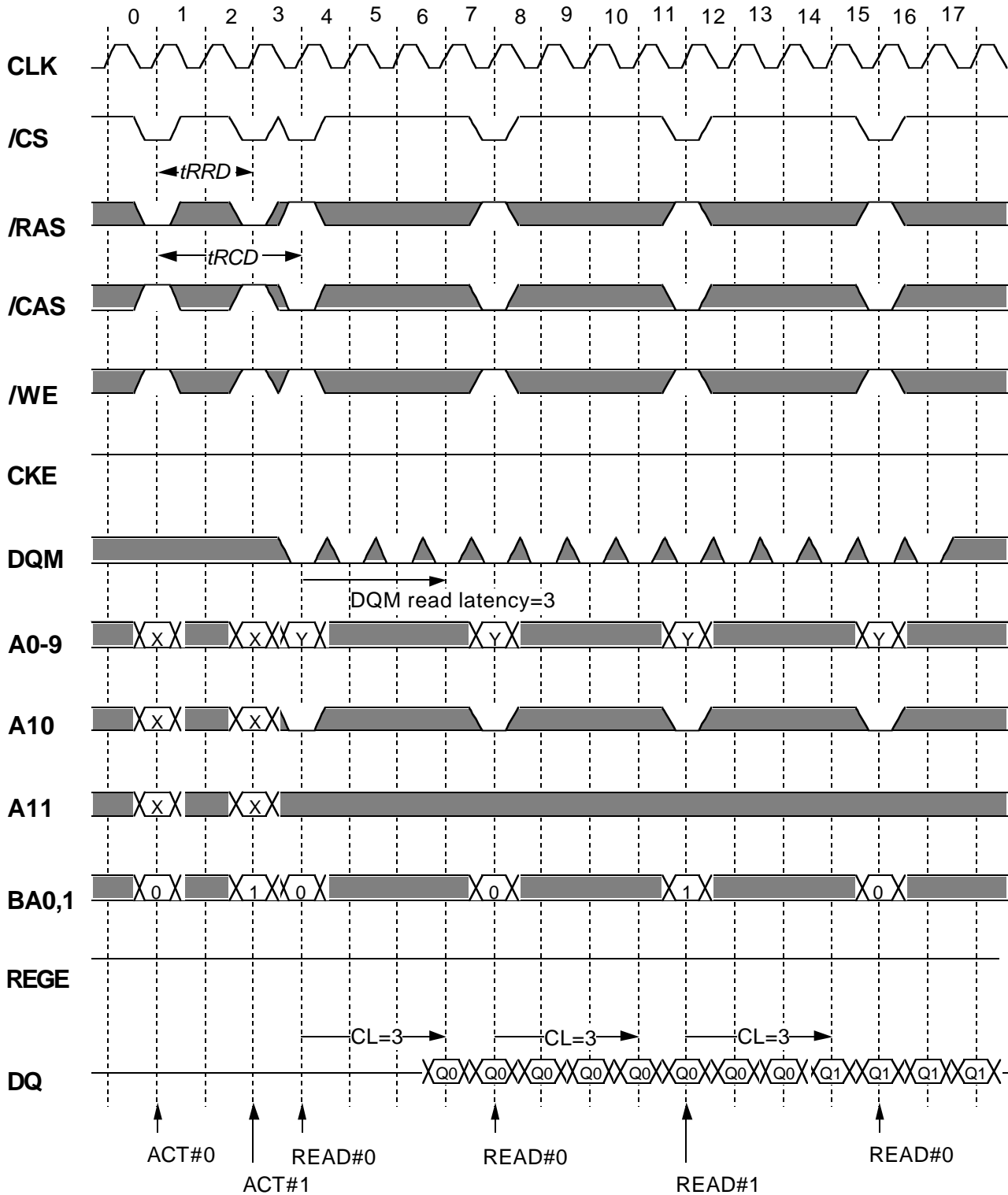
Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Page Mode Burst Read (multi bank)

BL=4, Latch mode(REGE="H")

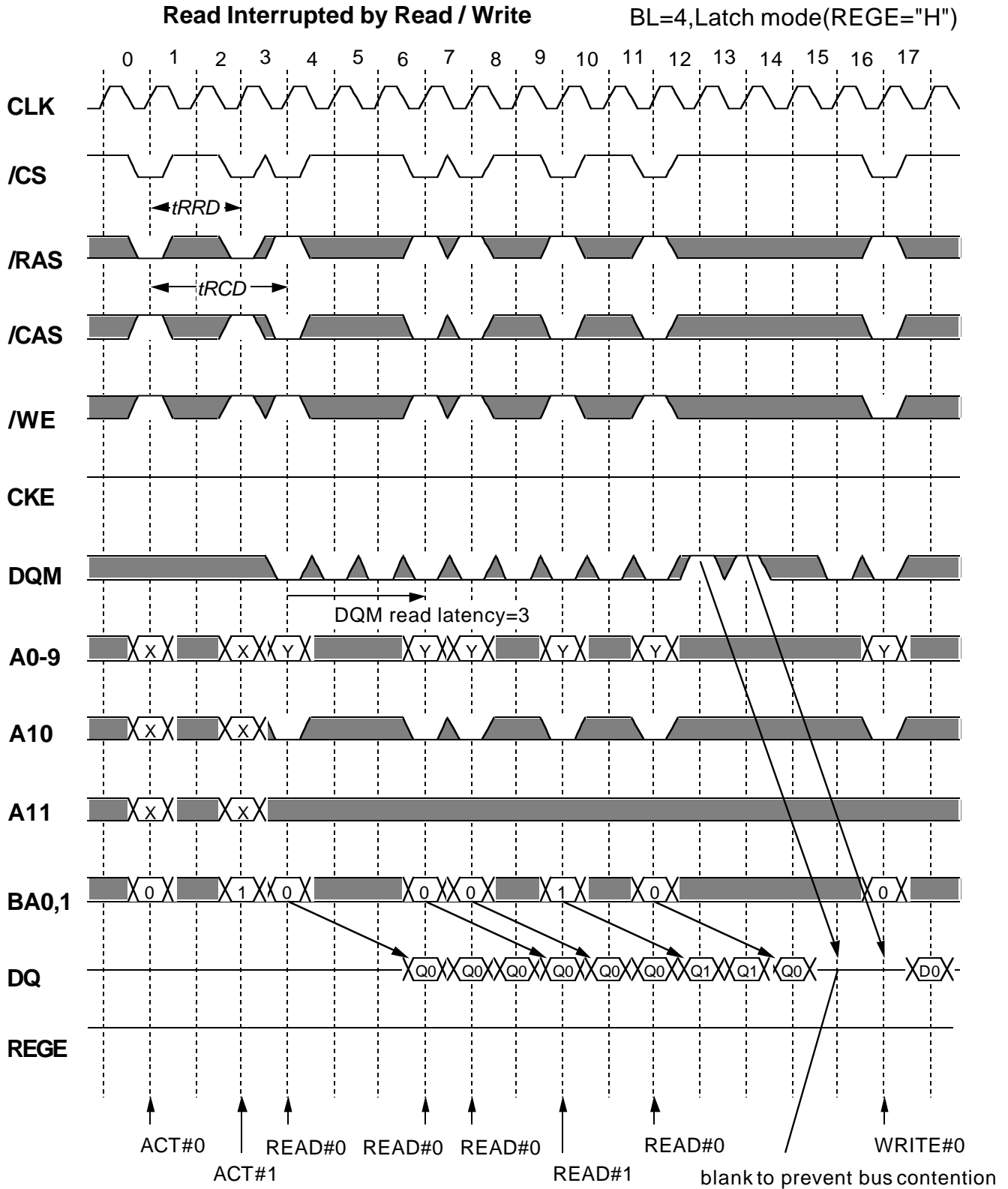


Italic parameter indicates minimum case

Preliminary Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM



Burst Read can be interrupted by Read or Write of any active bank.

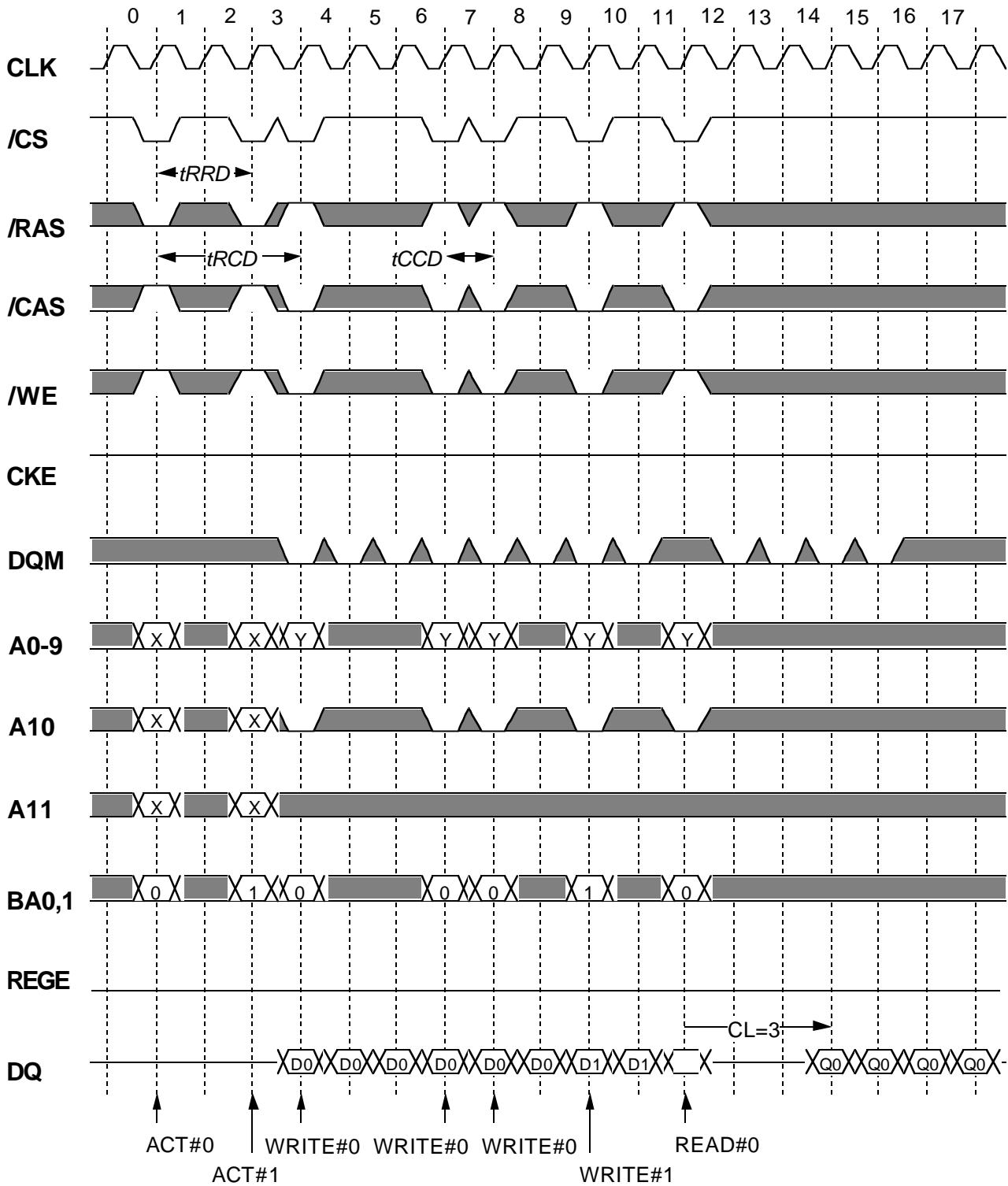
Italic parameter indicates minimum case

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Write Interrupted by Write / Read

BL=4, Buffer mode (REGE="L")



Burst Write can be interrupted by Write or Read of any active bank.

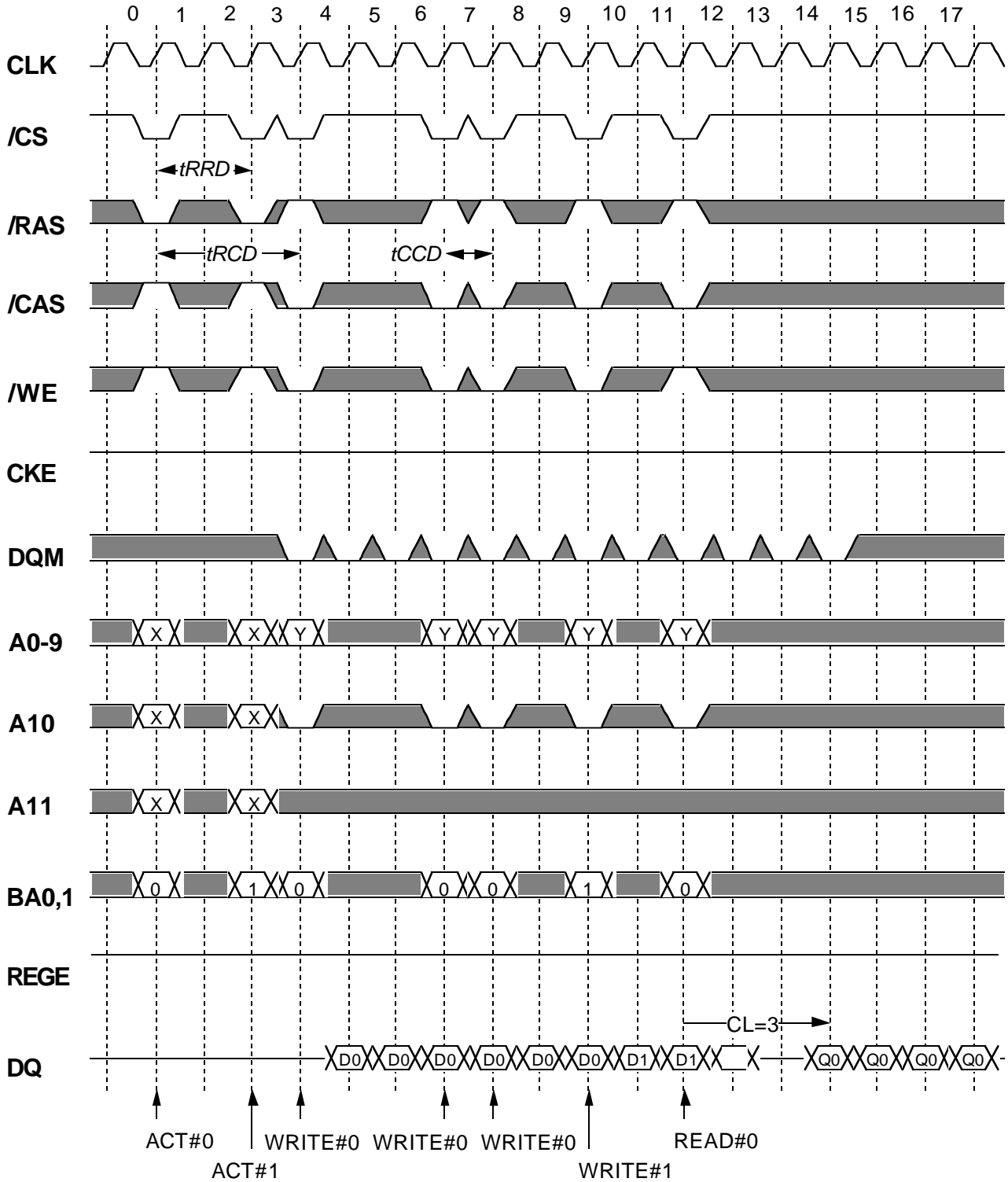
Italic parameter indicates minimum case

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Write Interrupted by Write / Read

BL=4, Latch mode (REGE="H")



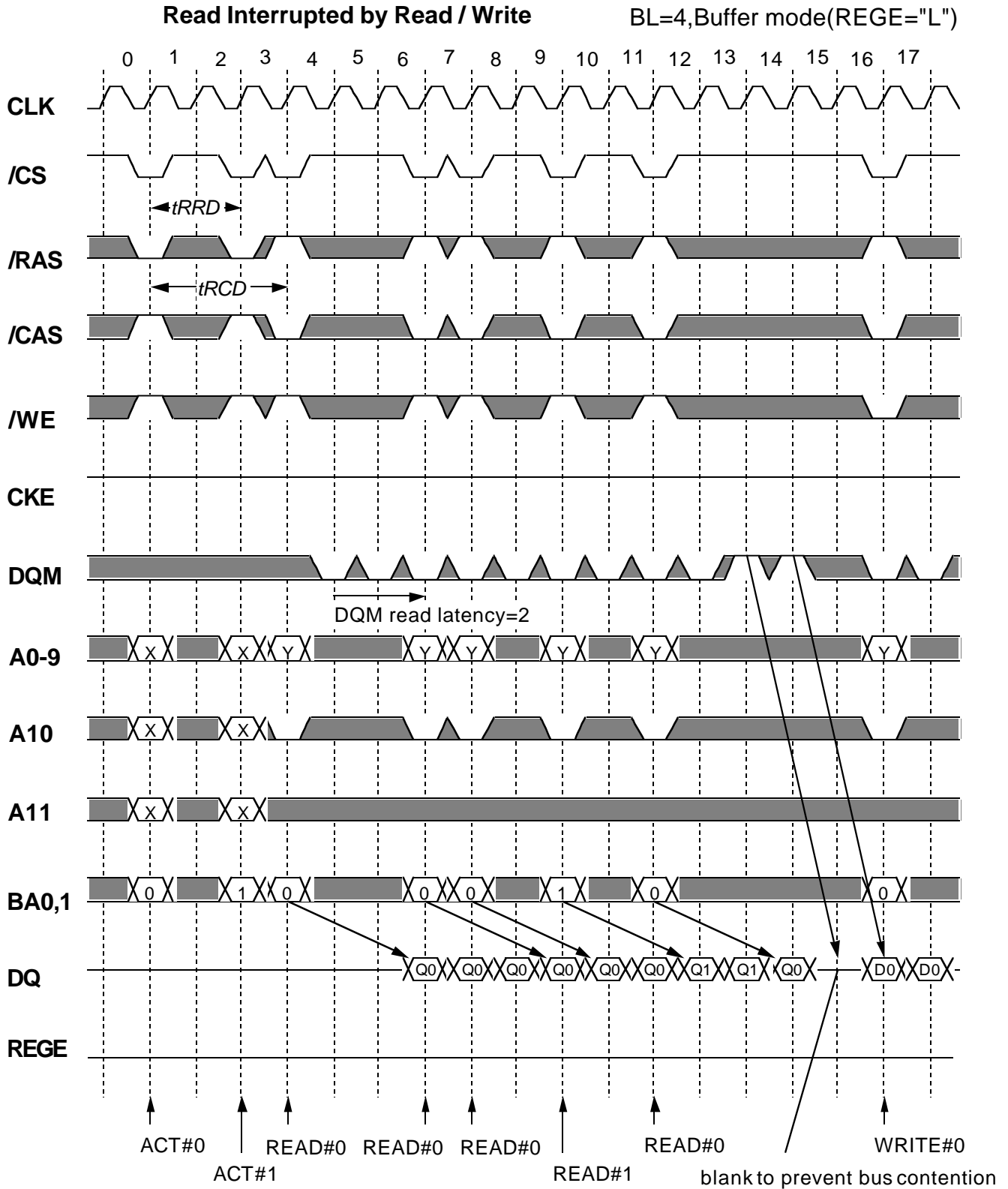
Burst Write can be interrupted by Write or Read of any active bank.

Italic parameter indicates minimum case

Preliminary Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM



Burst Read can be interrupted by Read or Write of any active bank.

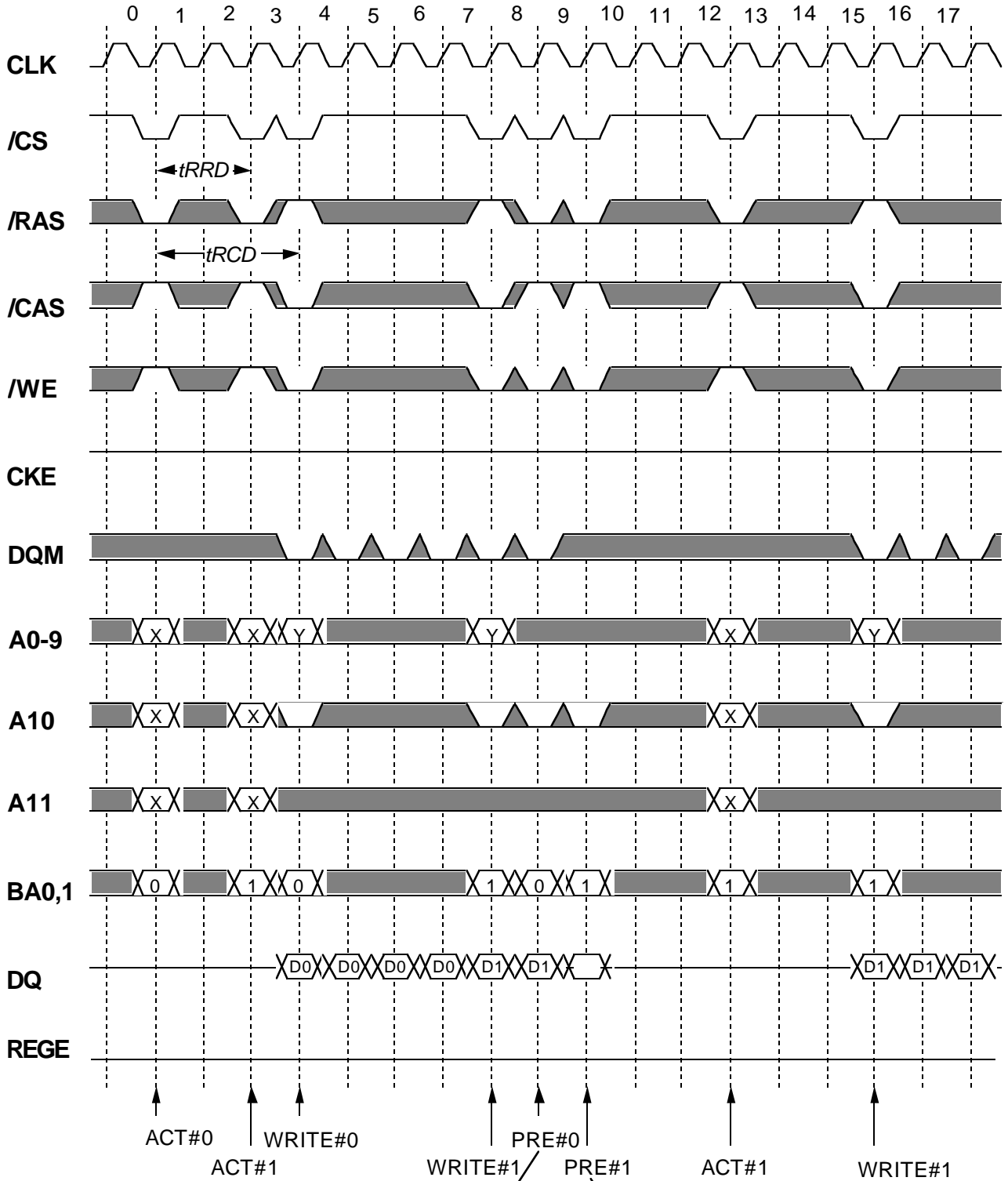
Italic parameter indicates minimum case

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Write Interrupted by Precharge

BL=4, Buffer mode (REGE="L")



Burst Write is not interrupted by Precharge of the other bank.

Burst Write is interrupted by Precharge of the same bank.

Italic parameter indicates minimum case

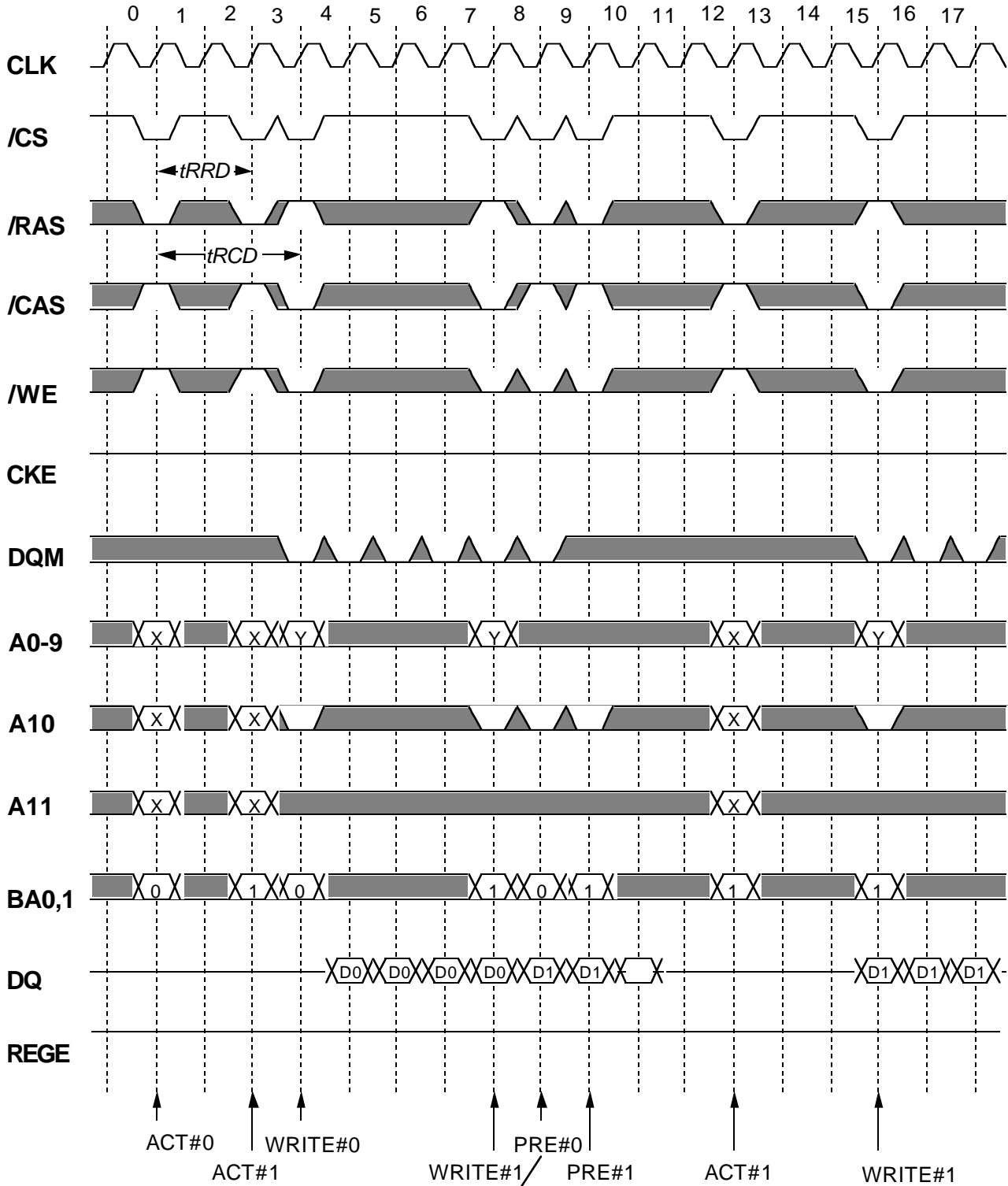
Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Write Interrupted by Precharge

BL=4, Latch mode (REGE="H")



Burst Write is not interrupted by Precharge of the other bank.

Burst Write is interrupted by Precharge of the same bank.

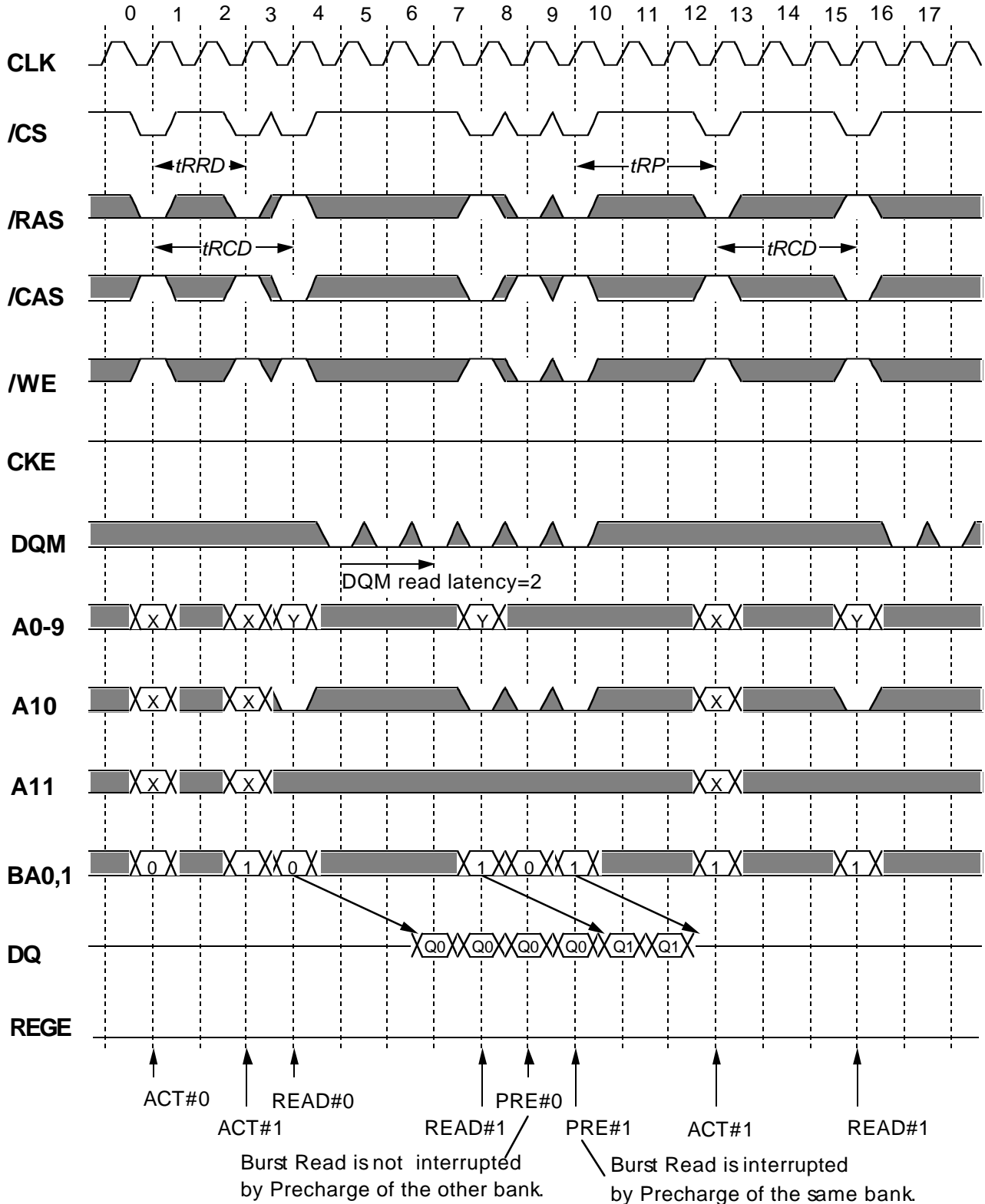
Italic parameter indicates minimum case

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Read Interrupted by Precharge

BL=4, Buffer mode (REGE="L")



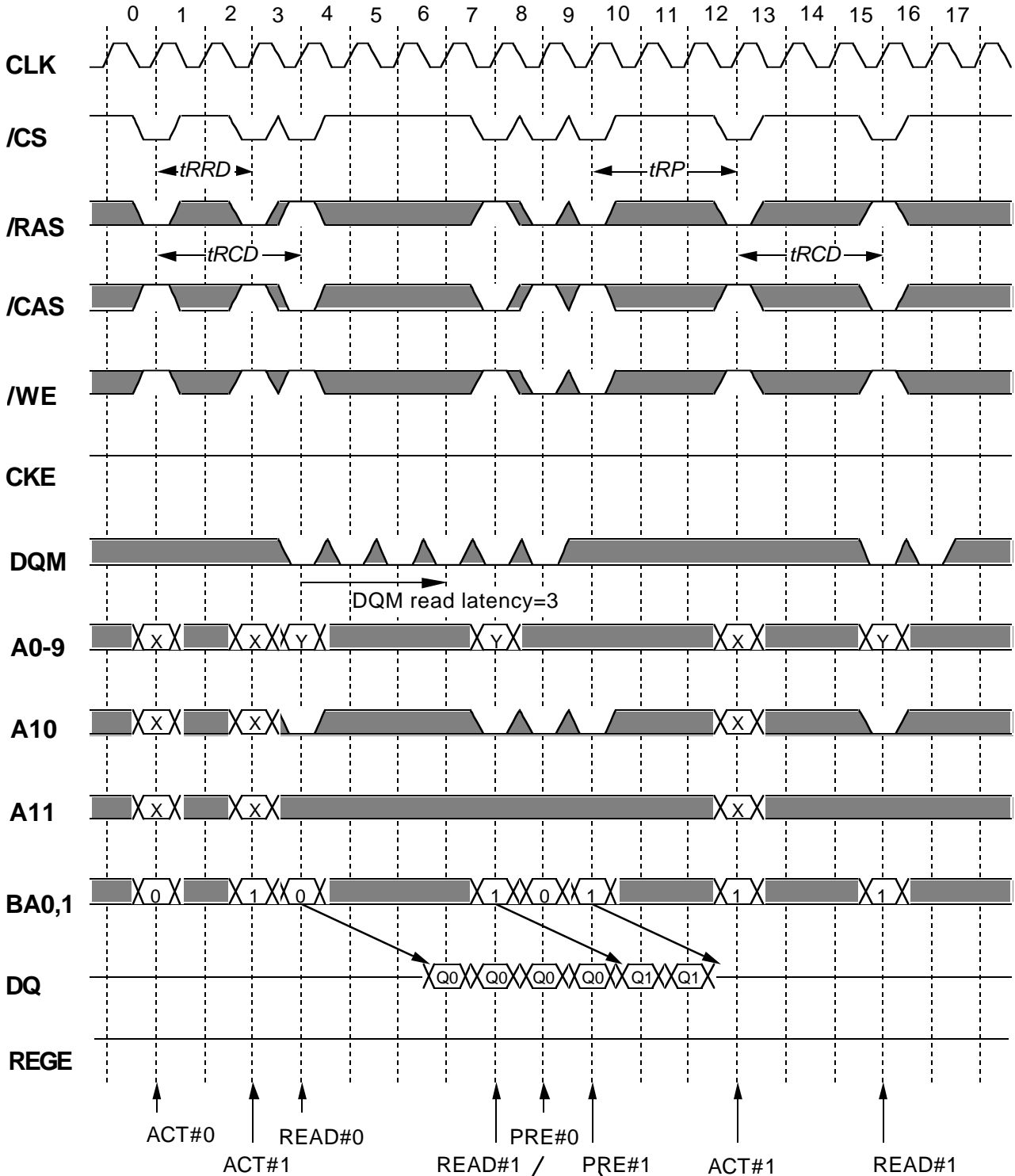
Italic parameter indicates minimum case

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Read Interrupted by Precharge

BL=4, Latch mode (REGE="H")



Burst Read is not interrupted by Precharge of the other bank.

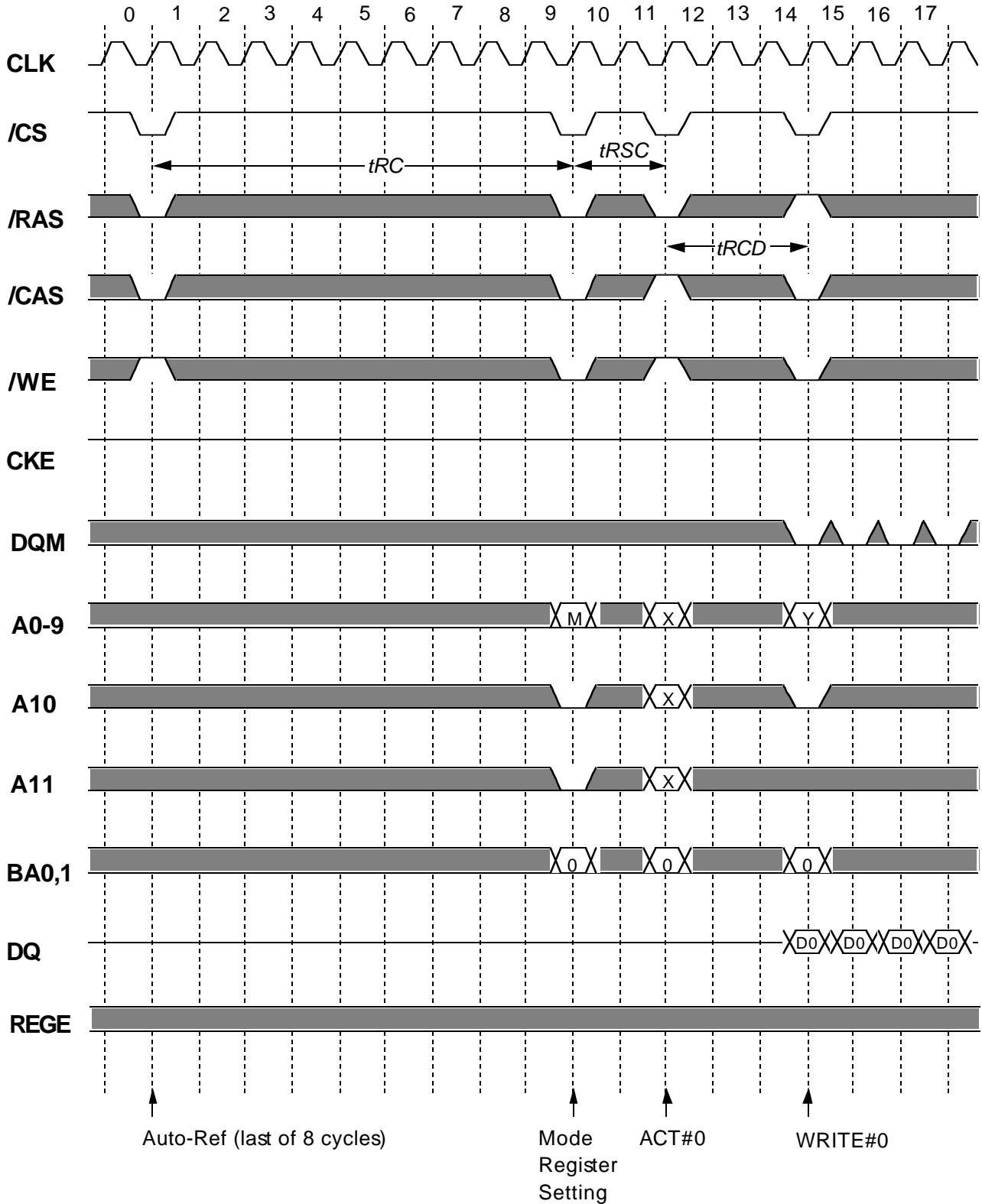
Burst Read is interrupted by Precharge of the same bank.

Italic parameter indicates minimum case

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Mode Register Setting

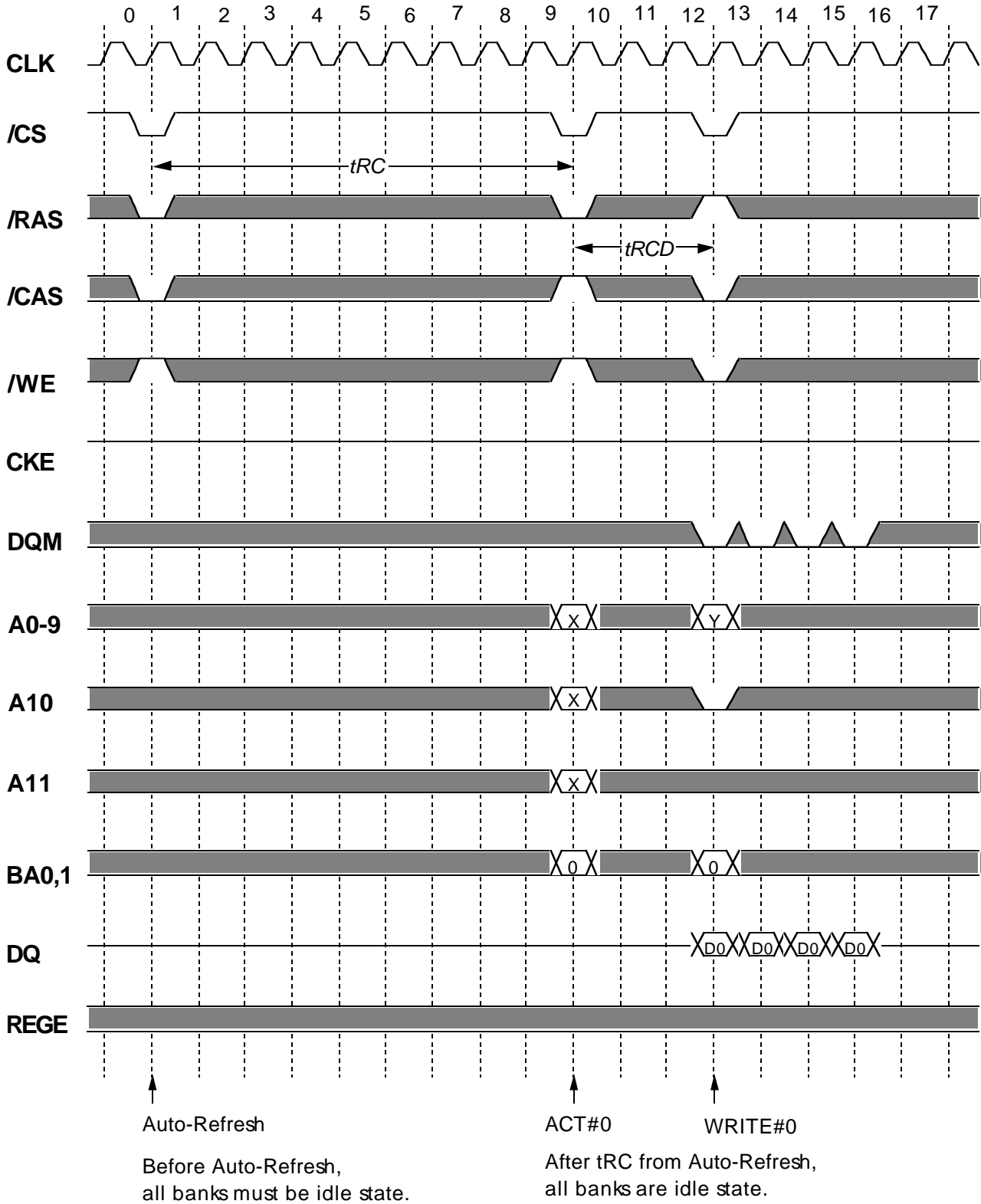


Italic parameter indicates minimum case

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Auto-Refresh @BL=4

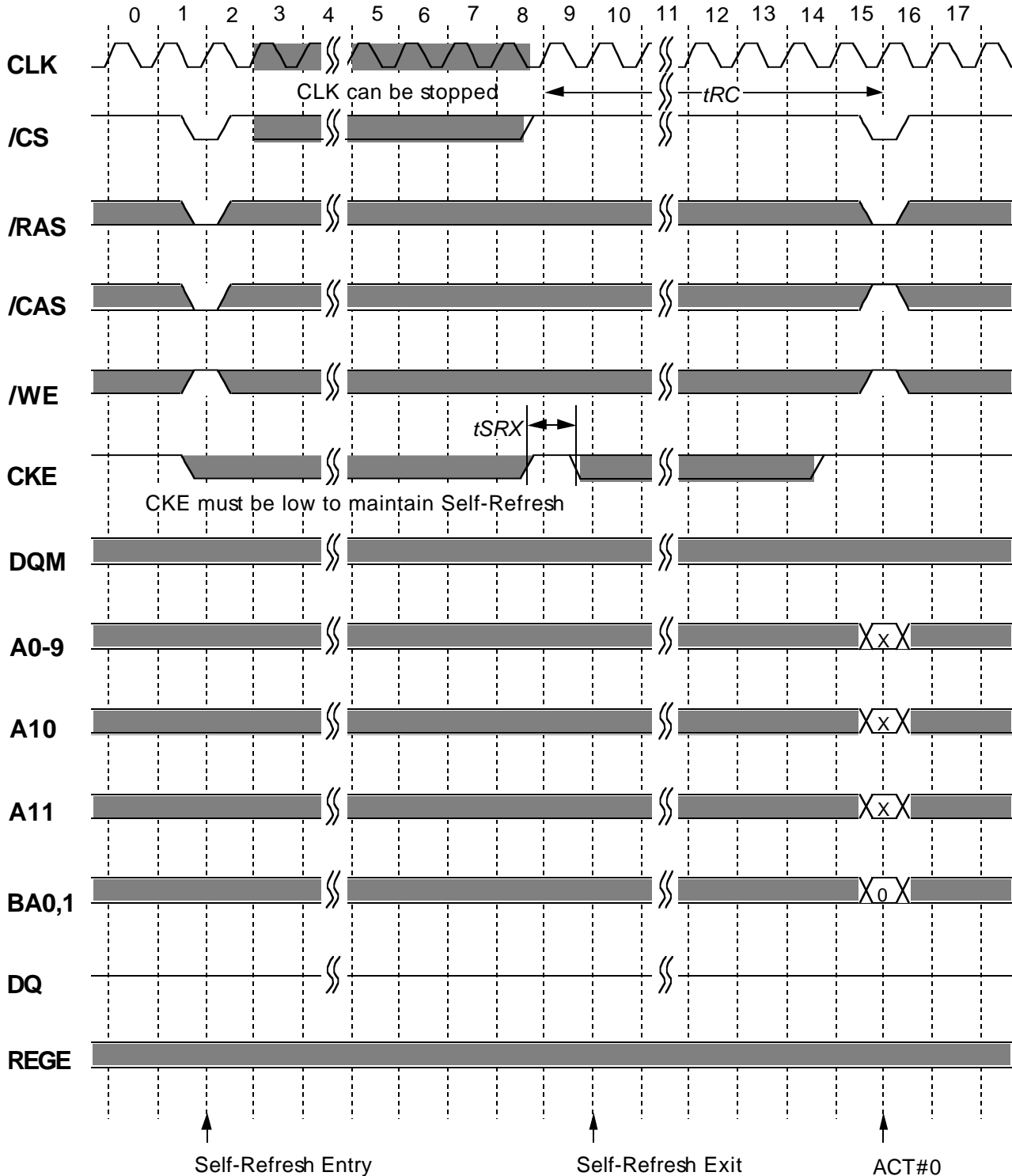


Italic parameter indicates minimum case

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Self-Refresh



Before Self-Refresh Entry,
all banks must be idle state.

After t_{RC} from Self-Refresh Exit,
all banks are idle state.

Italic parameter indicates minimum case

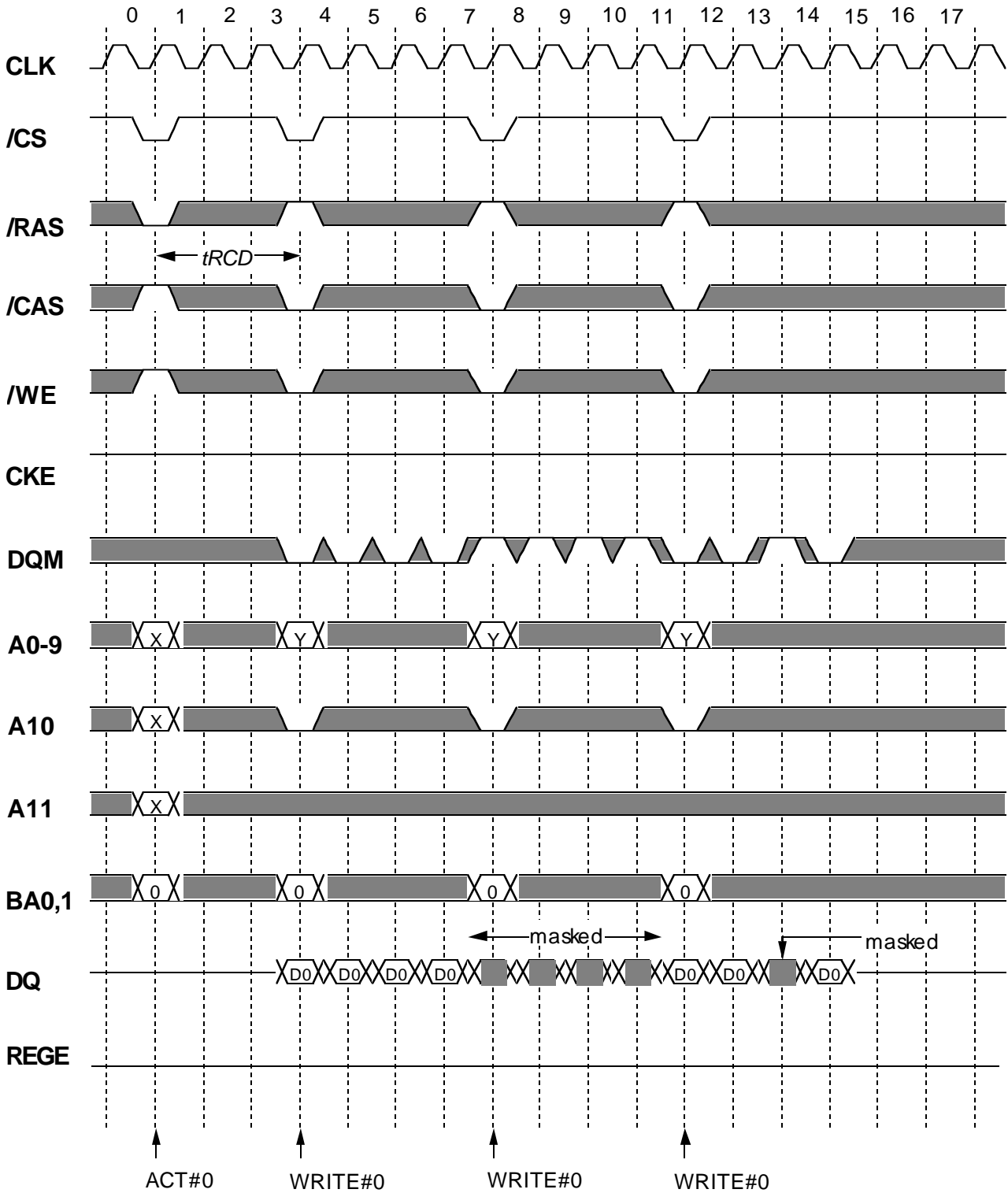
Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

DQM Write Mask @BL=4

BL=4, Buffer mode (REGE="L")



Italic parameter indicates minimum case

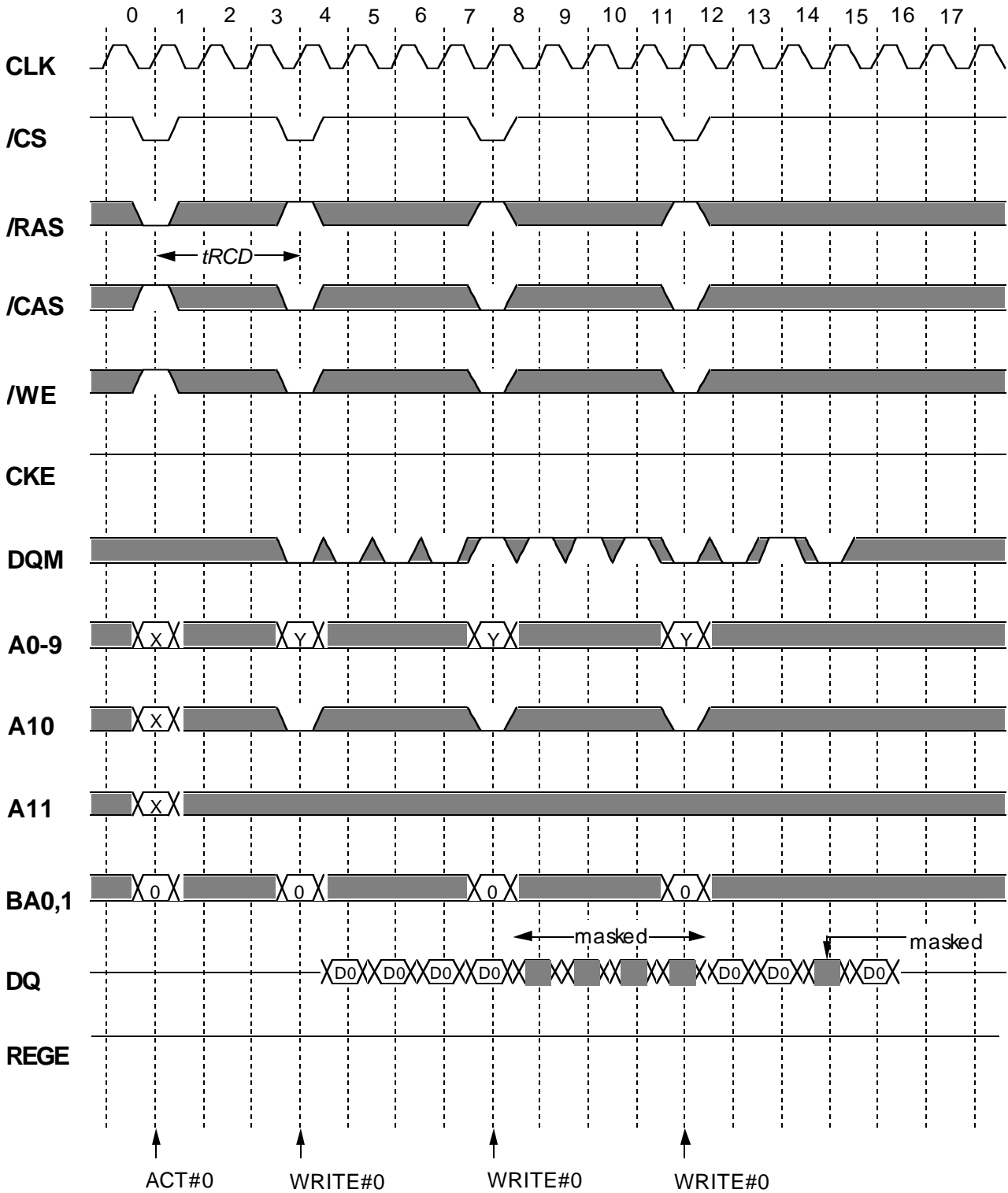
Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

DQM Write Mask @BL=4

BL=4, Latch mode (REGE="H")



Italic parameter indicates minimum case

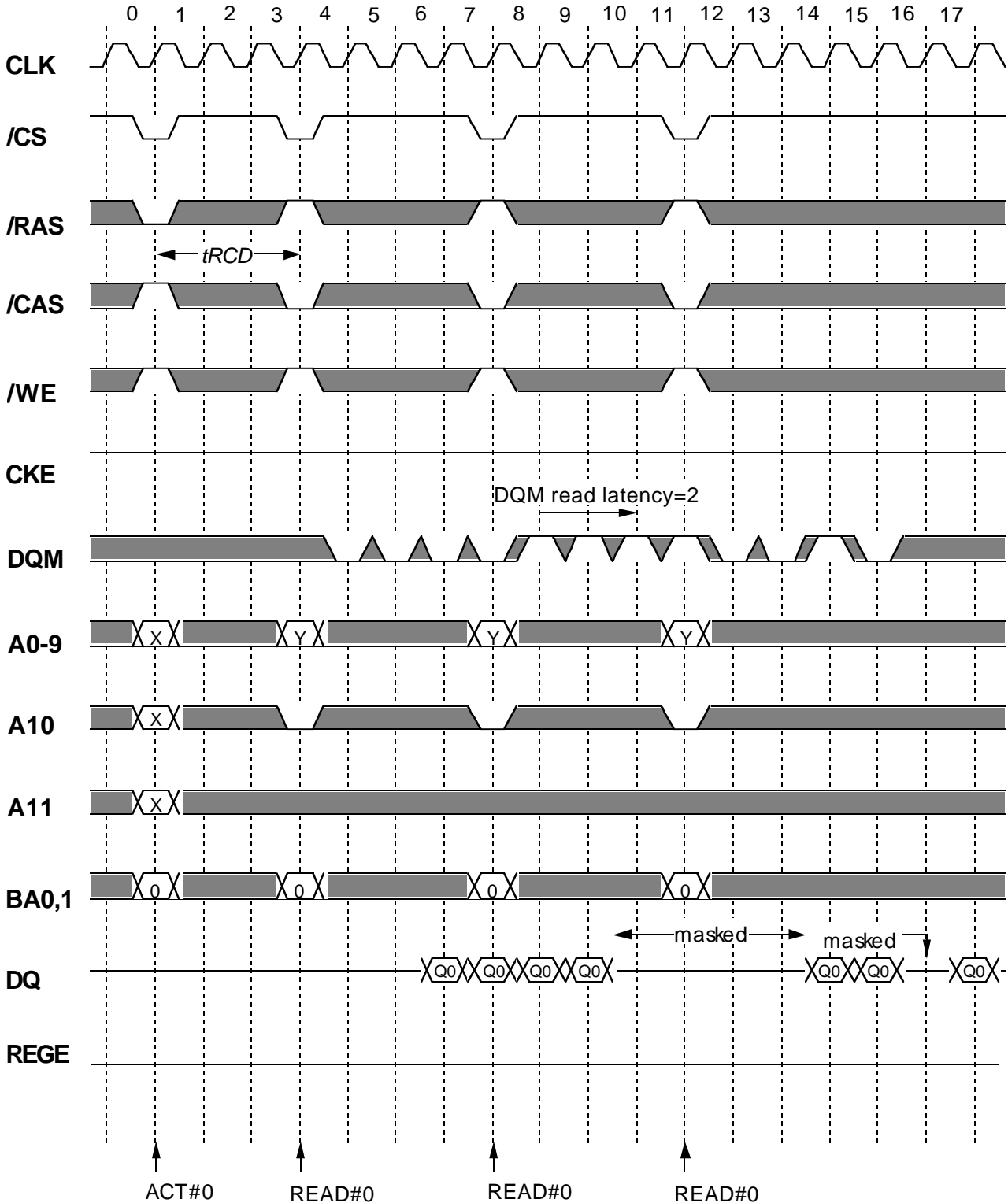
Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

DQM Read Mask @BL=4 CL=3

BL=4, Buffer mode (REGE="L")



Italic parameter indicates minimum case

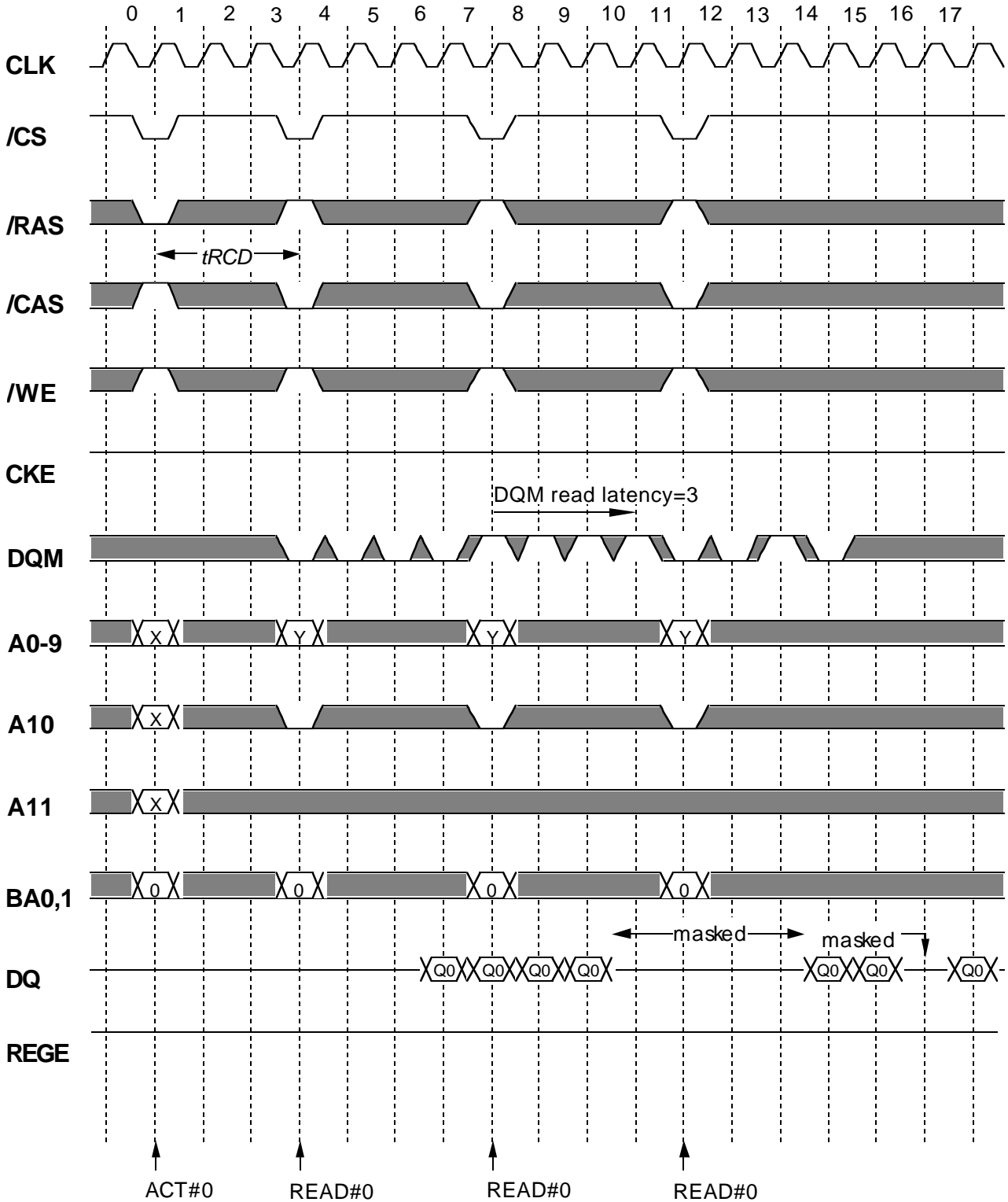
Preliminary Spec.

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2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

DQM Read Mask @BL=4 CL=3

BL=4,Latch mode(REGE="H")



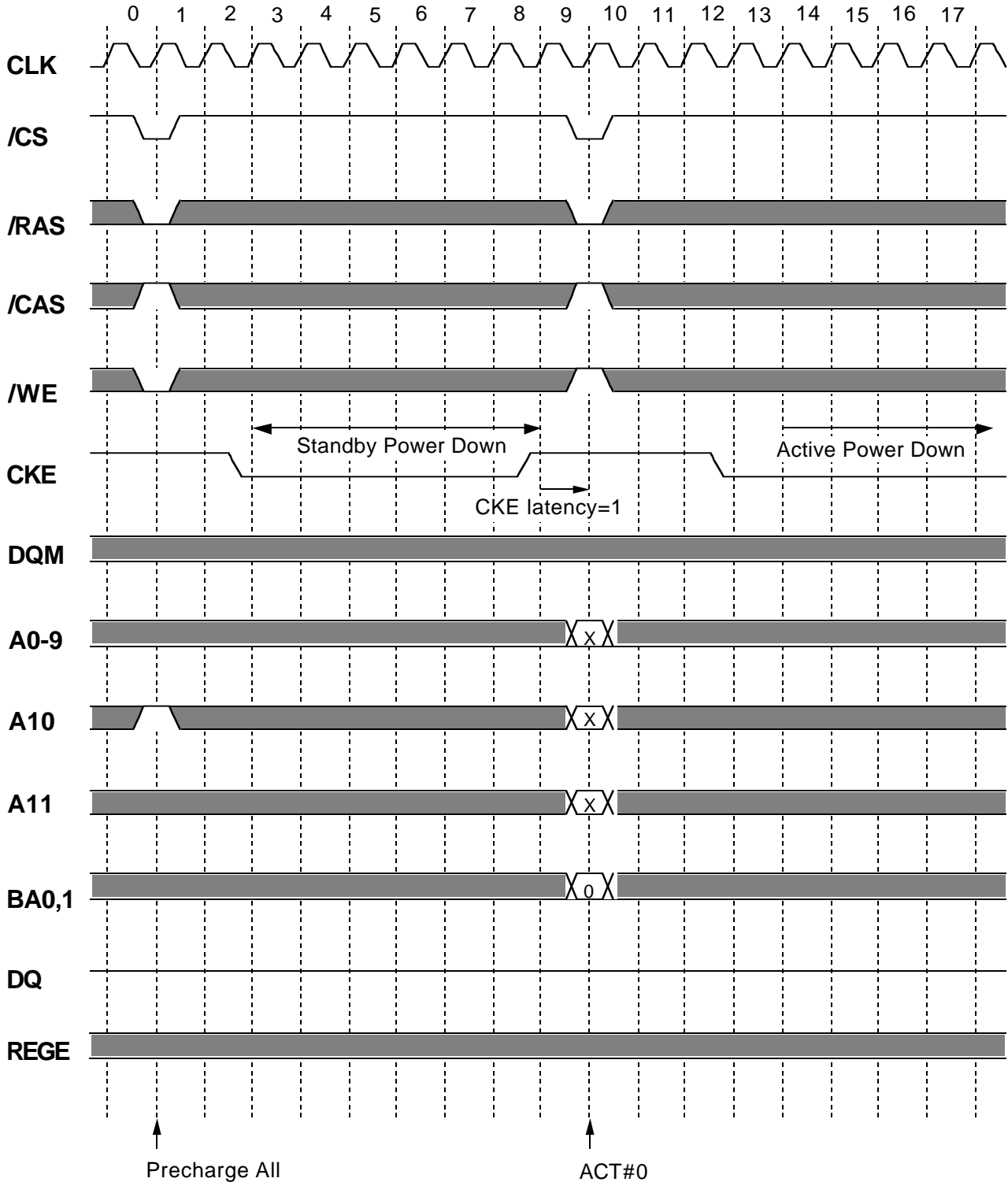
Italic parameter indicates minimum case

Preliminary
Spec.

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2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Power Down



Italic parameter indicates minimum case

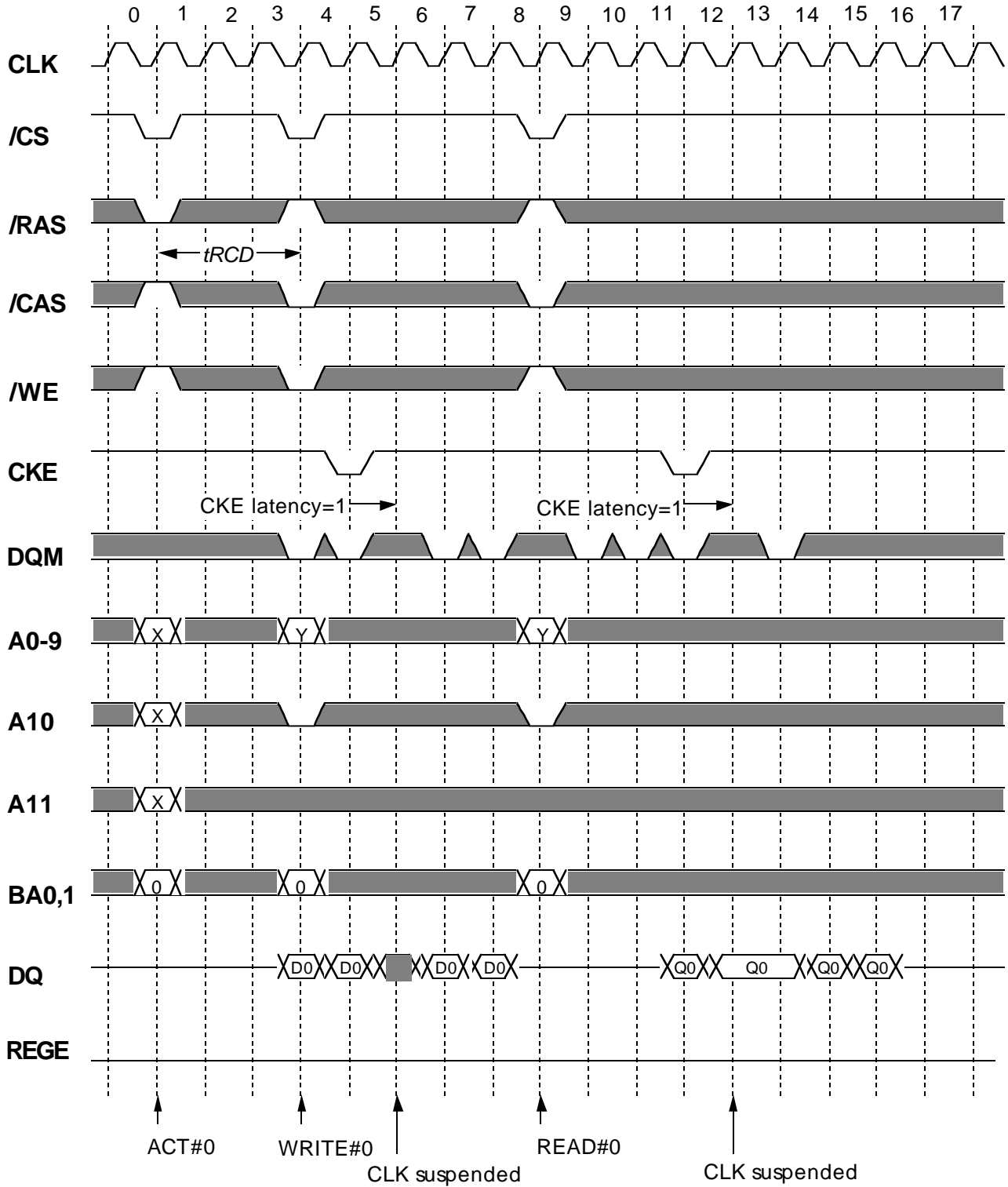
Preliminary
Spec.

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2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

CLK Suspend @BL=4 CL=3

BL=4, Buffer mode (REGE="L")



Italic parameter indicates minimum case

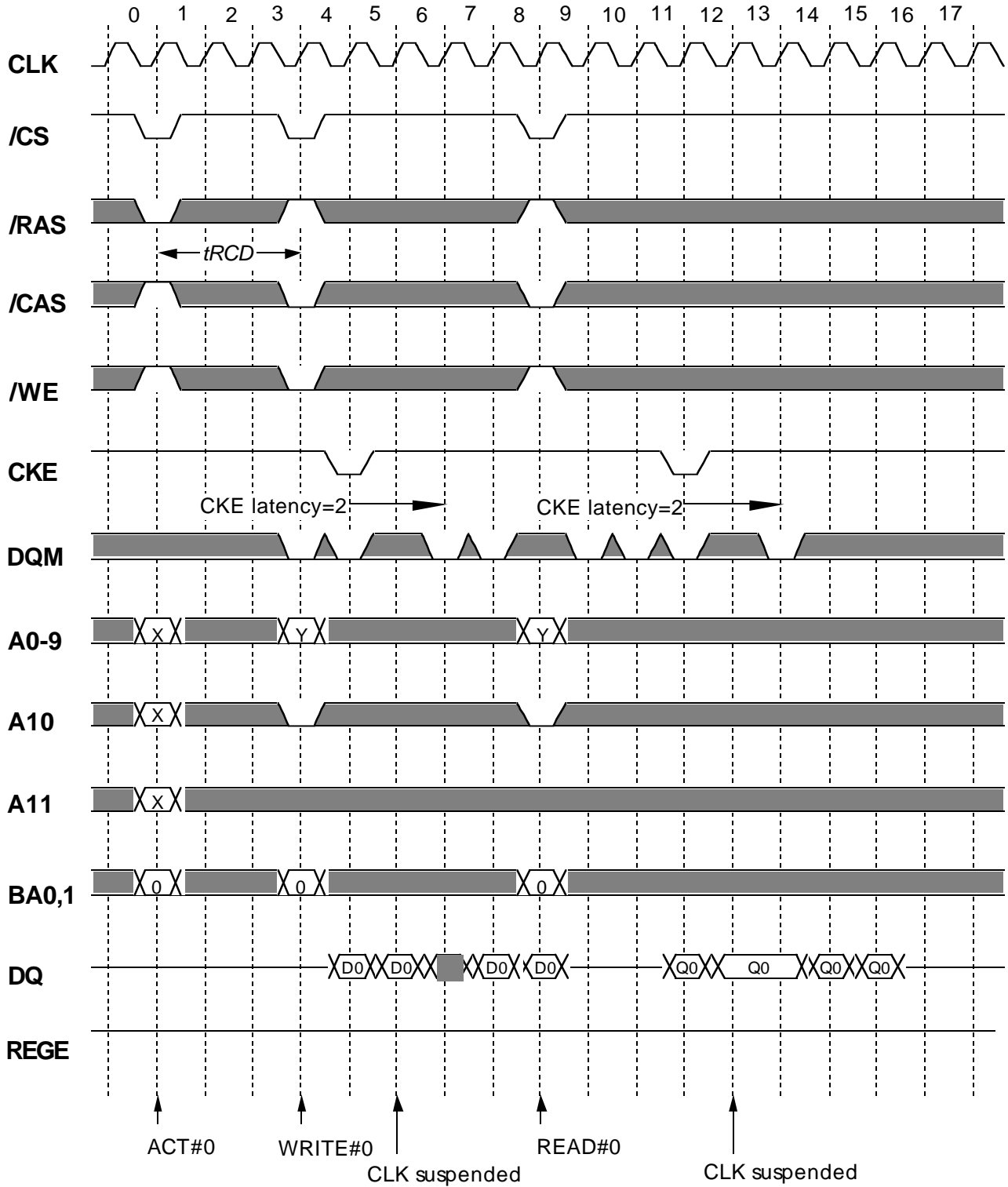
Preliminary
Spec.

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

CLK Suspend @BL=4 CL=3

BL=4, Latch mode (REGE="H")



Italic parameter indicates minimum case

Preliminary
Spec.

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2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Serial Presence Detect Table I

| Byte | Function described | SPD entry data | SPD DATA(hex) | |
|------|--|---|---------------|----|
| 0 | Defines # bytes written into serial memory at module mfgr | 128 | 80 | |
| 1 | Total # bytes of SPD memory device | 256 Bytes | 08 | |
| 2 | Fundamental memory type | SDRAM | 04 | |
| 3 | # Row Addresses on this assembly | A0-A11 | 0C | |
| 4 | # Column Addresses on this assembly | A0-A10 | 0B | |
| 5 | # Module Banks on this assembly | 1BANK | 01 | |
| 6 | Data Width of this assembly... | x72 | 48 | |
| 7 | ... Data Width continuation | 0 | 00 | |
| 8 | Voltage interface standard of this assembly | LVTTL | 01 | |
| 9 | SDRAM Cycletime at Max. Supported CAS Latency (CL). Cycle time for CL=3 | 10ns | A0 | |
| 10 | SDRAM Access from Clock tAC for CL=3 | 6ns | 60 | |
| 11 | DIMM Configuration type (Non-parity,Parity,ECC) | ECC | 02 | |
| 12 | Refresh Rate/Type | self refresh(15.625uS) | 80 | |
| 13 | SDRAM width,Primary DRAM | x4 | 04 | |
| 14 | Error Checking SDRAM data width | x4 | 04 | |
| 15 | Minimum Clock Delay,Back to Back Random Column Addresses | 1 | 01 | |
| 16 | Burst Lengths Supported | 1/2/4/8/Full page | 8F | |
| 17 | # Banks on Each SDRAM device | 4bank | 04 | |
| 18 | CAS# Latency | 2/3 | 06 | |
| 19 | CS# Latency | 0 | 01 | |
| 20 | Write Latency | 0 | 01 | |
| 21 | SDRAM Module Attributes | buffered,registered | 1F | |
| 22 | SDRAM Device Attributes:General | Precharge All,Auto precharge Write1/Read Burst | 0E | |
| 23 | SDRAM Cycle time(2nd highest CAS latency) Cycle time for CL=2 | -7 | 10ns | A0 |
| | | -8 | 13ns | D0 |
| 24 | SDRAM Access form Clock(2nd highest CAS latency) tAC for CL=2 | -7 | 6ns | 60 |
| | | -8 | 7ns | 70 |
| 25 | SDRAM Cycle time(3rd highest CAS latency) | N/A | 00 | |
| 26 | SDRAM Access form Clock(3rd highest CAS latency) | N/A | 00 | |
| 27 | Precharge to Active Minimum | 20ns | 14 | |
| 28 | Row Active to Row Active Min. | 20ns | 14 | |
| 29 | RAS to CAS Delay Min | 20ns | 14 | |
| 30 | Active to Precharge Min | 50ns | 32 | |

Preliminary
Spec.

MITSUBISHI LSIs

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

Serial Presence Detect Table II

| | | | |
|--------|--|------------------|------------------------------------|
| 31 | Density of each bank on module | 256MByte | 40 |
| 32 | Command and Address signal input setup time | 2ns | 20 |
| 33 | Command and Address signal input hold time | 1ns | 10 |
| 34 | Data signal input setup time | 2ns | 20 |
| 35 | Data signal input hold time | 1ns | 10 |
| 36-61 | Superset Information (may be used in future) | option | 00 |
| 62 | SPD Revision | rev 1.2A | 12 |
| 63 | Checksum for bytes 0-62 | Check sum for -7 | 60 |
| | | Check sum for -8 | A0 |
| 64-71 | Manufactures Jedec ID code per JEP-108E | MITSUBISHI | 1CFFFFFFFFFFFFFF |
| 72 | Manufacturing location | Miyoshi,Japan | 01 |
| | | Tajima,Japan | 02 |
| | | NC,USA | 03 |
| | | Germany | 04 |
| 73-90 | Manufactures Part Number | MH32S72QJA-7 | 4D483332533732514A412D372020202020 |
| | | MH32S72QJA-8 | 4D483332533732514A412D382020202020 |
| 91-92 | Revision Code | PCB revision | rrrr |
| 93-94 | Manufacturing date | year/week code | yyww |
| 95-98 | Assembly Serial Number | serial number | sssssss |
| 99-125 | Manufacture Specific Data | option | 00 |
| 126 | Intel specification frequency | 100MHz | 64 |
| 127 | Intel specification CAS# Latency support | -7 CL=2/3,AP,CK0 | 8F |
| | | -8 CL=3,AP,CK0 | 8D |
| 128+ | Unused storage locations | open | 00 |

MH32S72QJA-7, -8

2415919104-BIT (33554432-WORD BY 72-BIT) Synchronous DYNAMIC RAM

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