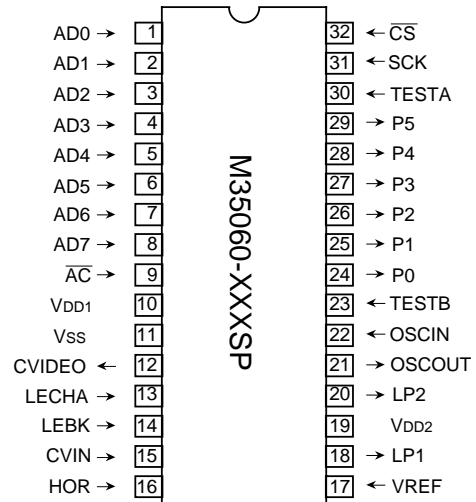## DESCRIPTION

M35060-XXXSP is CATV screen display control IC which can display 40 (horizontal) ✕ 16 (vertical). It has built-in SYRAM which can be used with character ROM.

It uses a silicon gate CMOS process and it housed in a small 32-pin shrink DIP package. For M35060-001SP and M35060-002SP that are standard ROM versions of M35060-XXXSP, the character patterns are also mentioned.

FEATURES

- Screen composition .... 40 characters ✕ 16 lines
- Number of characters displayed .... 680 (Max.)
- Character composition .... 12 ✕ 13 dot matrix
- Characters available   character ROM .... 256 characters
                           SYRAM .... 63 characters
- Character sizes available   horizontal .... 2 (once, twice)
                              vertical .... 2 (once, twice)
                              setting by every line
- Display locations available
    Horizontal direction .... 480 locations
    Vertical direction .... 235 locations
- Blinking .... character units
    Cycle .... approximately 1 second, or approximately 0.5 seconds
    Duty .... 25%, 50% or 75%
- Data input .... 8-bit parallel ✕ 3
- Coloring   Character coloring .... 8 colors choices per character
             Background coloring ..... 8 colors choices per character
             Raster coloring .... 8 colors choices per screen
- Blanking   Character size blanking
                                    Border size blanking
                                    Matrix-outline
                                    Halftone blanking
                                    Can be set by every line
- General-purpose output ports   Combined port output 6
                                   (switching to RGB output)
- RAM erase .... Display RAM erasing by every line
                                   SYRAM erasing separately
- Scrolling .... Bit by bit smooth scroll implemented by software
- Composite synchronizating signal generation .... Built-in
                                   (PAL, NTSC, M-PAL)
- Display oscillation circuit .... Built-in
- Synchronous separation circuit .... Built-in
- Synchronous correction circuit .... Built-in

PIN CONFIGURATION (TOP VIEW)

Pin	Signal		Pin	Signal
1	AD0 →		32	← $\overline{CS}$
2	AD1 →		31	← SCK
3	AD2 →		30	← TESTA
4	AD3 →		29	→ P5
5	AD4 →		28	→ P4
6	AD5 →		27	→ P3
7	AD6 →		26	→ P2
8	AD7 →		25	→ P1
9	$\overline{AC}$ →		24	→ P0
10	V$_{DD1}$		23	← TESTB
11	V$_{SS}$		22	← OSCIN
12	CVIDEO ←		21	→ OSCOUT
13	LECHA →		20	→ LP2
14	LEBK →		19	V$_{DD2}$
15	CVIN →		18	→ LP1
16	HOR →		17	← VREF

M35060-XXXSP

Outline 32P4B

MITSUBISHI ELECTRIC

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

PIN DESCRIPTION

Symbol	Pin name	Input/Output	Function
AD0~AD7	Parallel data input	Input	These input pins determine address and data of the Display RAM, Control RAM, and Overlay RAM (SYRAM) by 8-bit parallel. Hysteresis input is required.
$\overline{AC}$	Auto-clear input	Input	When this input pin transitions from "H" to "L", the device is reset. Built-in a pull-up resistor. Hysteresis input is required.
V_{DD1}	Power pin	—	Digital power supply pin. This pin must be connected to + 5V.
V_{SS}	Earthing pin	—	Ground pin. This pin must be connected to 0V.
CVIDEO	Composite video signal output	Output	This pin outputs the composite video signal. The output signal is 2Vp-p. In superimpose mode, this pin's signal consists of the OSD signal combined with the input composite signal CVIN.
LECHA	Character level input	Input	This input pin is used for controlling the "white" character color level of the OSD signal.
LEBK	Black level input	Input	This input pin is used for controlling the "black" character color level of the OSD signal.
CVIN	Composite video signal input	Input	This input pin is used for the superimpose mode. An external composite signal may be input through this pin and mixed with the internally generated OSD signal.
HOR	Synchronous signal input	Input	This input pin is used to input the same signal as CVIN. The horizontal and vertical sync signals are then extracted internally within the device.
VREF	Slice level input	Input	This input pin is used to determine the slice voltage for extracting the sync signals from the video composite signal.
LP1	Filter output 1	Output	This is filter output pin 1.
V_{DD2}	Power pin	—	Analog power supply pin. This pin must be connected to +5V.
LP2	Filter output 2	Output	This is filter output pin 2.
OSCOUT	The pins for attaching an external oscillator circuit for generating the synchronization signal.	Output	These are the pins for attaching an external oscillator circuit for generating the synchronization signal:
OSCIN		Input	NTSC (3.580MHz), PAL (4.434MHz), M-PAL (3.576MHz).
TESTB	Test input	Input	Factory test pin. The pin must be connected to GND.
P0	Port output	Output	This output pin can be configured to port P0 or YM output.
P1	Port output	Output	This output pin can be configured to port P1 or BLNK output.
P2	Port output	Output	This output pin can be configured to port P2 or B output.
P3	Port output	Output	This output pin can be configured to port P3 or G output.
P4	Port output	Output	This output pin can be configured to port P4 or R output.
P5	Port output	Output	This output pin can be configured to port P5 or CSYN output.
TESTA	Test input	Input	Factory test pin. The pin must be connected to GND.
SCK	Clock input for data input	Input	This pin is enabled when the $\overline{CS}$ pin is "L". Data input to pins AD0~AD7 is latched at the rising edge of this signal. This pin is hysteresis input.
$\overline{CS}$	Chip select input	Input	This is chip selection input pin. When this pin is "L", transmission is enabled. This pin is hysteresis input.

MITSUBISHI ELECTRIC

BLOCK DIAGRAM
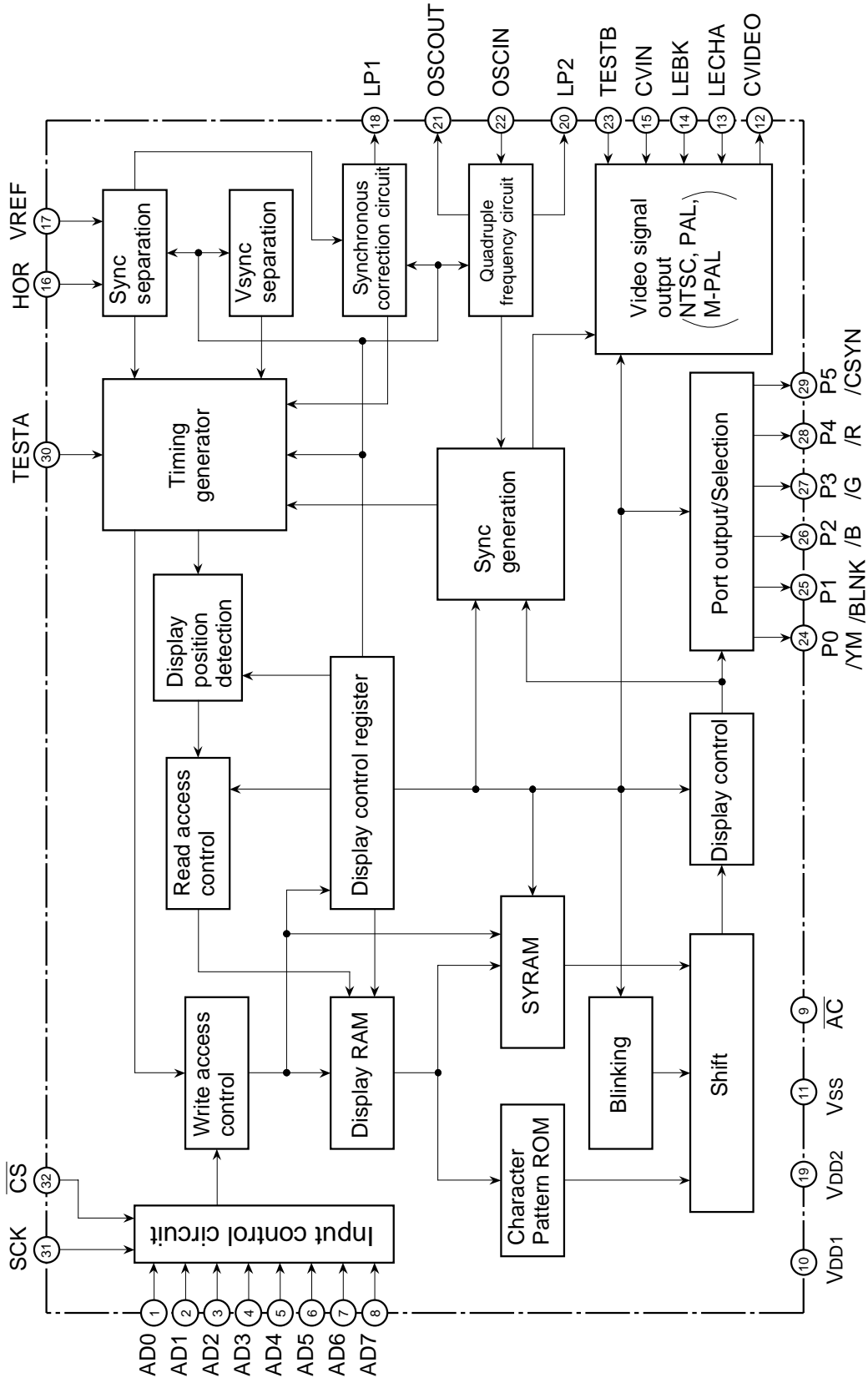
MEMORY CONSTRUCTION

Address 000_{16} to $2A7_{16}$ are assigned to the display RAM, $2A8_{16}$ to $2B0_{16}$ are assigned to the display control registers and 300_{16} to $6EC_{16}$ are assigned to SYRAM.

The internal circuit is reset and all display control registers (address $2A8_{16}$ to $2B0_{16}$) are set to "0". The memory constitution of display RAM and register is shown in Figure 1 and the memory constitution of SYRAM is shown in Figure 2.

Table 1 The memory constitution of display RAM and register

address	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
000_{16}	SB	SG	SR	SYC5	SYC4	SYC3	SYC2	SYC1	SYC0	BB	BG	BR	BLINK	CB	CG	CR	C7	C6	C5	C4	C3	C2	C1	C0
ℓ	SY color setting			SYRAM setting						Raster color setting			BLINK	Character color setting			Character setting							
$2A7_{16}$	SB	SG	SR	SYC5	SYC4	SYC3	SYC2	SYC1	SYC0	BB	BG	BR	BLINK	CB	CG	CR	C7	C6	C5	C4	C3	C2	C1	C0
$2A8_{16}$	–	TEST3	TEST2	TEST1	TEST0	TEST11	TEST10	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
$2A9_{16}$	–	–	–	BLINK3	BLINK2	BLINK1	BLINK0	HSZ16	HSZ15	HSZ14	HSZ13	HSZ12	HSZ11	HSZ10	HSZ9	HSZ8	HSZ7	HSZ6	HSZ5	HSZ4	HSZ3	HSZ2	HSZ1	HSZ0
$2AA_{16}$	–	–	–	TEST12	EQP	TEST20	HIDE	VSZ16	VSZ15	VSZ14	VSZ13	VSZ12	VSZ11	VSZ10	VSZ9	VSZ8	VSZ7	VSZ6	VSZ5	VSZ4	VSZ3	VSZ2	VSZ1	VSZ0
$2AB_{16}$	–	–	TEST26	TEST25	PHASE2	PHASE1	PHASE0	DSP016	DSP015	DSP014	DSP013	DSP012	DSP011	DSP010	DSP009	DSP008	DSP007	DSP006	DSP005	DSP004	DSP003	DSP002	DSP001	DSP000
$2AC_{16}$	–	–	–	TEST21	LINEB	LINEG	LINER	DSP116	DSP115	DSP114	DSP113	DSP112	DSP111	DSP110	DSP109	DSP108	DSP107	DSP106	DSP105	DSP104	DSP103	DSP102	DSP101	DSP100
$2AD_{16}$	–	TEST23	TEST22	SERS3	SERS2	SERS1	SERS0	ERS16	ERS15	ERS14	ERS13	ERS12	ERS11	ERS10	ERS9	ERS8	ERS7	ERS6	ERS5	ERS4	ERS3	ERS2	ERS1	ERS0
$2AE_{16}$	–	–	–	–	–	SEND4	SEND3	SEND2	SEND1	SEND0	SST4	SST3	SST2	SST1	SST0	SLIN4	SLIN3	SLIN2	SLIN1	SLIN0	SBIT3	SBIT2	SBIT1	SBIT0
$2AF_{16}$	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	ALL24	SRAND2	SRAND1	SRAND0	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0
$2B0_{16}$	–	TEST19	TEST18	TEST17	TEST24	LEVEL2	LEVEL1	LEVEL0	$\overline{\text{INT}}$ NON	$\overline{\text{PAL}}$ NTSC	MPAL	PALH	TEST16	TEST15	SEPV1	SEPV0	BLK	–	DSPONV	DSPON	–	SELCOR	–	EX

TEST_n (n = number) is MITSUBISHI test memory. Set 0 to all bits.

Table 2 The memory constitution of SYRAM

address	DA17 ~ DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	SYRAM code
300_{16} ℓ $30C_{16}$	0	SYEX ⋮ SYEX	S00B ⋮ S00B	S00A ⋮ S00A	S009 ⋮ S009	S008 ⋮ S008	S007 ⋮ S007	S006 ⋮ S006	S005 ⋮ S005	S004 ⋮ S004	S003 ⋮ S003	S002 ⋮ S002	S001 ⋮ S001	S000 ⋮ S000	00_{16}
310_{16} ℓ $31C_{16}$	0	SYEX ⋮ SYEX	S01B ⋮ S01B	S01A ⋮ S01A	S019 ⋮ S019	S018 ⋮ S018	S017 ⋮ S017	S016 ⋮ S016	S015 ⋮ S015	S014 ⋮ S014	S013 ⋮ S013	S012 ⋮ S012	S011 ⋮ S011	S010 ⋮ S010	01_{16}
ℓ	⋮	⋮						ℓ							ℓ
$6D0_{16}$ ℓ $6DC_{16}$	0	SYEX ⋮ SYEX	S3DB ⋮ S3DB	S3DA ⋮ S3DA	S3D9 ⋮ S3D9	S3D8 ⋮ S3D8	S3D7 ⋮ S3D7	S3D6 ⋮ S3D6	S3D5 ⋮ S3D5	S3D4 ⋮ S3D4	S3D3 ⋮ S3D3	S3D2 ⋮ S3D2	S3D1 ⋮ S3D1	S3D0 ⋮ S3D0	$3D_{16}$
$6E0_{16}$ ℓ $6EC_{16}$	0	SYEX ⋮ SYEX	S3EB ⋮ S3EB	S3EA ⋮ S3EA	S3E9 ⋮ S3E9	S3E8 ⋮ S3E8	S3E7 ⋮ S3E7	S3E6 ⋮ S3E6	S3E5 ⋮ S3E5	S3E4 ⋮ S3E4	S3E3 ⋮ S3E3	S3E2 ⋮ S3E2	S3E1 ⋮ S3E1	S3E0 ⋮ S3E0	$3E_{16}$

ℓ : Name or value changes by definite ratio.

⋮ : The same name or value continues.

MITSUBISHI ELECTRIC

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM.

The screen constitution is shown in Figure 1.

The hexadecimal numbers in the boxes show the display RAM address

Fig. 1   Screen constitution

REGISTERS DESCRIPTION

(1) Address $2A8_{16}$

DA	Register	Status	Function	Remarks
0	VP0	0 / 1	If VS is the vertical display start location,	The vertical start location is specified using the 8 bits from VP7 to VP0. VP7 to VP0 < 14_{16} are not available.
1	VP1	0 / 1	$VS = H \times \left(\sum_{n=0}^{7} 2^n VP_n \right)$	
2	VP2	0 / 1	H: Cycle with the horizontal synchronizing pulse	
3	VP3	0 / 1		
4	VP4	0 / 1		
5	VP5	0 / 1		
6	VP6	0 / 1		
7	VP7	0 / 1		
8	HP0	0 / 1	If HS is the horizontal display start location,	The horizontal start location is specified using the 9 bits from HP8 to HP0. HP8 to HP0 < 19_{16} are not available.
9	HP1	0 / 1	$HS = T \times \left(\sum_{n=0}^{8} 2^n HP_n + 9 \right)$	
A	HP2	0 / 1	T: Cycle with the display clock	
B	HP3	0 / 1		
C	HP4	0 / 1		
D	HP5	0 / 1		
E	HP6	0 / 1		
F	HP7	0 / 1		
10	HP8	0 / 1		
11	TEST10	0 / 1	Test mode (Must be cleared to 0.)	
12	TEST11	0 / 1		
13	TEST0	0 / 1		
14	TEST1	0 / 1		
15	TEST2	0 / 1		
16	TEST3	0 / 1		
17	—	0 / 1	Must be cleared to 0.	

HOR

TV screen

VS

HS

VERT

Character displaying area

1 bit weights 1 clock.

Note: The mark ◯ around the status value means the reset status by the "L" level is input to AC pin.

MITSUBISHI ELECTRIC

(2) Address 2A9$_{16}$

DA	Register	Status	Contents / Function		Remarks
0	HSZ0	0 / 1			Set to line 0 of display RAM
1	HSZ1	0 / 1			Set to line 1 of display RAM
2	HSZ2	0 / 1			Set to line 2 of display RAM
3	HSZ3	0 / 1			Set to line 3 of display RAM
4	HSZ4	0 / 1			Set to line 4 of display RAM
5	HSZ5	0 / 1			Set to line 5 of display RAM
6	HSZ6	0 / 1			Set to line 6 of display RAM
7	HSZ7	0 / 1			Set to line 7 of display RAM
8	HSZ8	0 / 1			Set to line 8 of display RAM
9	HSZ9	0 / 1			Set to line 9 of display RAM
A	HSZ10	0 / 1			Set to line 10 of display RAM
B	HSZ11	0 / 1			Set to line 11 of display RAM
C	HSZ12	0 / 1			Set to line 12 of display RAM
D	HSZ13	0 / 1			Set to line 13 of display RAM
E	HSZ14	0 / 1			Set to line 14 of display RAM
F	HSZ15	0 / 1			Set to line 15 of display RAM
10	HSZ16	0 / 1			Set to line 16 of display RAM
11	BLINK0	0 / 1			Blinking duty ratio can be altered.
12	BLINK1	0 / 1			
13	BLINK2	0	Cycle approximately 1 second.		Blinking cycle can be altered.
		1	Cycle approximately 0.5 second.		
14	BLINK3	0	Normal blinking		Character is in flashing state.
		1	Normal character, reversed character alternation display.		Character is always displayed (normal character, reversed character).
15	—	0 / 1	Must be cleared to 0.		
16	—	0 / 1			
17	—	0 / 1			

The Function column for HSZ registers shows:

HSZx	Horizontal direction character size
0	1T/dot
1	2T/dot

T: Display clock

The Function column for BLINK registers shows:

BLINK1 \ BLINK0	0	1
0	Blinking OFF	Duty 25%
1	Duty 50%	Duty 75%

(3) Address 2AA$_{16}$

DA	Register	Contents		Remarks
		Status	Function	
0	VSZ0	0		Set to line 0 of display RAM
		1		
1	VSZ1	0		Set to line 1 of display RAM
		1		
2	VSZ2	0		Set to line 2 of display RAM
		1		
3	VSZ3	0		Set to line 3 of display RAM
		1		
4	VSZ4	0		Set to line 4 of display RAM
		1		
5	VSZ5	0		Set to line 5 of display RAM
		1		
6	VSZ6	0		Set to line 6 of display RAM
		1		
7	VSZ7	0		Set to line 7 of display RAM
		1		
8	VSZ8	0		Set to line 8 of display RAM
		1		
9	VSZ9	0		Set to line 9 of display RAM
		1		
A	VSZ10	0		Set to line 10 of display RAM
		1		
B	VSZ11	0		Set to line 11 of display RAM
		1		
C	VSZ12	0		Set to line 12 of display RAM
		1		
D	VSZ13	0		Set to line 13 of display RAM
		1		
E	VSZ14	0		Set to line 14 of display RAM
		1		
F	VSZ15	0		Set to line 15 of display RAM
		1		
10	VSZ16	0		Set to line 16 of display RAM
		1		
11	HIDE	0	SYRAM writting over	Decided by register LINER, G and B or DAC bit of SYRAM.
		1	SYRAM writting over or character erasing	
12	TEST20	0	Test mode (Must be cleared to 0.)	
		1		
13	EQP	0	It does not include equivalent pulse.	
		1	It includes equivalent pulse.	
14	TEST12	0	Test mode (Must be cleared to 0.)	
		1		
15	—	0	Must be cleared to 0.	
		1		
16	—	0		
		1		
17	—	0		
		1		

Within the Function column (rows 0–10):

VSZx	Vertical direction character size
0	1H/dot
1	2H/dot

H: Horizontal synchronous pulse

MITSUBISHI ELECTRIC

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(4) Address 2AB$_{16}$

DA	Register	Status	Contents			Remarks
			Function			
0	DSP0 00	0				Set to line 0 of display RAM
		1	DSP0XX / DSP1XX	0	1	
1	DSP0 01	0				Set to line 1 of display RAM
		1	0	Character	Border	
2	DSP0 02	0				Set to line 2 of display RAM
		1	1	Matrix-outline	Halftone (Note)	
3	DSP0 03	0				Set to line 3 of display RAM
		1	Set by combination of DSP0XX (address 2AB$_{16}$ and DSP1XX) and DSP1XX (address 2AC$_{16}$).			
4	DSP0 04	0	At internal synchronous mode (EX = 1), display monitor signal area is all blanking signal (BLNK output) area.			Set to line 4 of display RAM
		1				
5	DSP0 05	0				Set to line 5 of display RAM
		1				
6	DSP0 06	0	Note: For halftone display, it is necessary to input the external composite video signal to the CVIN terminal, and externally connect a 100 to 200 resistor in series.			Set to line 6 of display RAM
		1				
7	DSP0 07	0	However, the halftone display is possible only with superimposed displays.			Set to line 7 of display RAM
		1				
8	DSP0 08	0				Set to line 8 of display RAM
		1				
9	DSP0 09	0				Set to line 9 of display RAM
		1				
A	DSP0 10	0				Set to line 10 of display RAM
		1				
B	DSP0 11	0				Set to line 11 of display RAM
		1				
C	DSP0 12	0				Set to line 12 of display RAM
		1				
D	DSP0 13	0				Set to line 13 of display RAM
		1				
E	DSP0 14	0				Set to line 14 of display RAM
		1				
F	DSP0 15	0				Set to line 15 of display RAM
		1				
10	DSP0 16	0				Set to line 16 of display RAM
		1				
11	PHASE 0	0	PHASE 2 / PHASE 1 / PHASE 0 / Color (SELCOR=0 / SELCOR=1)			Raster color setting.
		1	0 0 0 Black Black			
12	PHASE 1	0	0 0 1 Red Red–2			
		1	0 1 0 Green Green–2 / 0 1 1 Yellow Yellow			
13	PHASE 2	0	1 0 0 Blue Gray / 1 0 1 Magenta Yellow–2			
		1	1 1 0 Cyan Cyan / 1 1 1 White White			Refer Fig 3, 4 about phase angle.
14	TEST25	0	Test mode (Must be cleared to 0.)			
		1				
15	TEST26	0				
		1				
16	—	0	Must be cleared to 0.			
		1				
17	—	0				
		1				

(5) Address 2AC$_{16}$

DA	Register	Status	Contents / Function	Remarks
0	DSP1 00	0 / 1		Set to line 0 of display RAM
1	DSP1 01	0 / 1		Set to line 1 of display RAM
2	DSP1 02	0 / 1		Set to line 2 of display RAM
3	DSP1 03	0 / 1		Set to line 3 of display RAM
4	DSP1 04	0 / 1		Set to line 4 of display RAM
5	DSP1 05	0 / 1		Set to line 5 of display RAM
6	DSP1 06	0 / 1		Set to line 6 of display RAM
7	DSP1 07	0 / 1		Set to line 7 of display RAM
8	DSP1 08	0 / 1		Set to line 8 of display RAM
9	DSP1 09	0 / 1		Set to line 9 of display RAM
A	DSP1 10	0 / 1		Set to line 10 of display RAM
B	DSP1 11	0 / 1		Set to line 11 of display RAM
C	DSP1 12	0 / 1		Set to line 12 of display RAM
D	DSP1 13	0 / 1		Set to line 13 of display RAM
E	DSP1 14	0 / 1		Set to line 14 of display RAM
F	DSP1 15	0 / 1		Set to line 15 of display RAM
10	DSP1 16	0 / 1		Set to line 16 of display RAM
11	LINER	0 / 1		SYRAM color setting. Color is decided by DAC bit (SYEX) of SYRAM or HIDE register.
12	LINEG	0 / 1		
13	LINEB	0 / 1		Refer Fig. 3, 4 about phase angle.
14	TEST21	0 / 1	Test mode (Must be cleared to 0.)	
15	—	0 / 1		
16	—	0 / 1	Must be cleared to 0.	
17	—	0 / 1		

Function detail for DSP1 00–16 (combination table):

DSP1XX \ DSP0XX	0	1
0	Character	Border
1	Matrix-outline	Halftone (Note)

Set by combination of DSP0XX (address 2AB$_{16}$ and DSP1XX) and DSP1XX (address 2AC$_{16}$).
At internal synchronous mode (EX = 1), display monitor signal area is all blanking signal (BLNK output) area.

Note: For halftone display, it is necessary to input the external composite video signal to the CVIN terminal, and externally connect a 100 to 200 resistor in series.
However, the halftone display is possible only with superimposed displays.

Color table for LINER / LINEG / LINEB:

LINE B	LINE G	LINE R	Color SELCOR=0	Color SELCOR=1
0	0	0	Black	Black
0	0	1	Red	Red–2
0	1	0	Green	Green–2
0	1	1	Yellow	Yellow
1	0	0	Blue	Gray
1	0	1	Magenta	Yellow–2
1	1	0	Cyan	Cyan
1	1	1	White	White

(6) Address 2AD$_{16}$

DA	Register	Contents		Remarks
		Status	Function	
0	ERS0	0	Erase display RAM	Set to line 0 of display RAM
		1		
1	ERS1	0		Set to line 1 of display RAM
		1		
2	ERS2	0	It is unnecessary to reset these registers to "0". Multiple settings of ERS$_n$ is not allowed.	Set to line 2 of display RAM
		1		
3	ERS3	0		Set to line 3 of display RAM
		1		
4	ERS4	0		Set to line 4 of display RAM
		1		
5	ERS5	0		Set to line 5 of display RAM
		1		
6	ERS6	0		Set to line 6 of display RAM
		1		
7	ERS7	0		Set to line 7 of display RAM
		1		
8	ERS8	0		Set to line 8 of display RAM
		1		
9	ERS9	0		Set to line 9 of display RAM
		1		
A	ERS10	0		Set to line 10 of display RAM
		1		
B	ERS11	0		Set to line 11 of display RAM
		1		
C	ERS12	0		Set to line 12 of display RAM
		1		
D	ERS13	0		Set to line 13 of display RAM
		1		
E	ERS14	0		Set to line 14 of display RAM
		1		
F	ERS15	0		Set to line 15 of display RAM
		1		
10	ERS16	0		Set to line 16 of display RAM
		1		
11	SERS0	0	Erase SYRAM	Set to SYRAM code 00$_{16}$ ~ 0F$_{16}$
		1		
12	SERS1	0		Set to SYRAM code 10$_{16}$ ~ 1F$_{16}$
		1		
13	SERS2	0	It is unnecessary to reset these registers to "0". Multiple settings of SERS$_n$ is not allowed.	Set to SYRAM code 20$_{16}$ ~ 2F$_{16}$
		1		
14	SERS3	0		Set to SYRAM code 30$_{16}$ ~ 3E$_{16}$
		1		
15	TEST22	0	Test mode (Must be cleared to 0.)	
		1		
16	TEST23	0		
		1		
17	—	0	Must be cleared to 0.	
		1		

Erase display RAM table:

ERSx	RAM erase
0	do erase
1	do not erase

Erase SYRAM table:

SERSx	SYRAM erase
0	do erase
1	do not erase

(7) Address $2AE_{16}$

DA	Register	Contents		Remarks
		Status	Function	
0	SBIT0	0	Set display start bit of scroll block: $SA = \sum_{n=0}^{3} 2^n (SBITn)$	Setting valid $SA = 0$ to 12 invalid $SA = 13$ to 15
		1		
1	SBIT1	0		
		1		
2	SBIT2	0		
		1		
3	SBIT3	0		
		1		
4	SLIN0	0	Set display start line of scroll block: $SB = \sum_{n=0}^{4} 2^n (SLINn)$	Setting valid $SB = 0$ to 16 invalid $SB = 17$ to 31
		1		
5	SLIN1	0		
		1		
6	SLIN2	0		
		1		
7	SLIN3	0		
		1		
8	SLIN4	0		
		1		
9	SST0	0	Set start line of scroll block (last line number of the fixed block 1): $SC = \sum_{n=0}^{4} 2^n (SSTn)$	Setting valid $SC = 0$ to 15 invalid $SC = 16$ to 31
		1		
A	SST1	0		
		1		
B	SST2	0		
		1		
C	SST3	0		
		1		
D	SST4	0		
		1		
E	SEND0	0	Set start line of fixed block 2 (last line number of the scroll block): $SD = \sum_{n=0}^{4} 2^n (SENDn)$	When the scrolling on setting valid $SD = 2$ to 17 invalid $SD = 18$ to 31 When the scrolling off set $SD = 0$
		1		
F	SEND1	0		
		1		
10	SEND2	0		
		1		
11	SEND3	0		$SD > SC + 2$
		1		
12	SEND4	0		
		1		
13	—	0	Must be cleared to 0.	
		1		
14	—	0		
		1		
15	—	0		
		1		
16	—	0		
		1		
17	—	0		
		1		

Note: When the scrolling on, set the ratio which will be $SC < SB < SD$.

MITSUBISHI ELECTRIC
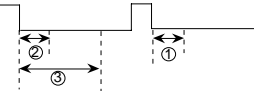
(8) Address 2AF$_{16}$

DA	Register	Contents		Remarks
		Status	Function	
0	PTC0	0	Port P0 output	Select P0 pin
		1	YM output	
1	PTC1	0	Port P1 output	Select P1 pin
		1	BLNK output	
2	PTC2	0	Port P2 output	Select P2 pin
		1	B output	
3	PTC3	0	Port P3 output	Select P3 pin
		1	G output	
4	PTC4	0	Port P4 output	Select P4 pin
		1	R output	
5	PTC5	0	Port P5 output	Select P5 pin
		1	CSYN output	
6	PTD0	0	When port output: 0 output, when YM output: negative polarity.	Select data of P0 pin
		1	When port output: 1 output, when YM output: polarity.	
7	PTD1	0	When port output: 0 output, when BLNK output: negative polarity.	Select data of P1 pin
		1	When port output: 1 output, when BLNK output: polarity.	
8	PTD2	0	When port output: 0 output, when B output: negative polarity.	Select data of P2 pin
		1	When port output: 1 output, when B output: polarity.	
9	PTD3	0	When port output: 0 output, when G output: negative polarity.	Select data of P3 pin
		1	When port output: 1 output, when G output: polarity.	
A	PTD4	0	When port output: 0 output, when R output: negative polarity.	Select data of P4 pin
		1	When port output: 1 output, when R output: polarity.	
B	PTD5	0	When port output: 0 output, when CSYN output: negative polarity.	Select data of P5 pin
		1	When port output: 1 output, when CSYN output: polarity.	
C	SRAND0	0	*(see SRAND table below)*	Condition of border display is changeable.
		1		
D	SRAND1	0		
		1		
E	SRAND2	0		
		1	Vertical direction is 1 dot only.	
F	ALL24	0	Blanking with all 40 characters in matrix-outline mode	Horizontal display range can be altered when all characters are in matrix-outline size. At external synchronous, set to 0. Operation of character code FF$_{16}$ becomes ineffective.
		1	Horizontal display period fully blanked with all characters in matrix-outline size.	
10	PC0	0	Display frequency f$_T$ control $f_T = f_H \times \{ \sum_{n=0}^{7} (2^n PC_n) + 512 \}$	PC7 ~ PC0 < 36$_{16}$, PC7 ~ PC0 > C6$_{16}$ is not available.
		1		
11	PC1	0		
		1		
12	PC2	0		
		1		
13	PC3	0		
		1		
14	PC4	0		
		1		
15	PC5	0		
		1		
16	PC6	0		
		1		
17	PC7	0		
		1		

SRAND1	SRAND0	SRAND2 = 0	SRAND2 = 1
0	0	Complete border = 1 dot	Right and dot border = 1 dot
0	1	Complete border = 2 dot	Right and dot border = 2 dot
1	0	Complete border = 3 dot	Right and dot border = 3 dot
1	1	Complete border = 4 dot	Right and dot border = 4 dot

Note: At EX (address 2B0$_{16}$) = "0" (external synchronous), setting "1" of ALL24 register is not available.
Refer Fig. 2 about PTC0 ~ 5, PTD0 ~ 5.

(9) Address 2B0$_{16}$

DA	Register	Contents		Remarks
		Status	Function	
0	EX	0	External synchronization	(Note)
		1	Internal synchronization	
1	—	0	Set to "0".	
		1		
2	SELCOR	0	Normal	Refer to Table 3, 4, 7 and 8.
		1	Mode of expansion	
3	—	0	Must be cleared to 0.	
		1		
4	DSPON	0	Digital output display OFF	
		1	Digital output display ON	
5	DSPONV	0	Composite video output display OFF	
		1	Composite video output display ON	
6	—	0	Must be cleared to 0.	
		1		
7	BLK	0	Matrix outline	Only at register "DSP1xx" = 1 (xx = 00 to 16) is available.
		1	Matrix outline + border	
8	SEPV0	0		Method of sync separation from composite video.
		1		
9	SEPV1	0		Case (1) condition: vertical sync must repeat 2X within (2) or (3); indicates this area.
		1		
A	TEST15	0	Test mode (Must be cleared to 0.)	
		1		
B	TEST16	0		
		1		
C	PALH	0	Interlace/noninterlace normal mode	Only at PAL and MPAL mode are available.
		1	Interlace/noninterlace expansion mode	
D	MPAL	0		
		1		
E	PAL/$\overline{\text{NTSC}}$	0		
		1		
F	$\overline{\text{INT}}$/NON	0	Interlace	
		1	Noninterlace	
10	LEVEL0	0	Composite video generation is off.	Refer to Table 5 and 6.
		1	Composite video generation is on.	
11	LEVEL1	0	Display clock is on (oscillating).	
		1	Display clock is off (not oscillating).	
12	LEVEL2	0	Sync separation is disabled.	
		1	Sync separation is enabled.	
13	TEST24	0	Test mode (Must be cleared to 0.)	
		1		
14	TEST17	0		
		1		
15	TEST18	0		
		1		
16	TEST19	0		
		1		
17	—	0	Must be cleared to 0.	
		1		

For DA 8/9 (SEPV0/SEPV1):

SEPV1	SEPV0	Composite Sync Spearation Function
0	0	Separation is performed during (1) in vertical blanking period
0	1	Separation is performed during (2) in vertical blanking period 1
1	0	Separation is performed during (3) in vertical blanking period
1	1	Unavailable

For DA D/E (MPAL / PAL/NTSC):

PAL/NTSC	MPAL	Format
0	0	NTSC
0	1	M-PAL
1	0	PAL
1	1	unavailable

Note: For internal synchronization, shut out (mute) the external video signal input to the CVIN terminal, outside the IC. This avoids external video signal leaks inside the IC.

MITSUBISHI ELECTRIC

REGISTER CONSTRUCTION COMPOSITION

Table 3 Color and phase of NTSC, PAL (SELCOR = 0)

PHASE2 / LINEB	PHASE1 / LINEG	PHASE0 / LINER	Phase (rad)		Color
			NTSC	PAL	
0	0	0	—	—	Black
0	0	1	7 /16	± 7 /16	Red
0	1	0	27 /16	∓ 5 /16	Green
0	1	1	/16	± /16	Yellow
1	0	0	17 /16	∓ 15 /16	Blue
1	0	1	11 /16	± 11 /16	Magenta
1	1	0	23 /16	∓ 9 /16	Cyan
1	1	1	—	—	White

Table 4 Color and phase of NTSC, PAL (SELCOR = 1)

PHASE2 / LINEB	PHASE1 / LINEG	PHASE0 / LINER	Phase (rad)		Color
			NTSC	PAL	
0	0	0	—	—	Black
0	0	1	7 /16	± 7 /16	Red-2
0	1	0	27 /16	∓ 5 /16	Green-2
0	1	1	/16	± /16	Yellow
1	0	0	—	—	Gray
1	0	1	/16	± /16	Yellow-2
1	1	0	23 /16	∓ 9 /16	Cyan
1	1	1	—	—	White

Fig. 2 Switching port output with R, G and B output

Table 5 Setting condition at LEVEL 0, 1 and 2

	At display clock operates	At display clock stops
LEVEL1	0	1
DSPON	1	0
DSPONV	1	0
CS̄ pin	L	H

No character display at display clock

Table 6 Setting condition at LEVEL 0, 1 and 2 (at operation)

	Operation state	Stop state
LEVEL0	1	0
LEVEL1	0	1
LEVEL2	1	0

Table 7 Video signal level (SELCOR = 0)

Color name	Phase (rad)		Luminance level (V)			Chroma amplitude (vs. color burst)		
	NTSC	PAL	Min.	Typ.	Max.	Min.	Typ.	Max.
Sync	—	—	1.3	1.5	1.7	—	—	—
Pedestal	—	—	1.9	2.1	2.3	—	—	—
Color Burst	0	±4 /16	1.9	2.1	2.3	—	1.0	—
Black	—	—	2.1	2.3	2.5	—	—	—
Red	7 /16 ± 2 /16	± 7 /16 ± 2 /16	2.3	2.5	2.7	1.5	3.0	4.5
Green	27 /16 ± 2 /16	∓ 5 /16 ± 2 /16	2.7	2.9	3.1	1.4	2.8	4.2
Yellow	/16 ± 2 /16	± /16 ± 2 /16	3.1	3.3	3.5	1.0	2.0	3.0
Blue	17 /16 ± 2 /16	∓ 15 /16 ± 2 /16	2.0	2.2	2.4	1.0	2.0	3.0
Mazenta	11 /16 ± 2 /16	± 11 /16 ± 2 /16	2.5	2.7	2.9	1.4	2.8	4.2
Cyan	23 /16 ± 2 /16	∓ 9 /16 ± 2 /16	2.9	3.1	3.3	1.5	3.0	4.5
White	—	—	3.1	3.3	3.5	—	—	—

Table 8 Video signal level (SELCOR = 1)

Color name	Phase (rad)		Luminance level (V)			Chroma amplitude (vs. color burst)		
	NTSC	PAL	Min.	Typ.	Max.	Min.	Typ.	Max.
Sync	—	—	1.3	1.5	1.7	—	—	—
Pedestal	—	—	1.9	2.1	2.3	—	—	—
Color Burst	0	±4 /16	1.9	2.1	2.3	—	1.0	—
Black	—	—	2.1	2.3	2.5	—	—	—
Red-2	7 /16 ± 2 /16	± 7 /16 ± 2 /16	2.6	2.8	3.0	1.5	2.0	3.0
Green-2	27 /16 ± 2 /16	∓ 5 /16 ± 2 /16	3.1	3.3	3.5	0.5	1.0	1.5
Yellow	/16 ± 2 /16	± /16 ± 2 /16	3.1	3.3	3.5	1.0	2.0	3.0
Gray	—	—	2.8	3.0	3.2	—	—	—
Yellow-2	/16 ± 2 /16	± /16 ± 2 /16	3.2	3.4	3.6	0.4	0.8	1.2
Cyan	23 /16 ± 2 /16	∓ 9 /16 ± 2 /16	2.9	3.1	3.3	1.5	3.0	4.5
White	—	—	3.1	3.3	3.5	—	—	—

DISPLAY FORMS
1. Blanking mode

Display forms are shown in Table 9, display forms at each display mode are shown in Fig. 3.

Table 9 Display forms

Display mode	DSP1 xx (Address 2AC$_{16}$)	DSP0 xx (Address 2AB$_{16}$)	BLNK output
Character	0	0	Character size
Border	0	1	Border size
Matrix-outline	1	0	All blanking
Halftone	1	1	Blanking OFF
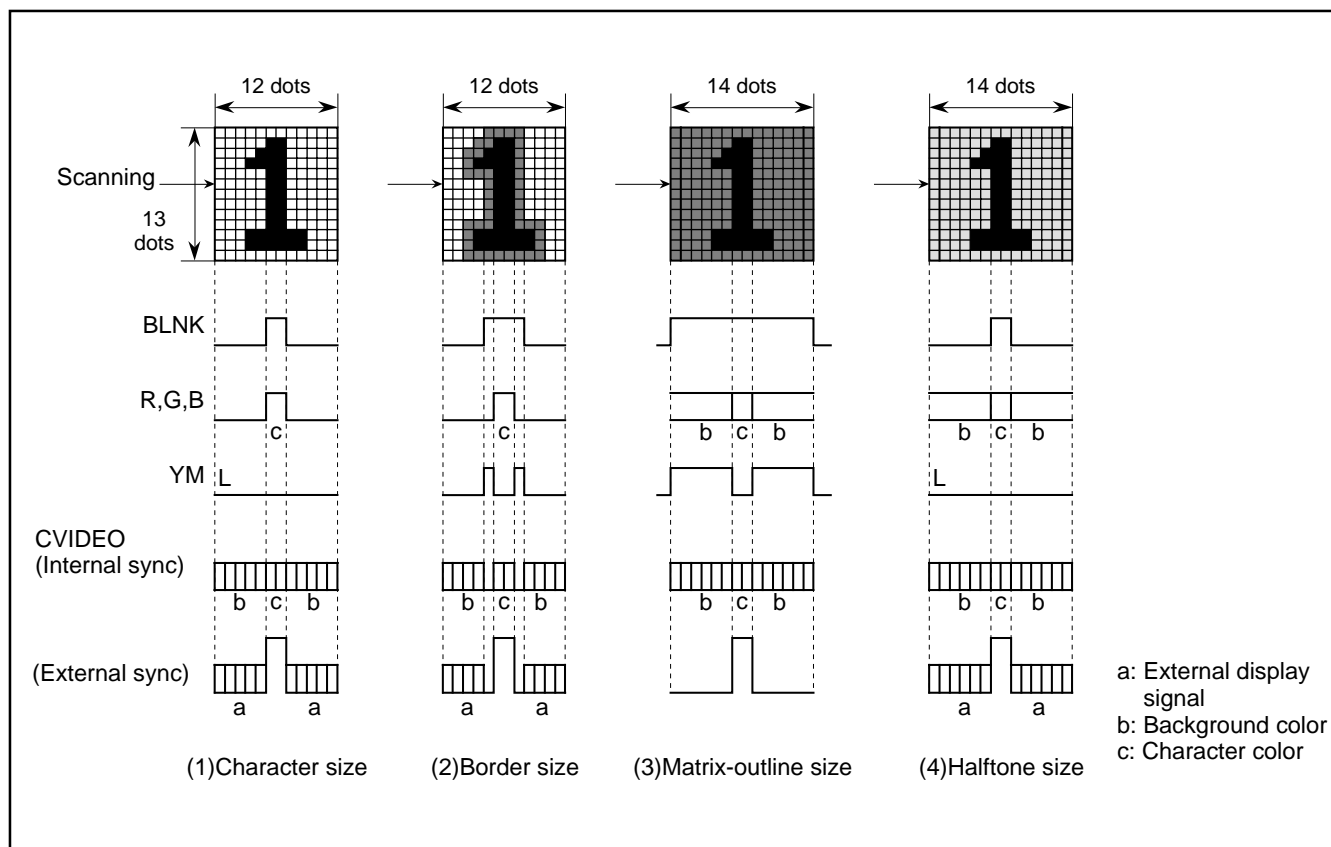
Fig. 3 Display forms at each display mode

MITSUBISHI ELECTRIC

For matrix and halftone, a character's number of dots in the horizontal direction increases to 14.

Figure 4 shows a display example for a case where adjacent characters have different background colors and for character code FF_{16}.
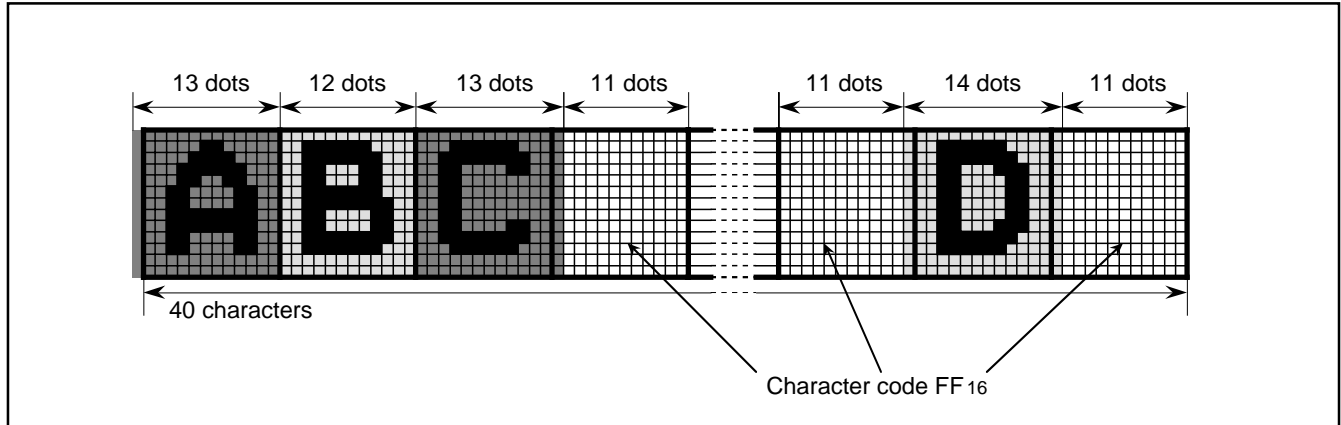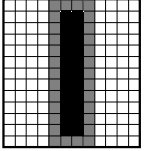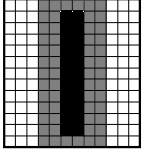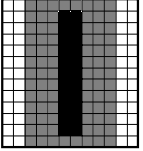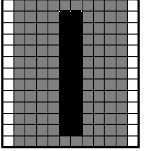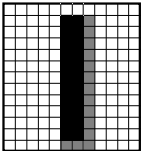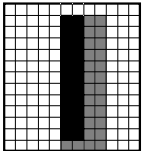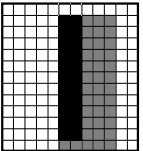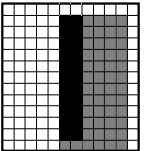
Fig. 4   Number of dots in the horizontal direction at matrix-outline or halftone

2. Border mode

In border mode, characters are displayed with borders. (Refer to Table 9.) In matrix and halftone modes also, characters are displayed with borders if the BLK register (address $2B0_{16}$) is set to 1.

Table 10 lists the types of borders.

Table 10   Bordering

SRAND2 (Address $2AF_{16}$) \ SRAND1, 0	00	01	10	11
0	1 dot in horizontal direction	2 dots in horizontal direction	3 dots in horizontal direction	4 dots in horizontal direction
1	1 dot in horizontal direction	2 dots in horizontal direction	3 dots in horizontal direction	4 dots in horizontal direction

Horizontal direction bordering is only 1 dot. When the character extends to the top line of the matrix, no border is left at the top, and when the character extends to the bottom (12th) line of the matrix, no border is left at the bottom.

3. Setting matrix outline

The ALL24 register (address 2AF$_{16}$) allows you to set a matrix outline. A matrix outline can be set for each line by using the DSP1XX register (address 2AC$_{16}$) .

However, this setting is inhibited if the EX register (address 2B0$_{16}$) is 0 (external sync). An example of how you set a matrix outline is shown in Figure 5.
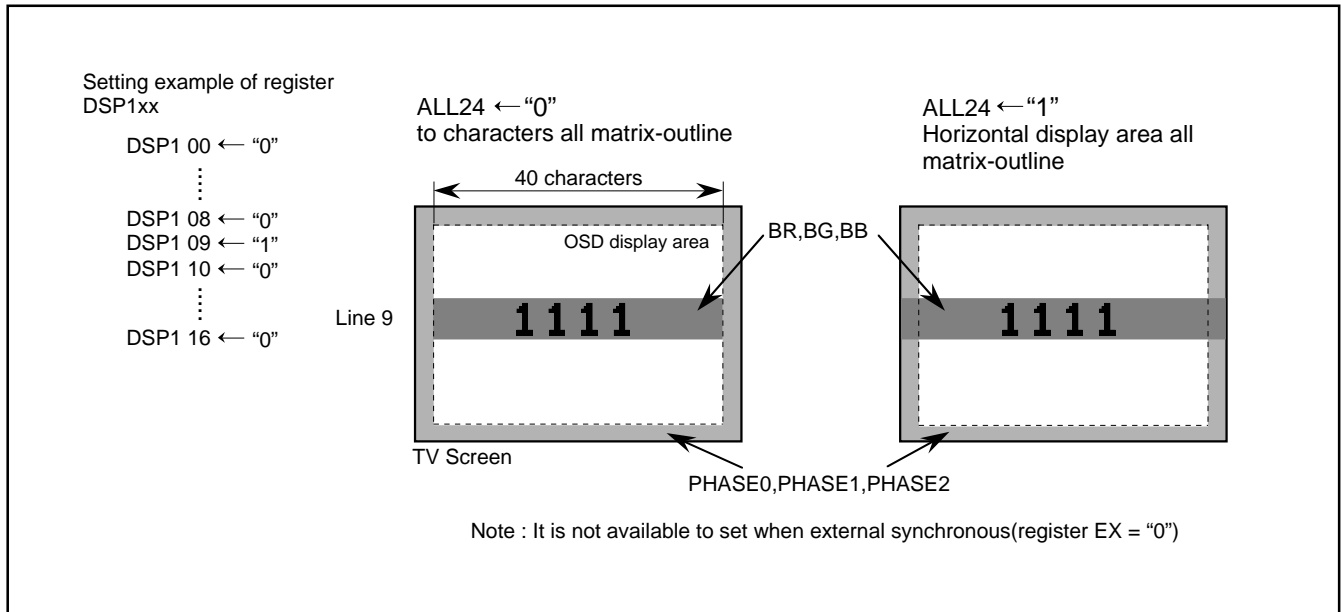
Fig. 5 Setting example all matrix-outline area

4. Blinking mode

Two patterns blinking by register BLINK3 (address 2A9$_{16}$) or BLINK bit of display RAM.

Blinking mode is shown in Table 11 (SYRAM do not blink).

Use registers BLINK0, 1, and 2 (address 2A9$_{16}$) to set the duty ratio and period that determines the blinking time. Tables 12 and 13 list the relationship between the register settings and the duty ratio and period.

Table 11 Blinking mode
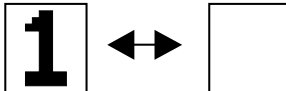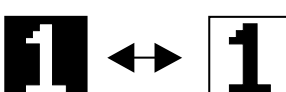
Table 12 Setting of duty ratio

BLINK1 \ BLINK0	0	1
0	Blink OFF	Duty 25%
1	Duty 50%	Duty 75%

Table 13 Setting of cycle

BLINK2	Cycle
0	Approximately 1 second (Vertical sync divided into 1/64)
1	Approximately 0.5 second (Vertical sync divided into 1/32)

MITSUBISHI ELECTRIC

5. Scroll display mode

The scroll display mode is entered by setting registers SBIT0 to 3 (SA), SLIN0 to 4 (SB), SST0 to 4 (SC), and SEND0 to 4 (SD) (all at address 2AE16). (Scroll is turned off when SD = 0.)

The screen is scrolled in the range from the (SC)'th line to the (SD-1)'th line, and sections above and below this range are fixed. The beginning line and beginning dot of scroll are the (SA)'th dot on the (SB)'th line.

The screen can be scrolled up or down by successively incrementing or decrementing SA and SB.

Figure 6 shows examples of how the display is scrolled. The scroll range in these examples contains 12 lines (second to the 13th lines). However, the screen can display only 11 lines at a time, and the remaining one line is handled as a dummy line and not displayed.

When displayed in order of SA = 0, 1, 2, and so on, the screen scrolls up. When displayed in order of SA = 12, 11, 10, and so on, the screen scrolls down.

(1) To scroll the screen up, write the dummy line after you set the 0th dot in SA but before setting the 1st dot.

(2) To scroll the screen down, write the dummy line after you set the 0th dot in SA but before setting the 12th dot of the preceding line.

Fig. 6 Scrolling example

6. Character font

(1) Character ROM

Images are composed on a 12 $\times$ 13 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

Character code FF_{16} is fixed as blank, without a background.
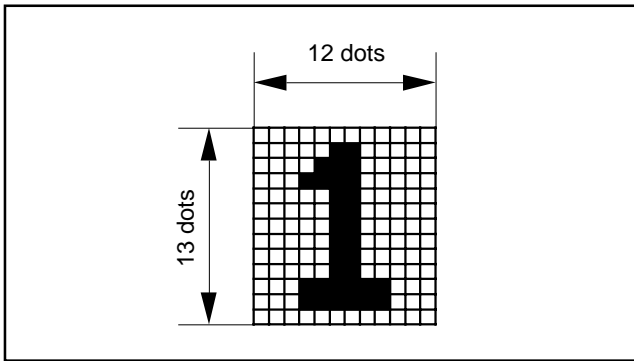
Fig. 7 Character construction

Fig. 8 Example for displaying a continuous pattern

(2) SYRAM

You can set characters for 63 letters per screen (SYRAM code 00_{16} to $3E_{16}$). Figure 9 shows an example of how to set.

Use display RAM's SYC5 to 0 (00_{16} to $3E_{16}$) to specify SYRAM.

Note that SYRAM code $3F_{16}$ is fixed to a blank, so you cannot set a character font to this code.

If you do not put SYRAM and a character together, use code $3F_{16}$.

MITSUBISHI ELECTRIC

(ex) SYRAM code 00_{16} .... Set character by setting data to address 300_{16} ~ $30C_{16}$

Address	DA																
	17	…	D	C	B	A	9	8	7	6	5	4	3	2	1	0
300_{16}	0	…	0	*	0	0	0	0	0	0	0	0	0	0	0	0
301_{16}	0	…	0	*	0	0	0	0	0	0	0	0	0	0	0	1
302_{16}	0	…	0	*	0	0	0	0	0	0	0	0	0	0	1	1
303_{16}	0	…	0	*	0	0	0	0	0	0	0	0	0	1	1	1
304_{16}	0	…	0	*	0	0	0	0	0	0	0	0	1	1	1	1
305_{16}	0	…	0	*	0	0	0	0	0	0	0	1	1	1	1	1
306_{16}	0	…	0	*	0	0	0	0	0	0	1	1	1	1	1	1
307_{16}	0	…	0	*	0	0	0	0	0	1	1	1	1	1	1	1
308_{16}	0	…	0	*	0	0	0	0	1	1	1	1	1	1	1	1
309_{16}	0	…	0	*	0	0	0	1	1	1	1	1	1	1	1	1
$30A_{16}$	0	…	0	*	0	0	1	1	1	1	1	1	1	1	1	1
$30B_{16}$	0	…	0	*	0	1	1	1	1	1	1	1	1	1	1	1
$30C_{16}$	0	…	0	*	1	1	1	1	1	1	1	1	1	1	1	1

13 dots

12 dots

13 dots

12 dots
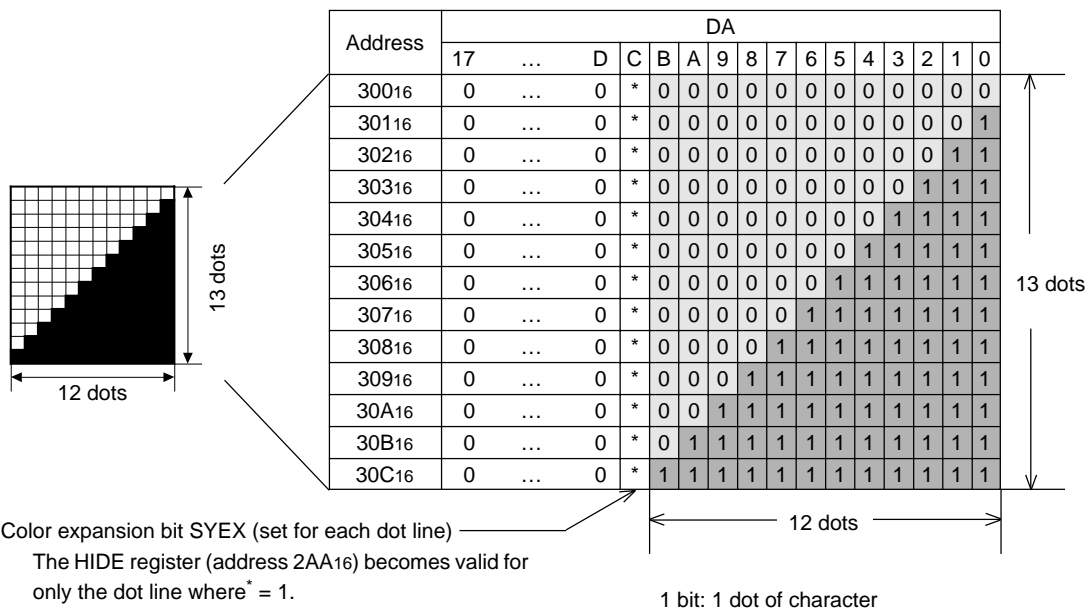
Color expansion bit SYEX (set for each dot line)
The HIDE register (address $2AA_{16}$) becomes valid for only the dot line where * = 1.
For details, refer to the next section, "(3) Compounding character ROM and SYRAM."

1 bit: 1 dot of character

Fig. 9 Setting example of SYRAM

(3) Compounding character ROM and SYRAM

You can compound characters in character ROM with SYRAM. The compounding method is determined by the SYEX color expansion bit and the HIDE register (address $2AA_{16}$).

For dot lines where SYEX = 0, the SYRAM color is set by the display RAM's SR, SG, and SB irrespective of the HIDE register's content.

If the HIDE register's content is 0, the SYRAM color for dot lines where SYEX = 1 is set by the LINER, LINEG, and LINEB registers (address $2AC_{16}$).

If the HIDE register's content is 1, the character ROM part of the dot lines where SYEX = 1 is overwritten in HIDE mode with colors set by the LINER, LINEG, and LINEB registers irrespective of the ROM's content and color. The color of the SYRAM part is set by the display RAM's SR, SG, and SB as in the case of dot lines where SYEX = 0.

Figure 10 shows an example for each instance of compounding.

When HIDE = 1, the character ROM's contents for dot lines where SYEX = 1 become invisible.

Fig. 10 Compounding example

MITSUBISHI ELECTRIC

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

EXAMPLE FOR DATA INPUT

Use an 8-bit parallel ✕ 3 serial input to set data in the display RAM, display control register, and SYRAM. Table 14 lists an example of how data is set.

Table 14   Data setting

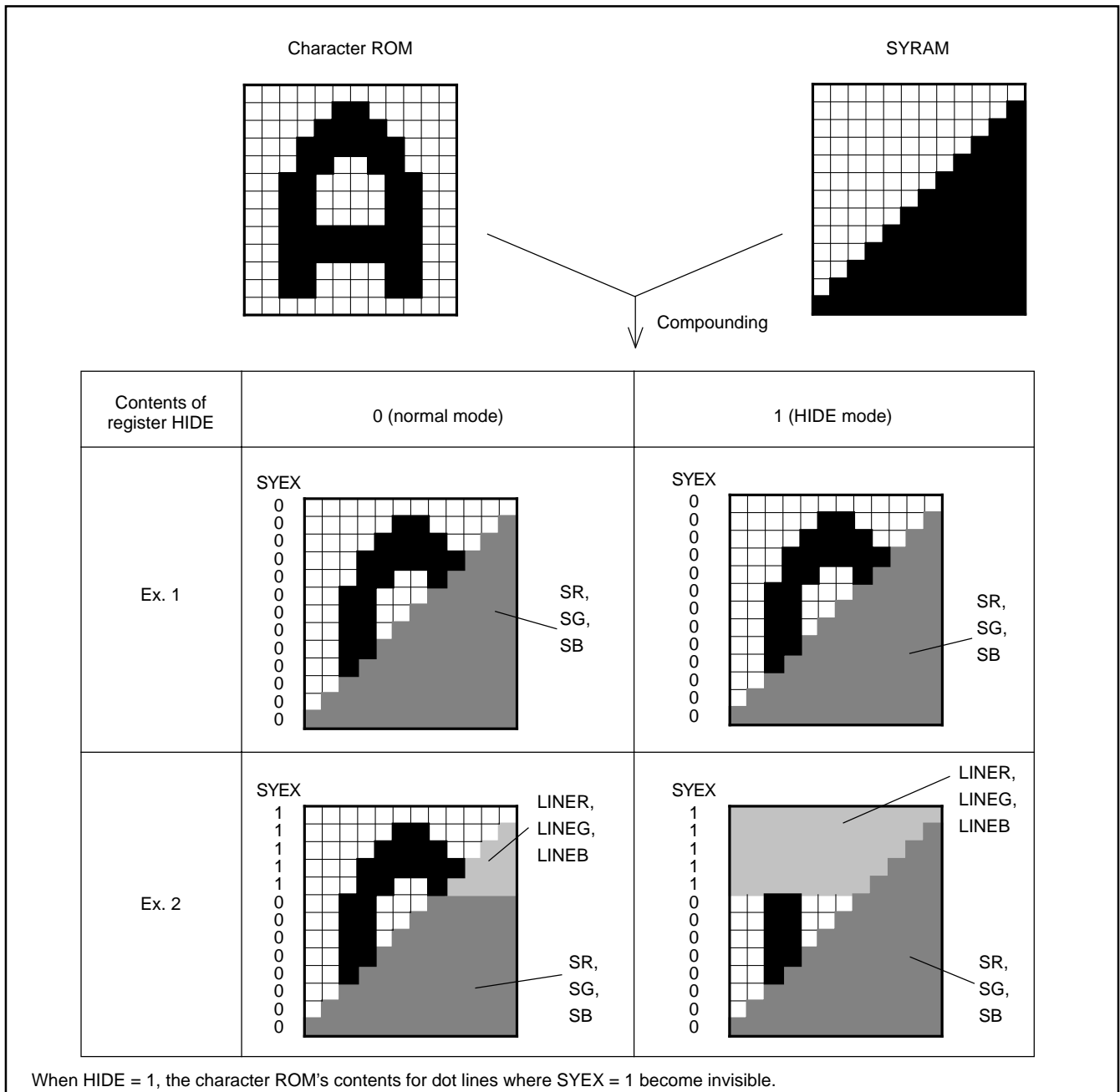| No.	Address/data	Remarks	DA0	DA1	DA2	DA3	DA4	DA5	DA6	DA7	DA8	DA9	DAA	DAB	DAC	DAD	DAE	DAF	DA10	DA11	DA12	DA13	DA14	DA15	DA16	DA17
1	Address ($2B0_{16}$)	Address setting	0	1	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	Data ($2B0_{16}$)	Display OFF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0
3	Data (300_{16})	Set addresses SYRAM 300_{16} ~ $6EC_{16}$	S000	S001	S002	S003	S004	S005	S006	S007	S008	S009	S00A	S00B	SYEX	0	0	0	0	0	0	0	0	0	0	0
4	Data (301_{16})		S010	S011	S012	S013	S014	S015	S016	S017	S018	S019	S01A	S01B	SYEX	0	0	0	0	0	0	0	0	0	0	0
~	~																									
822	Data ($6EC_{16}$)		S3E0	S3E1	S3E2	S3E3	S3E4	S3E5	S3E6	S3E7	S3E8	S3E9	S3EA	S3EB	SYEX	0	0	0	0	0	0	0	0	0	0	0
823	Address (000_{16})	Set address	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
824	Data (000_{16})	Set registers address display RAM 000_{16} ~ $2A7_{16}$	C0	C1	C2	C3	C4	C5	C6	C7	CR	CG	CB	BLINK	BR	BG	BB	SYC0	SYC1	SYC2	SYC3	SYC4	SYC5	SR	SG	SB
825	Data (001_{16})		C0	C1	C2	C3	C4	C5	C6	C7	CR	CG	CB	BLINK	BR	BG	BB	SYC0	SYC1	SYC2	SYC3	SYC4	SYC5	SR	SG	SB
~	~																									
1503	Data ($2A7_{16}$)		C0	C1	C2	C3	C4	C5	C6	C7	CR	CG	CB	BLINK	BR	BG	BB	SYC0	SYC1	SYC2	SYC3	SYC4	SYC5	SR	SG	SB
1504	Data ($2A8_{16}$)	Set registers address $2A8_{16}$ ~ $2AF_{16}$	VP0	VP1	VP2	VP3	VP4	VP5	VP6	VP7	HP0	HP1	HP2	HP3	HP4	HP5	HP6	HP7	HP8	0	0	0	0	0	0	0
1505	Data ($2A9_{16}$)		HSZ0	HSZ1	HSZ2	HSZ3	HSZ4	HSZ5	HSZ6	HSZ7	HSZ8	HSZ9	HSZ10	HSZ11	HSZ12	HSZ13	HSZ14	HSZ15	HSZ16	BLINK0	BLINK1	BLINK2	BLINK3	0	0	0
1506	Data ($2AA_{16}$)		VSZ0	VSZ1	VSZ2	VSZ3	VSZ4	VSZ5	VSZ6	VSZ7	VSZ8	VSZ9	VSZ10	VSZ11	VSZ12	VSZ13	VSZ14	VSZ15	VSZ16	HIDE	0	EQP	0	0	0	0
1507	Data ($2AB_{16}$)		DSP000	DSP001	DSP002	DSP003	DSP004	DSP005	DSP006	DSP007	DSP008	DSP009	DSP010	DSP011	DSP012	DSP013	DSP014	DSP015	DSP016	PHASE0	PHASE1	PHASE2	0	0	0	0
1508	Data ($2AC_{16}$)		DSP100	DSP101	DSP102	DSP103	DSP104	DSP105	DSP106	DSP107	DSP108	DSP109	DSP110	DSP111	DSP112	DSP113	DSP114	DSP115	DSP116	LINE R	LINE G	LINE B	0	0	0	0
1509	Data ($2AD_{16}$)		ERS0	ERS1	ERS2	ERS3	ERS4	ERS5	ERS6	ERS7	ERS8	ERS9	ERS10	ERS11	ERS12	ERS13	ERS14	ERS15	ERS16	SERS0	SERS1	SERS2	0	0	0	0
1510	Data ($2AE_{16}$)		SBIT0	SBIT1	SBIT2	SBIT3	SLIN0	SLIN1	SLIN2	SLIN3	SLIN4	SST0	SST1	SST2	SST3	SST4	SEND0	SEND1	SEND2	SEND3	SEND4	0	0	0	0	0
1511	Data ($2AF_{16}$)		PTC0	PTC1	PTC2	PTC3	PTC4	PTC5	PTD0	PTD1	PTD2	PTD3	PTD4	PTD5	SRAND0	SRAND1	SRAND2	ALL24	PC0	PC1	PC2	PC3	PC4	PC5	PC6	PC7
1512	Data ($2B0_{16}$)	Display ON	EX	SEL0	SEL/COR	0	1	1	0	BLK	SEPV0	SEPV1	0	0	0	0	0	1	1	0	1	0	0	0	0	0

SERIAL DATA INPUT TIMING

(1) The address consists of 8 bits ✕ 3.

(2) The data consists of 8 bits ✕ 3.

(3) The 8 bits ✕ 3 in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 24 bits (8 bits ✕ 3). Refer to Fig.12 about detail for address increment.
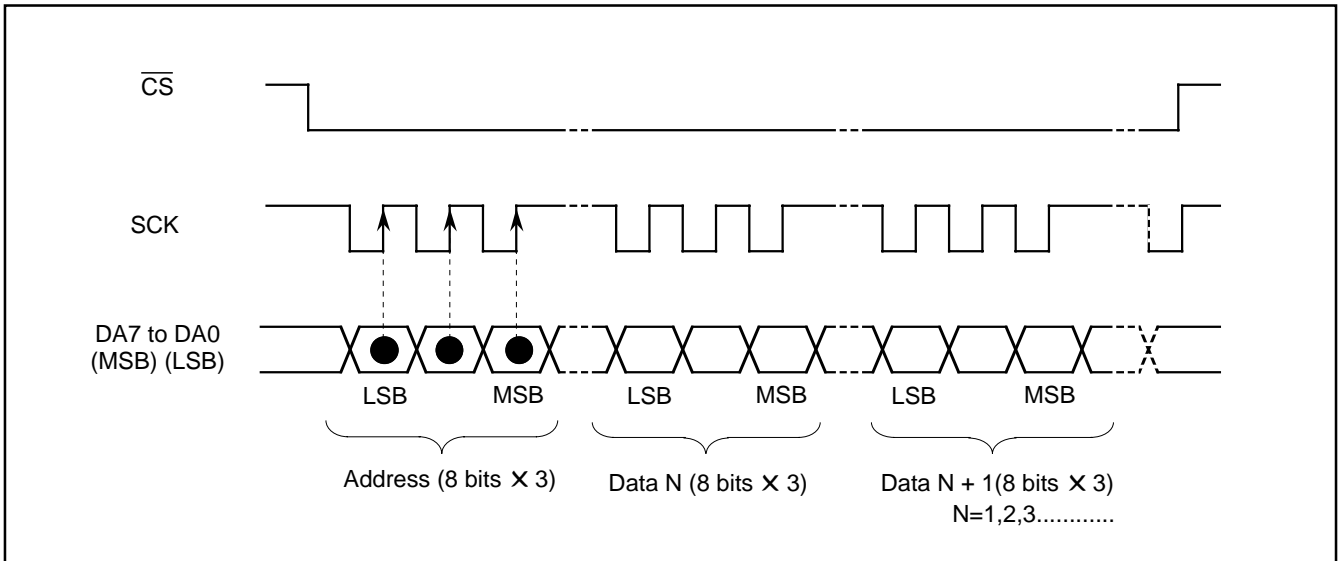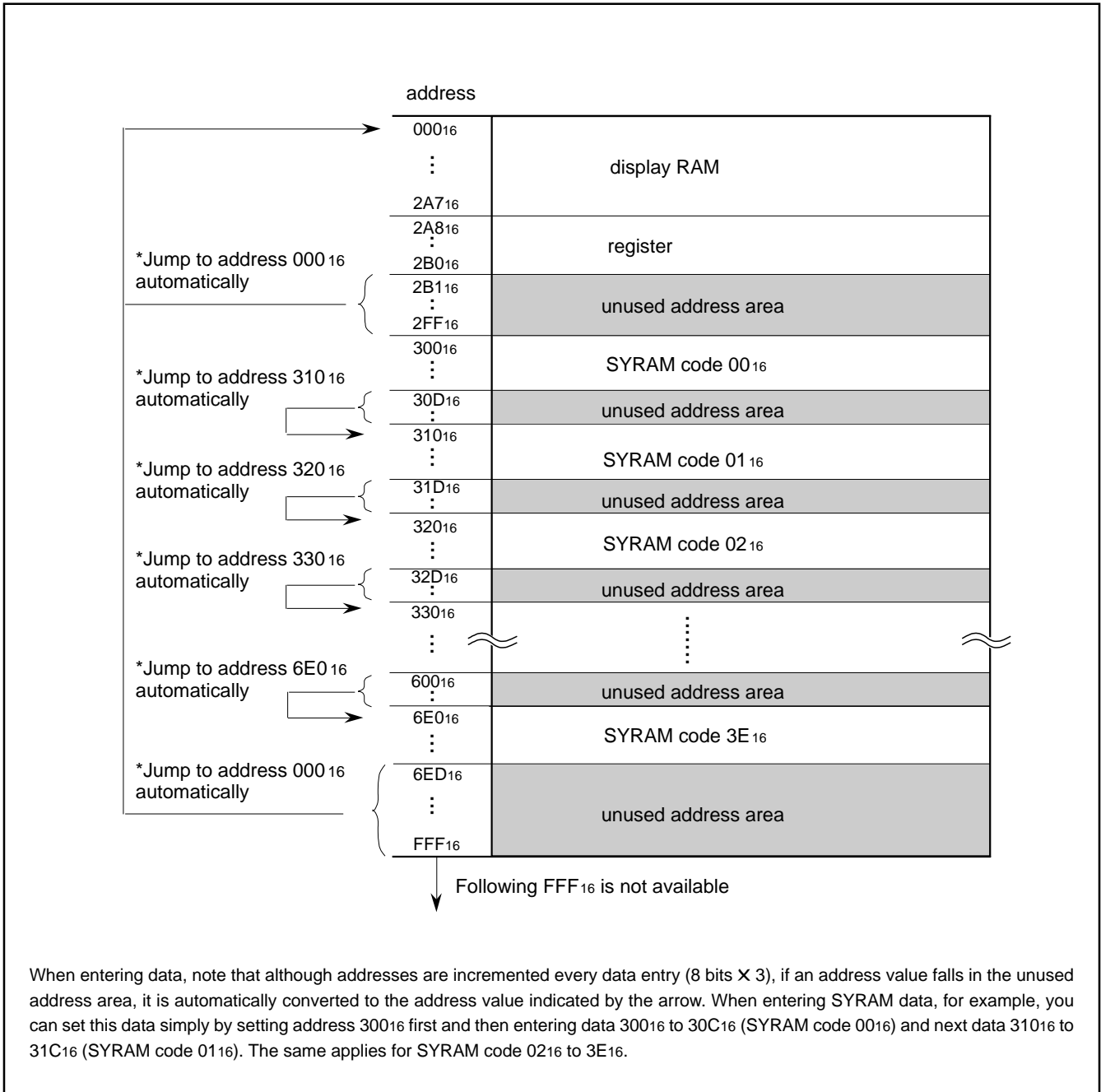

Fig. 11 Serial input timing

MITSUBISHI ELECTRIC

address	
000_{16}	
⋮	display RAM
$2A7_{16}$	
$2A8_{16}$ ⋮ $2B0_{16}$	register
$2B1_{16}$ ⋮ $2FF_{16}$	unused address area
300_{16} ⋮	SYRAM code 00_{16}
$30D_{16}$ ⋮	unused address area
310_{16} ⋮	SYRAM code 01_{16}
$31D_{16}$ ⋮	unused address area
320_{16} ⋮	SYRAM code 02_{16}
$32D_{16}$ ⋮	unused address area
330_{16} ⋮	⋮
600_{16} ⋮	unused address area
$6E0_{16}$	SYRAM code $3E_{16}$
$6ED_{16}$ ⋮ FFF_{16}	unused address area

*Jump to address 000_{16} automatically

*Jump to address 310_{16} automatically

*Jump to address 320_{16} automatically

*Jump to address 330_{16} automatically

*Jump to address $6E0_{16}$ automatically

*Jump to address 000_{16} automatically

Following FFF_{16} is not available

When entering data, note that although addresses are incremented every data entry (8 bits ✕ 3), if an address value falls in the unused address area, it is automatically converted to the address value indicated by the arrow. When entering SYRAM data, for example, you can set this data simply by setting address 300_{16} first and then entering data 300_{16} to $30C_{16}$ (SYRAM code 00_{16}) and next data 310_{16} to $31C_{16}$ (SYRAM code 01_{16}). The same applies for SYRAM code 02_{16} to $3E_{16}$.

Fig. 12 Address construction

M35060-XXXSP PERIPHERAL CIRCUIT
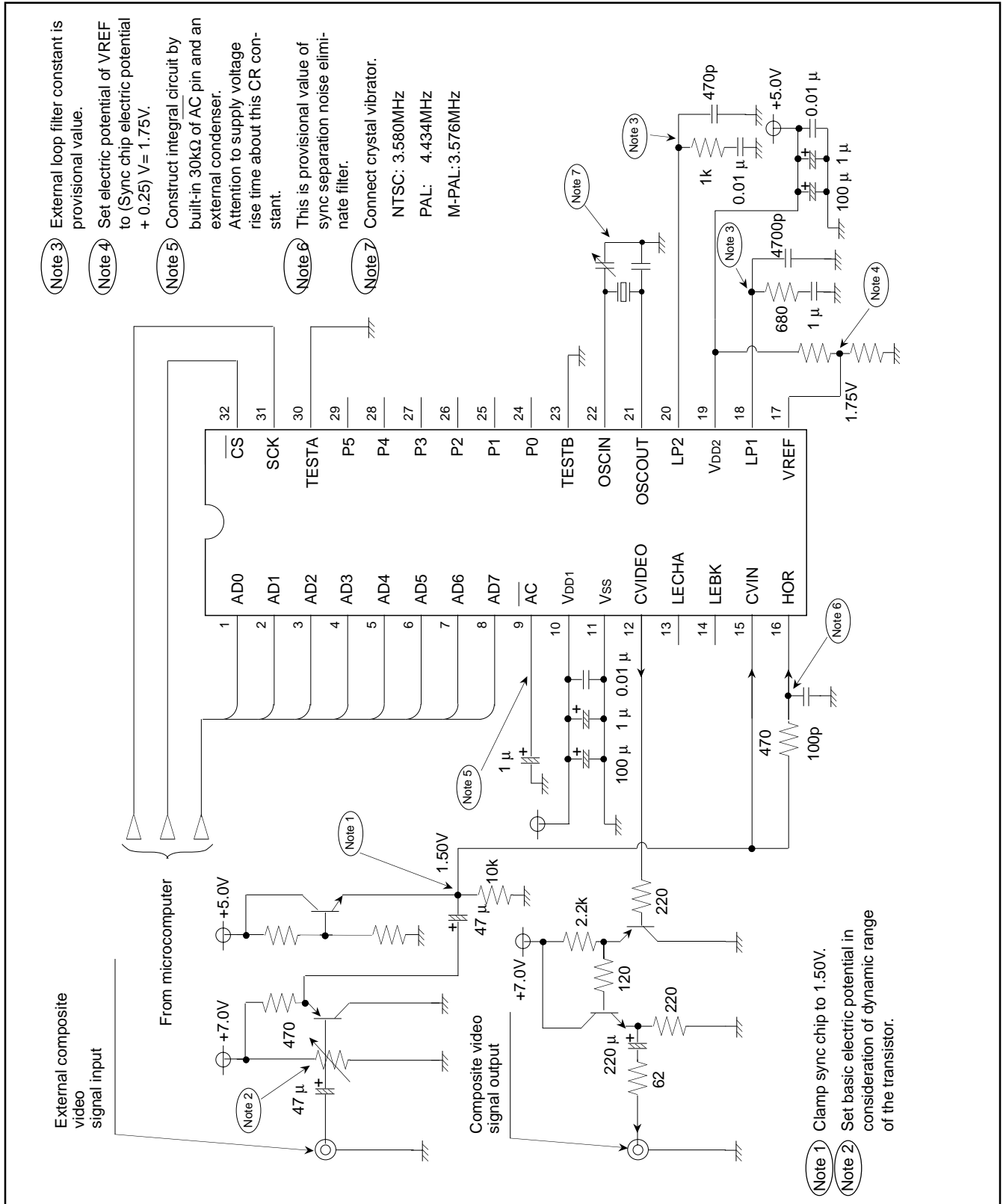
Fig.13 M35060-XXXSP example of peripheral circuit

MITSUBISHI ELECTRIC

TIMING REQUIREMENTS (Ta = – 20°C ~ + 70°C, VDD = 5.00 ± 0.25V unless otherwise noted)

DATA INPUT

Symbol	Paramenter	Limits			Unit
		Min.	Typ.	Max.	
tW (SCK)	SCK width	200	—	—	ns
tsu (CS)	$\overline{CS}$ setup time	200	—	—	ns
th (CS)	$\overline{CS}$ hold time	2	—	—	ms
tsu (AD)	AD setup time	200	—	—	ns
th (AD)	AD hold time	200	—	—	ns
th (SCK)	1 word hold time	2	—	—	ms
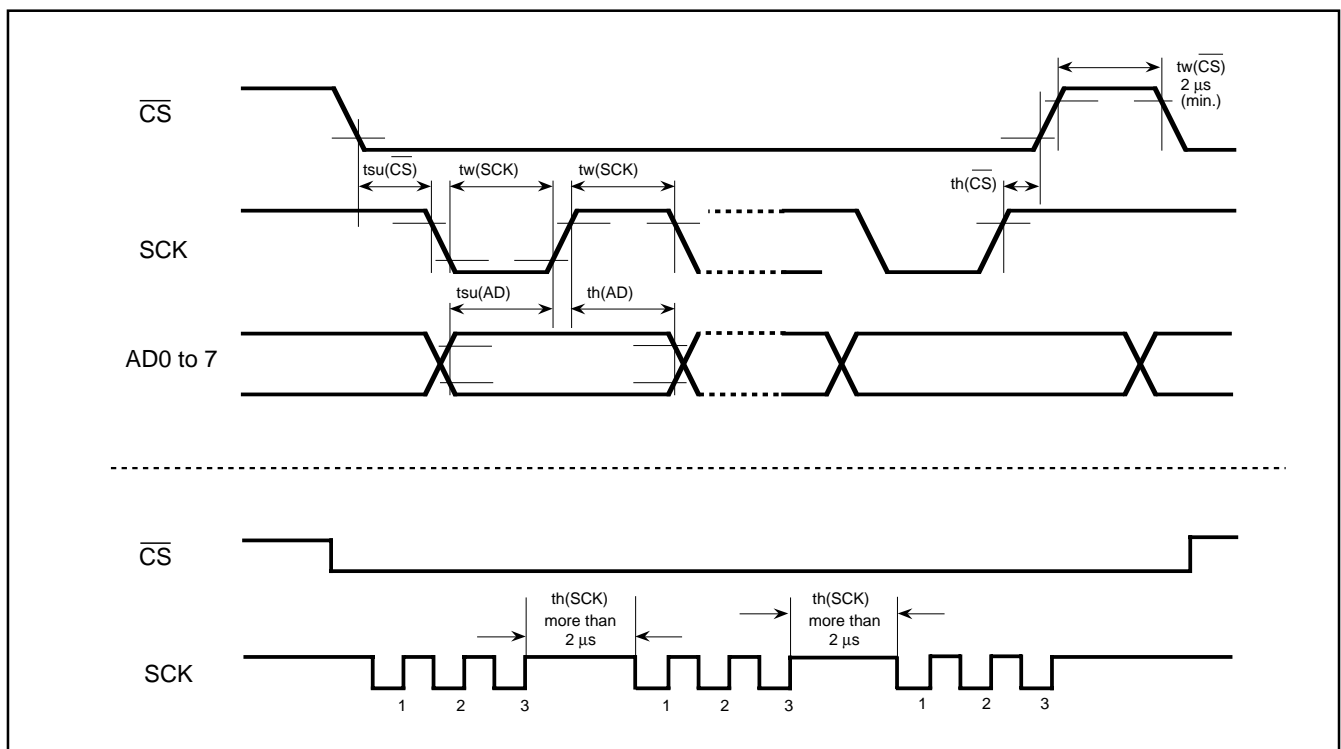
Fig. 14 Serial input timing requirements

27

PRECAUTIONS

1. Note for when starting of system
   Before setting registers at the starting of system, be sure to re-set the M35060-XXXSP by applying "L" level to the AC pin.

2. When power supply noise is generated, the internal oscillator circuit does not stabilize, whereby causing horizontal jitters across the picture display. Therefore, connect a bypass capacitor between the power supply and GND.

3. Note for when throwing power supply into the M35060-XXXSP
   When power to the M35060-XXXSP is activated, characters are sometimes output without defining the internal display RAM, composite RAM and register. Also, immediately after power is turned ON, up until the oscillator circuit stabilizes, data is sometimes not set correctly in the register. Therefore, use the following start-up procedure.

   (a) Throwing power supply into the M35060-XXXSP(AC pin = "L")
   (b) Auto-clear releasing (AC pin = "H")
   (c) 200 ms waiting state (stabilization period of internal oscillation circuit) Data input is forbidden.
   (d) Set register LEVELn
   (e) Set register PAL/NTSC
   (f) Set register PCn
   (g) 20 ms waiting state (stabilization period of internal oscillation circuit)
   Data input is forbidden.
   (h) Set other registers
   (i) Set SYRAM
   (j) Set display RAM
   (k) Set register DSPON and register DSPONV to display ON

4. Precautions when resuming internal oscillation from the OFF state.
   The internal oscillator circuit stops oscillating when register LEVEL = 1, DSPON = 0, DSPONV = 0 and CS terminal = H.
   When resuming internal oscillation from the OFF state, up until the oscillator circuit stabilizes, data is sometimes not set correctly in the register. Therefore, start oscillation as follows.
   (a) CS pin = "H" (oscillation stop)
   (b) CS pin = "L" (oscillation start)
   (c) 20 ms waiting state (stabilization period of internal oscillation circuit)
   (d) Set register LEVEL 1 = 0
   (e) Set other registers: SYRAM, display RAM
   (f) Set register DSPON and register DSPONV to display ON

5. Note for oscillation
   Make note of the fact that the internal oscillator circuit cannot stabilize in the below situations.
   (a)When the external composite video signal is discontinuous (changing channels etc.)
   (b) When change the setting of register PCn

(c) When change the setting of register LEVELn
When (a)~(c), set the display to OFF by registers DSPON and DSPONV before change the setting. Other registers' settings are forbidden during 20ms after the setting.

6. When no external composite video signal is input (Without a signal, characters cannot be displayed by external synchronization. Therefore, switch to internal synchronization.)

7. When signal level of the external composite video signal is extremely poor (With a weak electric field, character display is uncontrollable by external synchronization. Therefore, switch to internal synchronization.)

8. When a crystal oscillator is connected to OSCIN (22-pin) or OSCOUT (21-pin) (Talk with the manufacturer of the crystal oscillator you are using about matching it to this IC.)

ABSOLUTE MAXIMUM RATINGS (V_{DD} = 5.00V, T_a = − 20°C ~ +70°C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to V_{SS}.	− 0.3 ~ 6.0	V
V_I	Input voltage		V_{SS} − 0.3 < V_I < V_{DD} + 0.3	V
V_O	Output voltage		V_{SS} < V_O < V_{DD}	V
P_d	Power dissipation	T_a = 25°C	300	mW
T_{opr}	Operating temperature		− 20 ~ 70	°C
T_{stg}	Storage temperature		− 40 ~ 125	°C

RECOMMENDED OPERATIONAL CONDITIONS (V_{DD} = 5.00V, T_a = − 20°C ~ +70°C unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{DD}	Supply voltage	4.75	5.00	5.25	V
V_{IH}	"H" level input voltage $\overline{AC}$, $\overline{CS}$, SCK, AD0 ~ AD7	0.8 ✕ V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	"L" level input voltage $\overline{AC}$, $\overline{CS}$, SCK, AD0 ~ AD7	0	0	0.2 ✕ V_{DD}	V
V_{CVIN}	Composite video input supply voltage CVIN	—	2Vp-p	—	V
f_{OSCIN}	Oscillation frequency for synchronous signal	—	3.580 4.434 3.576	—	MHz

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.00V, T_a = +25°C unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	T_a = − 20°C ~ +70°C	4.75	5.00	5.25	V
I_{DD}	Supply current	V_{DD} = 5.00V	—	30	60	mV
V_{OH}	"H" level output voltage P0 ~ P5	V_{DD} = 4.75, I_{OH} = − 0.2mA	3.75	—	—	V
V_{OL}	"L" level output voltage P0 ~ P5	V_{DD} = 4.75, I_{OL} = 0.2mA	—	—	0.4	V
R_I	Pull-up resistance $\overline{AC}$	V_{DD} = 5.00V	10	30	100	kΩ

VIDEO SIGNAL INPUT CONDITIONS (V_{DD} = 5V, T_a = − 20°C ~ +70°C)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{IN-CU}	Composite video signal input clamp supply voltage	Sync-chip supply voltage	—	1.5	—	V

MITSUBISHI ELECTRIC

NOTE FOR SUPPLYING POWER

(1) Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35060-XXXSP is reset when the level of the auto clear input pin $\overline{AC}$ is "L".

This pin is hysteresis input with the pull-up resistor. The timing about power supplying of $\overline{AC}$ pin is shown in Figure 15.

tw is the interval after the supply voltage becomes $0.8 \times V_{DD}$ or more and before the supply voltage to the $\overline{AC}$ pin ($V\overline{AC}$) becomes $0.2 \times V_{DD}$ or more.

After supplying the power (V_{DD} and V_{SS}) to M35060-XXXSP, the tw time must be reserved for 1 ms or more.

Before starting input from the microcomputer, the waiting time (ts) must be reserved for 200 ms after the supply voltage to the $\overline{AC}$ pin becomes 0.8 ¥ V_{DD} or more.

(2) Timing of power supplying to $V_{DD}1$ pin and $V_{DD}2$ pin

The power need to supply to $V_{DD}1$ and $V_{DD}2$ at a time, though it is separated perfectly between the $V_{DD}1$ as the digital line and the $V_{DD}2$ as the analog line.
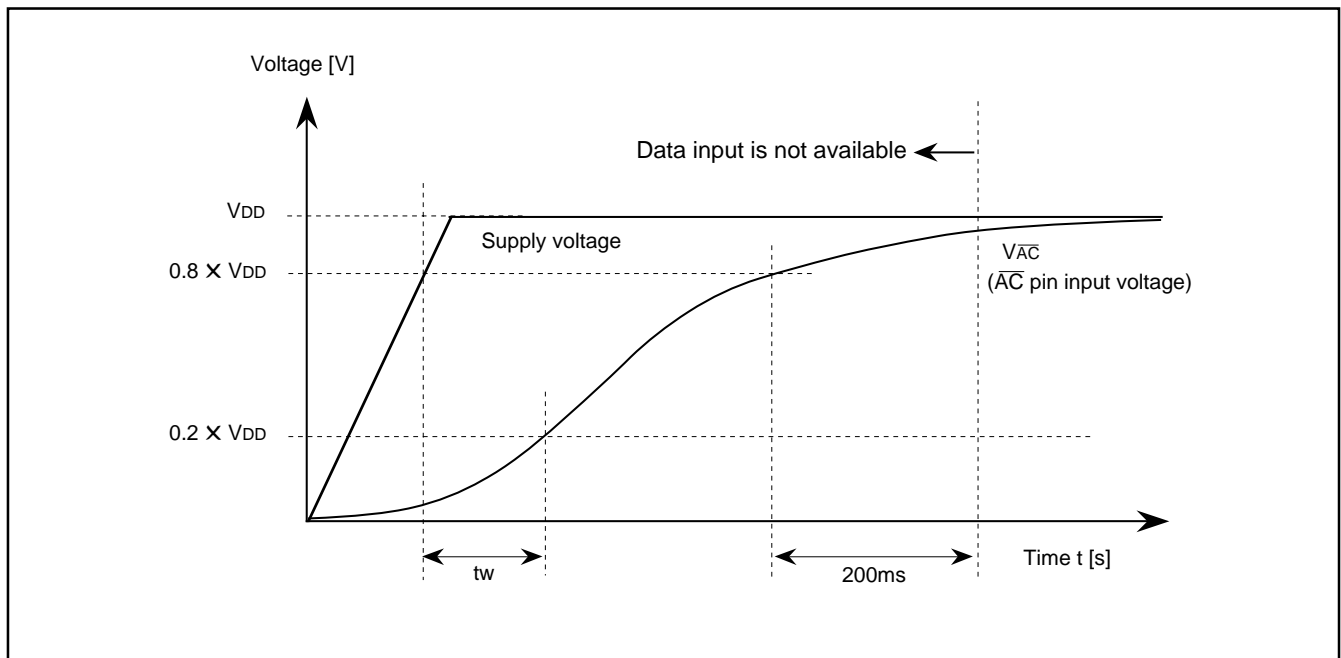
Fig. 15 Timing of power supplying to $\overline{AC}$ pin

PRECAUTIN FOR USE

| Notes on noise and latch-up |

Connect a capacitor (approx. 0.1μF) between pins V_{DD} and V_{SS} at the shortest distance using relatively thick wire to prevent noise and latch up.

ROM ORDERING METHOD

Please submit the information described below when ordering Mask ROM.

(1) ROM Order Confirmation Form 1
(2) Data to be written into mask ROM .... EPROM
(three sets containing the identical data)
(3) Mark Specification Form 1
(4) Program for character font generating + froppy disk in which character data is input.

MITSUBISHI ELECTRIC

STANDARD ROM TYPE: M35060-001SP

M35060-001SP is a standard ROM type of M35060-XXXSP.
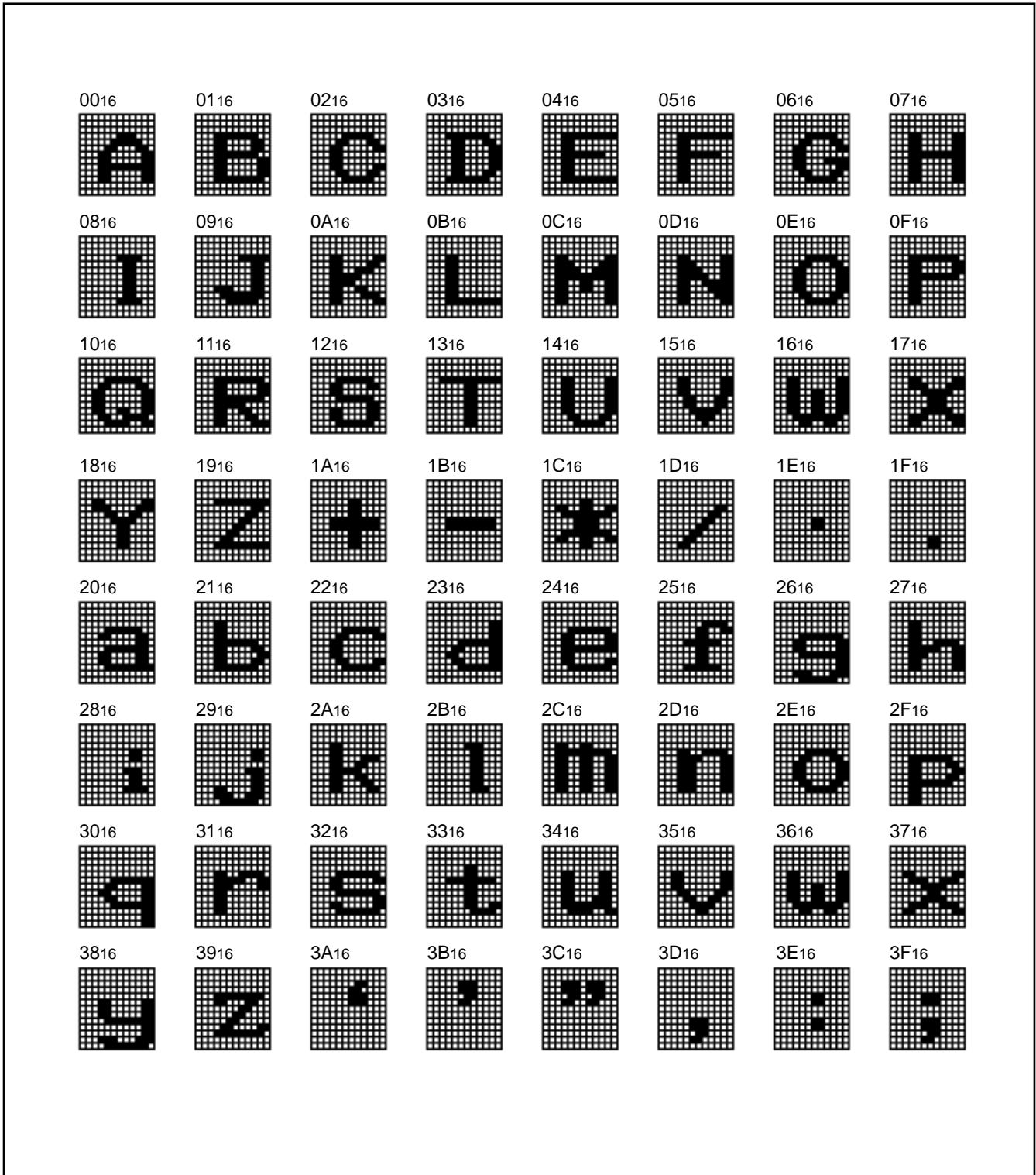
Character patterns are fixed to the contents of Figure 16 to 19.

Fig. 16 M35060-001SP character patterns (1)

Fig. 17 M35060-001SP character patterns (2)

Fig. 18 M35060-001SP character patterns (3)

Fig. 19 M35060-001SP character patterns (4)

STANDARD ROM TYPE: M35060-002SP

M35060-002SP is a standard ROM type of M35060-XXXSP.

Character patterns are fixed to the contents of Figure 20 to 23.
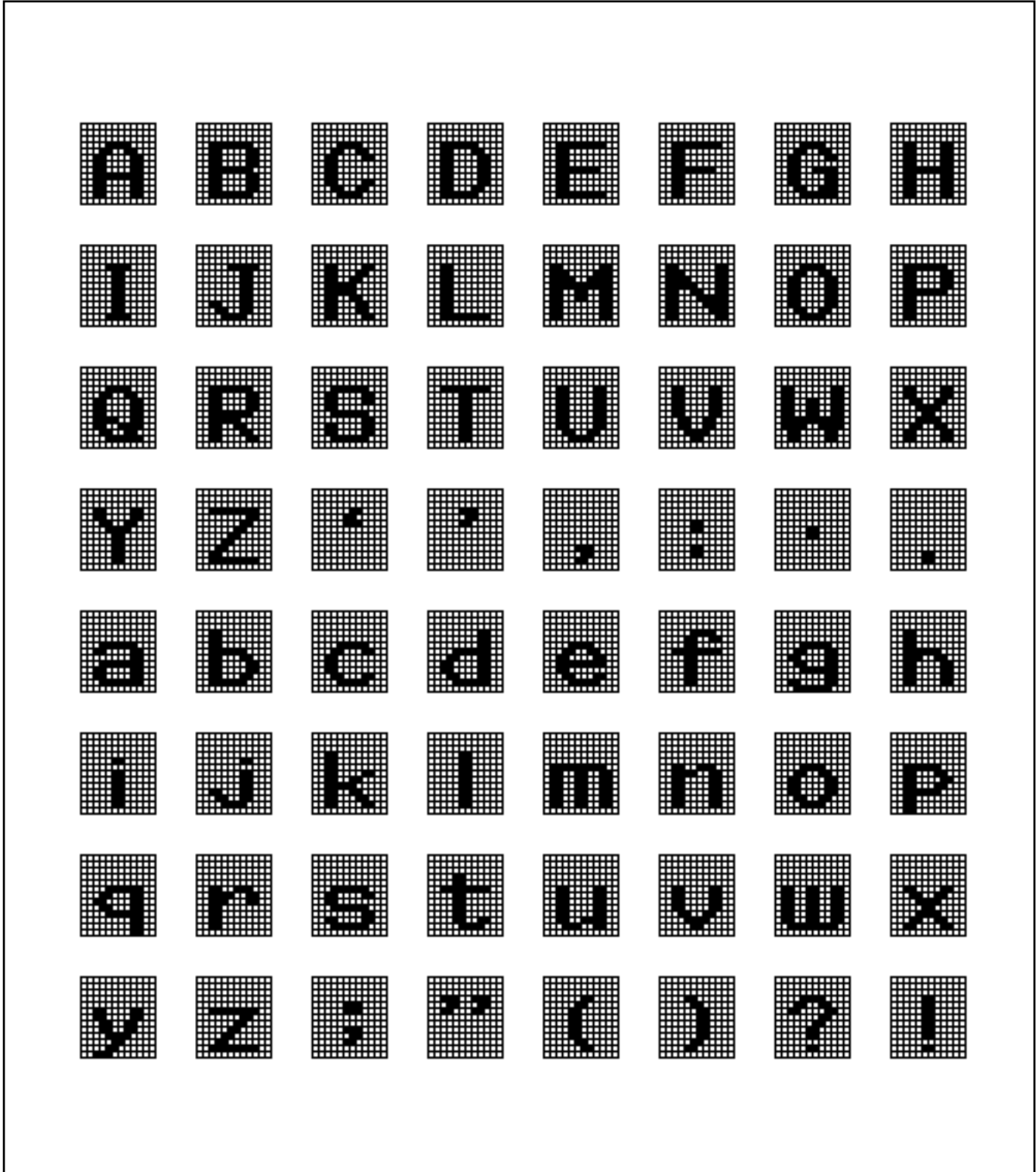
Fig. 20 M35060-002SP character patterns (1)
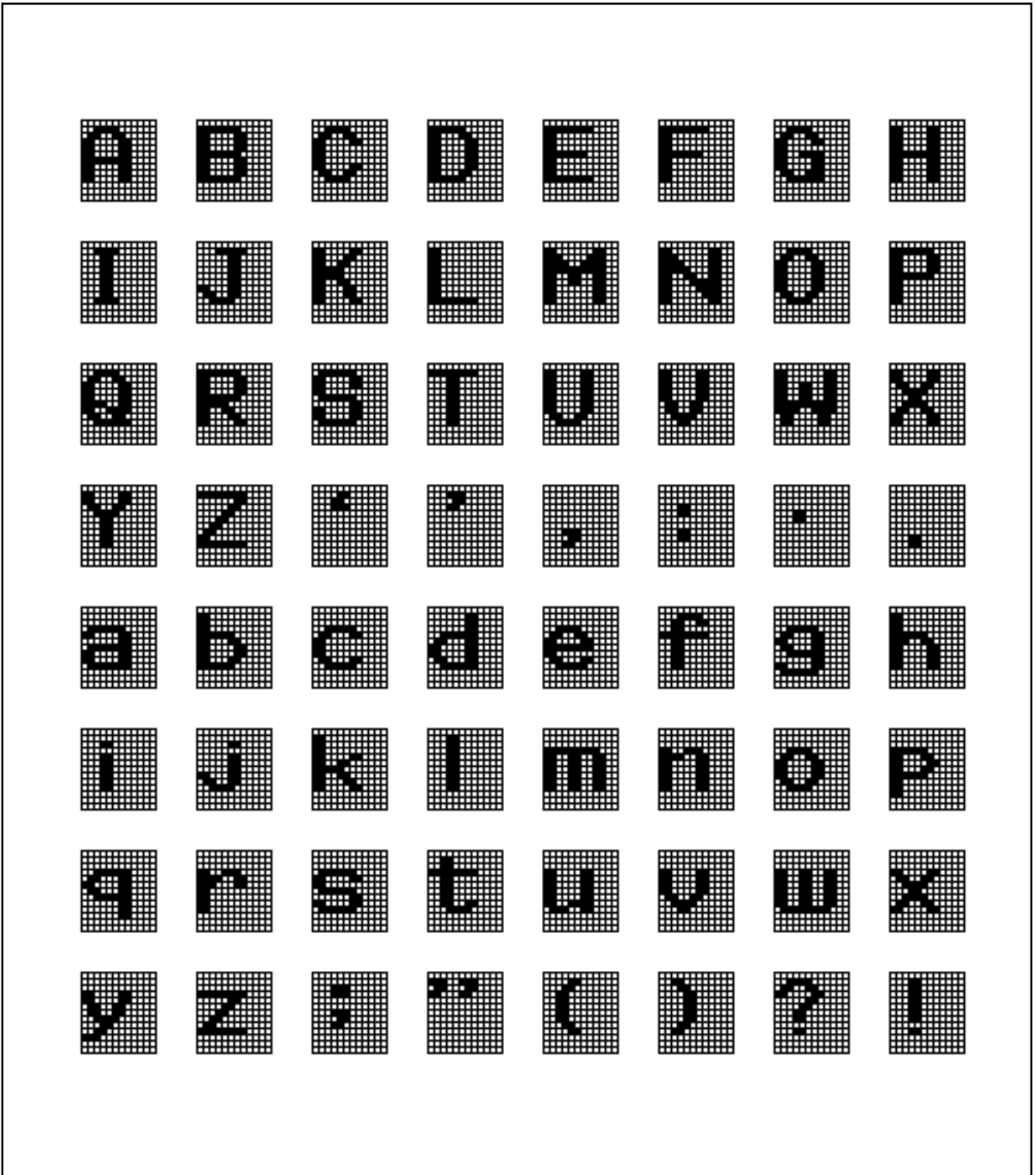
Fig. 21 M35060-002SP character patterns (2)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS
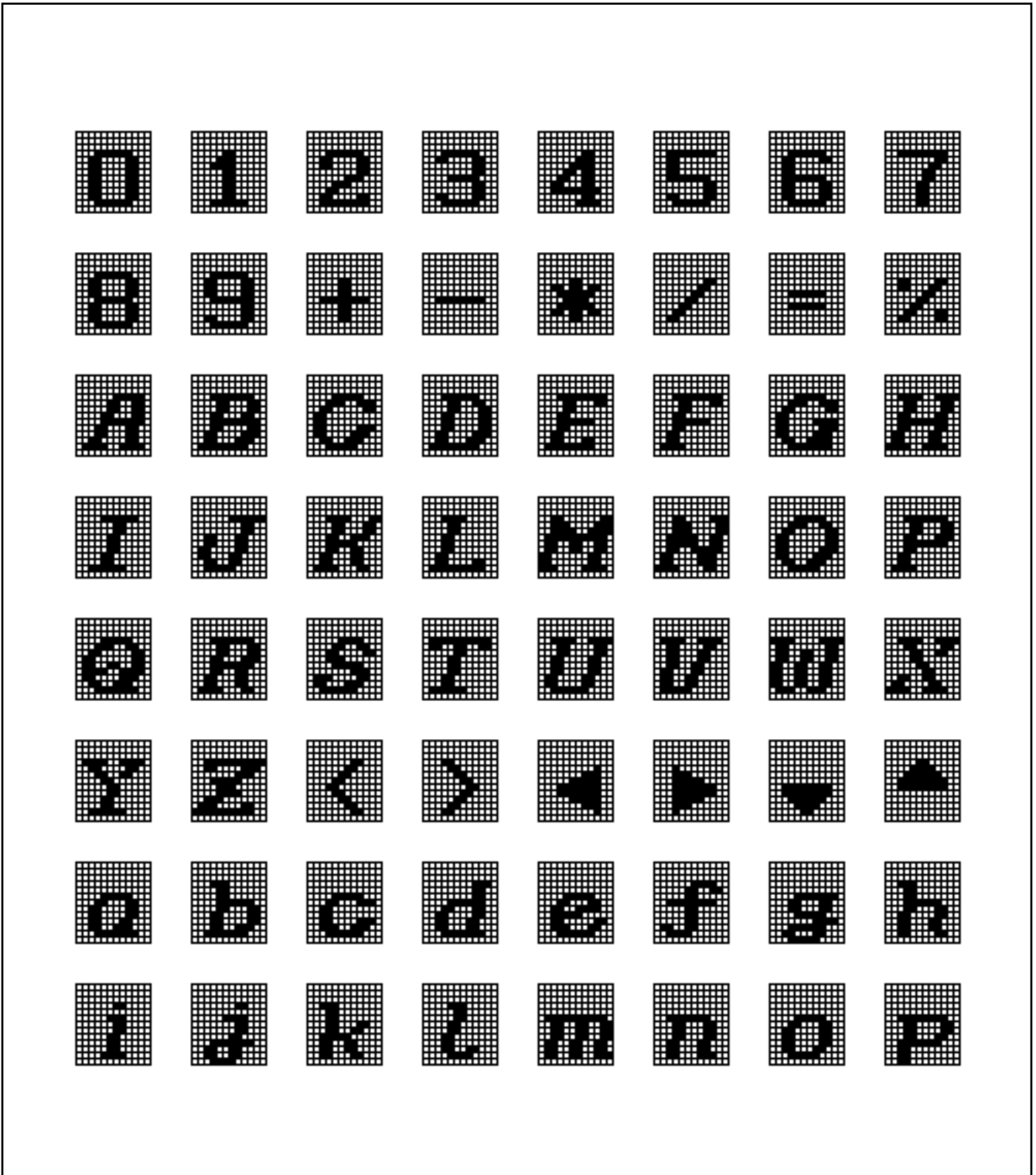
MITSUBISHI MICROCOMPUTERS

M35060-XXXSP

Fig. 22 M35060-002SP character patterns (3)
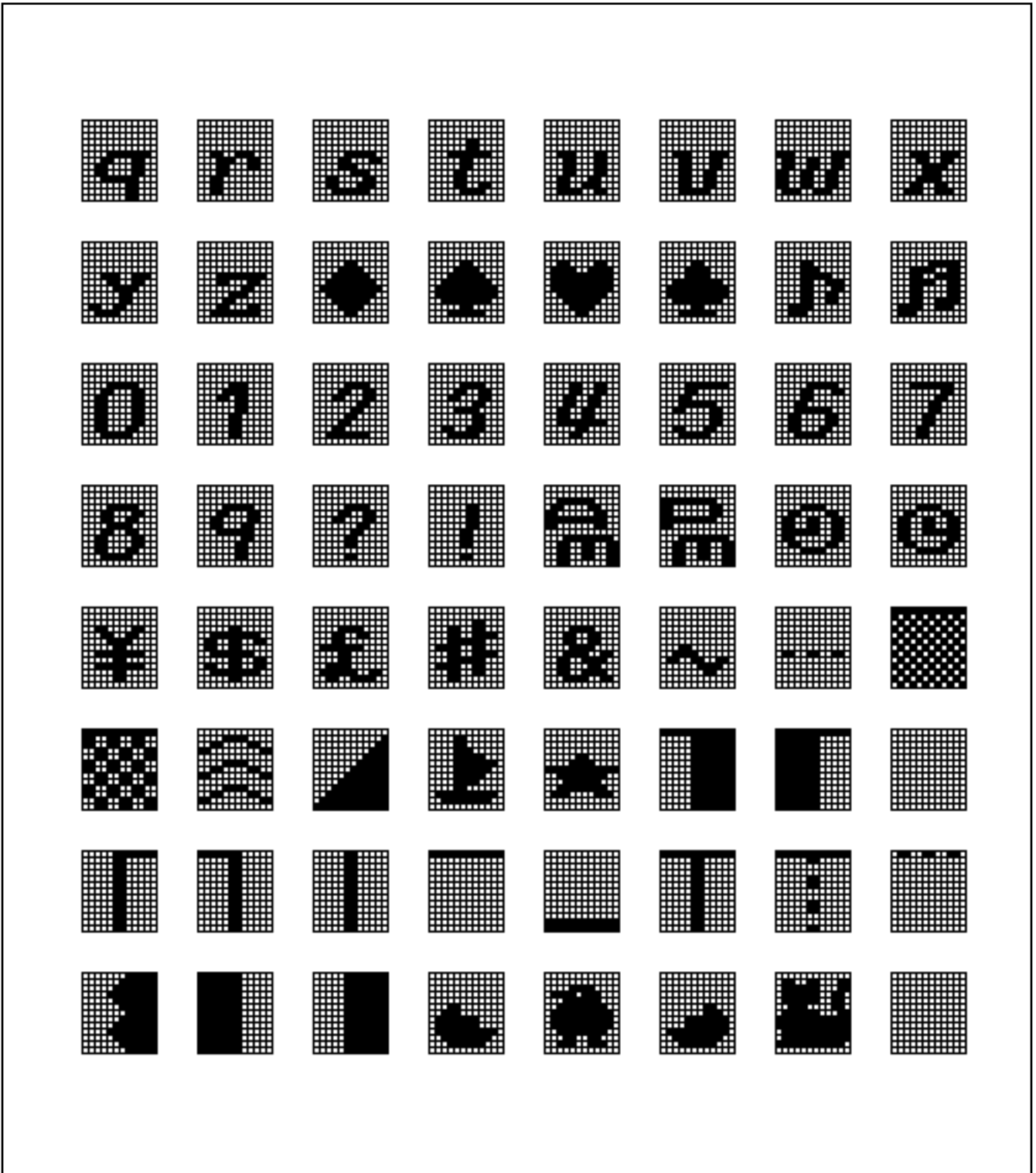
MITSUBISHI ELECTRIC

37

Fig. 23 M35060-002SP character patterns (4)

MITSUBISHI ELECTRIC CORPORATION
HEAD OFFICE: 2-2-3, MARUNOUCHI, CHIYODA-KU, TOKYO 100-8310, JAPAN

MITSUBISHI ELECTRIC