M37224M3-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

DESCRIPTION

The M37224M3-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. They are housed in a 42-pin shrink plastic molded DIP.

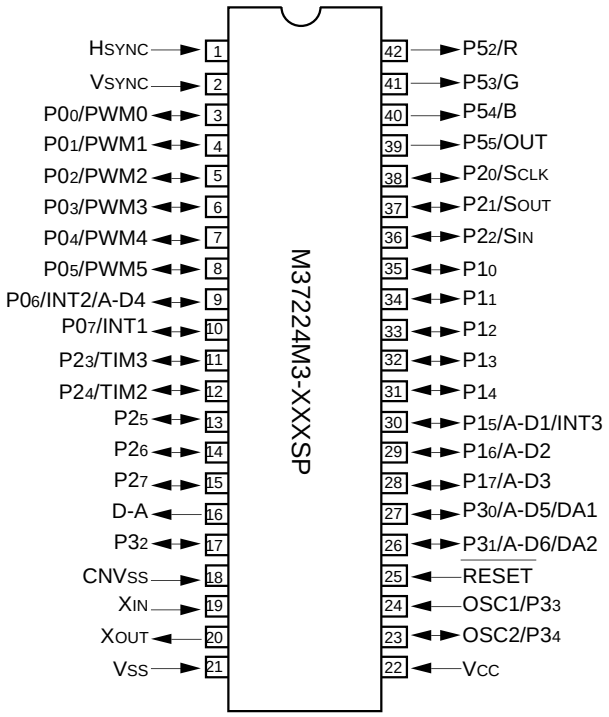
In addition to their simple instruction sets, the ROM, RAM and I/O addresses are placed on the same memory map to enable easy programming.

The M37224M3-XXXSP has a PWM output function and a OSD display function, so it is useful for a channel selection system for TV.

FEATURES

- Number of basic instructions 71
- Memory size
  - ROM ..... 12 K bytes
  - RAM ..... 256 bytes
  - ROM for display ..... 8 K bytes
  - RAM for display ..... 96 bytes
- Minimum instruction execution time
  ..... 0.5 μs (at 8 MHz oscillation frequency)
- Power source voltage ..... 5 V ± 10 %
- Power dissipation ..... 165 mW
  (at 8 MHz oscillation frequency, V_{CC}=5.5V, at CRT display)
- Subroutine nesting ..... 96 levels (maximum)
- Interrupts ..... 13 types, 13 vectors
- 8-bit timers 4
- Programmable I/O ports (Ports P0, P1, P2, $P3_0$–$P3_2$) 27
- Input ports (Ports $P3_3$, $P3_4$) 2
- Output ports (Ports $P5_2$–$P5_5$) 4
- 12 V withstand ports 6
- LED drive ports 4
- Serial I/O ..... 8-bit × 1 channel
- A-D comparator (6-bit resolution) ..... 6 channels
- D-A converter (6-bit resolution) 2
- PWM output circuit ..... 14-bit × 1, 8-bit × 6
- ROM correction function ..... 32 bytes × 2

PIN CONFIGURATION (TOP VIEW)



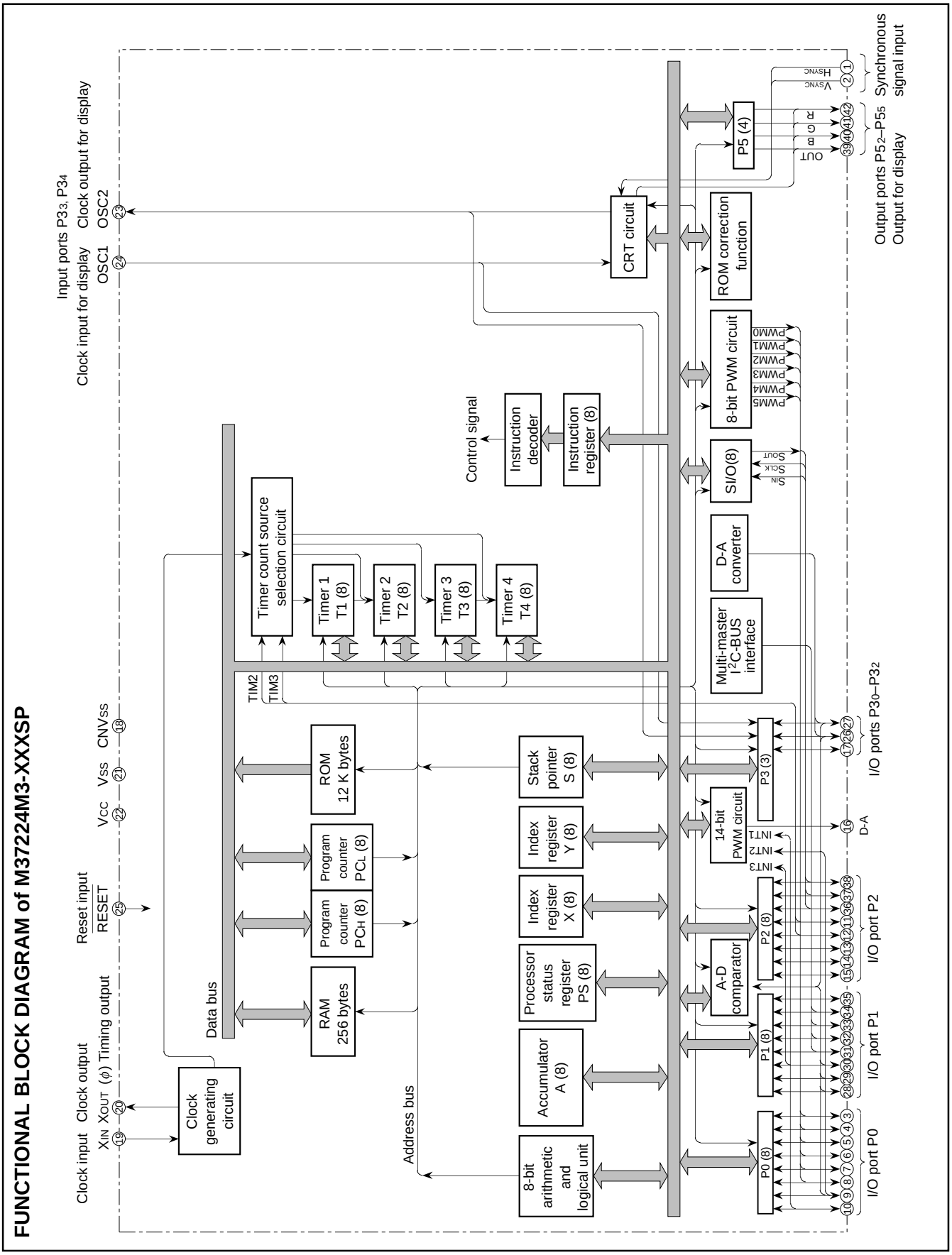
Outline 42P4B

- CRT display function
  - Number of display characters ..... 20 characters × 2 lines (16 lines maximum)
  - Kinds of characters ..... 128 kinds
  - Dot structure ..... 12 × 16 dots
  - Kinds of character sizes ..... 3 kinds
  - Kinds of character colors (It can be specified by the character) maximum 7 kinds (R, G, B)
  - Kinds of raster colors (maximum 7 kinds)
  - Display position
    - Horizontal ..... 64 levels
    - Vertical ..... 128 levels
  - Bordering (horizontal and vertical)

APPLICATION

TV

FUNCTIONAL BLOCK DIAGRAM of M37224M3-XXXSP



FUNCTIONS

Parameter			Functions
Number of basic instructions			71
Instruction execution time			0.5 μs (the minimum instruction execution time, at 8 MHz oscillation frequency)
Clock frequency			8 MHz (maximum)
Memory size	ROM		12 K bytes
	RAM		256 bytes
	CRT ROM		4 K bytes
	CRT RAM		80 bytes
Input/Output ports	P0	I/O	8-bit × 1 (N-channel open-drain output structure, can be used as PWM output pins, INT input pins, A-D input pin)
	$P1_0$–$P1_7$	I/O	8-bit × 1 (CMOS input/output structure, can be used as A-D input pins, INT input pin)
	$P2_0$, $P2_1$	I/O	2-bit × 1 (CMOS input/output or N-channel open-drain output structure, can be used as serial I/O pins)
	$P2_2$–$P2_7$	I/O	6-bit × 1 (CMOS input/output structure, can be used as serial input pin, external clock input pins)
	$P3_0$, $P3_1$	I/O	2-bit × 1 (CMOS input/output or N-channel open-drain output structure, can be used as A-D input pins, D-A conversion output pins)
	$P3_2$	I/O	1-bit × 1 (N-channel open-drain output structure)
	$P3_3$, $P3_4$	Input	2-bit × 1 (can be used as CRT display clock I/O pins)
	$P5_2$–$P5_5$	Output	4-bit × 1 (CMOS output structure, can be used as CRT output pins)
Serial I/O			8-bit × 1
A-D comparator			6 channels (6-bit resolution)
D-A converter			2 (7-bit resolution)
PWM output circuit			14-bit × 1, 8-bit × 6
Timers			8-bit timer × 4
ROM correction function			32 bytes × 2
Subroutine nesting			96 levels (maximum)
Interrupt			External interrupt × 3, Internal timer interrupt × 4, Serial I/O interrupt × 1, CRT interrupt × 1, f(X_{IN})/4096 interrupt × 1, V_{SYNC} interrupt × 1, BRK interrupt × 1
Clock generating circuit			2 built-in circuits (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Power source voltage			5 V ± 10 %
Power dissipation	CRT ON		165 mW typ. (at oscillation frequency f(X_{IN}) = 8 MHz, f_{CRT} = 8 MHz)
	CRT OFF		110 mW typ. (at oscillation frequency f(X_{IN}) = 8 MHz)
	In stop mode		1.65 mW (maximum)
Operating temperature range			–10 °C to 70 °C
Device structure			CMOS silicon gate process
Package			42-pin shrink plastic molded DIP
CRT display function	Number of display characters		20 characters × 2 lines (maximum 16 lines by software)
	Dot structure		12 × 16 dots
	Kinds of characters		128 kinds
	Kinds of character sizes		3 kinds
	Kinds of character colors		Maximum 7 kinds (R, G, B); can be specified by the character
	Display position (horizontal, vertical)		64 levels (horizontal) × 128 levels (vertical)

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Power source		Apply voltage of 5 V ± 10 % (typical) to V_{CC}, and 0 V to V_{SS}.
CNV_{SS}	CNV_{SS}		Connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for 2 μs or more (under normal V_{CC} conditions). If more time is needed for the quartz-crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic resonator or a quartz-crystal oscillator is connected between pins X_{IN} and X_{OUT}. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$P0_0$/PWM0–$P0_5$/PWM5, $P0_6$/INT2/A-D4, $P0_7$/INT1	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open-drain output. See notes at end of Table for full details of port P0 functions.
	PWM output	Output	Pins $P0_0$–$P0_5$ are also used as PWM output pins PWM0–PWM5 respectively. The output structure is N-channel open-drain output.
	External interrupt input	Input	Pins $P0_6$, $P0_7$ are also used as external interrupt input pins INT2, INT1 respectively.
	Analog input	Input	$P0_6$ pin is also used as analog input pin A-D4.
$P1_0$–$P1_4$, $P1_5$/A-D1/INT3, $P1_6$/A-D2, $P1_7$/A-D3	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output.
	Analog input	Input	Pins $P1_5$–$P1_7$ are also used as analog input pins A-D1 to A-D3 respectively.
	External interrupt input	Input	$P1_5$ pin is also used as external interrupt input pin INT3.
$P2_0$/S_{CLK}, $P2_1$/S_{OUT}, $P2_2$/S_{IN}, $P2_3$/TIM3, $P2_4$/TIM2, $P2_5$–$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output.
	External clock input	Input	Pins $P2_3$, $P2_4$ are also used as external clock input pins TIM3, TIM2 respectively.
	Serial I/O synchronous clock input/ output	I/O	$P2_0$ pin is also used as serial I/O synchronous clock input/output pin S_{CLK}. The output structure is N-channel open-drain output.
	Serial I/O data output	Output	Pin $P2_1$ is also used as serial I/O data output pin S_{OUT}. The output structure is N-channel open-drain output.
	Serial I/O data input	Input	Pin $P2_2$ is also used as serial I/O data input pin S_{IN}.
$P3_0$/A-D5/DA1, $P3_1$/A-D6/DA2, $P3_2$	I/O port P3	I/O	Ports $P3_0$–$P3_2$ are 3-bit I/O ports and have basically the same functions as port P0. Either CMOS output or N-channel open-drain output structure can be selected as the port $P3_0$ and $P3_1$. The output structure of port $P3_2$ is N-channel open-drain output.
	Analog input	Input	Pins $P3_0$, $P3_1$ are also used as analog input pins A-D5, A-D6 respectively.
	D-A conversion output	Output	Pins $P3_0$, $P3_1$ are also used as D-A conversion output pins DA1, DA2 respectively.
$P3_3$/OSC1, $P3_4$/OSC2	Input port P3	Input	Ports $P3_3$, $P3_4$ are 2-bit input ports.
	Clock input for CRT display	Input	$P3_3$ pin is also used as CRT display clock input pin OSC1.
	Clock output for CRT display	Output	$P3_4$ pin is also used as CRT display clock output pin OSC2. The output structure is CMOS output.

PIN DESCRIPTION (continued)

Pin	Name	Input/ Output	Functions
$P5_2$/R, $P5_3$/G, $P5_4$/B, $P5_5$/OUT	Output port P5	Output	Ports $P5_2$–$P5_5$ are a 4-bit output port. The output structure is CMOS output.
	CRT output	Output	Pins $P5_2$–$P5_5$ are also used as CRT output pins R, G, B, OUT respectively. The output structure is CMOS output.
H_{SYNC}	H_{SYNC} input	Input	This is a horizontal synchronous signal input for CRT.
V_{SYNC}	V_{SYNC} input	Input	This is a vertical synchronous signal input for CRT.
D-A	DA output	Output	This is a 14-bit PWM output pin.

Note : As shown in the memory map (Figure 5), port P0 is accessed as a memory at address $00C0_{16}$ of zero page. Port P0 has the port P0 direction register (address $00C1_{16}$ of zero page) which can be used to program each bit as an input (“0”) or an output (“1”). The pins programmed as “1” in the direction register are output pins. When pins are programmed as “0,” they are input pins. When pins are programmed as output pins, the output data are written into the port latch and then output. When data is read from the output pins, the output pin level is not read but the data of the port latch is read. This allows a previously-output value to be read correctly even if the output LOW voltage has risen, for example, because a light emitting diode was directly driven. The input pins are float, so the values of the pins can be read. When data is written into the input pin, it is written only into the port latch, while the pin remains in the floating state.

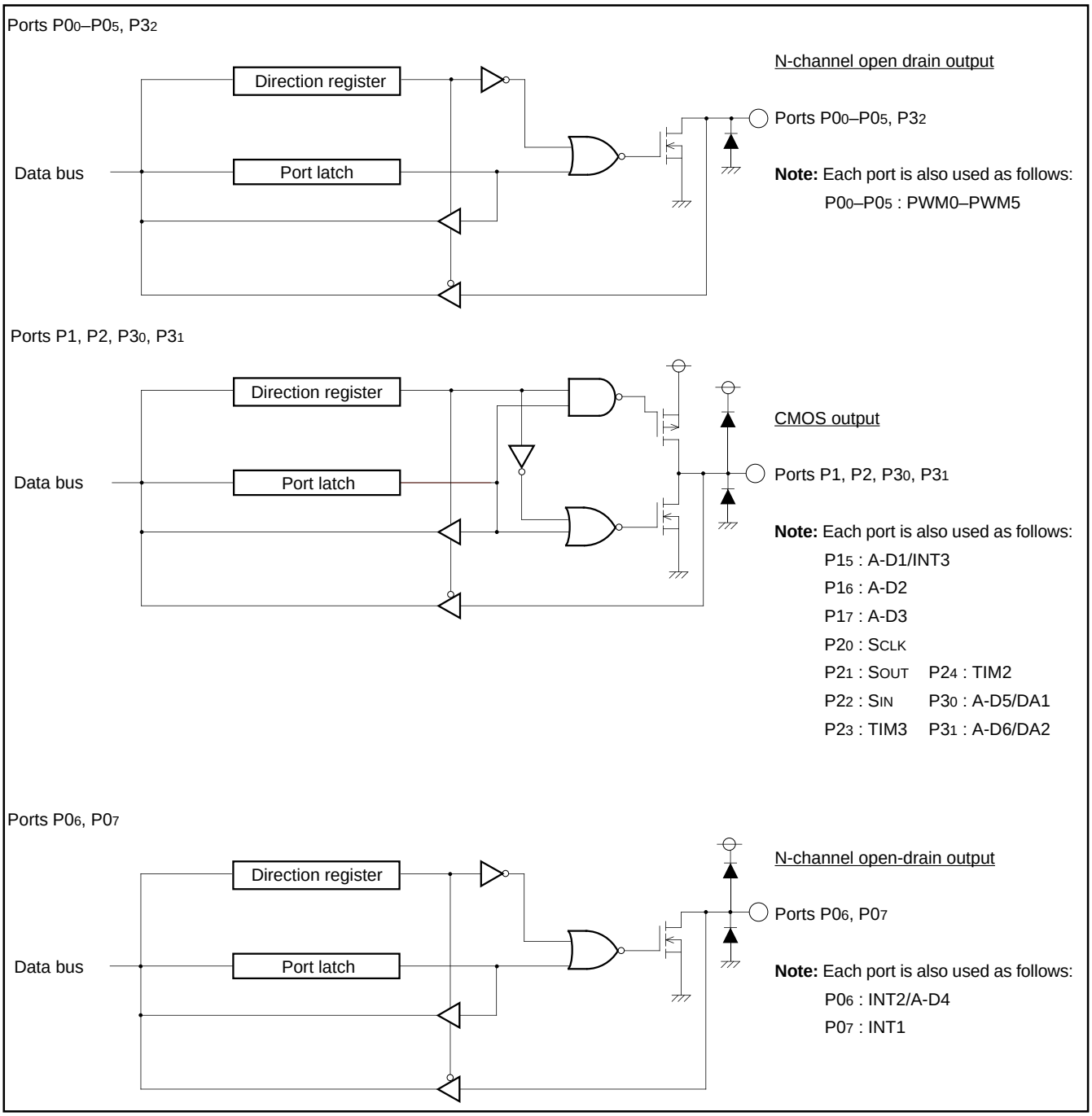


Fig. 1. I/O Pin Block Diagram (1)

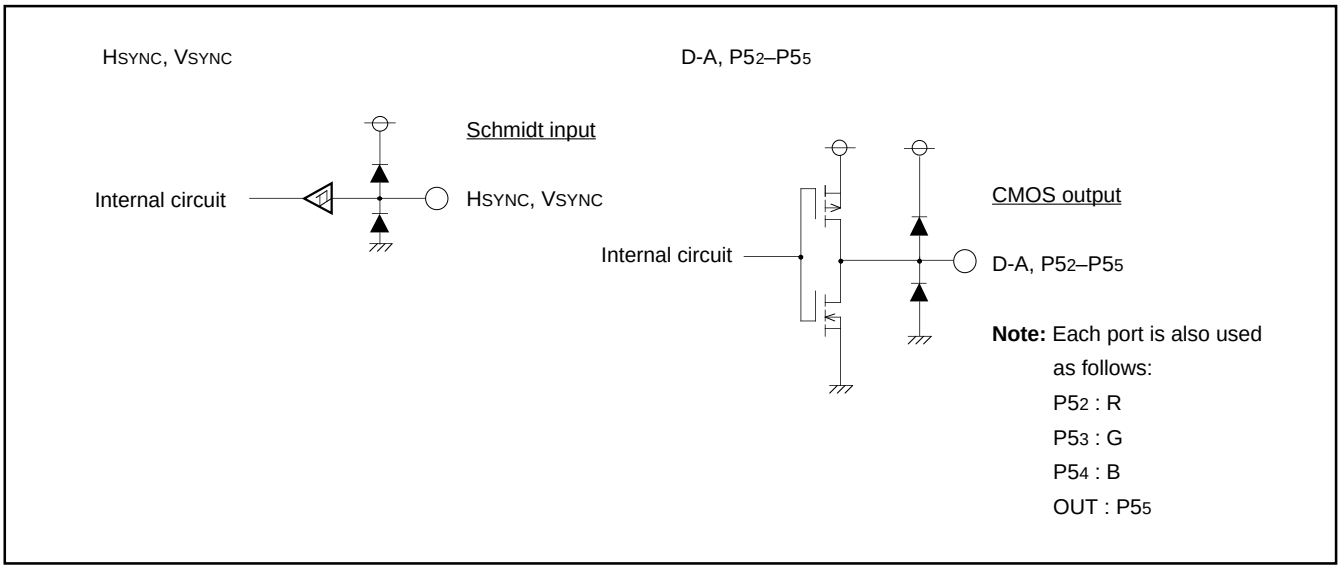


Fig. 2. I/O Pin Block Diagram (2)

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37224M3-XXXSP uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST, SLW instruction cannot be used.

The MUL, DIV, WIT and STP instructions can be used.

CPU Mode Register

The CPU mode register contains the stack page selection bit. The CPU mode register is allocated at address 00FB16.

CPU Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1	1		0	0

CPU mode register (CPUM (CM)) [Address FB16]

B	Name	Functions	After reset	R	W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: 1 0: 1 1: } Not available	0	R	W
2	Stack page selection bit (CM2) (See note)	0: 0 page 1: 1 page	1	R	W
3 to 7	Fix these bits to "1."		1	R	W

Note: This bit is set to "1" after the reset release.

Fig. 3. CPU Mode Register

MEMORY

Special Function Register (SFR) Area
The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

RAM
RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM
ROM is used for storing user programs as well as the interrupt vector area.

RAM for Display
RAM for display is used for specifying the character codes and colors to display.

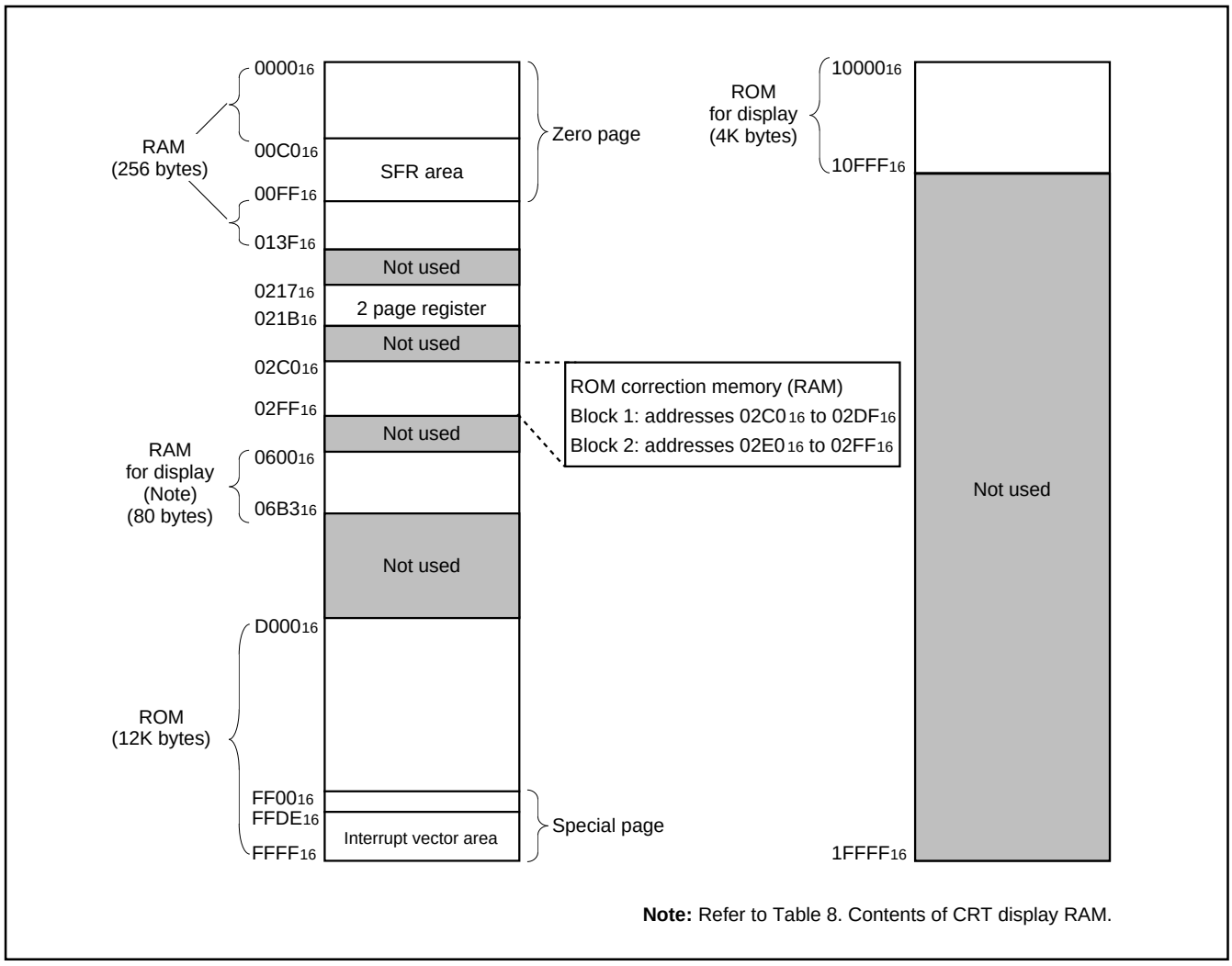
ROM for Display
ROM for display is used for storing character data.

Interrupt Vector Area
The interrupt vector area contains reset and interrupt vectors.

Zero Page
The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page
The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

ROM Correction Memory (RAM)
This is used as the program area for ROM correction.



Note: Refer to Table 8. Contents of CRT display RAM.

Fig. 4. Memory Map

■SFR Area (addresses $C0_{16}$ to DF_{16})

<Bit allocation>

: } Function bit

Name : } Function bit

: No function bit

0 : Fix this bit to "0" (do not write "1")

1 : Fix this bit to "1" (do not write "0")

<State immediately after reset>

0 : "0" immediately after reset

1 : "1" immediately after reset

? : Undefined immediately after reset

Address	Register	Bit allocation b7	b6	b5	b4	b3	b2	b1	b0	State immediately after reset b7	b6	b5	b4	b3	b2	b1	b0
$C0_{16}$	Port P0 (P0)									?							
$C1_{16}$	Port P0 direction register (D0)									00_{16}							
$C2_{16}$	Port P1 (P1)									?							
$C3_{16}$	Port P1 direction register (D1)									00_{16}							
$C4_{16}$	Port P2 (P2)									?							
$C5_{16}$	Port P2 direction register (D2)									00_{16}							
$C6_{16}$	Port P3 (P3)									0	0	0	?	?	?	?	?
$C7_{16}$	Port P3 direction register (D3)									00_{16}							
$C8_{16}$										?							
$C9_{16}$										?							
CA_{16}	Port P5 (P5)									0	0	?	?	?	?	?	?
CB_{16}	Port P5 direction register (D5)									00_{16}							
CC_{16}										?							
CD_{16}	Port P3 output mode control register (P3S)					DA2S	DA1S	P31S	P30S	00_{16}							
CE_{16}	DA-H register (DA-H)									?							
CF_{16}	DA-L register (DA-L)									0	0	?	?	?	?	?	?
$D0_{16}$	PWM0 register (PWM0)									?							
$D1_{16}$	PWM1 register (PWM1)									?							
$D2_{16}$	PWM2 register (PWM2)									?							
$D3_{16}$	PWM3 register (PWM3)									?							
$D4_{16}$	PWM4 register (PWM4)									?							
$D5_{16}$	PWM output control register 1 (PW)	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0	00_{16}							
$D6_{16}$	PWM output control register 2 (PN)				PN4	PN3	PN2			00_{16}							
$D7_{16}$										?							
$D8_{16}$										?							
$D9_{16}$										?							
DA_{16}										?							
DB_{16}										?							
DC_{16}	Serial I/O mode register (SM)		SM6	SM5	0	SM3	SM2	SM1	SM0	00_{16}							
DD_{16}	Serial I/O regsiter (SIO)									?							
DE_{16}	DA1 conversion register (DA1)	DA17	0	DA15	DA14	DA13	DA12	DA11	DA10	?							
DF_{16}	DA2 conversion register (DA2)	DA27	0	DA25	DA24	DA23	DA22	DA21	DA20	?							

Fig. 5. Memory Map of SFR (special function register) (1)

■SFR Area (addresses $E0_{16}$ to FF_{16})

<Bit allocation>

: } Function bit

Name : } Function bit

: No function bit

0 : Fix this bit to "0" (do not write "1")

1 : Fix this bit to "1" (do not write "0")

<State immediately after reset>

0 : "0" immediately after reset

1 : "1" immediately after reset

? : Undefined immediately after reset

Address	Register	Bit allocation b7							b0	State immediately after reset b7							b0
$E0_{16}$	Horizontal register (HR)			HR5	HR4	HR3	HR2	HR1	HR0	00_{16}							
$E1_{16}$	Vertical register 1 (CV1)		CV16	CV15	CV14	CV13	CV12	CV11	CV10	0	?	?	?	?	?	?	?
$E2_{16}$	Vertical register 1 (CV1)		CV26	CV25	CV24	CV23	CV22	CV21	CV20	0	?	?	?	?	?	?	?
$E3_{16}$										?							
$E4_{16}$	Character size register (CS)					CS21	CS20	CS11	CS10	0	0	0	0	?	?	?	?
$E5_{16}$	Border selection register (MD)						MD20		MD10	0	0	0	0	0	?	0	?
$E6_{16}$	Color register 0 (CO0)			CO05		CO03	CO02	CO01	0	00_{16}							
$E7_{16}$	Color register 1 (CO1)			CO15		CO13	CO12	CO11	0	00_{16}							
$E8_{16}$	Color register 2 (CO2)			CO25		CO23	CO22	CO21	0	00_{16}							
$E9_{16}$	Color register 3 (CO3)			CO35		CO33	CO32	CO31	0	00_{16}							
EA_{16}	CRT control register (CO)						CC2	CC1	CC0	00_{16}							
EB_{16}										?							
EC_{16}	CRT port control register (CRTP)	OP7	OP6	OP5	OUT		R/G/B	VSYC	HSYC	00_{16}							
ED_{16}	CRT clock selection register (CK)	0	0	0	0	0	0	CK1	CK0	00_{16}							
EE_{16}	A-D control register 1 (AD1)				ADM4		ADM2	ADM1	ADM0	0	0	0	?	0	0	0	0
EF_{16}	A-D control register 2 (AD2)			ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	00_{16}							
$F0_{16}$	Timer 1 (TM1)									FF_{16}							
$F1_{16}$	Timer 2 (TM2)									07_{16}							
$F2_{16}$	Timer 3 (TM3)									FF_{16}							
$F3_{16}$	Timer 4 (TM4)									07_{16}							
$F4_{16}$	Timer 12 mode register (T12M)			0	T12M4	T12M3	T12M2	T12M1	T12M0	00_{16}							
$F5_{16}$	Timer 34 mode register (T34M)			T34M5	T34M4	T34M3	T34M2	T34M1	T34M0	00_{16}							
$F6_{16}$	PWM5 register (PWM5)									?							
$F7_{16}$										?							
$F8_{16}$										?							
$F9_{16}$	Interrupt input polarity register (RE)	0		RE5	RE4	RE3	0	0		0	0	0	0	0	0	0	?
FA_{16}	Test register (TEST)	00_{16}								00_{16}							
FB_{16}	CPU mode register (CPUM)	1	1	1	1	1	CM2	0	0	FC_{16}							
FC_{16}	Interrupt request register 1 (IREQ1)	IT3R		VSCR	CRTR	TM4R	TM3R	TM2R	TM1R	00_{16}							
FD_{16}	Interrupt request register 2 (IREQ2)	0			MSR		S1R	IT2R	IT1R	00_{16}							
FE_{16}	Interrupt control register 1 (ICON1)	IT3E		VSCE	CRTE	TM4E	TM3E	TM2E	TM1E	00_{16}							
FF_{16}	Interrupt control register 2 (ICON2)	0	0	0	MSE	0	S1E	IT2E	IT1E	00_{16}							

Fig. 6. Memory Map of SFR (special function register) (2)

■SFR Area (addresses 217_{16} to $21B_{16}$)

<Bit allocation>

: } Function bit
Name : }

: No function bit

0 : Fix this bit to "0" (do not write "1")

1 : Fix this bit to "1" (do not write "0")

<State immediately after reset>

0 : "0" immediately after reset

1 : "1" immediately after reset

? : Undefined immediately after reset

Address	Register	Bit allocation b7 b0	State immediately after reset b7 b0
217_{16}	ROM correction address 1 (high-order)		00
218_{16}	ROM correction address 1 (low-order)		00
219_{16}	ROM correction address 2 (high-order)		00
$21A_{16}$	ROM correction address 2 (low-order)		00
$21B_{16}$	ROM correction enable register (RCR)	— — — — 0 0 RC1 RC0	? ? ? ? 0 0 0 0

Fig. 7. Memory Map of 2 Page Register

<Bit allocation>

: } Function bit
Name : }

: No function bit

0 : Fix this bit to "0" (do not write "1")

1 : Fix this bit to "1" (do not write "0")

<State immediately after reset>

0 : "0" immediately after reset

1 : "1" immediately after reset

? : Undefined immediately after reset

Register	Bit allocation b7 b0	State immediately after reset b7 b0
Processor status register (PS)	N V T B D I Z C	? ? ? ? ? 1 ? ?
Program counter (PC_H)		Contents of address $FFFF_{16}$
Program counter (PC_L)		Contents of address $FFFE_{16}$

Fig. 8. Internal State of Processor Status Register and Program Counter at Reset

INTERRUPTS

Interrupts can be caused by 13 different sources consisting of 4 external, 7 internal, 1 software, and reset. Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted,

(1) The contents of the program counter and processor status register are automatically stored into the stack.
(2) The interrupt disable flag I is set to "1" and the corresponding interrupt request bit is set to "0."
(3) The jump destination address stored in the vector address enters the program counter.

Other interrupts are disabled when the interrupt disable flag is set to "1."

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figures 10 to 14 show the interrupt-related registers.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1," interrupt request bit is "1," and the interrupt disable flag is "0." The interrupt request bit can be set to "0" by a program, but not set to "1." The interrupt enable bit can be set to "0" and "1" by a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 9 shows interrupt control.

Interrupt Causes

(1) VSYNC and CRT interrupts
The VSYNC interrupt is an interrupt request synchronized with the vertical sync signal.
The CRT interrupt occurs after character block display to the CRT is completed.

(2) INT1, INT2, INT3 interrupts
With an external interrupt input, the system detects that the level of a pin changes from "L" to "H" or from "H" to "L," and generates an interrupt request. The input active edge can be selected by bits 3, 4 and 5 of the interrupt input polarity register (address $00F9_{16}$) : when this bit is "0," a change from "L" to "H" is detected; when it is "1," a change from "H" to "L" is detected. Note that all bits are cleared to "0" at reset.

(3) Timer 1, 2, 3 and 4 interrupts
An interrupt is generated by an overflow of timer 1, 2, 3 or 4.

(4) Serial I/O interrupt
This is an interrupt request from the clock synchronous serial I/O function.

Table 1. Interrupt Vector Addresses and Priority

Interrupt Source	Priority	Vector Addresses	Remarks
Reset	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
CRT interrupt	2	$FFFD_{16}$, $FFFC_{16}$	
INT2 interrupt	3	$FFFB_{16}$, $FFFA_{16}$	Active edge selectable
INT1 interrupt	4	$FFF9_{16}$, $FFF8_{16}$	Active edge selectable
Timer 4 interrupt	5	$FFF5_{16}$, $FFF4_{16}$	
f(XIN)/4096 interrupt	6	$FFF3_{16}$, $FFF2_{16}$	
VSYNC interrupt	7	$FFF1_{16}$, $FFF0_{16}$	Active edge selectable
Timer 3 interrupt	8	$FFEF_{16}$, $FFEE_{16}$	
Timer 2 interrupt	9	$FFED_{16}$, $FFEC_{16}$	
Timer 1 interrupt	10	$FFEB_{16}$, $FFEA_{16}$	
Serial I/O interrupt	11	$FFE9_{16}$, $FFE8_{16}$	
INT3 interrupt	12	$FFE5_{16}$, $FFE4_{16}$	Active edge selectable
BRK instruction interrupt	13	$FFDF_{16}$, $FFDE_{16}$	Non-maskable (software interrupt)

(5) f(XIN)/4096 interrupt
This interrupt occurs regularly with a f(XIN)/4096 period. Set bit 0 of the PWM output control register 1 to "0."

(6) BRK instruction interrupt
This software interrupt has the least significant priority. It does not have a corresponding interrupt enable bit, and it is not affected by the interrupt disable flag I (non-maskable).

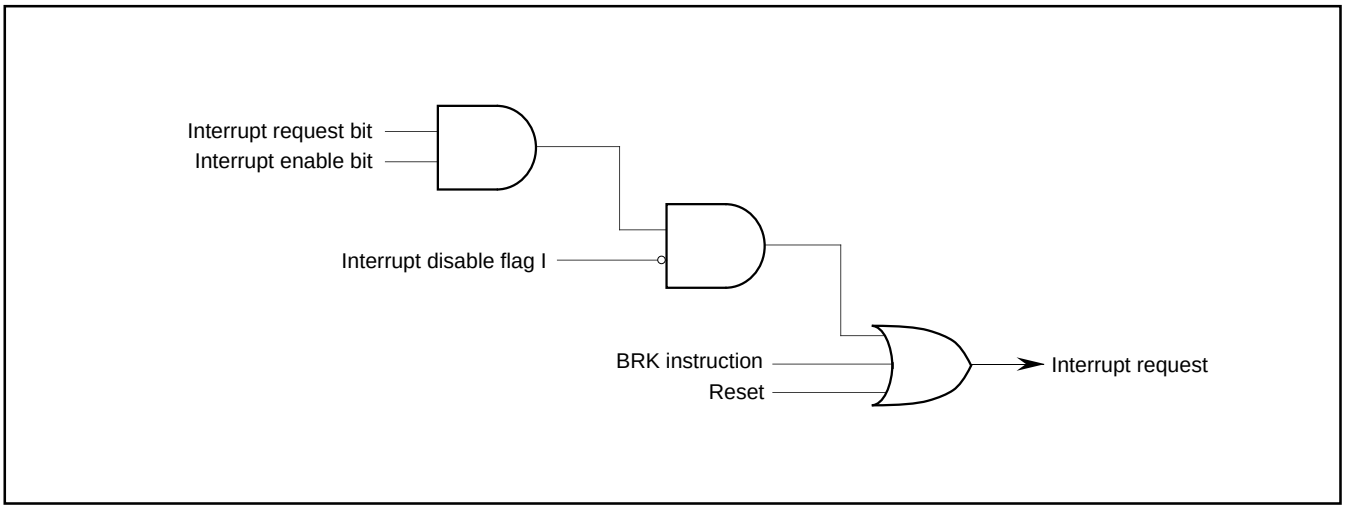
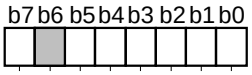


Fig. 9. Interrupt Control

Interrupt Request Register 1

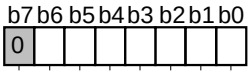


Interrupt request register 1 (IREQ1) [Address 00FC16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
4	CRT interrupt request bit (CRTR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
5	VSYNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—
7	INT3 interrupt request bit (IT3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻

Fig. 10. Interrupt Request Register 1

Interrupt Request Register 2



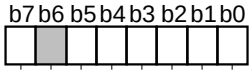
Interrupt request register 2 (IREQ2) [Address 00FD16]

B	Name	Functions	After reset	R	W
0	INT1 interrupt request bit (ITIR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	INT2 interrupt request bit (IT2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Serial I/O interrupt request bit (SIR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3, 5, 6	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—
4	f(XIN)/4096 interrupt request bit (MSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
7	Fix this bit to “0.”		0	R	W

✻: “0” can be set by software, but “1” cannot be set.

Fig. 11. Interrupt Request Register 2

Interrupt Control Register 1

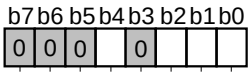


Interrupt control register 1 (ICON1) [Address 00FE16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt enable bit (TM1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Timer 2 interrupt enable bit (TM2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Timer 3 interrupt enable bit (TM3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	Timer 4 interrupt enable bit (TM4E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	CRT interrupt enable bit (CRTE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	VSYNC interrupt enable bit (VSCE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—
7	INT3 interrupt enable bit (IN3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W

Fig. 12. Interrupt Control Register 1

Interrupt Control Register 2

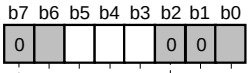


Interrupt control register 2 (ICON2) [Address 00FF16]

B	Name	Functions	After reset	R	W
0	INT1 interrupt enable bit (IT1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	INT2 interrupt enable bit (IT2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Serial I/O interrupt enable bit (SIE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3, 5 to 7	Fix these bits to “0.”		0	R	W
4	f(XIN)/4096 interrupt enable bit (MSE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W

Fig. 13. Interrupt Control Register 2

Interrupt Input Polarity Register



Interrupt input polarity register(RE) [Address 00F9 16]

B	Name	Functions	After reset	R	W
0	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		Indeterminate	R	—
1, 2	Fix these bits to “0.”		0	R	W
3	INT1 polarity switch bit (RE3)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	INT2 polarity switch bit (RE4)	0 : Positive polarity 1 : Negative polarity	0	R	W
5	INT3 polarity switch bit (RE5)	0 : Positive polarity 1 : Negative polarity	0	R	W
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—
7	Fix this bit to “0.”		0	R	W

Fig. 14. Interrupt Input Polarity Register

TIMERS

The M37224M3-XXXSP has 4 timers: timer 1, timer 2, timer 3, and timer 4. All timers are 8-bit timer with the 8-bit timer latch. The timer block diagram is shown in Figure 17.

All of the timers count down and their divide ratio is 1/(n+1), where n is the value of timer latch. By writing a count value to the corresponding timer latch (addresses $00F0_{16}$ to $00F3_{16}$), the value is also set to a timer, simultaneously.

The count value is decremented by 1. The timer interrupt request bit is set to "1" by a timer overflow at the next count pulse, after the count value reaches "00_{16}".

(1) Timer 1

Timer 1 can select one of the following count sources:

- f(X_{IN})/16
- f(X_{IN})/4096

The count source of timer 1 is selected by setting bit 0 of the timer 12 mode register (address $00F4_{16}$).

Timer 1 interrupt request occurs at timer 1 overflow.

(2) Timer 2

Timer 2 can select one of the following count sources:

- f(X_{IN})/16
- Timer 1 overflow signal
- External clock from the TIM2 pin

The count source of timer 2 is selected by setting bits 1 and 4 of timer 12 mode register (address $00F4_{16}$). When timer 1 overflow signal is a count source for timer 2, timer 1 functions as an 8-bit prescaler.

Timer 2 interrupt request occurs at timer 2 overflow.

(3) Timer 3

Timer 3 can select one of the following count sources:

- f(X_{IN})/16
- External clock from the H_{SYNC} pin
- External clock from the TIM3 pin

The count source of timer 3 is selected by setting bits 0 and 5 of timer 34 mode register (address $00F5_{16}$)

Timer 3 interrupt request occurs at timer 3 overflow.

(4) Timer 4

Timer 4 can select one of the following count sources:

- f(X_{IN})/16
- f(X_{IN})/2
- Timer 3 overflow signal

The count source of timer 3 is selected by setting bits 1 and 4 of timer 34 mode register (address $00F5_{16}$). When timer 3 overflow signal is a count source for timer 4, timer 3 functions as an 8-bit prescaler.

Timer 4 interrupt request occurs at timer 4 overflow.

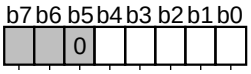
At reset, timers 3 and 4 are connected by hardware and "FF_{16}" is automatically set in timer 3; "07_{16}" in timer 4. The f(X_{IN})/16 is selected as the timer 3 count source. The internal reset is released by timer 4 overflow in this state and the internal clock is connected.

At execution of the STP instruction, timers 3 and 4 are connected by hardware and "FF_{16}" is automatically set in timer 3; "07_{16}" in timer 4. However, the f(X_{IN})/16 is not selected as the timer 3 count source. So set bit 0 of timer 34 mode register (address $00F5_{16}$) to "0" before execution of the STP instruction (f(X_{IN})/16 is selected as the timer 3 count source). The internal STP state is released by timer 4 overflow in this state and the internal clock is connected.

As a result of the above procedure, the program can start under a stable clock.

Timer-related registers are shown in Figures 15 and 16.

Timer 12 Mode Register

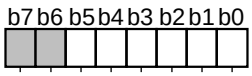


Timer 12 mode register (T12M) [Address $00F4_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 1 count source selection bit (T12M0)	0: $f(X_{IN})/16$ 1: $f(X_{IN})/4096$	0	R	W
1	Timer 2 count source selection bit (T12M1)	0: Internal clock 1: External clock from TIM2 pin	0	R	W
2	Timer 1 count stop bit (T12M2)	0: Count start 1: Count stop	0	R	W
3	Timer 2 count stop bit (T12M3)	0: Count start 1: Count stop	0	R	W
4	Timer 2 internal count source selection bit (T12M4)	0: $f(X_{IN})/16$ 1: Timer 1 overflow	0	R	W
5	Fix this bit to "0."		0	R	W
6,7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Fig. 15. Timer 12 Mode Register

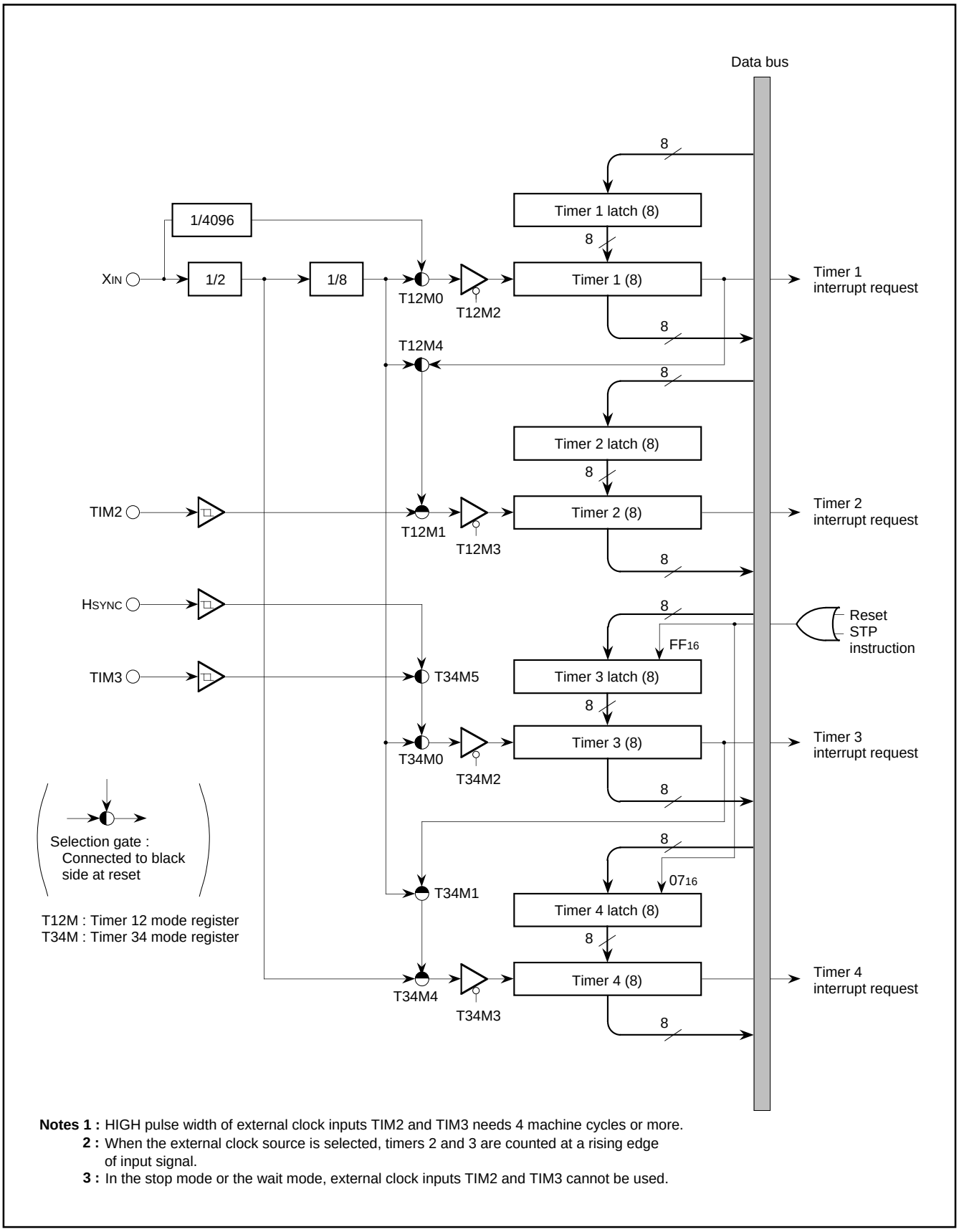
Timer 34 Mode Register



Timer 34 mode register (T34M) [Address $00F5_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 3 count source selection bit (T34M0)	0: $f(X_{IN})/16$ 1: External clock	0	R	W
1	Timer 4 internal count source selection bit (T34M1)	0: Timer 3 overflow 1: $f(X_{IN})/16$	0	R	W
2	Timer 3 count stop bit (T34M2)	0: Count start 1: Count stop	0	R	W
3	Timer 4 count stop bit (T34M3)	0: Count start 1: Count stop	0	R	W
4	Timer 4 count source selection bit (T34M4)	0: Internal clock 1: $f(X_{IN})/2$	0	R	W
5	Timer 3 external count source selection bit (T34M5)	0: External clock from TIM3 pin 1: External clock from H_{SYNC} pin	0	R	W
6,7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Fig. 16. Timer 34 Mode Register



Notes 1 : HIGH pulse width of external clock inputs TIM2 and TIM3 needs 4 machine cycles or more.
2 : When the external clock source is selected, timers 2 and 3 are counted at a rising edge of input signal.
3 : In the stop mode or the wait mode, external clock inputs TIM2 and TIM3 cannot be used.

Fig. 17. Timer Block Diagram

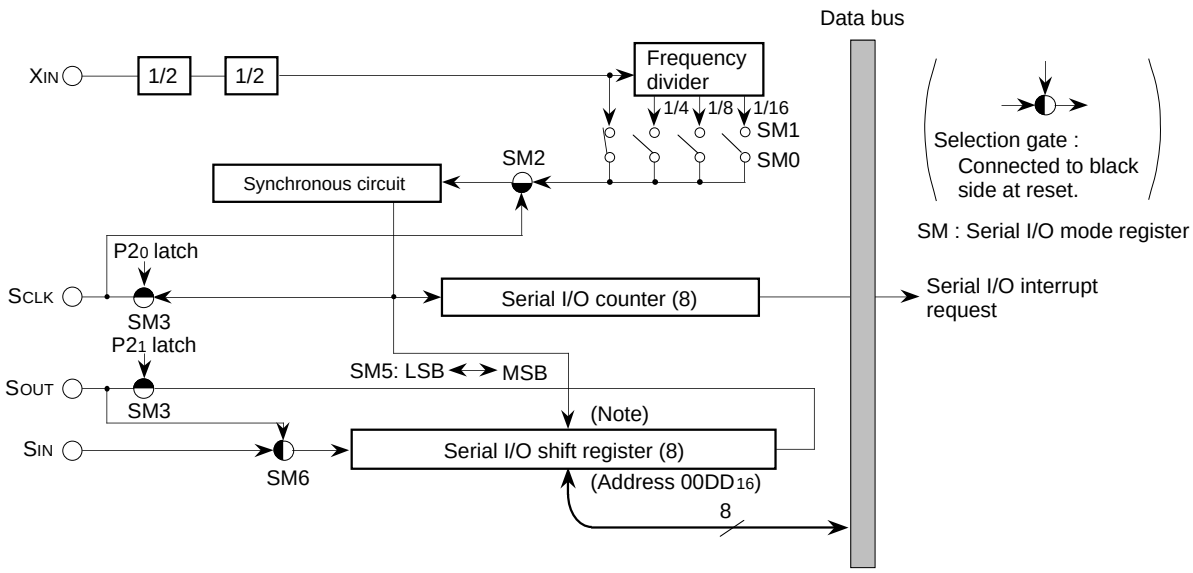
SERIAL I/O

The M37224M3-XXXSP has a built-in serial I/O which can either transmit or receive 8-bit data serially in the clock synchronous mode.

The serial I/O block diagram is shown in Figure 18. The synchronous clock I/O pin (SCLK), and data I/O pins (SOUT, SIN) also function as port P2.

Bit 2 of the serial I/O mode register (address 00DC16) selects whether the synchronous clock is supplied internally or externally (from the P20/SCLK pin). When an internal clock is selected, bits 1 and 0 select whether f(XIN) is divided by 4, 16, 32, or 64. Bit 3 selects whether port P2 is used for serial I/O or not. To use the P22/SIN pin as the SIN pin, set the bit 2 of the port P2 direction register (address 00C516) to "0."

The operation of the serial I/O is described below. The operation differs depending on the clock source; external clock or internal clock.



Note: When the data is set in the serial I/O register (address 00DD 16), the register functions as the serial I/O shift register.

Fig. 18. Serial I/O Block Diagram

Internal clock: The serial I/O counter is set to “7” during the write cycle into the serial I/O register (address 00DD16), and the transfer clock goes “H” forcibly. At each falling edge of the transfer clock after the write cycle, serial data is output from the SOUT pin. Transfer direction can be selected by bit 5 of the serial I/O mode register. At each rising edge of the transfer clock, data is input from the SIN pin and data in the serial I/O register is shifted 1 bit.

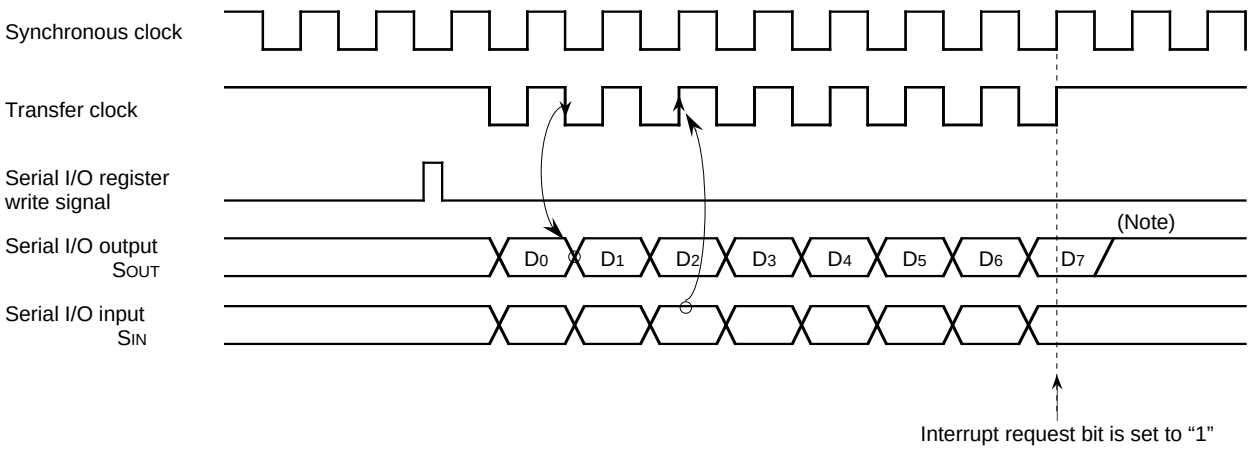
After the transfer clock has counted 8 times, the serial I/O counter becomes “0” and the transfer clock stops at HIGH. At this time the interrupt request bit is set to “1.”

External clock: When an external clock is selected as the clock source, the interrupt request is set to “1” after the transfer clock has been counted 8 counts. However, transfer operation does not stop, so the clock should be controlled externally. Use the external clock of 1MHz or less with a duty cycle of 50%.

The serial I/O timing is shown in Figure 19. When using an external clock for transfer, the external clock must be held at HIGH for initializing the serial I/O counter. When switching between an internal clock and an external clock, do not switch during transfer. Also, be sure to initialize the serial I/O counter after switching.

Notes 1: On programming, note that the serial I/O counter is set by writing to the serial I/O register with the bit managing instructions, such as SEB and CLB.

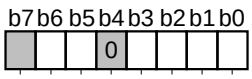
2: When an external clock is used as the synchronous clock, write transmit data to the serial I/O register when the transfer clock input level is HIGH.



Note : When an internal clock is selected, the SOUT pin is at high-impedance after transfer is completed.

Fig. 19. Serial I/O Timing (for LSB first)

Serial I/O Mode Register



Serial I/O mode register (SM) [Address $00DC_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Internal synchronous clock selection bits (SM0, SM1)	b1 b0 0 0: f(XIN)/4 0 1: f(XIN)/16 1 0: f(XIN)/32 1 1: f(XIN)/64	0	R	W
2	Synchronous clock selection bit (SM2)	0: External clock 1: Internal clock	0	R	W
3	Serial I/O port selection bit (SM3)	0: P20, P21 functions as port 1: SCLK, SOUT	0	R	W
4	Fix this bit to “0.”		0	R	W
5	Transfer direction selection bit (SM5)	0: LSB first 1: MSB first	0	R	W
6	Serial input pin selection bit (SM6)	0: Input signal from SIN pin 1: Input signal from SOUT pin	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—

Fig. 20. Serial I/O Mode Register

Serial I/O Common Transmission/Reception Mode

By writing "1" to bit 6 of the serial I/O mode register, signals SIN and SOUT are switched internally to be able to transmit or receive the serial data.

Figure 21 shows signals on serial I/O common transmission/reception mode.

Note: When receiving the serial data after writing "FF16" to the serial I/O register.

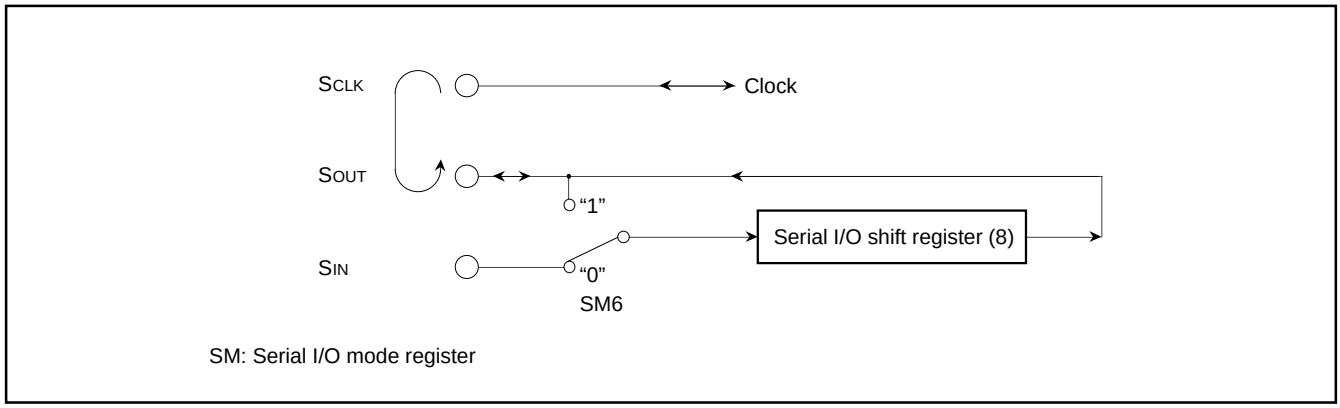


Fig. 21. Signals on Serial I/O Common Transmission/Reception Mode

PWM OUTPUT FUNCTION

The M37224M3-XXXSP is equipped with a 14-bit PWM (DA) and six 8-bit PWMs (PWM0–PWM5). DA has a 14-bit resolution with the minimum resolution bit width of 0.25 μs and a repeat period of 4096 μs (for f(X_{IN}) = 8 MHz). PWM0–PWM5 have the same circuit structure and an 8-bit resolution with minimum resolution bit width of 4 μs and repeat period of 1024 μs (for f(X_{IN}) = 8 MHz).

Figure 22 shows the PWM block diagram. The PWM timing generating circuit applies individual control signals to PWM0–PWM5 using f(X_{IN}) divided by 2 as a reference signal.

(1) Data Setting

When outputting DA, first set the high-order 8 bits to the DA-H register (address $00CE_{16}$), then the low-order 6 bits to the DA-L register (address $00CF_{16}$). When outputting PWM0–PWM5, set 8-bit output data to the PWMi register (i means 0 to 5; addresses $00D0_{16}$ to $00D4_{16}$, $00F6_{16}$).

(2) Transmitting Data from Register to PWM circuit

Data transfer from the 8-bit PWM register to the 8-bit PWM circuit is executed at writing data to the register.

The signal output from the 8-bit PWM output pin corresponds to the contents of this register.

Also, data transfer from the DA register (addresses $00CE_{16}$ and $00CF_{16}$) to the 14-bit PWM circuit is executed at writing data to the DA-L register (address $00CF_{16}$). Reading from the DA-H register (address $00CE_{16}$) means reading this transferred data. Accordingly, it is possible to confirm the data being output from the D-A output pin by reading the DA register.

(3) Operating of 8-bit PWM

The following explains PWM operation.

First, set the bit 0 of PWM output control register 1 (address $00D5_{16}$) to “0” (at reset, this bit 0 already set to “0” automatically), so that the PWM count source is supplied.

PWM0–PWM5 are also used as pins $P0_0$–$P0_5$ respectively. For PWM0–PWM5, set the corresponding bits of the port P0 direction register to “1” (output mode). And select each output polarity by bit 3 of PWM output control register 2(address $00D6_{16}$). Then, set bits 2 to 7 of PWM output control register 1 to “1” (PWM output).

The PWM waveform is output from the PWM output pins by setting these registers.

Figure 23 shows the 8-bit PWM timing. One cycle (T) is composed of 256 (2^8) segments. The 8 kinds of pulses, relative to the weight of each bit (bits 0 to 7), are output inside the circuit during 1 cycle. Refer to Figure 23 (a). The 8-bit PWM outputs waveform performed a OR operation of pulses corresponding to the contents of bits 0 to 7 of the 8-bit PWM register. Several examples are shown in Figure 23 (b). 256 kinds of output (HIGH area: 0/256 to 255/256) are selected by changing the contents of the PWM register. A length of entirely HIGH cannot be output, i.e. 256/256.

(4) Operating of 14-bit PWM

As with 8-bit PWM, set the bit 0 of the PWM output control register 1 (address $00D5_{16}$) to “0” (at reset, bit 0 is already set to “0” automatically), so that the PWM count source is supplied. Next, select the output polarity by bit 2 of PWM output control register 2 (address $00D6_{16}$). Then, the 14-bit PWM outputs from the D-A output pin by setting bit 1 of PWM output control register 1 to “0” (at reset, this bit already set to “0” automatically) to select the DA output.

The output example of the 14-bit PWM is shown in Figure 24.

The 14-bit PWM divides the data of the DA latch into the low-order 6 bits and the high-order 8 bits.

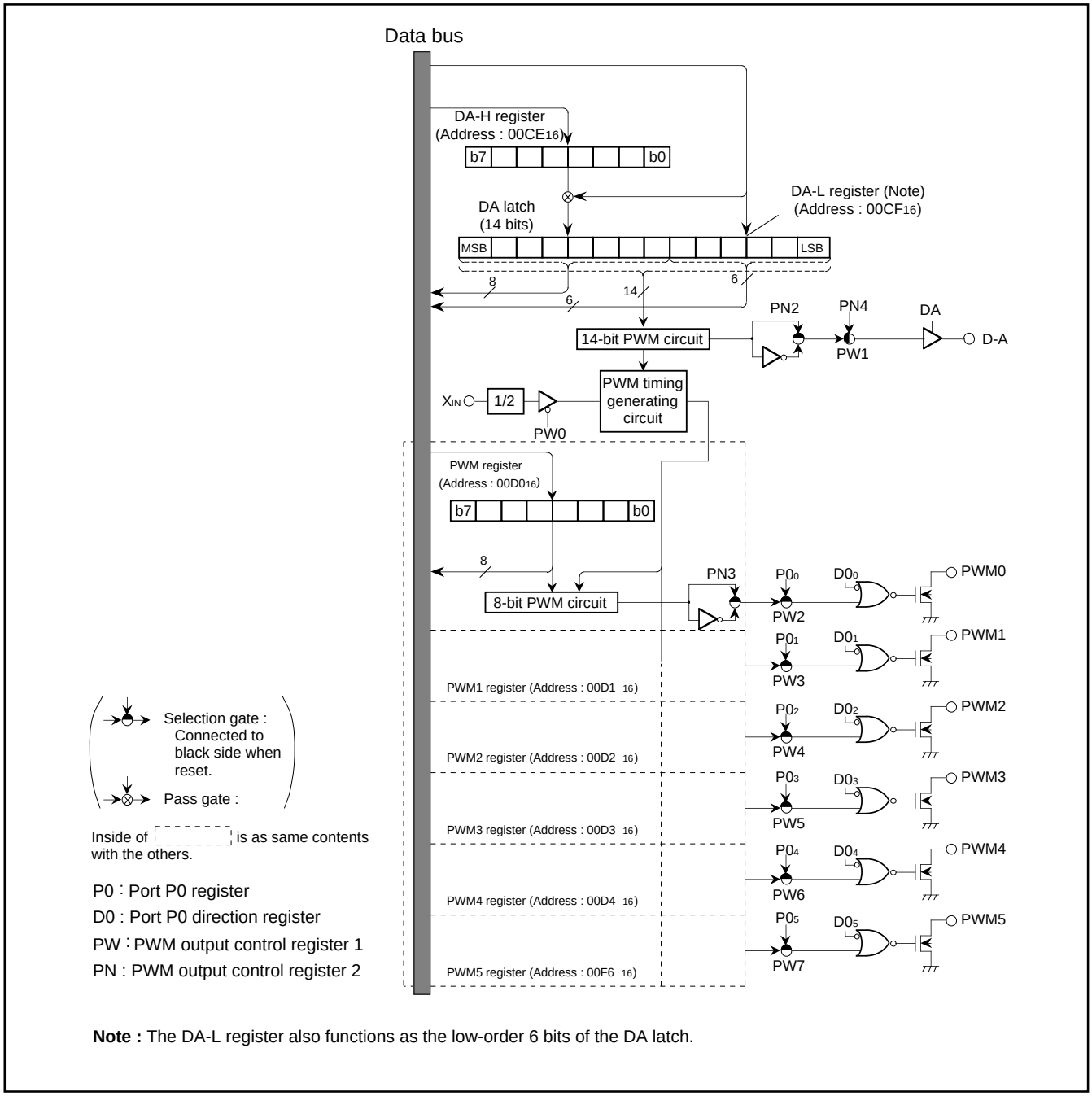
The fundamental waveform is determined with the high-order 8-bit data “D_H.” A “H” level area with a length $\tau \times D_H$(“H” level area of fundamental waveform) is output every short area of “t” = 256τ = 64 μs (τ is the minimum resolution bit width of 0.25 μs). The “H” level area increase interval (t_m) is determined with the low-order 6-bit data “D_L.” The “H” level are of smaller intervals “t_m” shown in Table 6 is longer by τ than that of other smaller intervals in PWM repeat period “T” = 64t. Thus, a rectangular waveform with the different “H” width is output from the D-A pin. Accordingly, the PWM output changes by τ unit pulse width by changing the contents of the DA-H and DA-L registers. A length of entirely “H” output cannot be output, i. e. 256/256.

(5) Output after Reset

At reset the output of port $P0_0$–$P0_5$ is in the high-impedance state, and the contents of the PWM register and the PWM circuit are undefined. Note that after reset, the PWM output is undefined until setting the PWM register.

Table 2. Relation between Low-order 6-bit Data and High-level Area Increase Interval

Low-order 6 Bits of Data	Area Longer by τ than That of Other t_m (m = 0 to 63)
0 0 0 0 0 0 (LSB)	Nothing
0 0 0 0 0 1	m = 32
0 0 0 0 1 0	m = 16, 48
0 0 0 1 0 0	m = 8, 24, 40, 56
0 0 1 0 0 0	m = 4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m = 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m = 1, 3, 5, 7, ... 57, 59, 61, 63



Note : The DA-L register also functions as the low-order 6 bits of the DA latch.

Fig. 22. PWM Block Diagram

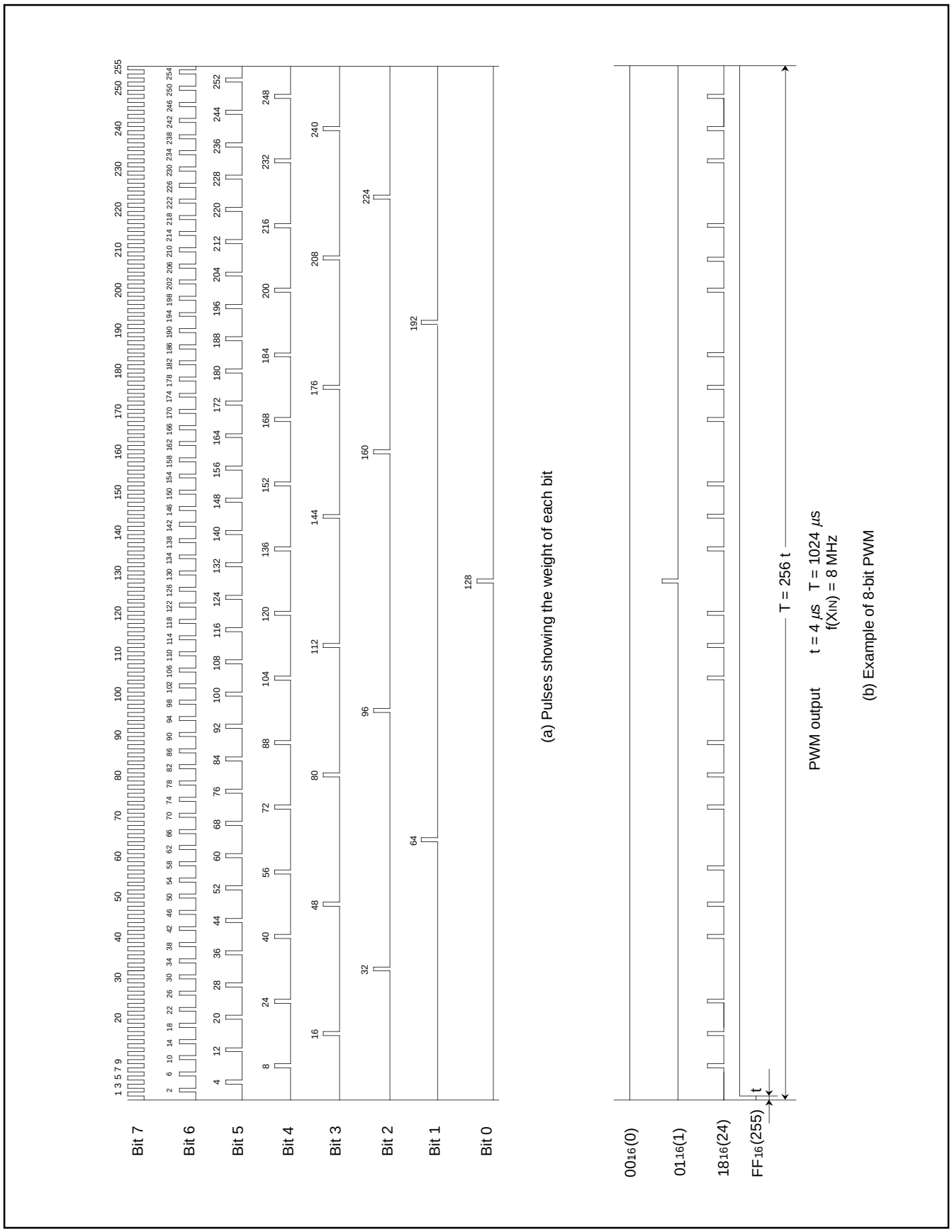


Fig. 23. 8-bit PWM Timing

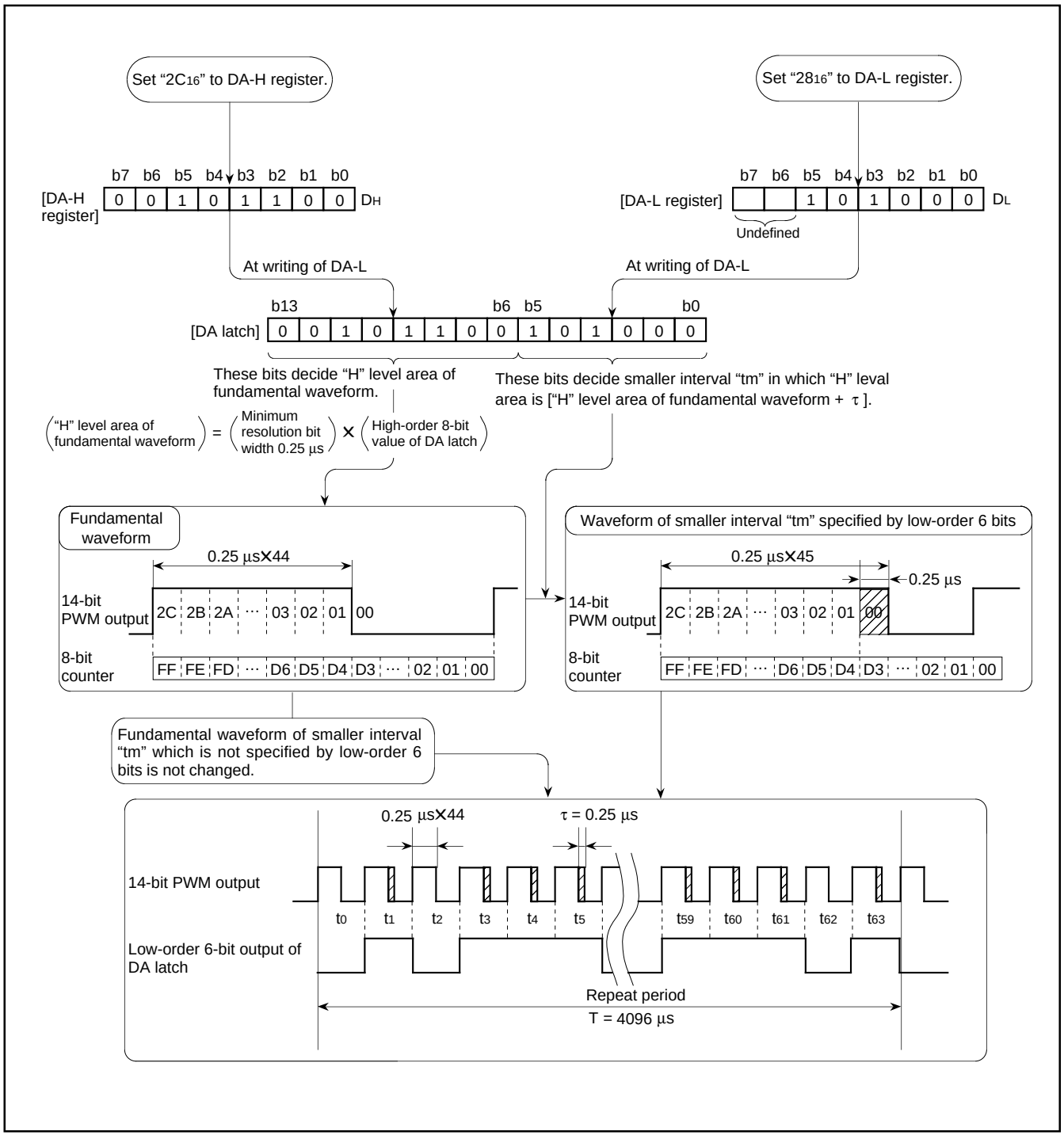
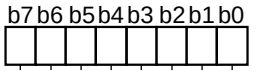


Fig. 24. 14-bit PWM Output Example (f(XIN) = 8 MHz)

PWM Output Control Register 1

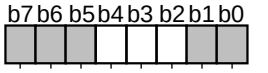


PWM output control register 1 (PW) [Address $00D5_{16}$]

B	Name	Functions	After reset	R	W
0	DA, PWM count source selection bit (PW0)	0 : Count source supply 1 : Count source stop	0	R	W
1	DA/PN4 output selection bit (PW1)	0 : DA output 1 : PN4 output	0	R	W
2	$P0_0$/PWM0 output selection bit (PW2)	0: $P0_0$ output 1: PWM0 output	0	R	W
3	$P0_1$/PWM1 output selection bit (PW3)	0: $P0_1$ output 1: PWM1 output	0	R	W
4	$P0_2$/PWM2 output selection bit (PW4)	0: $P0_2$ output 1: PWM2 output	0	R	W
5	$P0_3$/PWM3 output selection bit (PW5)	0: $P0_3$ output 1: PWM3 output	0	R	W
6	$P0_4$/PWM4 output selection bit (PW6)	0: $P0_4$ output 1: PWM4 output	0	R	W
7	$P0_5$/PWM5 output selection bit (PW7)	0: $P0_5$ output 1: PWM5 output	0	R	W

Fig. 25. PWM Output Control Register 1

PWM Output Control Register 2



PWM output control register 2 (PN) [Address $00D6_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—
2	DA output polarity selection bit (PN3)	0 : Positive polarity 1 : Negative polarity	0	R	W
3	PWM output polarity selection bit (PN4)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	DA general-purpose output bit (PN5)	0 : Output LOW 1 : Output HIGH	0	R	W
5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Fig. 26. PWM Output Control Register 2

A-D COMPARATOR

A-D comparator consists of 6-bit D-A converter and comparator. A-D comparator block diagram is shown in Figure 27.

The reference voltage "V_{ref}" for D-A conversion is set by bits 0 to 5 of the A-D control register 2 (address $00EF_{16}$).

The comparison result of the analog input voltage and the reference voltage "V_{ref}" is stored in bit 4 of the A-D control register 1 (address $00EE_{16}$).

For A-D comparison, set "0" to corresponding bits of the direction register to use ports as analog input pins. Write the data for select of analog input pins to bits 0 to 2 of the A-D control register 1 and write the digital value corresponding to V_{ref} to be compared to the bits 0 to 5 of the A-D control register 2. The voltage comparison starts by writing to the A-D control register 2, and it is completed after 16 machine cycles (NOP instruction × 8).

Table 3. Relation between Contents of A-D Control Register 2 and Reference Voltage "V_{ref}"

A-D Control Register 2						Reference Voltage "V_{ref}"
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	0	0	1/128 V_{CC}
0	0	0	0	0	1	3/128 V_{CC}
0	0	0	0	1	0	5/128 V_{CC}
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	0	1	123/128 V_{CC}
1	1	1	1	1	0	125/128 V_{CC}
1	1	1	1	1	1	127/128 V_{CC}

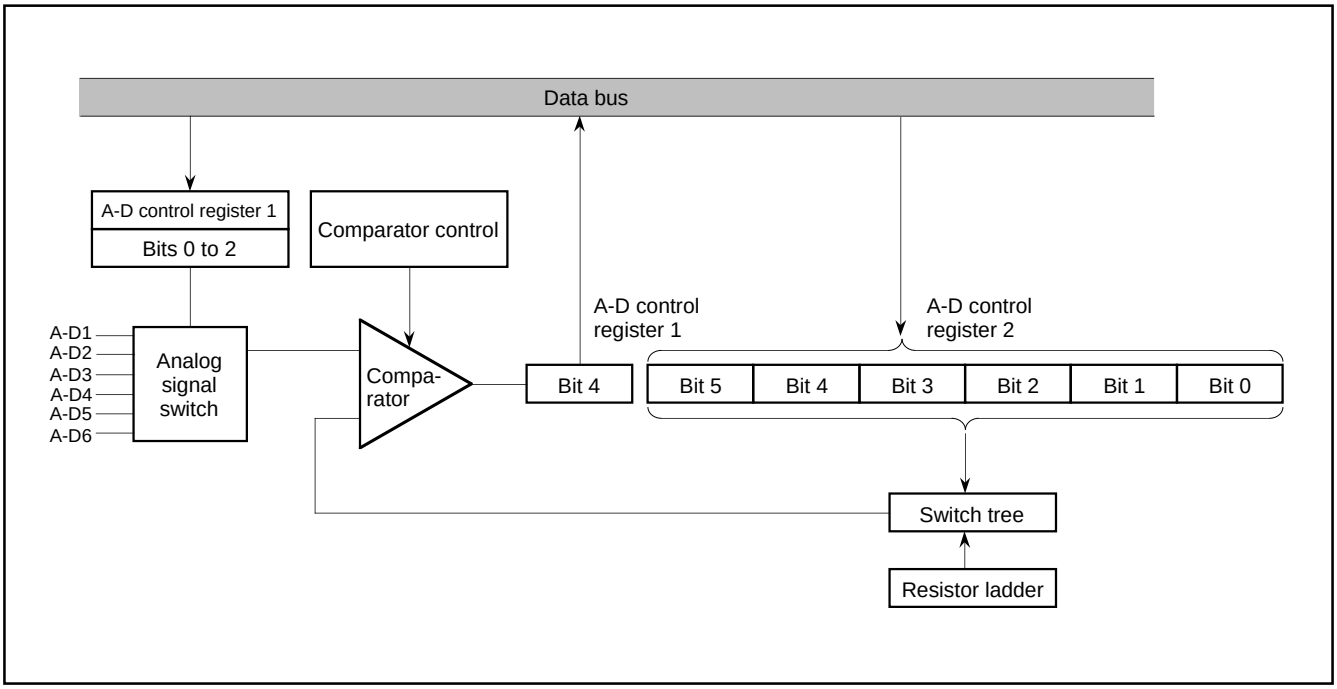
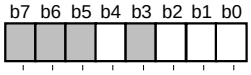


Fig. 27. A-D Comparator Block Diagram

A-D Control Register 1

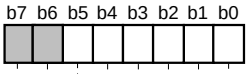


A-D control register 1 (AD1) [Address $00EE_{16}$]

B	Name	Functions	After reset	R	W
0 to 2	Analog input pin selection bits (ADM0 to ADM2)	b2 b1 b0 0 0 0 : A-D1 0 0 1 : A-D2 0 1 0 : A-D3 0 1 1 : A-D4 1 0 0 : A-D5 1 0 1 : A-D6 1 1 0 : } Do not set. 1 1 1 : }	0	R	W
3, 5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
4	Storage bit of comparison result (ADM4)	0: Input voltage < reference voltage 1: Input voltage > reference voltage	Indeterminate	R	—

Fig. 28. A-D Control Register 1

A-D Control Register 2



A-D control register 2(AD2) [Address $00EF_{16}$]

B	Name	Functions	After reset	R	W
0 to 5	D-A converter set bits (ADC0 to ADC5)	b5 b4 b3 b2 b1 b0 0 0 0 0 0 0 : 1/128Vcc 0 0 0 0 0 1 : 3/128Vcc 0 0 0 0 1 0 : 5/128Vcc ⋮ 1 1 1 1 0 1 : 123/128Vcc 1 1 1 1 1 0 : 125/128Vcc 1 1 1 1 1 1 : 127/128Vcc	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are reed out, the values are " 0."		0	R	—

Fig. 29. A-D Control Register 2

D-A CONVERTER

The M37224M3-XXXSP has 2 D-A converters with 6-bit resolution. D-A converter block diagram is shown in Figure 30.

D-A conversion is performed by setting the value in the DA conversion register. The result of D-A conversion is output from the DA pin by setting "1" to the DA output enable bit of the port P3 output mode control register (bits 2 and 3 at address $00CD_{16}$).

The output analog voltage V is determined with the value n (n: decimal number) in the DA conversion register.

$$V = V_{CC} \times \frac{n}{128} \quad (n = 0 \text{ to } 127)$$

The DA output does not build in a buffer, so connect an external buffer when driving a low-impedance load.

Table 4. Relation between Contents of D-A Conversion Register and Output Voltage

D-A Conversion Register							Output
Bit 7	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Voltage "V"
0	0	0	0	0	0	0	0/128 Vcc
1	0	0	0	0	0	0	1/128 Vcc
0	0	0	0	0	0	1	2/128 Vcc
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	125/128 Vcc
0	1	1	1	1	1	1	126/128 Vcc
1	1	1	1	1	1	1	127/128 Vcc

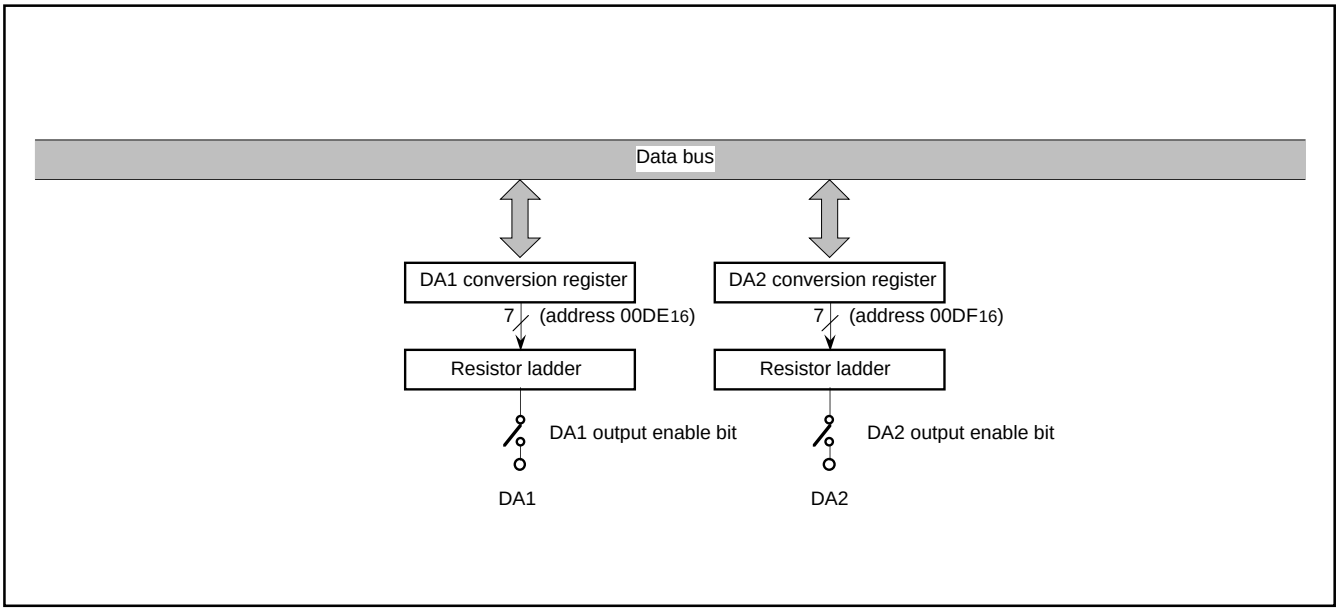
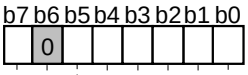


Fig. 30. D-A Converter Block Diagram

DAi Conversion Register

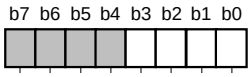


DAi conversion register (DAi) (i = 1 and 2) [Address 00DE16, 00DF16]

B	Name	Functions	After reset	R	W
0 to 5, 7	DA conversion set bits (DAi0 to DAi5)	b7 b5 b4 b3 b2 b1 b0 0 0 0 0 0 0 0 : 0/128Vcc 1 0 0 0 0 0 1 : 1/128Vcc 0 0 0 0 0 1 0 : 2/128Vcc ⋮ 1 1 1 1 1 1 0 : 125/128Vcc 0 1 1 1 1 1 1 : 126/128Vcc 1 1 1 1 1 1 1 : 127/128Vcc	Indeterminate	R	W
6	Fix this bit to “0.”		0	R	W

Fig. 31. DAi Conversion Register

Port P3 Output Mode Control Register



Port P3 output mode control register (P3S) [address 00CD16]

B	Name	Functions	After reset	R	W
0	$P3_0$ output structure selection bit (P30S)	0 : CMOS output 1 : N-channel open-drain output	0	R	W
1	$P3_1$ output structure selection bit (P31S)	0 : CMOS output 1 : N-channel open-drain output	0	R	W
2	DA1 output enable bit	0 : $P3_0$ input/output 1 : DA1 output	0	R	W
3	DA2 output enable bit	0 : $P3_1$ input/output 1 : DA2 output	0	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Fig. 32. Port P3 Output Mode Control Register

CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 5 outlines the CRT display functions of the M37224M3-XXXSP. The M37224M3-XXXSP incorporates a CRT display circuit of 20 characters × 2 lines. CRT display is controlled by the CRT control register. Up to 128 kinds of characters can be displayed. The colors can be specified for each character and up to 4 kinds of colors can be displayed on one screen. A combination of up to 7 colors can be obtained by using each output signal (R, G, and B).

Characters are displayed in a 12 × 16 dots configuration to obtain smooth character patterns (refer to Figure 33).

The following shows the procedure how to display characters on the CRT screen.

① Write the display character code in the display RAM.
② Specify the display color by using the color register.
③ Write the color register in which the display color is set in the display RAM.
④ Specify the vertical position by using the vertical position register.
⑤ Specify the character size by using the character size register.
⑥ Specify the horizontal position by using the horizontal position register.
⑦ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT display starts according to the input of the V_{SYNC} signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (3 lines or more) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 34 shows the CRT display control register. Figure 35 shows the block diagram of the CRT display circuit.

Table 5. Outline of CRT Display Functions

Parameter		Functions
Number of display characters		20 characters × 2 lines
Dot structure		12 × 16 dots (refer to Figure 33)
Kinds of characters		128 kinds
Kinds of character sizes		3 kinds
Color	Kinds of colors	1 screen: 4 kinds, maximum 7 kinds
	Coloring unit	A character
Display expansion		Possible (multiline display)
Raster coloring		Possible (maximum 7 kinds)

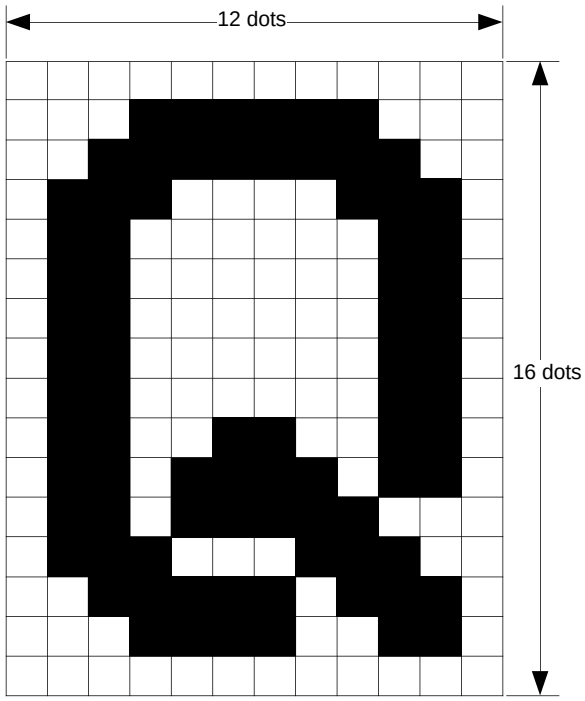


Fig. 33. CRT Display Character Configuration

CRT Control Register

b7 b6 b5 b4 b3 b2 b1 b0

CRT control register (CC) [Address 00EA$_{16}$]

B	Name	Functions	After reset	R	W
0	All-blocks display control bit (CC0) (See note)	0 : All-blocks display off 1 : All-blocks display on	0	R	W
1	Block 1 display control bit (CC1)	0 : Block 1 display off 1 : Block 1 display on	0	R	W
2	Block 2 display control bit (CC2)	0 : Block 2 display off 1 : Block 2 display on	0	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Note: Display is controlled by logical product (AND) between the all-blocks display control bit and each block control bit.

Fig. 34. CRT Control Register

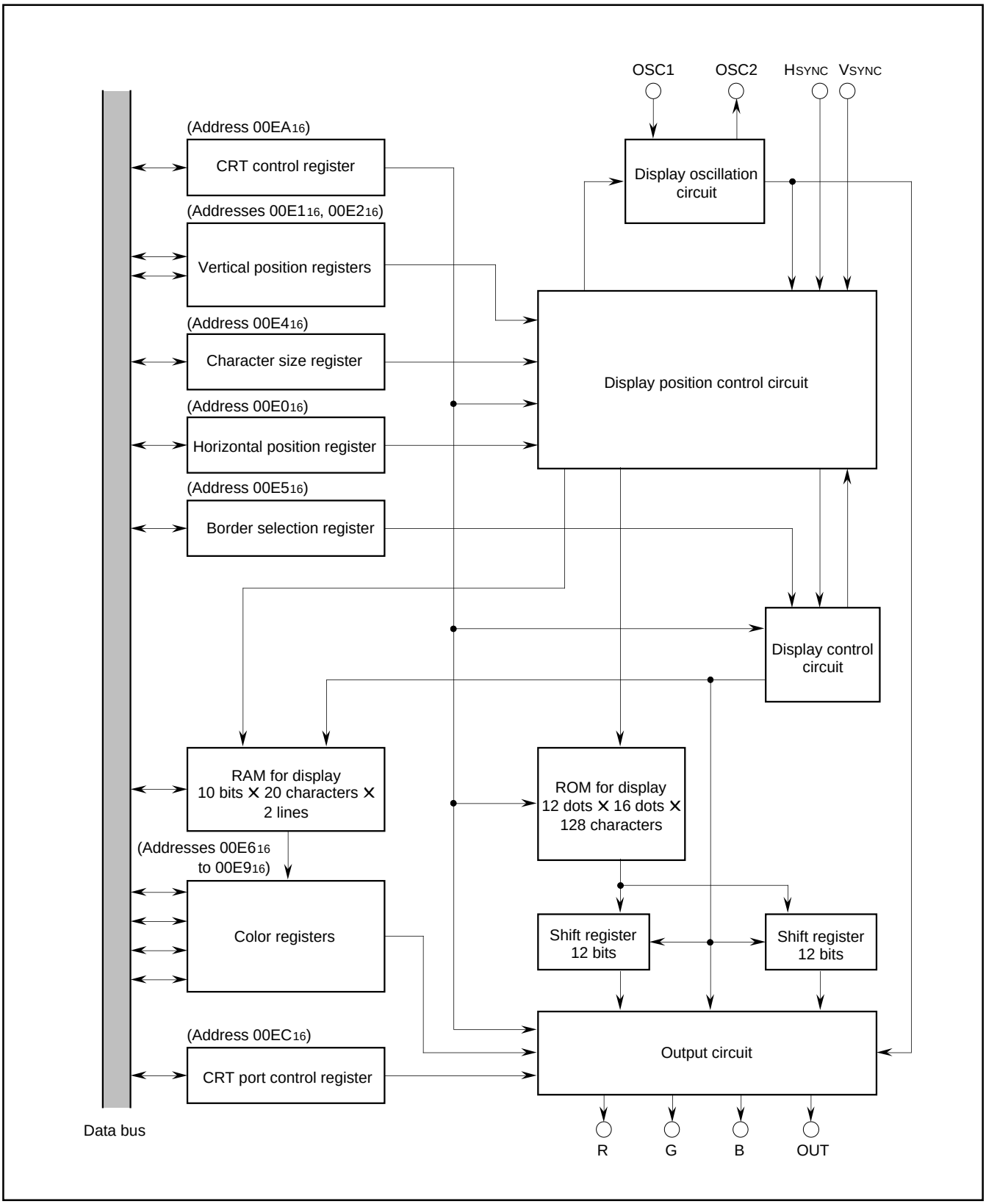


Fig. 35. Block Diagram of CRT Display Circuit

(2) Display Position

The display positions of characters are specified in units called a "block." There are 2 blocks, block 1 and block 2. Up to 20 characters can be displayed in each block (refer to (4) Memory for Display).

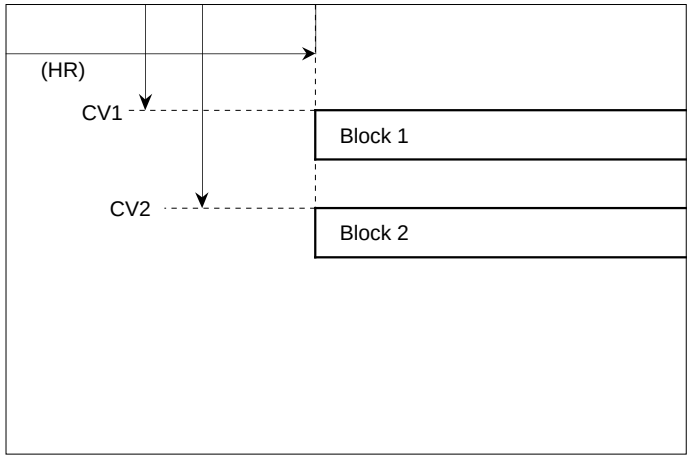
The display position of each block can be set in both horizontal and vertical directions by software.

The display position in the horizontal direction can be selected for all blocks in common from 64-step display positions in units of 4Tc (Tc = oscillating cycle for display).

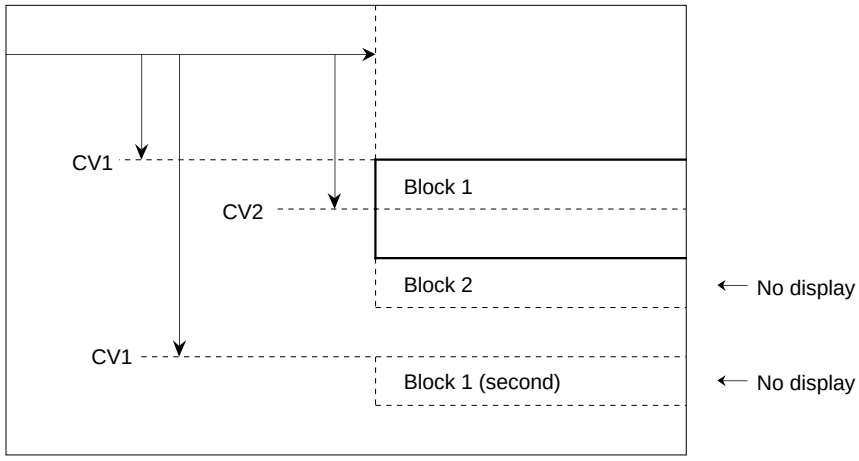
The display position in the vertical direction for each block can be selected from 128-step display positions in units of 4 scanning lines.

Block 2 is displayed after the display of block 1 is completed (refer to Figure 36 (a)). Accordingly, if the display of block 2 starts during the display of block 1, only block 1 is displayed. Similarly, when multiline display, block 1 is displayed after the display of block 2 is completed (refer to Figure 36 (b)).

The vertical position can be specified from 128-step positions (4 scanning lines per a step) for each block by setting values "00_{16}" to "$7F_{16}$" to bits 0 to 6 in the vertical position register (addresses $00E1_{16}$ and $00E2_{16}$). Figure 38 shows the structure of the vertical position register.



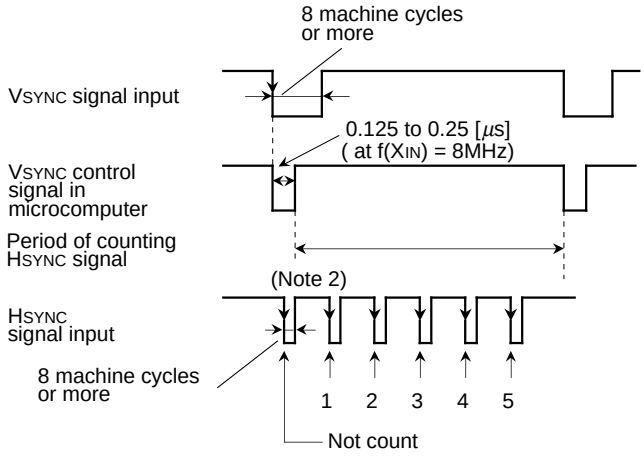
(a) Example when each block is separated



(b) Example when block 2 overlaps with block 1

Fig. 36. Display Position

The display position in the vertical direction is determined by counting the horizontal sync signal (HSYNC). At this time when VSYNC and HSYNC are positive polarity (negative polarity), it starts to count the rising edge (falling edge) of HSYNC signal from after about 1 machine cycle of rising edge (falling edge) of VSYNC signal. So interval from rising edge (falling edge) of VSYNC signal to rising edge (falling edge) of HSYNC signal needs enough time (2 machine cycles or more) for avoiding jitter. The polarity of HSYNC and VSYNC signals can select with the CRT port control register (address 00EC16).

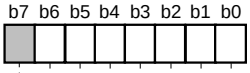


When bits 0 and 1 of the CRT port control register (address 00EC16) are set to "1" (negative polarity)

Notes 1 : The vertical position is determined by counting falling edge of H SYNC signal after rising edge of VSYNC control signal in the microcomputer.
2 : Do not generate falling edge of HSYNC signal near rising edge of VSYNC control signal in microcomputer to avoid jitter.
3 : The pulse width of VSYNC and HSYNC needs 8 machine cycles or more.

Fig. 37. Supplement Explanation for Display Position

Vertical Position Register i

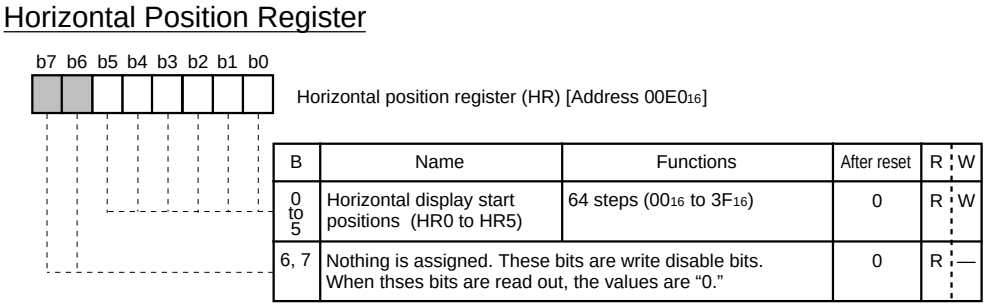


Vertical position register i (CVi) (i = 1 and 2) [Addresses 00E116, 00E216]

B	Name	Functions	After reset	R	W
0 to 6	Vertical display start positions (CVi : CVi0 to CVi6)	128 steps (0016 to 7F16)	Indeterminate	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

Fig. 38. Vertical Position Register i

The horizontal position is common to all blocks, and can be set in 64 steps (where 1 step is 4Tc, Tc being the display oscillation period) as values "00$_{16}$" to "3F$_{16}$" in bits 0 to 5 of the horizontal position register (address 00E0$_{16}$). The structure of the horizontal position register is shown in Figure 39.



B	Name	Functions	After reset	R	W
0 to 5	Horizontal display start positions (HR0 to HR5)	64 steps (00$_{16}$ to 3F$_{16}$)	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When thses bits are read out, the values are "0."		0	R	—

Fig. 39. Horizontal Position Register

(3) Character Size

The size of characters to be displayed can be from 3 sizes for each block. Use the character size register (address 00E4$_{16}$) to set a character size. The character size of block 1 can be specified by using bits 0 and 1 of the character size register; the character size of block 2 can be specified by using bits 2 and 3. Figure 40 shows the character size register.

The character size can be selected from 3 sizes: minimum size, medium size and large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the oscillating cycle for display (Tc) in the width (horizontal) direction. The minimum size consists of [1 scanning line] × [1Tc]; the medium size consists of [2 scanning lines] × [2Tc]; and the large size consists of [3 scanning lines] × [3Tc]. Table 6 shows the relation between the set values in the character size register and the character sizes.

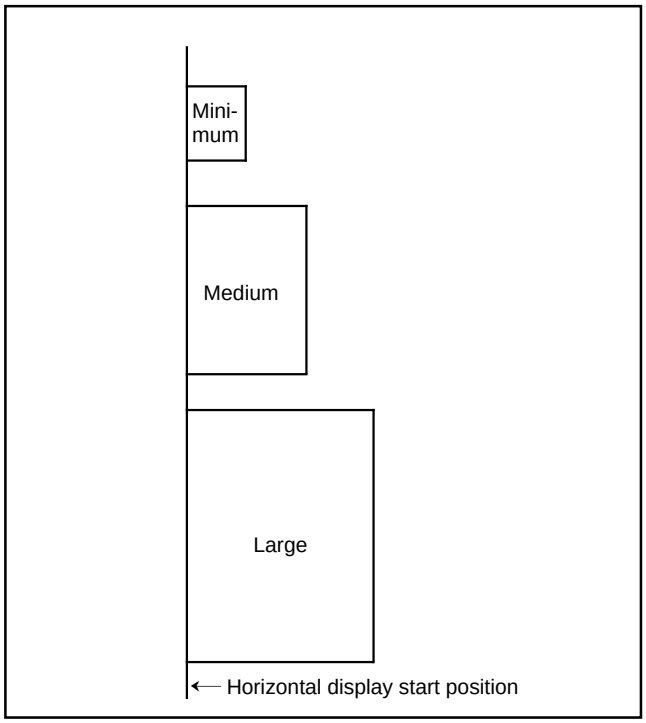


Fig. 41. Display Start Position of each Character Size (horizontal direction)

Character Size Register

b7 b6 b5 b4 b3 b2 b1 b0

Character size register (CS) [Address 00E4$_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Character size of block 1 selection bits (CS10, CS11)	00 : Minimum size 01 : Medium size 10 : Large size 11 : Do not set.	Indeterminate	R	W
2,3	Character size of block 2 selection bits (CS20,CS21)	00 : Minimum size 01 : Medium size 10 : Large size 11 : Do not set.	Indeterminate	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Fig. 40. Character Size Register

Table 6. Relation between Set Values in Character Size Register and Character Sizes

Set Values of Character Size Register		Character Size	Width (horizontal) Direction Tc: oscillating cycle for display	Height (vertical) Direction Scanning Lines
CSn1	CSn0			
0	0	Minimum	1Tc	1
0	1	Medium	2Tc	2
1	0	Large	3Tc	3
1	1	This is not available		

Note: The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal display start position is common to all blocks even when the character size varies with each block (refer to Figure 41).

(4) Memory for Display

There are 2 types of display memory : CRT display ROM (addresses 10000_{16} to $10FFF_{16}$) used to store character dot data (masked) and CRT display RAM (addresses 0600_{16} to $06B3_{16}$) used to specify the colors of characters to be displayed. The following describes each type of display memory.

① **ROM for display (addresses 10000_{16} to $10FFF_{16}$)**

The CRT display ROM contains dot pattern data for characters to be displayed. For characters stored in this ROM to be actually displayed, it is necessary to specify them by writing the character code inherent to each character (code determined based on the addresses in the CRT display ROM) into the CRT display RAM. The character code list is shown in Table 7.

The CRT display ROM has a capacity of 4 K bytes. Since 32 bytes are required for 1 character data, the ROM can stores up to 128 kinds of characters.

The CRT display ROM space is broadly divided into 2 areas. The [vertical 16 dots] × [horizontal (left side) 8 dots] data of display characters are stored in addresses 10000_{16} to $107FF_{16}$; the [vertical 16 dots] × [horizontal (right side) 4 dots] data of display characters are stored in addresses 10800_{16} to $10FFF_{16}$ (refer to Figure 42). Note however that the high-order 4 bits in the data to be written to addresses 10800_{16} to $10FFF_{16}$ must be set to "1" (by writing data "FX_{16}").

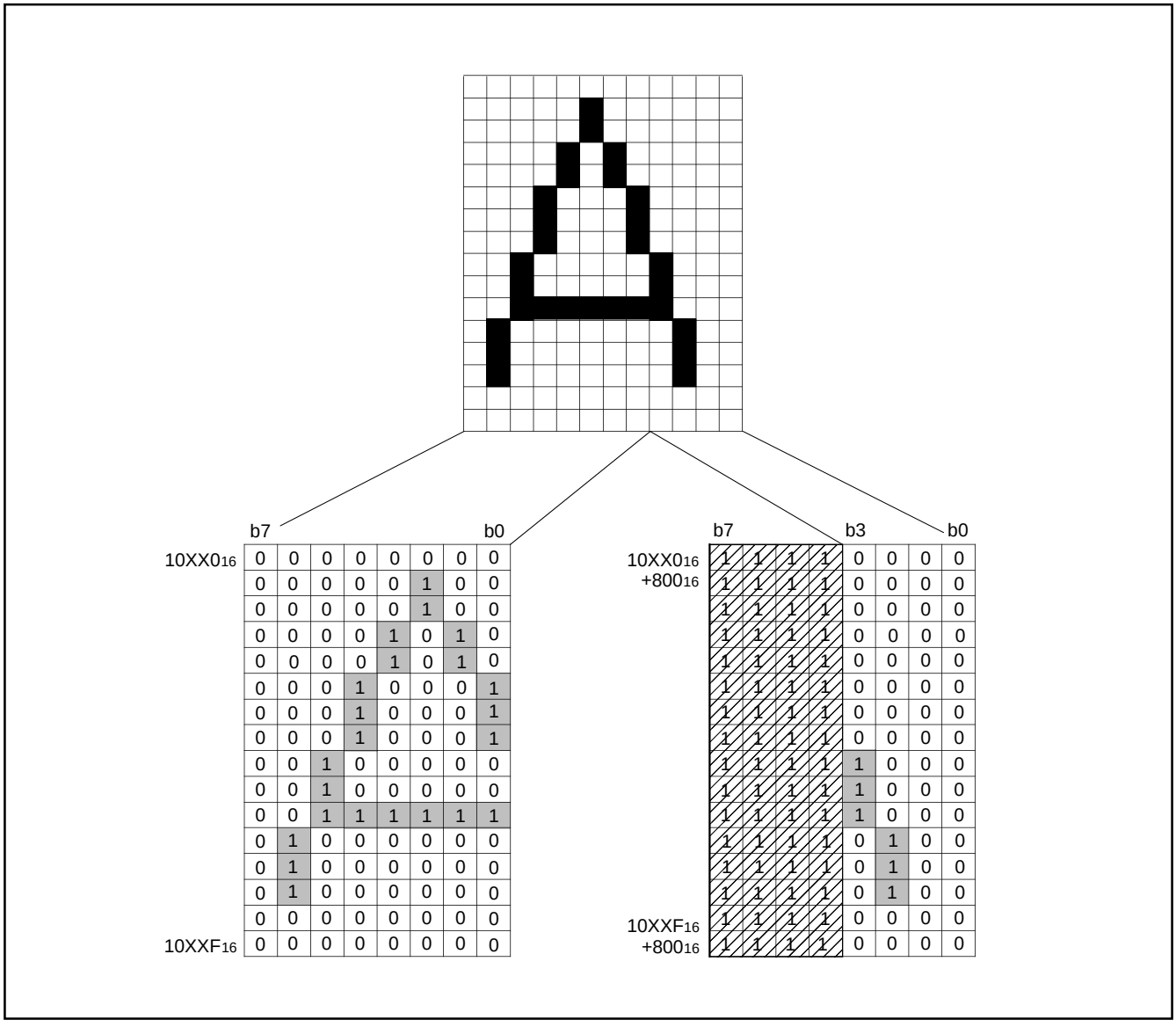


Fig. 42. Display Character Stored Data

Table 7. Character Code List (partially abbreviated)

Character code	Character data storage address	
	Left 8 dots lines	Right 4 dots lines
00_{16}	10000_{16} to $1000F_{16}$	10800_{16} to $1080F_{16}$
01_{16}	10010_{16} to $1001F_{16}$	10810_{16} to $1081F_{16}$
02_{16}	10020_{16} to $1002F_{16}$	10820_{16} to $1082F_{16}$
03_{16}	10030_{16} to $1003F_{16}$	10830_{16} to $1083F_{16}$
:	:	:
$7E_{16}$	$107E0_{16}$ to $107EF_{16}$	$10FE0_{16}$ to $10FEF_{16}$
$7F_{16}$	$107F0_{16}$ to $107FF_{16}$	$10FF0_{16}$ to $10FFF_{16}$

② RAM for display (addresses 0600_{16} to $06B3_{16}$)

The CRT display RAM is allocated at addresses 0600_{16} to $06B3_{16}$, and is divided into a display character code specification part and display color specification part for each block. Table 8 shows the contents of the CRT display RAM.

For example, to display 1 character position (the left edge) in block 1, write the character code in address 0600_{16} and write the color register No. to the low-order 2 bits (bits 0 and 1) in address 0680_{16}. The color register No. to be written here is one of the 4 color registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers. The structure of the CRT display RAM is shown in Figure 43.

Table 8. Contents of CRT Display RAM

Block	Display Position (from left)	Character Code Specification	Color Specification
Block 1	1st character	0600_{16}	0680_{16}
	2nd character	0601_{16}	0681_{16}
	3rd character : 18th character	0602_{16} : 0611_{16}	0682_{16} : 0691_{16}
	19th character	0612_{16}	0692_{16}
	20th character	0613_{16}	0693_{16}
Not used		0614_{16} to $061F_{16}$	0694_{16} to $069F_{16}$
Block 2	1st character	0620_{16}	$06A0_{16}$
	2nd character	0621_{16}	$06A1_{16}$
	3rd character : 18th character	0622_{16} : 0631_{16}	$06A2_{16}$: $06B1_{16}$
	19th character	0632_{16}	$06B2_{16}$
	20th character	0633_{16}	$06B3_{16}$

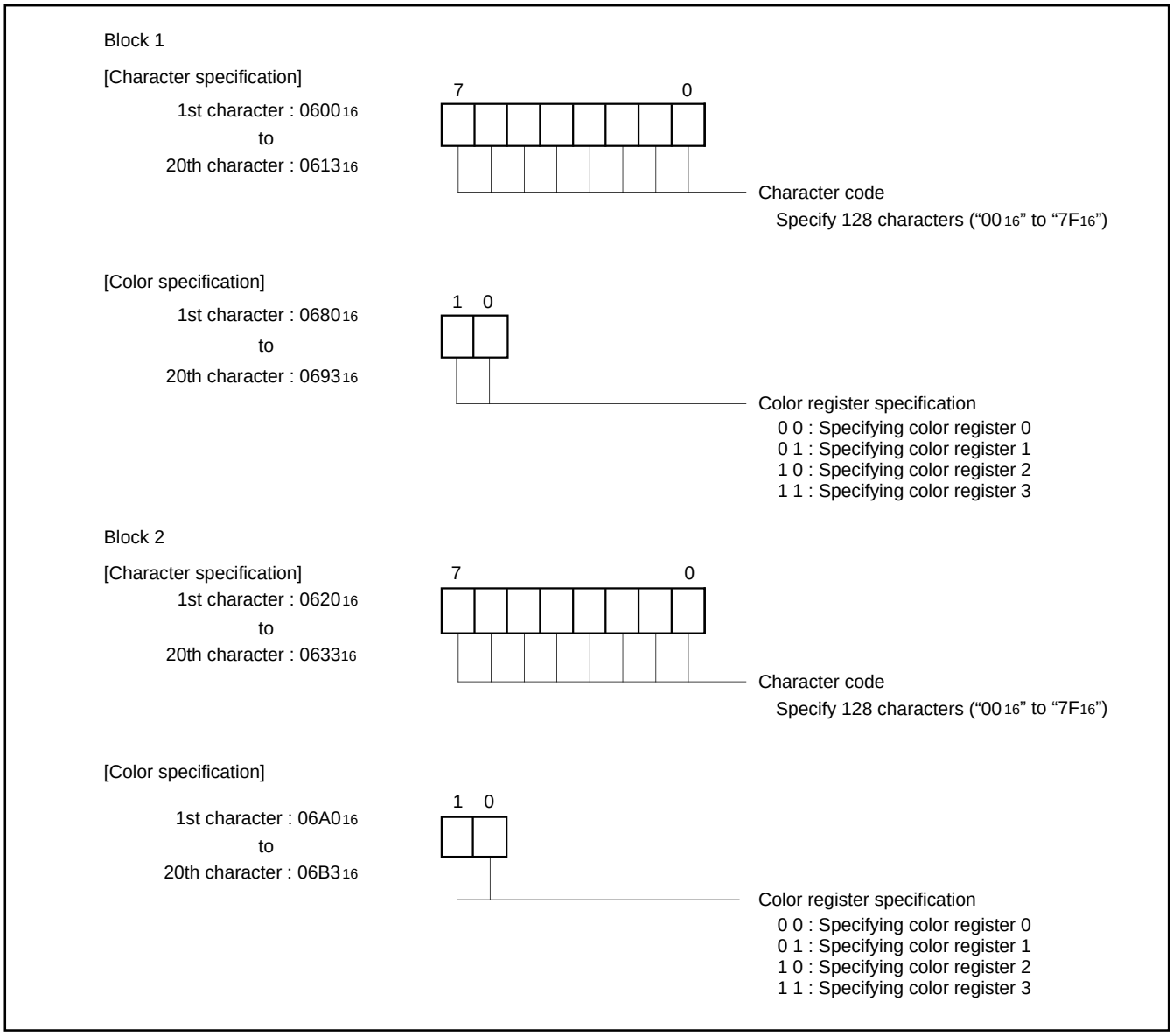


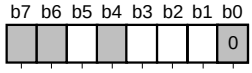
Fig. 43. Structure of CRT Display RAM

(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the 4 registers (CO0 to CO3: addresses 00E6$_{16}$ to 00E9$_{16}$) and then specifying that color register with the CRT display RAM. There are 3 color outputs; R, G and B. By using a combination of these outputs, it is possible to set 2^3–1 (when no output) = 7 colors. However, since only 4 color registers are available, up to 4 colors can be disabled at one time.

R, G and B outputs are set by using bits 1 to 3 in the color register. Bit 5 is used to specify whether a character output or blank output. Figure 44 shows the color register.

Color Register i



Color register i (COi) (i = 0 to 3) [Addresses 00E6$_{16}$ to 00E9$_{16}$]

B	Name	Functions	After reset	R	W
0	Fix this bit to "0."		0	R	—
1	B signal output selection bit (COi1)	0 : No character is output 1 : Character is output	0	R	W
2	G signal output selection bit (COi2)	0 : No character is output 1 : Character is output	0	R	W
3	R signal output selection bit (COi3)	0 : No character is output 1 : Character is output	0	R	W
4, 6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
5	OUT signal output control bit (COi5)	0 : Character is output 1 : Blank is output	0	R	W

Fig. 44. Color Registers

(6) Character Border Function

An border of 1 clock (1 dot) equivalent size can be added to a character to be displayed in both horizontal and vertical directions. The border is output from the OUT pin. In this case, set bit 5 of a color register to “0” (character is output).

Border can be specified in units of block by using the border selection register (address 00E5$_{16}$). Figure 45 shows the border selection register. Table 9 shows the relationship between the values set in the border selection register and the character border function.

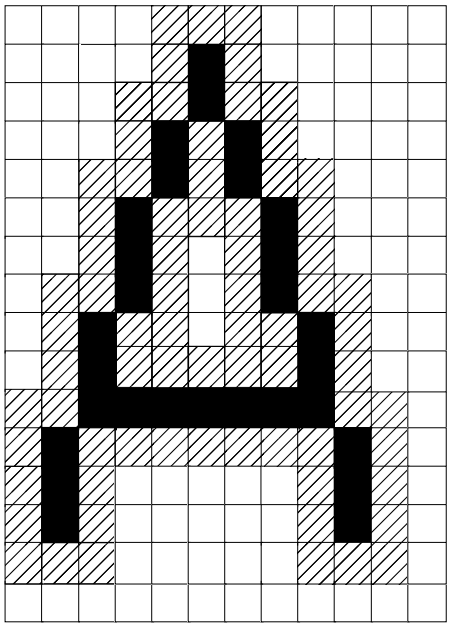


Fig. 46. Example of Border

Border Selection Register

b7 b6 b5 b4 b3 b2 b1 b0

Border selection register (MD) [Address 00E5$_{16}$]

B	Name	Functions	After reset	R	W
0	Block 1 OUT output border selection bit (MD10)	0 : Same output as R, G, B is output 1 : Border output	Indeterminate	R	W
1	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—
2	Block 2 OUT output border selection bit (MD20)	0 : Same output as R, G, B is output 1 : Border output	Indeterminate	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Fig. 45. Border Selection Register

Table 9. Relationship between Set Value in Border Selection Register and Character Border Function

Border Selection Register MDn0	Functions	Example of Output
0	Ordinary	R, G, B output OUT output
1	Border including character	R, G, B output OUT output

(7) Multiline Display

The M37224M3-XXXSP can ordinarily display 2 lines on the CRT screen by displaying 2 blocks at different vertical positions. In addition, it can display up to 16 lines by using CRT interrupts.
A CRT interrupt request occurs at the point at which display of each block has been completed. In other words, when a scanning line reaches the point of the display position (specified by the vertical position registers) of a certain block, the character display of that block starts, and an interrupt occurs at the point at which the scanning line exceeds the block.

Note: A CRT interrupt does not occur at the end of display when the block is not displayed. In other words, if a block is set to off display with the display control bit of the CRT control register (address 00EA16), a CRT interrupt request does not occur (refer to Figure 47).

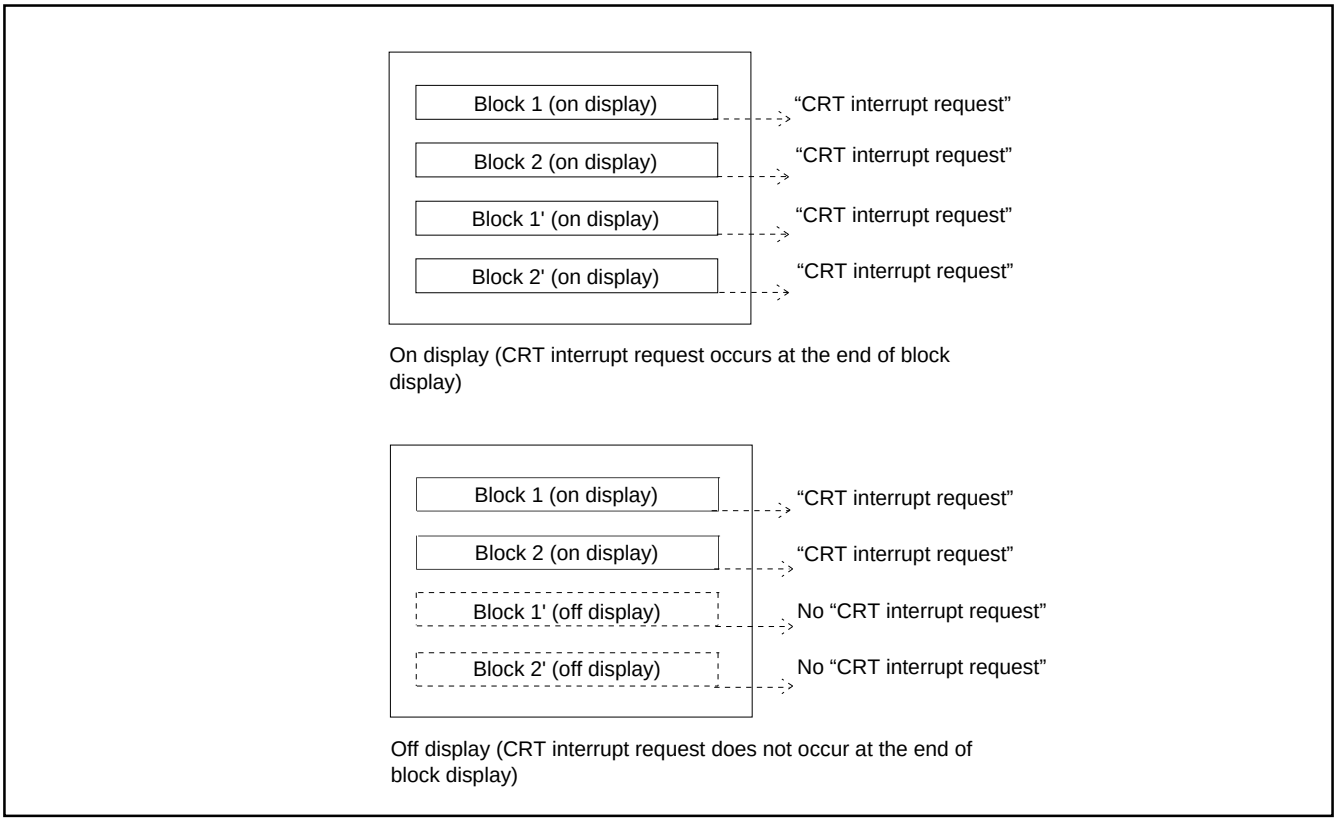


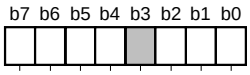
Fig. 47. Timing of CRT Interrupt Request

(8) CRT Output Pin Control

The CRT output pins R, G, B, and OUT can also function as ports $P5_2$, $P5_3$, $P5_4$ and $P5_5$. Set the corresponding bit of the port P5 direction register (address $00CB_{16}$) to "0" to specify these pins as CRT output pins, or set it to "1" to specify it as an general-purpose port P5 pins.

The input polarity of signals H_{SYNC} and V_{SYNC} and output polarity of signals R, G, B, and OUT can be specified with the bits of the CRT port control register (address $00EC_{16}$) . Set a bit to "0" to specify positive polarity; set it to "1" to specify negative polarity. The structure of the CRT port control register is shown in Figure 48.

CRT Port Control Register



CRT port control register (CRTP) [Address $00EC_{16}$]

B	Name	Functions	After reset	R	W
0	H_{SYNC} input polarity switch bit (HSYC)	0 : Positive polarity 1 : Negative polarity	0	R	W
1	V_{SYNC} input polarity switch bit (VSYC)	0 : Positive polarity 1 : Negative polarity	0	R	W
2	R/G/B output polarity switch bit (R/G/B)	0 : Positive polarity 1 : Negative polarity	0	R	W
3	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—
4	OUT output polarity switch bit (OUT)	0 : Positive polarity 1 : Negative polarity	0	R	W
5	R signal output switch bit (OP5)	0 : R signal output 1 : MUTE signal output	0	R	W
6	G signal output switch bit (OP6)	0 : G signal output 1 : MUTE signal output	0	R	W
7	B signal output switch bit (OP7)	0 : B signal output 1 : MUTE signal output	0	R	W

Fig. 48. CRT Port Control Register

(9) Raster Coloring Function

An entire screen (raster) can be colored by setting the bits 5 to 7 of the CRT port control register. Since each of the R, G, and B pins can be switched to raster coloring output, 7 raster colors can be obtained. If the R, G, and B pins have been set to MUTE signal output, a raster coloring signal is output in the part except a no-raster colored character (in Figure 49, a character “O”) during 1 horizontal scanning period. This ensures that character colors do not mix with the raster color. In this case, MUTE signal is output from the OUT1 pin.
An example in which a magenta character “I” and a red character “O” are displayed with blue raster coloring is shown in Figure 49.

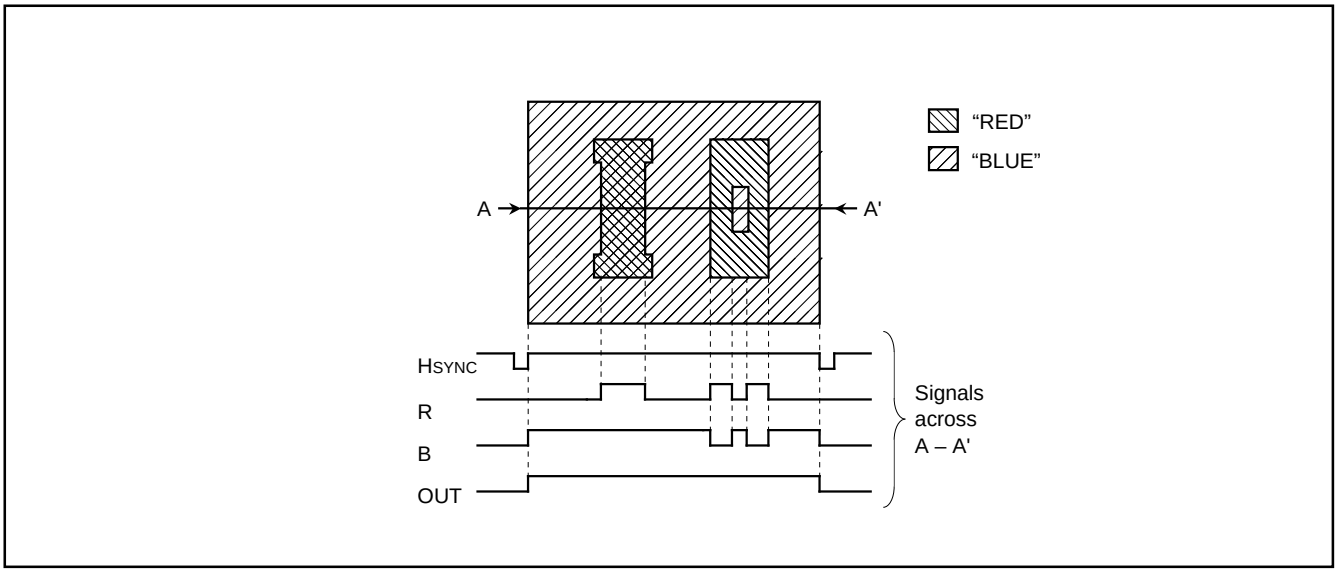


Fig. 49. Example of Raster Coloring

(10) Clock for Display

As a clock for display to be used for CRT display, it is possible to select one of the following 4 types.

- Main clock supplied from the X_{IN} pin
- Main clock supplied from the X_{IN} pin divided by 1.5
- Clock from the LC or RC supplied from the pins OSC1 and OSC2.
- Clock from the ceramic resonator or quartz-crystal oscillator supplied from the pins OSC1 and OSC2.

This clock for display can be selected for each block by the CRT clock selection register (address $00ED_{16}$).

When selecting the main clock, set the oscillation frequency to 8 MHz.

CRT Clock Selection Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0		

CRT clock selection register (CK) [Address $00ED_{16}$]

B	Name	Functions				After reset	R	W
0, 1	CRT clock selection bits (CK0,CK1)	b1	b0	Functions		0	R	W
		0	0	The clock for display is supplied by connecting RC or LC across the pins OSC1 and OSC2.				
		0	1	Since the main clock is used as the clock for display, the oscillation frequency is limited. Because of this, the character size in width (horizontal) direction is also limited. In this case, pins OSC1 and OSC2 are also used as input ports $P3_3$ and $P3_4$ respectively.	CRT oscillation frequency = $f(X_{IN})$			
		1	0		CRT oscillation frequency = $f(X_{IN})/1.5$			
		1	1	The clock for display is supplied by connecting the following across the pins OSC1 and OSC2. • a ceramic resonator only for CRT display and a feedback resistor • a quartz-crystal oscillator only for CRT display and a feedback resistor (Note)				
2 to 7	Fix these bits to "0."					0	R	W

Note: It is necessary to connect other ceramic resonator or quartz-crystal oscillator across the pins X_{IN} and X_{OUT}.

Fig. 50. CRT Clock Selection Register

ROM CORRECTION FUNCTION

This can correct program data in ROM. Up to 2 addresses (2 blocks) can be corrected, a program for correction is stored in the ROM correction memory in RAM. The ROM memory for correction is 32 bytes × 2 blocks.

Block 1 : addresses $02C0_{16}$ to $02DF_{16}$

Block 2 : addresses $02E0_{16}$ to $02FF_{16}$

Set the address of the ROM data to be corrected into the ROM correction address register. When the value of the counter matches the ROM data address in the ROM correction address, the main program branches to the correction program stored in the ROM memory for correction. To return from the correction program to the main program, the op code and operand of the JMP instruction (total of 3 bytes) are necessary at the end of the correction program. When the blocks 1 and 2 are used in series, the above instruction is not needed at the end of the block 1.

The ROM correction function is controlled by the ROM correction enable register.

Notes 1 : Specify the first address (op code address) of each instruction as the ROM correction address.

2 : Use the JMP instruction (total of 3 bytes) to return from the main program to the correction program.

3 : Do not set the same ROM correction address to the blocks 1 and 2.

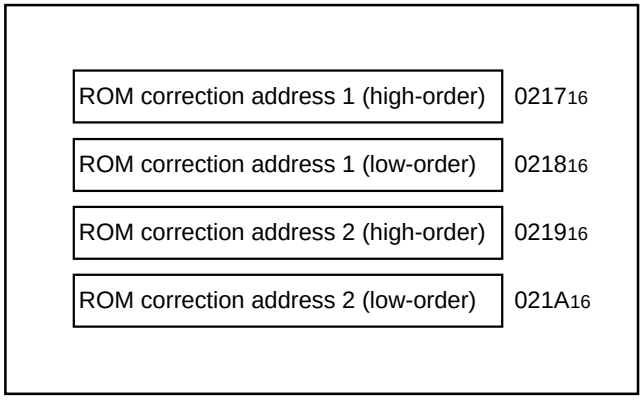
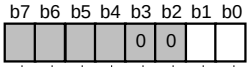


Fig. 51. ROM Correction Address Registers

ROM Correction Enable Register



ROM correction enable register (RCR) [Address $021B_{16}$]

B	Name	Functions	After reset	R	W
0	Block 1 enable bit (RC0)	0: Disabled 1: Enabled	0	R	W
1	Block 2 enable bit (RC1)	0: Disabled 1: Enabled	0	R	W
2,3	Fix these bits to "0."		0	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Fig. 52. ROM Correction Enable Register

RESET CIRCUIT

When the oscillation of a quartz-crystal oscillator or a ceramic resonator is stable and the power source voltage is 5 V ±10 %, hold the $\overline{\text{RESET}}$ pin at LOW for 2 μs or more, then return it to HIGH. Then, as shown in Figure 53, reset is released and the program starts from the address formed by using the content of address FFFF16 as the high-order address and the content of the address FFFE16 as the low-order address. The internal state of microcomputer at reset are shown in Figures 5 to 8.

An example of the reset circuit is shown in Figure 53.

The reset input voltage must be kept 0.6 V or less until the power source voltage surpasses 4.5 V.

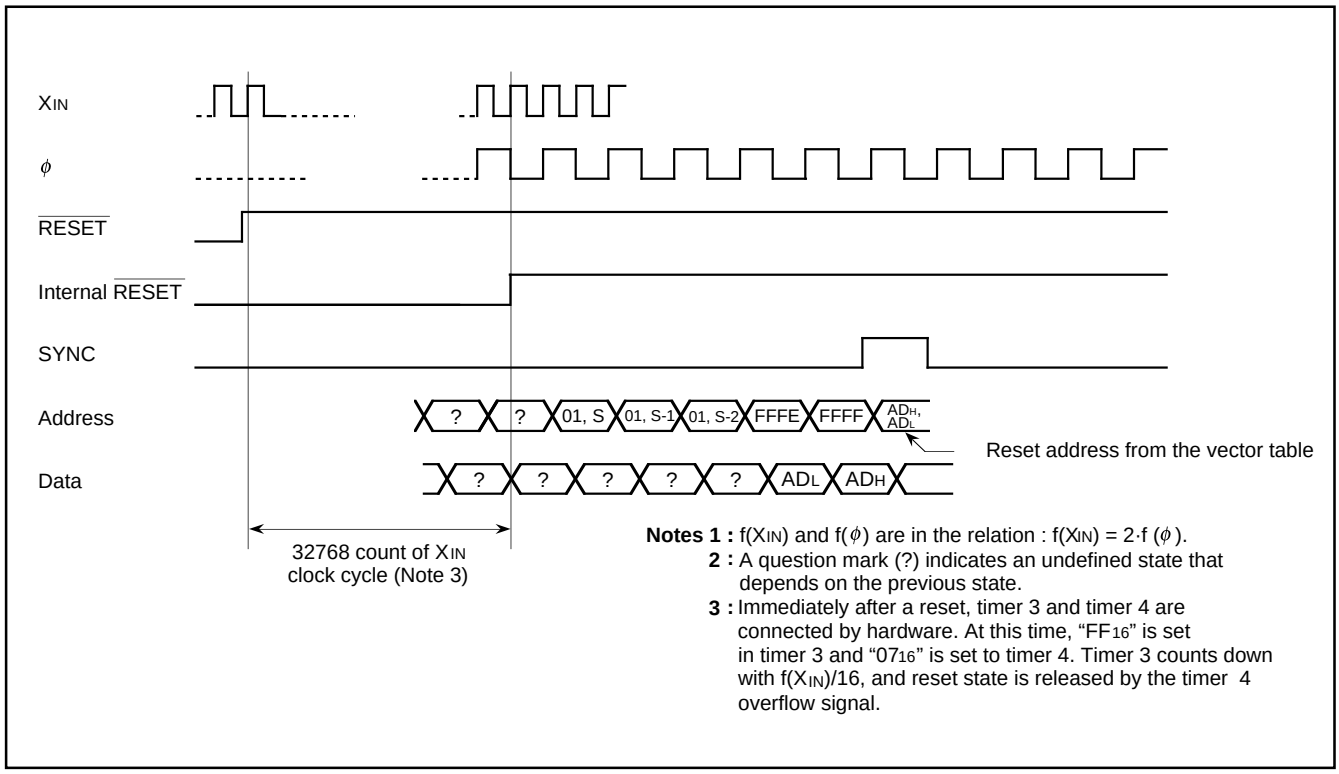


Fig. 53. Reset Sequence

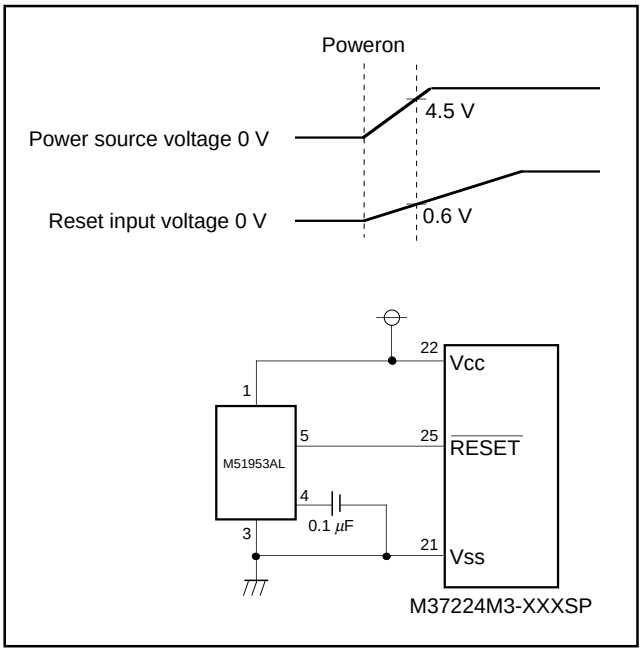


Fig. 54. Example of Reset Circuit

CLOCK GENERATING CIRCUIT

The built-in clock generating circuit is shown in Figure 57. When the STP instruction is executed, the internal clock ϕ stops at HIGH. At the same time, timers 3 and 4 are connected by hardware and "FF$_{16}$" is set in timer 3 and "07$_{16}$" is set in the timer 4. Select f(XIN)/16 as the timer 3 count source (set bit 0 of the timer 34 mode register to "0" before the execution of the STP instruction). Moreover, set the timer 3 and timer 4 interrupt enable bits to disabled ("0") before execution of the STP instruction). The oscillator restarts when external interrupt is accepted. However, the internal clock ϕ keeps its HIGH until timer 4 overflows, allowing time for oscillation stabilization when a ceramic resonator or a quartz-crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the HIGH but the oscillator continues running. This wait state is released when an interrupt is accepted (Note). Since the oscillator does not stop, the next instruction can be executed at once.

When returning from the stop or the wait state, to accept an interrupt, set the corresponding interrupt enable bit to "1" before executing the STP or the WIT instructions.

Note: In the wait mode, the following interrupts are invalid.
(1) VSYNC interrupt
(2) CRT interrupt
(3) f(XIN)/4096 interrupt
(4) Timer 1 interrupt using f(XIN)/4096 as count source
(5) Timer 2 interrupt using P24/TIM2 pin input as count source
(6) Timer 3 interrupt using P23/TIM3 pin input as count source
(7) Timer 4 interrupt using f(XIN)/2 as count source
(8) Multi-master I^{2}C-BUS interface interrupt

A circuit example using a ceramic resonator (or a quartz-crystal oscillator) is shown in Figure 55. Use the circuit constants in accordance with the resonator manufacture's recommended values. A circuit example with external clock input is shown in Figure 56. Input the clock to the XIN pin, and open the XOUT pin.

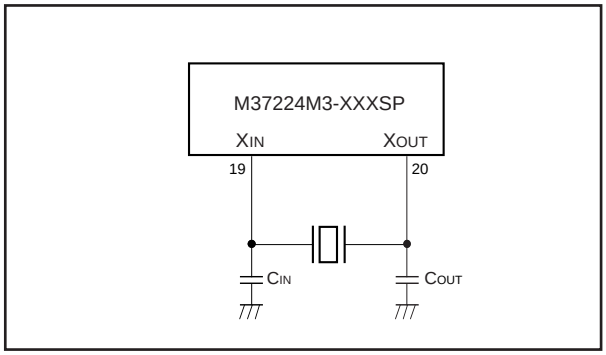


Fig. 55. Ceramic Resonator Circuit Example

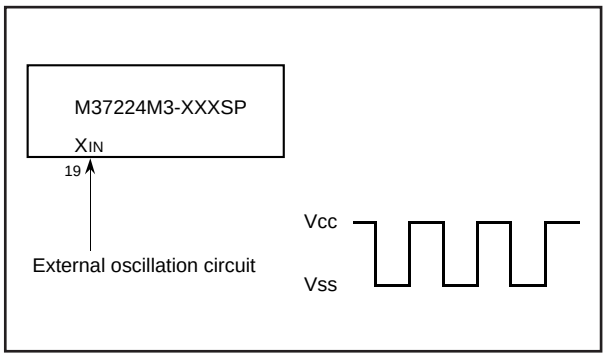


Fig. 56. External Clock Input Circuit Example

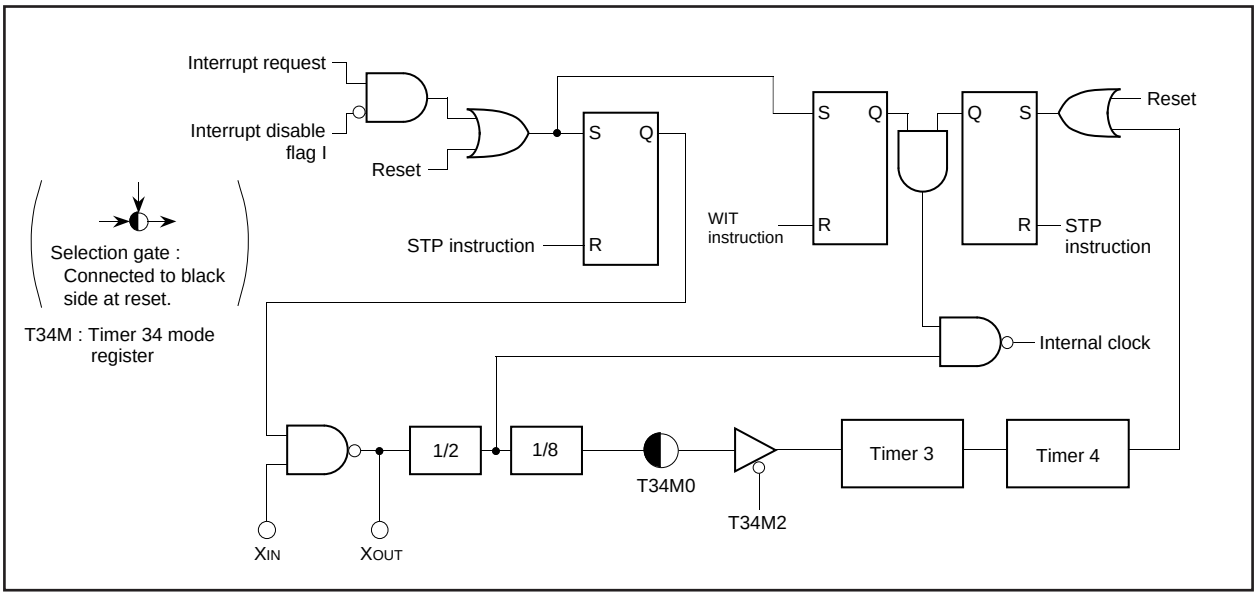


Fig. 57. Clock Generating Circuit Block Diagram

DISPLAY OSCILLATION CIRCUIT

The CRT display clock oscillation circuit has a built-in clock oscillation circuits, so that a clock for CRT display can be obtained simply by connecting an LC, an RC, a ceramic resonator or a quartz-crystal oscillator circuit across the pins OSC 1 and OSC 2. Select the clock for display with bits 0 and 1 of the CRT clock selection register (address $00ED_{16}$).

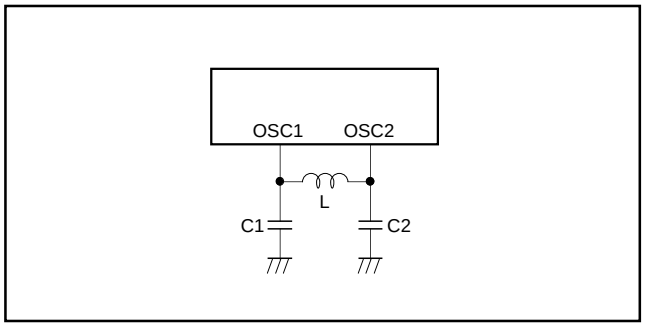
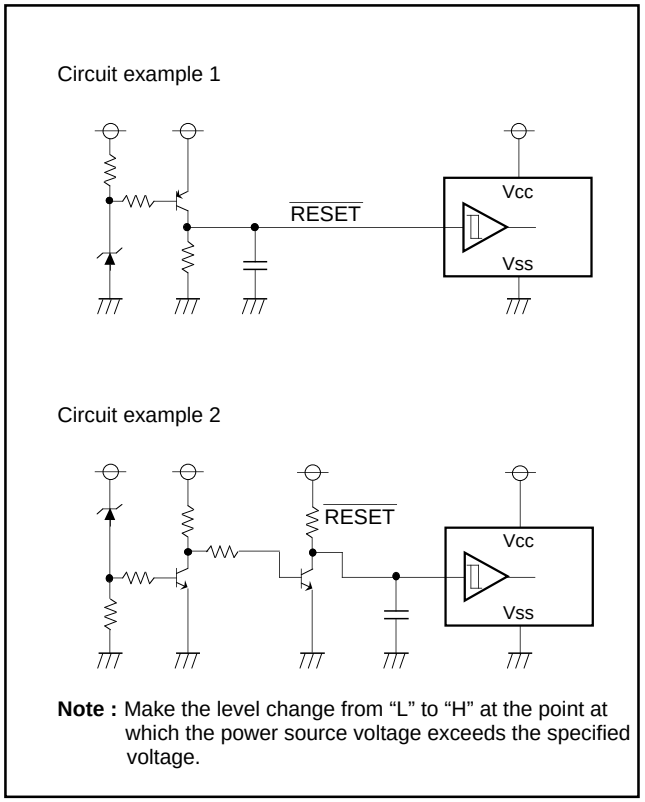


Fig. 58. Display Oscillation Circuit

AUTO-CLEAR CIRCUIT

When a power source is supplied, the auto-clear function will operate by connecting the following circuit to the $\overline{\text{RESET}}$ pin.



Note : Make the level change from "L" to "H" at the point at which the power source voltage exceeds the specified voltage.

Fig. 59. Auto-clear Circuit Example

ADDRESSING MODE

The memory access is reinforced with 17 kinds of addressing modes. Refer to SERIES 740 <Software> User's Manual for details.

MACHINE INSTRUCTIONS

There are 71 machine instructions. Refer to SERIES 740 <Soft- ware> User's Manual for details.

PROGRAMMING NOTES

(1) The divide ratio of the timer is 1/(n+1).
(2) Even though the BBC and BBS instructions are executed immediately after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. At least one instruction cycle is needed (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) After the ADC and SBC instructions are executed (in the decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instruction is executed.
(4) An NOP instruction is needed immediately after the execution of a PLP instruction.
(5) In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\ \mu F$) directly between the V_{CC} pin–V_{SS} pin and the V_{CC} pin–CNV_{SS} pin, using a thick wire.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation From.
(2) Mask Specification From.
(3) Data to be written to ROM, in EPROM form (32-pin DIP Type 27C101, three identical copies).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage	V_{CC}	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6	V
V_I	Input voltage	CNV_{SS}		–0.3 to 6	V
V_I	Input voltage	$P0_0$–$P0_7$,$P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, OSC1, X_{IN}, H_{SYNC}, V_{SYNC}, $\overline{RESET}$		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	$P0_6$, $P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_2$, R, G, B, OUT, D-A, X_{OUT}, OSC2		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	$P0_0$–$P0_5$		–0.3 to 13	V
I_{OH}	Circuit current	R, G, B, OUT, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, D-A		0 to 1 (Note 1)	mA
I_{OL1}	Circuit current	R, G, B, OUT, $P0_6$, $P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_2$, D-A		0 to 2 (Note 2)	mA
I_{OL2}	Circuit current	$P0_0$–$P0_5$		0 to 1 (Note 2)	mA
I_{OL3}	Circuit current	$P2_4$–$P2_7$		0 to 10 (Note 3)	mA
P_d	Power dissipation		T_a = 25 °C	550	mW
T_{opr}	Operating temperature			–10 to 70	°C
T_{stg}	Storage temperature			–40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (T_a = –10 °C to 70 °C, V_{CC} = 5 V ± 10 %, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (Note 4), During CPU, CRT operation		4.5	5.0	5.5	V
V_{SS}	Power source voltage		0	0	0	V
V_{IH1}	HIGH input voltage	$P0_0$–$P0_7$,$P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, S_{IN}, S_{CLK}, H_{SYNC}, V_{SYNC}, $\overline{RESET}$, X_{IN}, OSC1, TIM2, TIM3, INT1, INT2, INT3	0.8V_{CC}		V_{CC}	V
V_{IL1}	LOW input voltage	$P0_0$–$P0_7$,$P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$	0		0.4 V_{CC}	V
V_{IL2}	LOW input voltage	H_{SYNC}, V_{SYNC}, $\overline{RESET}$,TIM2, TIM3, INT1, INT2, INT3, X_{IN}, OSC1, S_{IN}, S_{CLK}	0		0.2 V_{CC}	mA
I_{OH}	HIGH average output current (Note 1)	R, G, B, OUT, D-A, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$			1	mA
I_{OL1}	LOW average output current (Note 2)	R, G, B, OUT, D-A, $P0_6$, $P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_2$			2	mA
I_{OL2}	LOW average output current (Note 2)	$P0_0$–$P0_5$			1	mA
I_{OL3}	LOW average output current (Note 3)	$P2_4$–$P2_7$			10	mA
f_{CPU}	Oscillation frequency (for CPU operation) (Note 5)	X_{IN}	7.9	8.0	8.1	MHz
f_{CRT}	Oscillation frequency (for CRT display) (Note 5)	OSC1	5.0		8.0	MHz
f_{hs1}	Input frequency	TIM2, TIM3			100	kHz
f_{hs2}	Input frequency	S_{CLK}			1	MHz

Notes 1: The total current that flows out of the IC must be 20 mA (max.).
2: The total input current to IC (I_{OL1} + I_{OL2}) must be 30 mA or less.
3: The total average input current for ports $P2_4$–$P2_7$ to IC must be 20 mA or less.
4: Connect 0.1 μF or more capacitor externally between the power source pins V_{CC}–V_{SS} so as to reduce power source noise. Also connect 0.1 μF or more capacitor externally between the pins V_{CC}–CNV_{SS}.
5: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit.

ELECTRIC CHARACTERISTICS (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 8 MHz, T_a = –10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
I_{CC}	Power source current	System operation	V_{CC} = 5.5 V, f(X_{IN}) = 8 MHz	CRT OFF		20	40	mA
				CRT ON		30	60	
		Stop mode	V_{CC} = 5.5 V, f(X_{IN}) = 0				300	μA
V_{OH}	HIGH output voltage	R, G, B, OUT, D-A, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$	V_{CC} = 4.5 V, I_{OH} = –0.5 mA		2.4			V
V_{OL}	LOW output voltage	R, G, B, OUT, D-A, $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_2$	V_{CC} = 4.5 V, I_{OL} = 0.5 mA				0.4	V
	LOW output voltage	$P2_4$–$P2_7$	V_{CC} = 4.5 V, I_{OL} = 10.0 mA				3.0	V
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$	V_{CC} = 5.0 V			0.5	1.3	V
	Hysteresis (Note)	H_{SYNC}, V_{SYNC}, TIM2, TIM3, INT1, INT2, INT3, S_{IN}, S_{CLK}	V_{CC} = 5.0 V			0.5	1.3	
I_{IZH}	HIGH input leak current	$\overline{RESET}$, $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, H_{SYNC}, V_{SYNC}	V_{CC} = 5.5 V, V_I = 5.5 V				5	μA
I_{IZL}	LOW input leak current	$\overline{RESET}$, $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, H_{SYNC}, V_{SYNC}	V_{CC} = 5.5 V, V_I = 0 V				5	μA
I_{OZH}	HIGH output leak current	$P0_0$–$P0_5$	V_{CC} = 5.5 V, V_O = 12 V				10	μA

Note: $P0_6$, $P0_7$, $P1_5$, $P2_3$, $P2_4$ have the hysteresis when these pins are used as interrupt input pins or timer input pins. $P2_0$–$P2_2$ have the hysteresis when these pins are used as serial I/O pins.

A-D COMPARATOR CHARACTERISTICS

(V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 8 MHz, T_a = –10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				6	bits
—	Absolute accuracy		0	±1	±2	LSB

Note: When V_{CC} = 5 V, 1 LSB = 5/64 V.

D-A CONVERTER CHARACTERISTICS

(V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 8 MHz, T_a = –10 °C to 70 °C, unless otherwise noted)

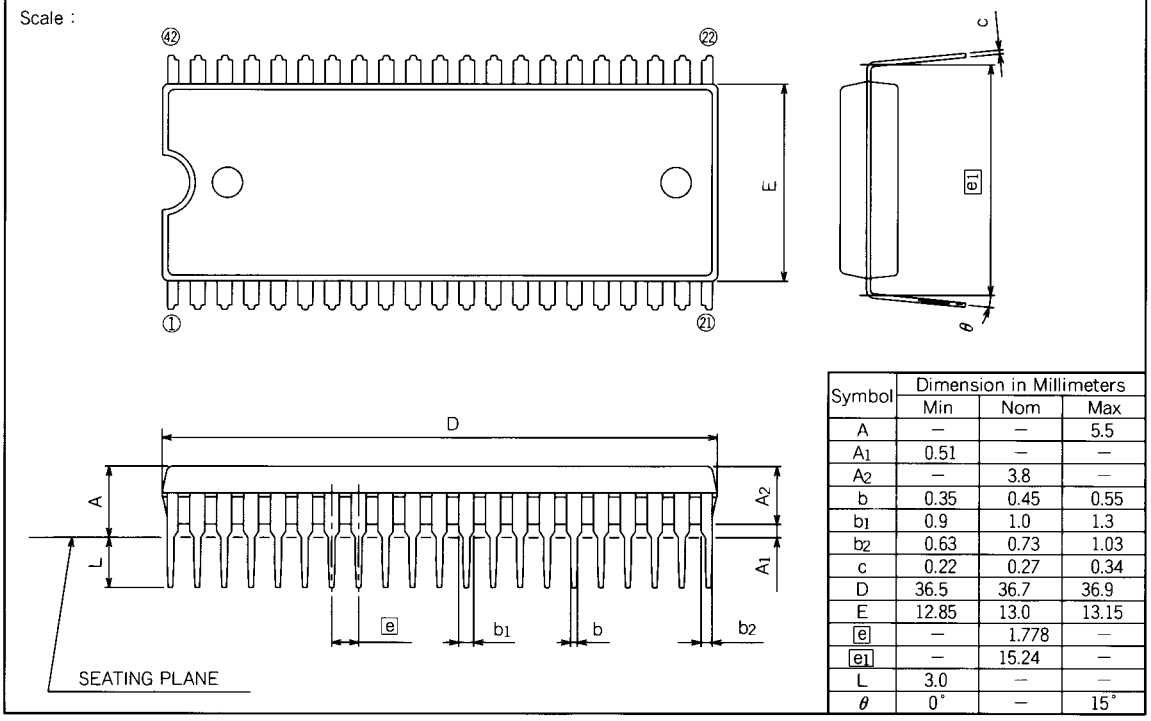
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				7	bits
—	Absolute accuracy				2	%
tsu	Setting time				3	μs
R_O	Output resistor		1	2.5	4	kΩ

PACKAGE OUTLINE

42P4B — Plastic 42pin 600mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP42-P-600-1.78	—	4.1	Alloy 42/Cu Alloy

Scale :



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	5.5
A_1	0.51	—	—
A_2	—	3.8	—
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
b_2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	36.5	36.7	36.9
E	12.85	13.0	13.15
e	—	1.778	—
e_1	—	15.24	—
L	3.0	—	—
θ	0°	—	15°

GZZ–SH11–11B < 6XA0 >

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37224M3-XXXSP
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

✵ 1. Confirmation

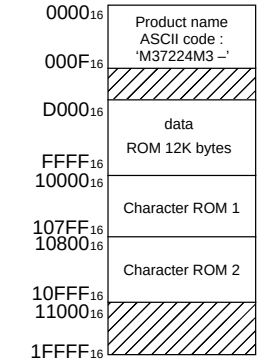
Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)

☐ **27C101**

EPROM address



(1) Set "FF$_{16}$" in the shaded area.
(2) Write the ASCII codes that indicate the product name of "M37220M3–" to addresses 0000 $_{16}$ to 000F$_{16}$.

EPROM data check item (confirm the EPROM data and check " ✓" the appropriate box)

- Is "FF$_{16}$" in the shaded area ? → Yes ☐
- Are the ASCII codes that indicates the product name of "M37224M3–" to addresses 0000 $_{16}$ to 000F$_{16}$? → Yes ☐

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered. Fill out the appropriate mark specification form (42P4B for M37224M3-XXXSP) and attach to the mask ROM confirmation form.

✵ 3. Comments (1/3)

GZZ–SH11–22B <6XA0 >

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37224M3-XXXSP
MITSUBISHI ELECTRIC

How to Write the Product Name and Character ROM Data onto EPROMs

Addresses 0000_{16} to $000F_{16}$ store the product name, and addresses 10000_{16} to $10FFF_{16}$ store the character pattern. If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Please make sure the data is written correctly.

1. How to input the name of the product with the ASCII code
   ASCII codes 'M37224M3-' are listed on the right.
   The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = 4 D $_{16}$	0008_{16}	'–' = 2 D $_{16}$
0001_{16}	'3' = 3 3 $_{16}$	0009_{16}	F F $_{16}$
0002_{16}	'7' = 3 7 $_{16}$	$000A_{16}$	F F $_{16}$
0003_{16}	'2' = 3 2 $_{16}$	$000B_{16}$	F F $_{16}$
0004_{16}	'2' = 3 2 $_{16}$	$000C_{16}$	F F $_{16}$
0005_{16}	'4' = 3 4 $_{16}$	$000D_{16}$	F F $_{16}$
0006_{16}	'M' = 4 D $_{16}$	$000E_{16}$	F F $_{16}$
0007_{16}	'3' = 3 3 $_{16}$	$000F_{16}$	F F $_{16}$

2. Inputting the character ROM
   Input the character ROM data by dividing it into character ROM1 and character ROM2. For the character ROM data, see the next page and on.

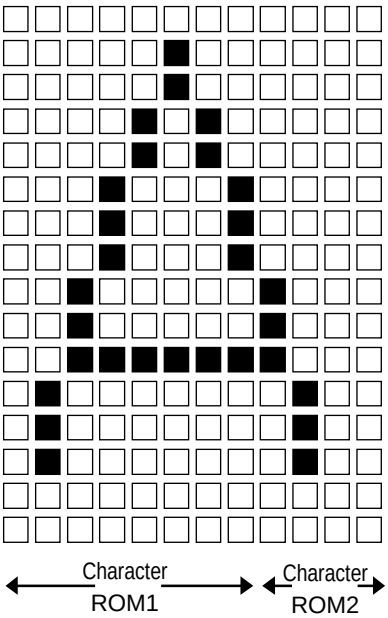
GZZ–SH11–22B< 6XA0 >

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37224M3-XXXSP
MITSUBISHI ELECTRIC

The structure of character ROM (divided of 12 ×16 dots font)

Example

Character code "$1A_{16}$"



Example $101A0_{16}$ to $101AF_{16}$

	b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	
0	0 0 0 0 0 0 0 0	00_{16}
1	0 0 0 0 0 1 0 0	04_{16}
2	0 0 0 0 0 1 0 0	04_{16}
3	0 0 0 0 1 0 1 0	$0A_{16}$
4	0 0 0 0 1 0 1 0	$0A_{16}$
5	0 0 0 1 0 0 0 1	11_{16}
6	0 0 0 1 0 0 0 1	11_{16}
7	0 0 0 1 0 0 0 1	11_{16}
8	0 0 1 0 0 0 0 0	20_{16}
9	0 0 1 0 0 0 0 0	20_{16}
A	0 0 1 1 1 1 1 1	$3F_{16}$
B	0 1 0 0 0 0 0 0	40_{16}
C	0 1 0 0 0 0 0 0	40_{16}
D	0 1 0 0 0 0 0 0	40_{16}
E	0 0 0 0 0 0 0 0	00_{16}
F	0 0 0 0 0 0 0 0	00_{16}

Example $109A0_{16}$ to $109AF_{16}$

	b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0	
0	1 1 1 1 0 0 0 0	$F0_{16}$
1	1 1 1 1 0 0 0 0	$F0_{16}$
2	1 1 1 1 0 0 0 0	$F0_{16}$
3	1 1 1 1 0 0 0 0	$F0_{16}$
4	1 1 1 1 0 0 0 0	$F0_{16}$
5	1 1 1 1 0 0 0 0	$F0_{16}$
6	1 1 1 1 0 0 0 0	$F0_{16}$
7	1 1 1 1 0 0 0 0	$F0_{16}$
8	1 1 1 1 1 0 0 0	$F8_{16}$
9	1 1 1 1 1 0 0 0	$F8_{16}$
A	1 1 1 1 1 0 0 0	$F8_{16}$
B	1 1 1 1 0 1 0 0	$F4_{16}$
C	1 1 1 1 0 1 0 0	$F4_{16}$
D	1 1 1 1 0 1 0 0	$F4_{16}$
E	1 1 1 1 0 0 0 0	$F0_{16}$
F	1 1 1 1 0 0 0 0	$F0_{16}$

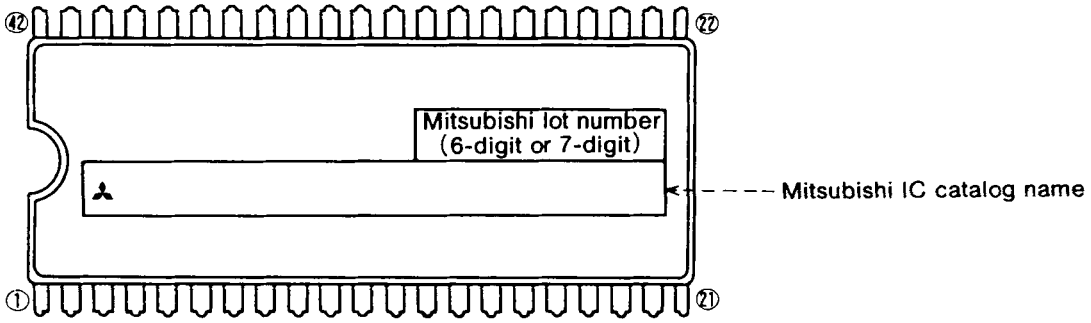
F_{16}

42P4B (42-PIN SHRINK DIP) MARK SPECIFICATION FORM

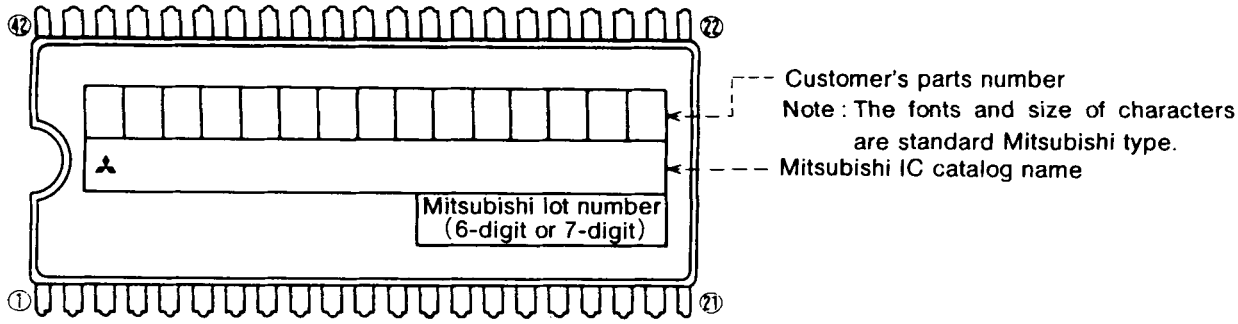
Mitsubishi IC catalog name ☐

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark

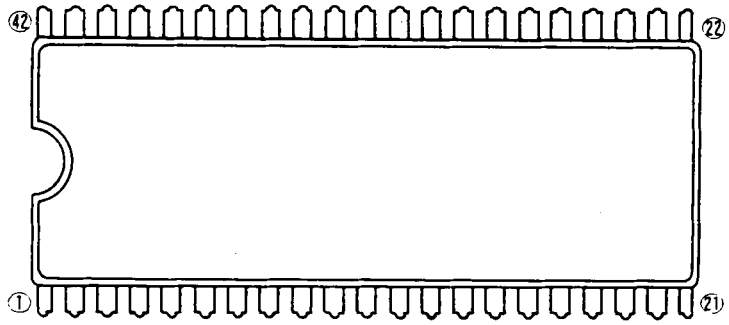


B. Customer's Parts Number + Mitsubishi Catalog Name



Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 15 characters :
Only 0~9, A~Z, +, −, /, (,), &, ©, . (period), and , (comma) are usable.
4 : If the Mitsubishi logo ⅄ is not required, check the box on the right. ⅄Mitsubishi logo is not required ☐

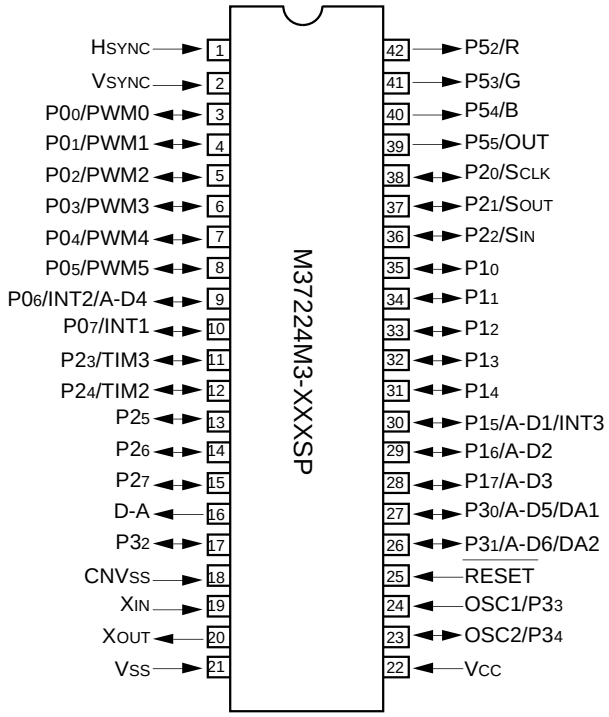
C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.
Special logo required
The standard Mitsubishi font is used for all characters except for a logo. ☐

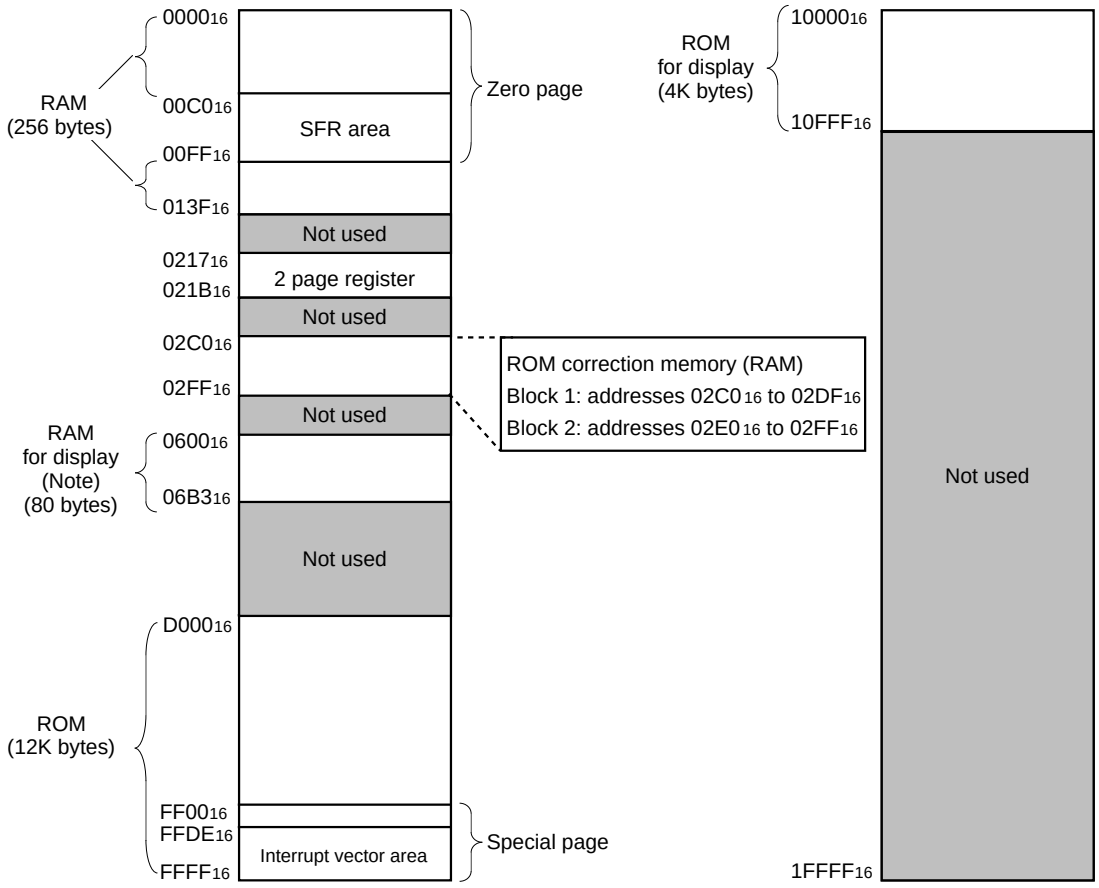
APPENDIX

Pin Configuration (TOP VIEW)



Outline 42P4B

Memory Map



Note: Refer to Table 8. Contents of CRT display RAM.

Memory Map of Special Function Register (SFR)

■SFR Area (addresses $C0_{16}$ to DF_{16})

<Bit allocation>

: } Function bit
Name : } Function bit

: No function bit

0 : Fix this bit to "0" (do not write "1")

1 : Fix this bit to "1" (do not write "0")

<State immediately after reset >

0 : "0" immediately after reset

1 : "1" immediately after reset

? : Undefined immediately after reset

Address	Register	Bit allocation b7 b6 b5 b4 b3 b2 b1 b0	State immediately after reset b7 b6 b5 b4 b3 b2 b1 b0
$C0_{16}$	Port P0 (P0)		?
$C1_{16}$	Port P0 direction register (D0)		00_{16}
$C2_{16}$	Port P1 (P1)		?
$C3_{16}$	Port P1 direction register (D1)		00_{16}
$C4_{16}$	Port P2 (P2)		?
$C5_{16}$	Port P2 direction register (D2)		00_{16}
$C6_{16}$	Port P3 (P3)		0 0 0 ? ? ? ? ?
$C7_{16}$	Port P3 direction register (D3)		00_{16}
$C8_{16}$			?
$C9_{16}$			?
CA_{16}	Port P5 (P5)		0 0 ? ? ? ? ? ?
CB_{16}	Port P5 direction register (D5)		00_{16}
CC_{16}			?
CD_{16}	Port P3 output mode control register (P3S)	DA2S DA1S P31S P30S	00_{16}
CE_{16}	DA-H register (DA-H)		?
CF_{16}	DA-L register (DA-L)		0 0 ? ? ? ? ? ?
$D0_{16}$	PWM0 register (PWM0)		?
$D1_{16}$	PWM1 register (PWM1)		?
$D2_{16}$	PWM2 register (PWM2)		?
$D3_{16}$	PWM3 register (PWM3)		?
$D4_{16}$	PWM4 register (PWM4)		?
$D5_{16}$	PWM output control register 1 (PW)	PW7 PW6 PW5 PW4 PW3 PW2 PW1 PW0	00_{16}
$D6_{16}$	PWM output control register 2 (PN)	PN4 PN3 PN2	00_{16}
$D7_{16}$			?
$D8_{16}$			?
$D9_{16}$			?
DA_{16}			?
DB_{16}			?
DC_{16}	Serial I/O mode register (SM)	SM6 SM5 0 SM3 SM2 SM1 SM0	00_{16}
DD_{16}	Serial I/O regsiter (SIO)		?
DE_{16}	DA1 conversion register (DA1)	DA17 0 DA15 DA14 DA13 DA12 DA11 DA10	?
DF_{16}	DA2 conversion register (DA2)	DA27 0 DA25 DA24 DA23 DA22 DA21 DA20	?

■ SFR Area (addresses $E0_{16}$ to FF_{16})

<Bit allocation>

Name : } Function bit

: No function bit

0 : Fix this bit to "0" (do not write "1")

1 : Fix this bit to "1" (do not write "0")

<State immediately after reset>

0 : "0" immediately after reset

1 : "1" immediately after reset

? : Undefined immediately after reset

Address	Register	Bit allocation b7							b0	State immediately after reset b7							b0
$E0_{16}$	Horizontal register (HR)			HR5	HR4	HR3	HR2	HR1	HR0	00_{16}							
$E1_{16}$	Vertical register 1 (CV1)		CV16	CV15	CV14	CV13	CV12	CV11	CV10	0	?	?	?	?	?	?	?
$E2_{16}$	Vertical register 1 (CV1)		CV26	CV25	CV24	CV23	CV22	CV21	CV20	0	?	?	?	?	?	?	?
$E3_{16}$										?							
$E4_{16}$	Character size register (CS)					CS21	CS20	CS11	CS10	0	0	0	0	?	?	?	?
$E5_{16}$	Border selection register (MD)						MD20		MD10	0	0	0	0	0	?	0	?
$E6_{16}$	Color register 0 (CO0)			CO05		CO03	CO02	CO01	0	00_{16}							
$E7_{16}$	Color register 1 (CO1)			CO15		CO13	CO12	CO11	0	00_{16}							
$E8_{16}$	Color register 2 (CO2)			CO25		CO23	CO22	CO21	0	00_{16}							
$E9_{16}$	Color register 3 (CO3)			CO35		CO33	CO32	CO31	0	00_{16}							
EA_{16}	CRT control register (CO)						CC2	CC1	CC0	00_{16}							
EB_{16}										?							
EC_{16}	CRT port control register (CRTP)	OP7	OP6	OP5	OUT		R/G/B	VSYC	HSYC	00_{16}							
ED_{16}	CRT clock selection register (CK)	0	0	0	0	0	0	CK1	CK0	00_{16}							
EE_{16}	A-D control register 1 (AD1)				ADM4		ADM2	ADM1	ADM0	0	0	0	?	0	0	0	0
EF_{16}	A-D control register 2 (AD2)			ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	00_{16}							
$F0_{16}$	Timer 1 (TM1)									FF_{16}							
$F1_{16}$	Timer 2 (TM2)									07_{16}							
$F2_{16}$	Timer 3 (TM3)									FF_{16}							
$F3_{16}$	Timer 4 (TM4)									07_{16}							
$F4_{16}$	Timer 12 mode register (T12M)			0	T12M4	T12M3	T12M2	T12M1	T12M0	00_{16}							
$F5_{16}$	Timer 34 mode register (T34M)			T34M5	T34M4	T34M3	T34M2	T34M1	T34M0	00_{16}							
$F6_{16}$	PWM5 register (PWM5)									?							
$F7_{16}$										?							
$F8_{16}$										?							
$F9_{16}$	Interrupt input polarity register (RE)	0		RE5	RE4	RE3	0	0		0	0	0	0	0	0	0	?
FA_{16}	Test register (TEST)	00_{16}								00_{16}							
FB_{16}	CPU mode register (CPUM)	1	1	1	1	1	CM2	0	0	FC_{16}							
FC_{16}	Interrupt request register 1 (IREQ1)	IT3R		VSCR	CRTR	TM4R	TM3R	TM2R	TM1R	00_{16}							
FD_{16}	Interrupt request register 2 (IREQ2)	0			MSR		S1R	IT2R	IT1R	00_{16}							
FE_{16}	Interrupt control register 1 (ICON1)	IT3E		VSCE	CRTE	TM4E	TM3E	TM2E	TM1E	00_{16}							
FF_{16}	Interrupt control register 2 (ICON2)	0	0	0	MSE	0	S1E	IT2E	IT1E	00_{16}							

■SFR Area (addresses 217_{16} to $21B_{16}$)

<Bit allocation>

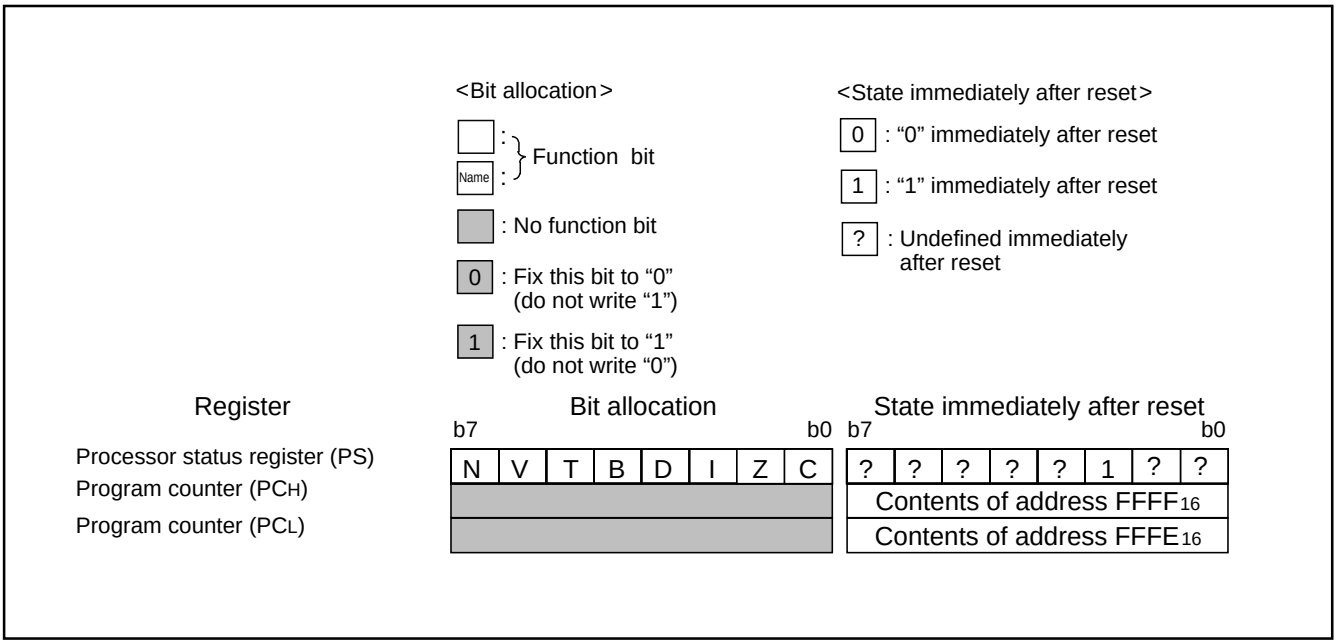
- : Function bit (Name)
- : No function bit
- 0 : Fix this bit to "0" (do not write "1")
- 1 : Fix this bit to "1" (do not write "0")

<State immediately after reset>

- 0 : "0" immediately after reset
- 1 : "1" immediately after reset
- ? : Undefined immediately after reset

Address	Register	Bit allocation b7 b6 b5 b4 b3 b2 b1 b0	State immediately after reset b7 b6 b5 b4 b3 b2 b1 b0
217_{16}	ROM correction address 1 (high-order)		00_{16}
218_{16}	ROM correction address 1 (low-order)		00_{16}
219_{16}	ROM correction address 2 (high-order)		00_{16}
$21A_{16}$	ROM correction address 2 (low-order)		00_{16}
$21B_{16}$	ROM correction enable register (RCR)	0 0 RC1 RC0	? ? ? ? 0 0 0 0

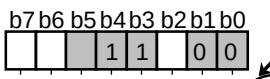
Internal State of Processor Status Register and Program Counter at Reset



Structure of Register

The figure of each register structure describes its functions, contents at reset, and attributes as follows:

CPU Mode Register



Bits — Values immediately after reset release (Note 1) — Bit attributes (Note 2)

CPU mode register (CPUM) (CM) [Address FB 16]

B	Name	Functions	After reset	R	W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: 1 0: 1 1: } Not available	0	R	W
2	Stack page selection bit (Note) (CM2)	0: 0 page 1: 1 page	0	R	W
3, 4	Fix these bits to "1."		1	R	W
5	Nothing is assigned. This bit is write disable bit. When this bit is read out, the value is "0."		1	R	W
6, 7	Clock switch bits (CM6, CM7)	b7 b6 0 0: f(XIN) = 8 MHz 0 1: f(XIN) = 12 MHz 1 0: f(XIN) = 16 MHz 1 1: Do not set	0	R	W

: Bit in which nothing is assigned

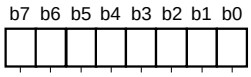
Notes 1: Values immediately after reset release
0••••••"0" after reset release
1••••••"1" after reset release
?••••••Indeterminate after reset release

2: Bit attributes••••••The attributes of control register bits are classified into 3 types : read-only, write-only and read and write. In the figure, these attributes are represented as follows :

R••••••Read
○ ••••••Read enabled
× ••••••Read disabled

W••••••Write
○ ••••••Write enabled
× ••••••Write disabled
✻ ••••••"0" can be set by software, but "1" cannot be set.

Port Pi Direction Register



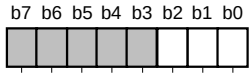
Port Pi direction register (Di) (i=0,1,2) [Addresses $00C1_{16}$, $00C3_{16}$, $00C5_{16}$]

B	Name	Functions	After reset	R	W
0	Port Pi direction register	0 : Port Pi_0 input mode 1 : Port Pi_0 output mode	0	R	W
1		0 : Port Pi_1 input mode 1 : Port Pi_1 output mode	0	R	W
2		0 : Port Pi_2 input mode 1 : Port Pi_2 output mode	0	R	W
3		0 : Port Pi_3 input mode 1 : Port Pi_3 output mode	0	R	W
4		0 : Port Pi_4 input mode 1 : Port Pi_4 output mode	0	R	W
5		0 : Port Pi_5 input mode 1 : Port Pi_5 output mode	0	R	W
6		0 : Port Pi_6 input mode 1 : Port Pi_6 output mode	0	R	W
7		0 : Port Pi_7 input mode 1 : Port Pi_7 output mode	0	R	W

Port Pi Direction Register

Addresses $00C1_{16}$, $00C3_{16}$, $00C5_{16}$

Port P3 Direction Register



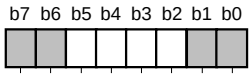
Port P3 direction register (D3) [Address $00C7_{16}$]

B	Name	Functions	After reset	R	W
0	Port P3 direction register	0 : Port $P3_0$ input mode 1 : Port $P3_0$ output mode	0	R	W
1		0 : Port $P3_1$ input mode 1 : Port $P3_1$ output mode	0	R	W
2		0 : Port $P3_2$ input mode 1 : Port $P3_2$ output mode	0	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Port P3 Direction Register

Address $00C7_{16}$

Port P5 Direction Register



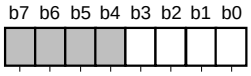
Port P5 direction register (D5) [Address $00CB_{16}$]

B	Name	Functions	After reset	R	W
0, 1, 6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
2 to 5	Port P5 direction register	0 : CRT output (R) 1 : Output port $P5_2$	0	R	W
		0 : CRT output (G) 1 : Output port $P5_3$	0	R	W
		0 : CRT output (B) 1 : Output port $P5_4$	0	R	W
		0 : CRT output (OUT) 1 : Output port $P5_5$	0	R	W

Port P5 Direction Register

Addresses $00CB_{16}$

Port P3 Output Mode Control Register



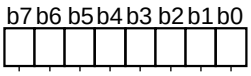
Port P3 output mode control register (P3S) [address $00CD_{16}$]

B	Name	Functions	After reset	R	W
0	$P3_0$ output structure selection bit (P30S)	0 : CMOS output 1 : N-channel open-drain output	0	R	W
1	$P3_1$ output structure selection bit (P31S)	0 : CMOS output 1 : N-channel open-drain output	0	R	W
2	DA1 output enable bit	0 : $P3_0$ input/output 1 : DA1 output	0	R	W
3	DA2 output enable bit	0 : $P3_1$ input/output 1 : DA2 output	0	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Port P3 Output Mode Control Register

Address $00CD_{16}$

PWM Output Control Register 1



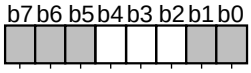
PWM output control register 1 (PW) [Address 00D5$_{16}$]

B	Name	Functions	After reset	R	W
0	DA, PWM count source selection bit (PW0)	0 : Count source supply 1 : Count source stop	0	R	W
1	DA/PN4 output selection bit (PW1)	0 : DA output 1 : PN4 output	0	R	W
2	P0$_0$/PWM0 output selection bit (PW2)	0: P0$_0$ output 1: PWM0 output	0	R	W
3	P0$_1$/PWM1 output selection bit (PW3)	0: P0$_1$ output 1: PWM1 output	0	R	W
4	P0$_2$/PWM2 output selection bit (PW4)	0: P0$_2$ output 1: PWM2 output	0	R	W
5	P0$_3$/PWM3 output selection bit (PW5)	0: P0$_3$ output 1: PWM3 output	0	R	W
6	P0$_4$/PWM4 output selection bit (PW6)	0: P0$_4$ output 1: PWM4 output	0	R	W
7	P0$_5$/PWM5 output selection bit (PW7)	0: P0$_5$ output 1: PWM5 output	0	R	W

PWM Output Control Register 1

Address 00D5$_{16}$

PWM Output Control Register 2



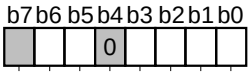
PWM output control register 2 (PN) [Address 00D6$_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—
2	DA output polarity selection bit (PN3)	0 : Positive polarity 1 : Negative polarity	0	R	W
3	PWM output polarity selection bit (PN4)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	DA general-purpose output bit (PN5)	0 : Output LOW 1 : Output HIGH	0	R	W
5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

PWM Output Control Register 2

Address 00D6$_{16}$

Serial I/O Mode Register



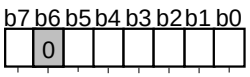
Serial I/O mode register (SM) [Address 00DC16]

B	Name	Functions	After reset	R	W
0, 1	Internal synchronous clock selection bits (SM0, SM1)	b1 b0 0 0: f(XIN)/4 0 1: f(XIN)/16 1 0: f(XIN)/32 1 1: f(XIN)/64	0	R	W
2	Synchronous clock selection bit (SM2)	0: External clock 1: Internal clock	0	R	W
3	Serial I/O port selection bit (SM3)	0: P20, P21 functions as port 1: SCLK, SOUT	0	R	W
4	Fix this bit to "0."		0	R	W
5	Transfer direction selection bit (SM5)	0: LSB first 1: MSB first	0	R	W
6	Serial input pin selection bit (SM6)	0: Input signal from SIN pin 1: Input signal from SOUT pin	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

Serial I/O Mode Register

Address 00DC16

DAi Conversion Register



DAi conversion register (DAi) (i = 1 and 2) [Address 00DE16, 00DF16]

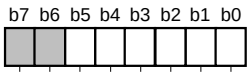
B	Name	Functions	After reset	R	W
0 to 5, 7	DA conversion set bits (DAi0 to DAi5)	b7 b5 b4 b3 b2 b1 b0 0 0 0 0 0 0 0 : 0/128Vcc 1 0 0 0 0 0 1 : 1/128Vcc 0 0 0 0 0 1 0 : 2/128Vcc 1 1 1 1 1 1 0 : 125/128Vcc 0 1 1 1 1 1 1 : 126/128Vcc 1 1 1 1 1 1 1 : 127/128Vcc	Indeterminate	R	W
6	Fix this bit to "0."		0	R	W

DAi Conversion Register

Addresses 00DE16, 00DF16

MITSUBISHI ELECTRIC

Horizontal Position Register



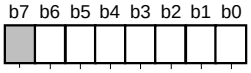
Horizontal position register (HR) [Address $00E0_{16}$]

B	Name	Functions	After reset	R	W
0 to 5	Horizontal display start positions (HR0 to HR5)	64 steps (00_{16} to $3F_{16}$)	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When thses bits are read out, the values are "0."		0	R	—

Horizontal Position Register

Address $00E0_{16}$

Vertical Position Register i



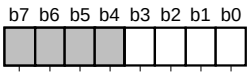
Vertical position register i (CVi) (i = 1 and 2) [Addresses $00E1_{16}$, $00E2_{16}$]

B	Name	Functions	After reset	R	W
0 to 6	Vertical display start positions (CVi : CVi0 to CVi6)	128 steps (00_{16} to $7F_{16}$)	Indeterminate	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—

Vertical Position Register i

Address $00E1_{16}$, $00E2_{16}$

Character Size Register



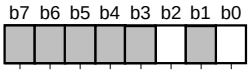
Character size register (CS) [Address $00E4_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Character size of block 1 selection bits (CS10, CS11)	00 : Minimum size 01 : Medium size 10 : Large size 11 : Do not set.	Indeterminate	R	W
2,3	Character size of block 2 selection bits (CS20,CS21)	00 : Minimum size 01 : Medium size 10 : Large size 11 : Do not set.	Indeterminate	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Character Size Register

Address $00E4_{16}$

Border Selection Register



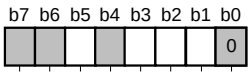
Border selection register (MD) [Address $00E5_{16}$]

B	Name	Functions	After reset	R	W
0	Block 1 OUT output border selection bit (MD10)	0 : Same output as R, G, B is output 1 : Border output	Indeterminate	R	W
1	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—
2	Block 2 OUT output border selection bit (MD20)	0 : Same output as R, G, B is output 1 : Border output	Indeterminate	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Border Selection Register

Address $00E5_{16}$

Color Register i



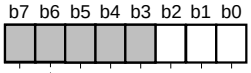
Color register i (COi) (i = 0 to 3) [Addresses $00E6_{16}$ to $00E9_{16}$]

B	Name	Functions	After reset	R	W
0	Fix this bit to "0."		0	R	—
1	B signal output selection bit (COi1)	0 : No character is output 1 : Character is output	0	R	W
2	G signal output selection bit (COi2)	0 : No character is output 1 : Character is output	0	R	W
3	R signal output selection bit (COi3)	0 : No character is output 1 : Character is output	0	R	W
4, 6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
5	OUT signal output control bit (COi5)	0 : Character is output 1 : Blank is output	0	R	W

Color Register i

Addresses $00E6_{16}$ to $00E9_{16}$

CRT Control Register



CRT control register (CC) [Address 00EA16]

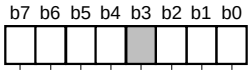
B	Name	Functions	After reset	R	W
0	All-blocks display control bit (CC0) (See note)	0 : All-blocks display off 1 : All-blocks display on	0	R	W
1	Block 1 display control bit (CC1)	0 : Block 1 display off 1 : Block 1 display on	0	R	W
2	Block 2 display control bit (CC2)	0 : Block 2 display off 1 : Block 2 display on	0	R	W
3 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Note: Display is controlled by logical product (AND) between the all-blocks display control bit and each block control bit.

CRT Control Register

Address 00EA16

CRT Port Control Register



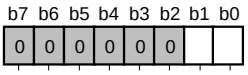
CRT port control register (CRTP) [Address 00EC16]

B	Name	Functions	After reset	R	W
0	HSYNC input polarity switch bit (HSYC)	0 : Positive polarity 1 : Negative polarity	0	R	W
1	VSYNC input polarity switch bit (VSYC)	0 : Positive polarity 1 : Negative polarity	0	R	W
2	R/G/B output polarity switch bit (R/G/B)	0 : Positive polarity 1 : Negative polarity	0	R	W
3	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—
4	OUT output polarity switch bit (OUT)	0 : Positive polarity 1 : Negative polarity	0	R	W
5	R signal output switch bit (OP5)	0 : R signal output 1 : MUTE signal output	0	R	W
6	G signal output switch bit (OP6)	0 : G signal output 1 : MUTE signal output	0	R	W
7	B signal output switch bit (OP7)	0 : B signal output 1 : MUTE signal output	0	R	W

CRT Port Control Register

Address 00EC16

CRT Clock Selection Register



CRT clock selection register (CK) [Address $00ED_{16}$]

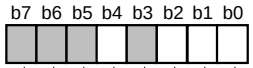
B	Name	Functions			After reset	R	W
0, 1	CRT clock selection bits (CK0,CK1)	b1	b0	Functions	0	R	W
		0	0	The clock for display is supplied by connecting RC or LC across the pins OSC1 and OSC2.			
		0	1	Since the main clock is used as the clock for display, the oscillation frequency is limited. Because of this, the character size in width (horizontal) direction is also limited. In this case, pins OSC1 and OSC2 are also used as input ports $P3_3$ and $P3_4$ respectively. CRT oscillation frequency = $f(X_{IN})$			
		1	0	CRT oscillation frequency = $f(X_{IN})/1.5$			
		1	1	The clock for display is supplied by connecting the following across the pins OSC1 and OSC2. • a ceramic resonator only for CRT display and a feedback resistor • a quartz-crystal oscillator only for CRT display and a feedback resistor (Note)			
2 to 7	Fix these bits to "0."				0	R	W

Note: It is necessary to connect other ceramic resonator or quartz-crystal oscillator across the pins X_{IN} and X_{OUT}.

CRT Clock Selection Register

Address $00ED_{16}$

A-D Control Register 1



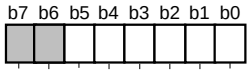
A-D control register 1 (AD1) [Address $00EE_{16}$]

B	Name	Functions	After reset	R	W
0 to 2	Analog input pin selection bits (ADM0 to ADM2)	b2 b1 b0 0 0 0 : A-D1 0 0 1 : A-D2 0 1 0 : A-D3 0 1 1 : A-D4 1 0 0 : A-D5 1 0 1 : A-D6 1 1 0 : } Do not set. 1 1 1 : }	0	R	W
3, 5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
4	Storage bit of comparison result (ADM4)	0: Input voltage < reference voltage 1: Input voltage > reference voltage	Indeterminate	R	—

A-D Control Register 1

Address $00EE_{16}$

A-D Control Register 2



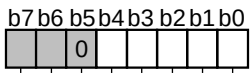
A-D control register 2(AD2) [Address 00EF16]

B	Name	Functions	After reset	R	W
0 to 5	D-A converter set bits (ADC0 to ADC5)	b5 b4 b3 b2 b1 b0 0 0 0 0 0 0 : 1/128Vcc 0 0 0 0 0 1 : 3/128Vcc 0 0 0 0 1 0 : 5/128Vcc 1 1 1 1 0 1 : 123/128Vcc 1 1 1 1 1 0 : 125/128Vcc 1 1 1 1 1 1 : 127/128Vcc	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are reed out, the values are " 0."		0	R	—

A-D Control Register 2

Address 00EF16

Timer 12 Mode Register



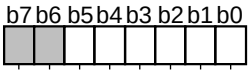
Timer 12 mode register (T12M) [Address 00F416]

B	Name	Functions	After reset	R	W
0	Timer 1 count source selection bit (T12M0)	0: f(XIN)/16 1: f(XIN)/4096	0	R	W
1	Timer 2 count source selection bit (T12M1)	0: Internal clock 1: External clock from TIM2 pin	0	R	W
2	Timer 1 count stop bit (T12M2)	0: Count start 1: Count stop	0	R	W
3	Timer 2 count stop bit (T12M3)	0: Count start 1: Count stop	0	R	W
4	Timer 2 internal count source selection bit (T12M4)	0: f(XIN)/16 1: Timer 1 overflow	0	R	W
5	Fix this bit to "0."		0	R	W
6,7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Timer 12 Mode Register

Address 00F416

Timer 34 Mode Register



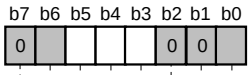
Timer 34 mode register (T34M) [Address 00F5$_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 3 count source selection bit (T34M0)	0: f(XIN)/16 1: External clock	0	R	W
1	Timer 4 internal count source selection bit (T34M1)	0: Timer 3 overflow 1: f(XIN)/16	0	R	W
2	Timer 3 count stop bit (T34M2)	0: Count start 1: Count stop	0	R	W
3	Timer 4 count stop bit (T34M3)	0: Count start 1: Count stop	0	R	W
4	Timer 4 count source selection bit (T34M4)	0: Internal clock 1: f(XIN)/2	0	R	W
5	Timer 3 external count source selection bit (T34M5)	0: External clock from TIM3 pin 1: External clock from HSYNC pin	0	R	W
6,7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Timer 34 Mode Register

Address 00F5$_{16}$

Interrupt Input Polarity Register



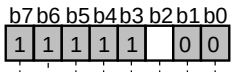
Interrupt input polarity register(RE) [Address 00F9$_{16}$]

B	Name	Functions	After reset	R	W
0	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		Indeterminate	R	—
1, 2	Fix these bits to "0."		0	R	W
3	INT1 polarity switch bit (RE3)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	INT2 polarity switch bit (RE4)	0 : Positive polarity 1 : Negative polarity	0	R	W
5	INT3 polarity switch bit (RE5)	0 : Positive polarity 1 : Negative polarity	0	R	W
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—
7	Fix this bit to "0."		0	R	W

Interrupt Input Polarity Register

Address 00F9$_{16}$

CPU Mode Register



CPU mode register (CPUM (CM)) [Address FB16]

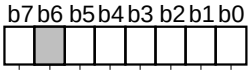
B	Name	Functions	After reset	R	W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: 1 0: 1 1: } Not available	0	R	W
2	Stack page selection bit (CM2) (See note)	0: 0 page 1: 1 page	1	R	W
3 to 7	Fix these bits to "1."		1	R	W

Note: This bit is set to "1" after the reset release.

CPU Mode Register

Address 00FB16

Interrupt Request Register 1



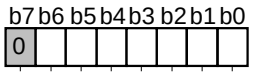
Interrupt request register 1 (IREQ1) [Address 00FC16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
4	CRT interrupt request bit (CRTR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
5	VSYNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—
7	INT3 interrupt request bit (IT3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻

Interrupt Request Register 1

Address 00FC16

Interrupt Request Register 2



Interrupt request register 2 (IREQ2) [Address 00FD16]

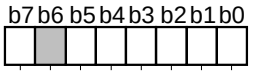
B	Name	Functions	After reset	R	W
0	INT1 interrupt request bit (ITIR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	INT2 interrupt request bit (IT2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Serial I/O interrupt request bit (SIR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3, 5, 6	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—
4	f(XIN)/4096 interrupt request bit (MSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
7	Fix this bit to "0."		0	R	W

✻: "0" can be set by software, but "1" cannot be set.

Interrupt Request Register 2

Address 00FD16

Interrupt Control Register 1



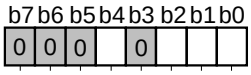
Interrupt control register 1 (ICON1) [Address 00FE16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt enable bit (TM1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Timer 2 interrupt enable bit (TM2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Timer 3 interrupt enable bit (TM3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	Timer 4 interrupt enable bit (TM4E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	CRT interrupt enable bit (CRTE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	VSYNC interrupt enable bit (VSCE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—
7	INT3 interrupt enable bit (IN3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W

Interrupt Control Register 1

Address 00FE16

Interrupt Control Register 2



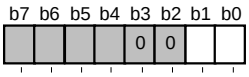
Interrupt control register 2 (ICON2) [Address 00FF16]

B	Name	Functions	After reset	R	W
0	INT1 interrupt enable bit (IT1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	INT2 interrupt enable bit (IT2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Serial I/O interrupt enable bit (SIE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3, 5 to 7	Fix these bits to "0."		0	R	W
4	f(XIN)/4096 interrupt enable bit (MSE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W

Interrupt Control Register 2

Address 00FF16

ROM Correction Enable Register



ROM correction enable register (RCR) [Address 021B16]

B	Name	Functions	After reset	R	W
0	Block 1 enable bit (RC0)	0: Disabled 1: Enabled	0	R	W
1	Block 2 enable bit (RC1)	0: Disabled 1: Enabled	0	R	W
2,3	Fix these bits to "0."		0	R	W
4 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

ROM Correction Enable Register

Address 021B16

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