PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS

M37736EHLXXXHP

PROM VERSION OF M37736MHLXXXHP

DESCRIPTION

The M37736EHLXXXHP is a single-chip microcomputer using the 7700 Family core. This single-chip microcomputer has a CPU and a bus interface unit. The CPU is a 16-bit parallel processor that can be an 8-bit parallel processor, and the bus interface unit enhances the memory access efficiency to execute instructions fast. This microcomputer also includes a 32 kHz oscillation circuit, in addition to the PROM, RAM, multiple-function timers, serial I/O, A-D converter, and so on.

Its strong points are the low power dissipation, the low supply voltage, and the small package.

In the M37736MHLXXXHP, as the multiplex method of the external bus, either of 2 types can be selected.

The M37736EHLXXXHP has the same function as the M37736MHLXXXHP except that the built-in ROM is PROM. (Refer to the basic function blocks description.)

FEATURES

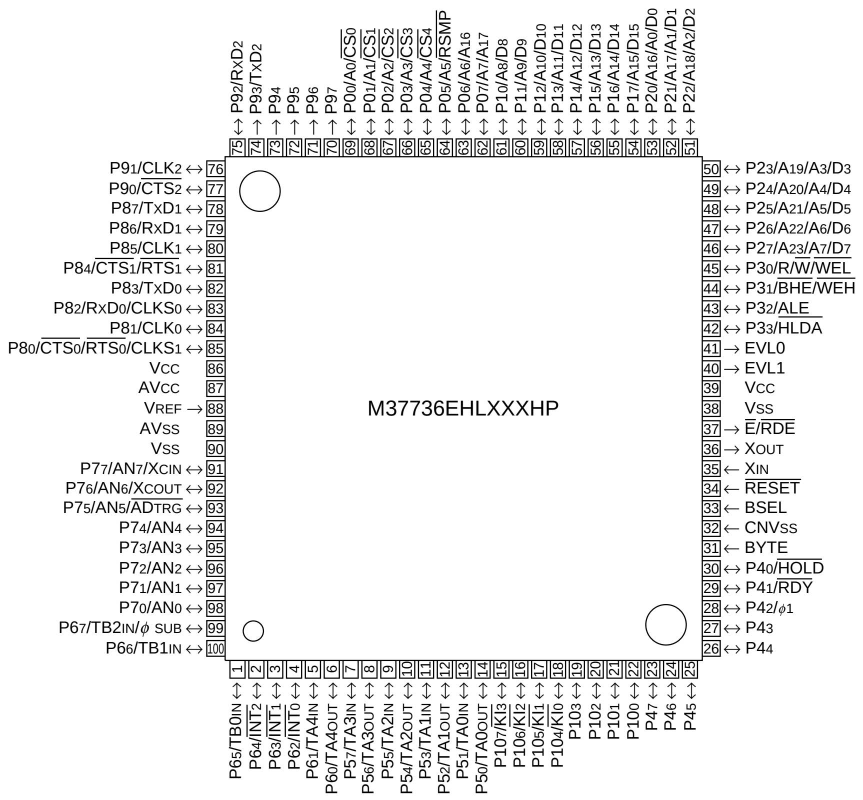
- Number of basic instructions 103
- Memory size PROM .... 124 Kbytes
  RAM .... 3968 bytes
- Instruction execution time
  The fastest instruction at 12 MHz frequency .... 333 ns
- Single power supply .... 2.7–5.5 V
- Low power dissipation (At 3 V supply voltage, 12 MHz frequency)
  .... 9 mW (Typ.)
- Interrupts .... 19 types, 7 levels
- Multiple-function 16-bit timer .... 5 + 3
- Serial I/O (UART or clock synchronous) 3
- 10-bit A-D converter .... 8-channel inputs
- 12-bit watchdog timer
- Programmable input/output, output
  (ports P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10) 84
- Clock generating circuit .... 2 circuits built-in
- Small package .... 100-pin plastic molded fine-pitch QFP
  (100P6Q-A;0.5 mm lead pitch)

APPLICATION

Control devices for general commercial equipment such as office automation, office equipment, personal information equipment, and others.

Control devices for general industrial equipment such as communication equipment, and others.

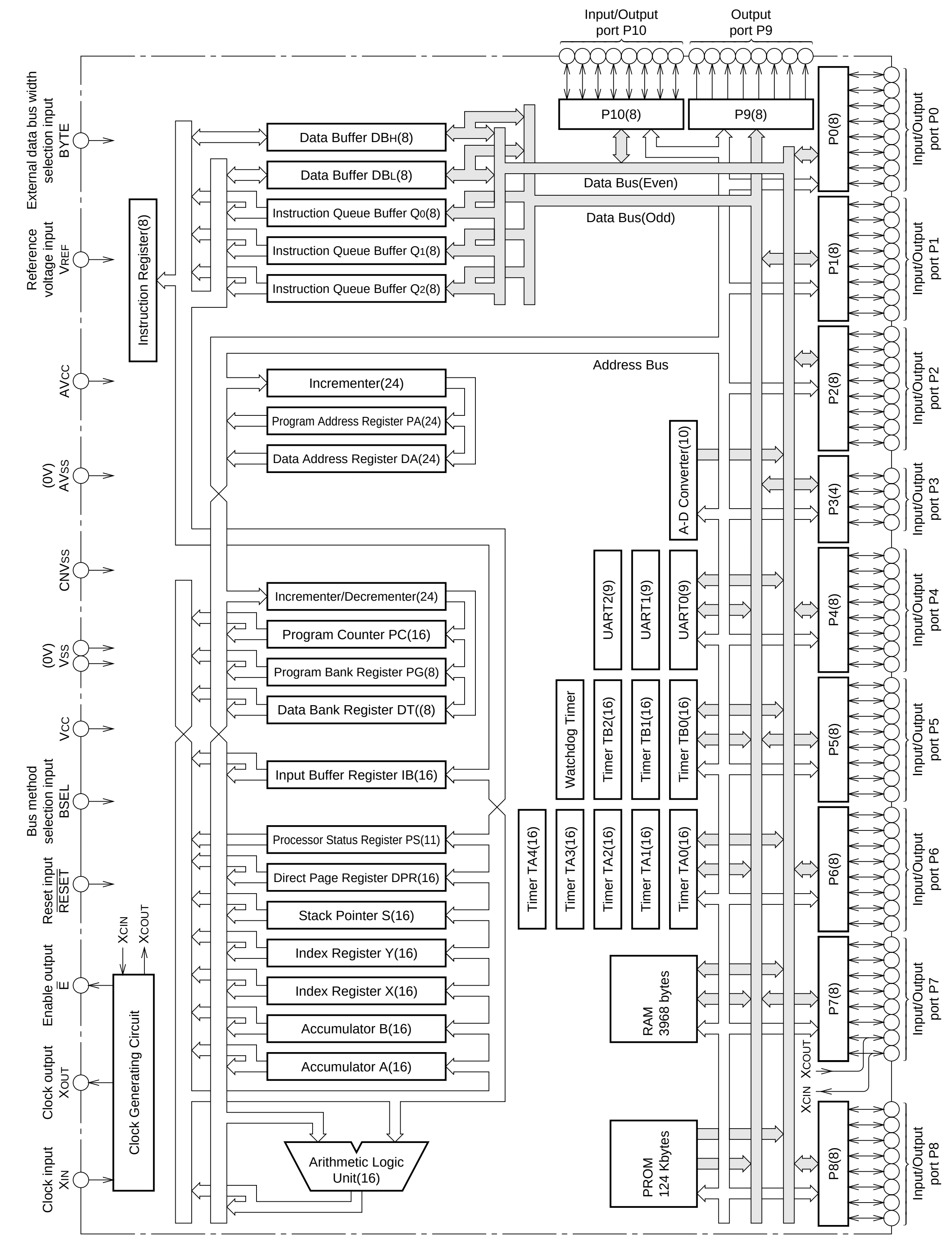
PIN CONFIGURATION (TOP VIEW)



Outline 100P6Q-A

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M37736EHLXXXHP BLOCK DIAGRAM



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

FUNCTIONS OF M37736EHLXXXHP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		333 ns (the fastest instruction at external clock 12 MHz frequency)
Memory size	PROM	124 Kbytes
	RAM	3968 bytes
Input/Output ports	P0 – P2, P4 – P8, P10	8-bit ✕ 9
	P3	4-bit ✕ 1
Output port	P9	8-bit ✕ 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit ✕ 5
	TB0, TB1, TB2	16-bit ✕ 3
Serial I/O		(UART or clock synchronous serial I/O) ✕ 3
A-D converter		10-bit ✕ 1 (8 channels)
Watchdog timer		12-bit ✕ 1
Interrupts		3 external types, 16 internal types Each interrupt can be set to the priority level (0 – 7.)
Clock generating circuit		2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Supply voltage		2.7 – 5.5 V
Power dissipation		9 mW (at 3 V supply voltage, external clock 12 MHz frequency)
		22.5 mW (at 5 V supply voltage, external clock 12 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		External bus mode A; maximum 16 Mbytes, External bus mode B; maximum 1 Mbytes
Operating temperature range		–40 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		100-pin plastic molded fine-pitch QFP (100P6Q-A;0.5 mm lead pitch)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

PIN DESCRIPTION

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source		Apply 2.7 – 5.5 V to Vcc and 0 V to Vss.
CNVss	CNVss input	Input	This pin controls the processor mode. Connect to Vss for the single-chip mode and the memory expansion mode, and to Vcc for the microprocessor mode.
$\overline{RESET}$	Reset input	Input	When “L” level is applied to this pin, the microcomputer enters the reset state.
X_{IN}	Clock input	Input	These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between X_{IN} and X_{OUT}. When an external clock is used, the clock source should be connected to the X_{IN} pin, and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	This pin functions as the enable signal output pin which indicates the access status in the internal bus. In the external bus mode B and the memory expansion mode or the microprocessor mode, this pin output signal $\overline{RDE}$.
BYTE	External data bus width selection input	Input	In the memory expansion mode or the microprocessor mode, this pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when “L” signal is input and an 8-bit width when “H” signal is input.
BSEL	Bus method select input	Input	In the memory expansion mode or the microprocessor mode, this pin determines the external bus mode. The bus mode becomes the external bus mode A when “H” signal is input, and the external bus mode B when “L” signal is input.
AVcc, AVss	Analog power source input		Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
$P0_0$ – $P0_7$	I/O port P0	I/O	In the single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset. In the memory expansion mode or the microprocessor mode, these pins output address (A_0 – A_7) at the external bus mode A, and these pins output signals $\overline{CS_0}$ – $\overline{CS_4}$ and $\overline{RSMP}$, and addresses (A_{16}, A_{17}) at the external bus mode B.
$P1_0$ – $P1_7$	I/O port P1	I/O	In the single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to “L” in the memory expansion mode or the microprocessor mode and external data bus has a 16-bit width, high-order data (D_8 – D_{15}) is input/output or an address (A_8 – A_{15}) is output. When the BYTE pin is “H” and an external data bus has an 8-bit width, only address (A_8 – A_{15}) is output.
$P2_0$ – $P2_7$	I/O port P2	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, low-order data (D_0 – D_7) is input/output or an address is output. When using the external bus mode A, the address is A_{16} – A_{23}. When using the external bus mode B, the address is A_0 – A_7.
$P3_0$ – $P3_3$	I/O port P3	I/O	In the single-chip mode, these pins have the same function as port P0. In the memory expansion mode or the microprocessor mode, R/$\overline{W}$, $\overline{BHE}$, ALE, and $\overline{HLDA}$ signals are output at the external bus mode A, and $\overline{WEL}$, $\overline{WEH}$, ALE, and $\overline{HLDA}$ signals are output at the external bus mode B.
$P4_0$ – $P4_7$	I/O port P4	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, $P4_0$, $P4_1$, and $P4_2$ become $\overline{HOLD}$ and $\overline{RDY}$ input pins, and a clock ϕ_1 output pin, respectively. Functions of the other pins are the same as in the single-chip mode. However, in the memory expansion mode, $P4_2$ can be selected as an I/O port.
$P5_0$ – $P5_7$	I/O port P5	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0 to A3.
$P6_0$ – $P6_7$	I/O port P6	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input ($\overline{INT_0}$ – $\overline{INT_2}$) and input pins for timers B0 to B2. $P6_7$ also functions as sub-clock ϕ_{SUB} output pin.
$P7_0$ – $P7_7$	I/O port P7	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins function as input pins for A-D converter. Additionally, $P7_6$ and $P7_7$ have the function as the output pin (X_{COUT}) and the input pin (X_{CIN}) of the sub-clock (32 kHz) oscillation circuit, respectively. When $P7_6$ and $P7_7$ are used as the X_{COUT} and X_{CIN} pins, connect a resonator or an oscillator between the both.
$P8_0$ – $P8_7$	I/O port P8	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART 0 and UART 1.
$P9_0$ – $P9_7$	Output port P9	Output	Port P9 is an 8-bit I/O port. These ports are floating when reset. When writing to the port latch, these ports become the output mode. $P9_0$ – $P9_3$ also function as I/O port for UART 2.
$P10_0$ – $P10_7$	I/O port P10	I/O	In addition to having the same functions as port P0 in the single-chip mode. $P10_4$ – $P10_7$ also function as input pins for key input interrupt input ($\overline{KI_0}$ – $\overline{KI_3}$).
EVL0, EVL1	———	Output	These pins should be left open.

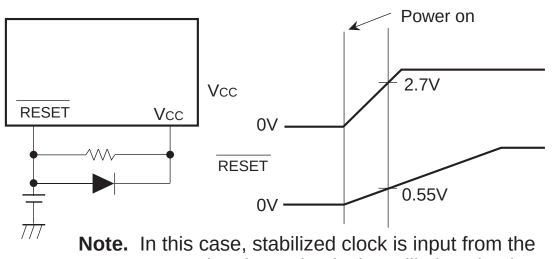
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

BASIC FUNCTION BLOCKS

The M37736EHLXXXHP has the same functions as the M37736MHBXXXGP except for the following :
(1) The built-in ROM is PROM.
(2) The package is different.
(3) The reset circuit is different.
Refer to the section on the M37736MHBXXXGP.

RESET CIRCUIT

The microcomputer is released from the reset state when the $\overline{\text{RESET}}$ pin is returned to “H” level after holding it at “L” level with the power source voltage at 2.7 – 5.5 V. Program execution starts at the address formed by setting address A_{23} – A_{16} to 00_{16}, A_{15} – A_8 to the contents of address $FFFF_{16}$, and A_7 – A_0 to the contents of address $FFFE_{16}$.
Figure 1 shows an example of a reset circuit. When the stabilized clock is input from the external to the main-clock oscillation circuit, the reset input voltage must be 0.55 V or less when the power source voltage reaches 2.7 V. When a resonator/oscillator is connected to the main-clock oscillation circuit, change the reset input voltage from “L” to “H” after the main-clock oscillation is fully stabilized.
The status of the internal registers during reset is the same as the M37736MHBXXXGP’s.



Note. In this case, stabilized clock is input from the external to the main-clock oscillation circuit. Perform careful evalvation at the system design level before using.

Fig. 1 Example of a reset circuit

PIN DESCRIPTION (EPROM MODE)

Pin	Name	Input/Output	Functions
V_{CC}, V_{SS}	Power supply		Supply 5V±10% to V_{CC} and 0V to V_{SS}.
CNV_{SS}	V_{PP} input	Input	Connect to V_{PP} when programming or verifing.
BYTE	V_{PP} input	Input	Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}.
X_{IN}	Clock input	Input	Connect a ceramic resonator between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	Keep open.
AV_{CC}, AV_{SS}	Analog supply input		Connect AV_{CC} to V_{CC} and AV_{SS} to V_{SS}.
V_{REF}	Reference voltage input	Input	Connect to V_{SS}.
$P0_0$ – $P0_7$	Address input (A_0 – A_7)	Input	Port P0 functions as the lower 8 bits address input (A_0 – A_7).
$P1_0$ – $P1_7$	Address input (A_8 – A_{15})	Input	Port P1 functions as the higher 8 bits address input (A_8 – A_{15}).
$P2_0$ – $P2_7$	Data I/O (D_0 – D_7)	I/O	Port P2 functions as the 8 bits data bus(D_0 – D_7).
$P3_0$	Address input (A_{16})	Input	$P3_0$ functions as the most significant bit address input (A_{16}).
$P3_1$ – $P3_3$	Input port P3	Input	Connect to V_{SS}.
$P4_0$ – $P4_7$	Input port P4	Input	Connect to V_{SS}.
$P5_0$ – $P5_7$	Control signal input	Input	$P5_0$, $P5_1$ and $P5_2$ function as $\overline{PGM}$, $\overline{OE}$ and $\overline{CE}$ input pins respectively. Connect $P5_3$, $P5_4$, $P5_5$ and $P5_6$ to V_{CC}. Connect $P5_7$ to V_{SS}.
$P6_0$ – $P6_7$	Input port P6	Input	Connect to V_{SS}.
$P7_0$ – $P7_7$	Input port P7	Input	Connect to V_{SS}.
$P8_0$ – $P8_7$	Input port P8	Input	Connect to V_{SS}.
$P9_0$ – $P9_7$	Input port P9	Input	Connect to V_{SS}.
$P10_0$ – $P10_7$	Input port P10	Input	Connect to V_{SS}.
BSEL	——	Input	Connect to V_{cc}.
EVL0,EVL1	——	Output	Keep open.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

EPROM MODE

The M37736EHLXXXHP features an EPROM mode in addition to its normal modes. When the $\overline{\text{RESET}}$ signal level is “L”, the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 2 shows the pin connections in the EPROM mode.

The EPROM mode is the 1M mode for the EPROM that is equivalent to the M5M27C101K.

When in the EPROM mode, ports P0, P1, P2, $P3_0$, $P5_0$, $P5_1$, $P5_2$, CNV_{SS} and BYTE are used for the EPROM (equivalent to the M5M27C101K). When in this mode, the built-in PROM can be programmed or read from using these pins in the same way as with the M5M27C101K.

This chip does not have Device Identifier Mode, so that set the corresponding program algorithm. The program area should specify address 01000_{16} – $1FFFF_{16}$.

Connect the clock which is either ceramic resonator or external clock to X_{IN} pin and X_{OUT} pin.

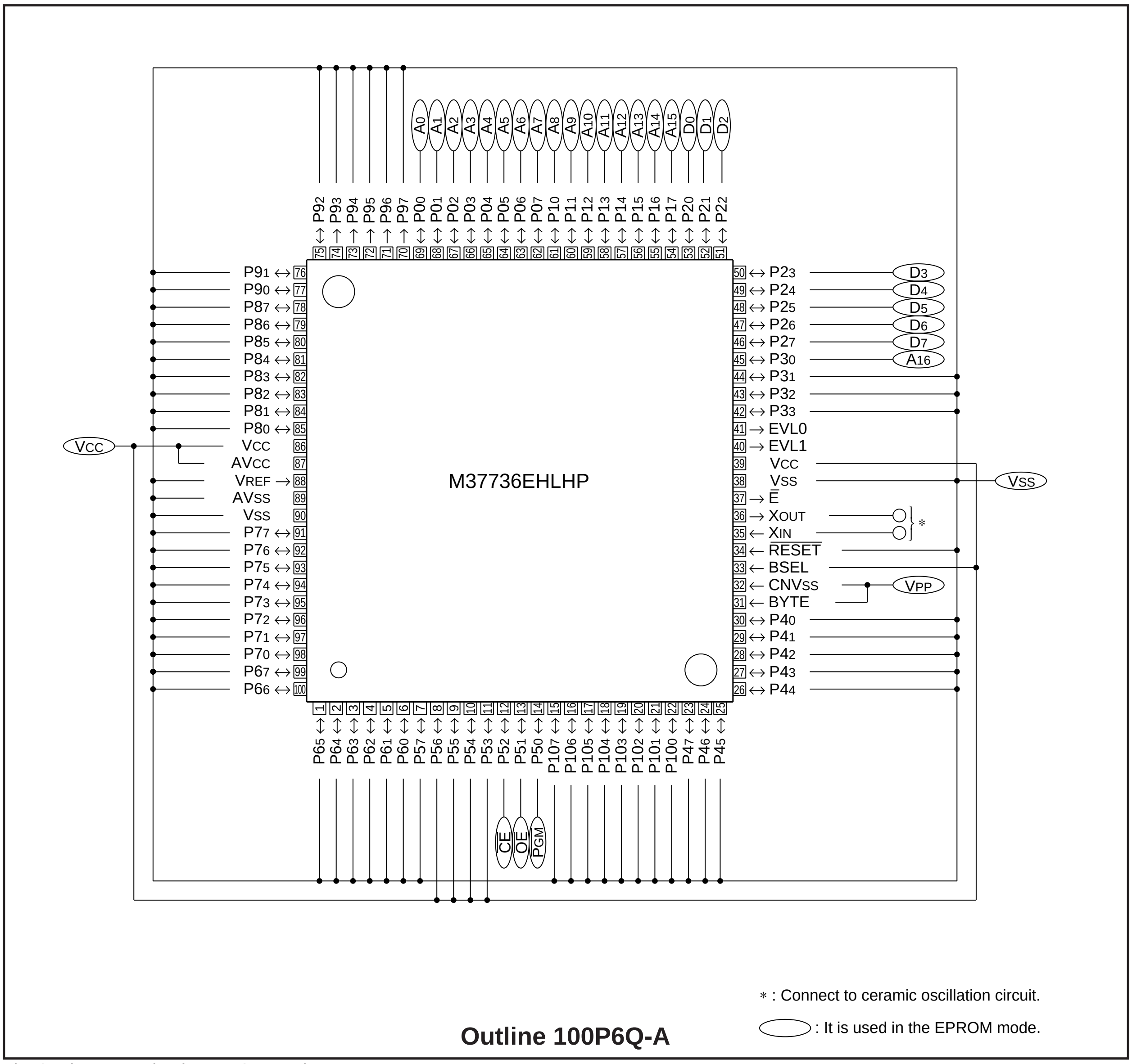


Fig. 2 Pin connection in EPROM mode

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Table 1 Pin function in EPROM mode

	M37736EHLXXXHP	M5M27C101K
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}, BYTE	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, P1, $P3_0$	A_0 – A_{16}
Data I/O	Port P2	D_0 – D_7
$\overline{CE}$	$P5_2$	$\overline{CE}$
$\overline{OE}$	$P5_1$	$\overline{OE}$
$\overline{PGM}$	$P5_0$	$\overline{PGM}$

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

FUNCTION IN EPROM MODE
1M mode (equivalent to the M5M27C101K)

Reading

To read the EPROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level. Input the address of the data (A_0 – A_{16}) to be read, and the data will be output to the I/O pins D_0 – D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Programming

Programming must be performed in 8 bits by a byte program. To program to the EPROM, set the $\overline{CE}$ pin to a "L" level and the $\overline{OE}$ pin to a "H" level. The CPU will enter the programming mode when 12.5 V is applied to the V_{PP} pin. The address to be programmed to is selected with pins A_0 – A_{16}, and the data to be programmed is input to pins D_0 – D_7. Set the $\overline{PGM}$ pin to a "L" level to being programming.

Programming operation

To program the M37736EHLXXXHP, first set V_{CC} = 6 V, V_{PP} = 12.5 V, and set the address to 01000_{16}. Apply a 0.2 ms programming pulse, check that the data can be read, and if it cannot be read OK, repeat the procedure, applying a 0.2 ms programming pulse and checking that the data can be read until it can be read OK. Record the accumulated number of pulse applied (X) before the data can be read OK, and then write the data again, applying a further once this number of pulses (0.2 × X ms).
When this series of programming operations is complete, increment the address, and continue to repeat the procedure above until the last address has been reached.
Finally, when all addresses have been programmed, read with V_{CC} = V_{PP} = 5 V (or V_{CC} = V_{PP} = 5.5 V).

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Data I/O
Read-out	V_{IL}	V_{IL}	X	5 V	5 V	Output
Output Disable	V_{IL}	V_{IH}	X	5 V	5 V	Floating
	V_{IH}	X	X	5 V	5 V	Floating
Programming	V_{IL}	V_{IH}	V_{IL}	12.5 V	6 V	Input
Programming Verify	V_{IL}	V_{IL}	V_{IH}	12.5 V	6 V	Output
Program Disable	V_{IH}	V_{IH}	V_{IH}	12.5 V	6 V	Floating

Note 1 : An X indicates either V_{IL} or V_{IH}.

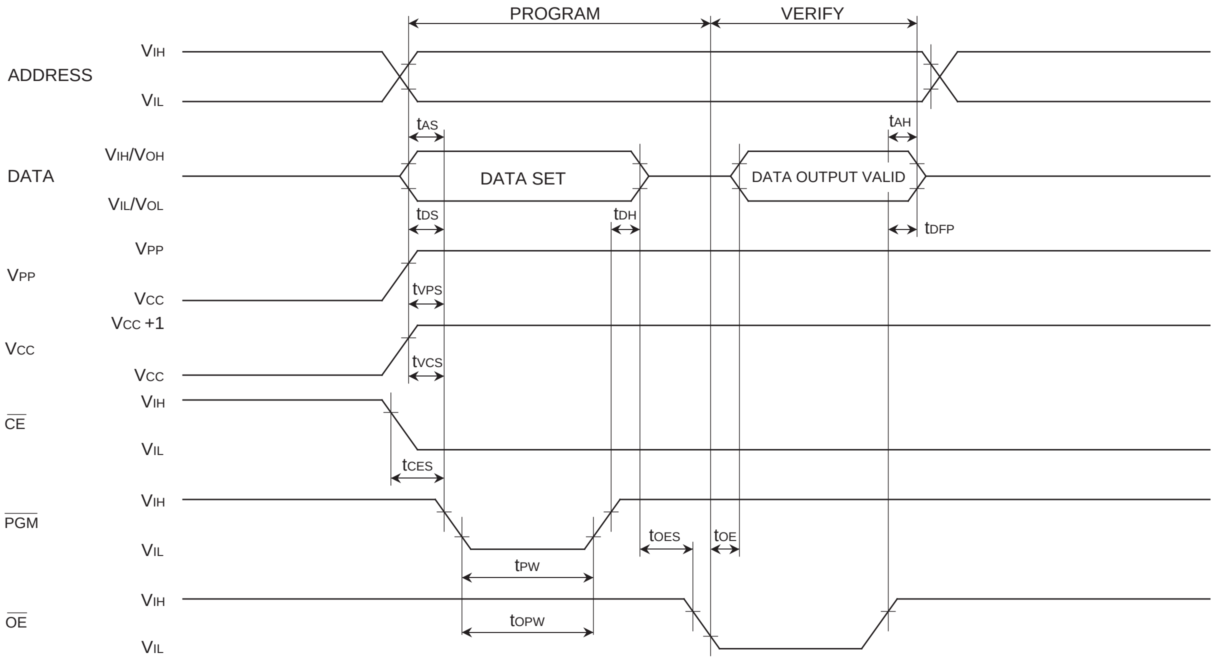
Programming operation (equivalent to the M5M27C101K)

AC ELECTRICAL CHARACTERISTICS (T_a = 25 ± 5 °C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address setup time		2			µs
t_{OES}	$\overline{OE}$ setup time		2			µs
t_{DS}	Data setup time		2			µs
t_{AH}	Address hold time		0			µs
t_{DH}	Data hold time		2			µs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			µs
t_{VPS}	V_{PP} setup time		2			µs
t_{PW}	$\overline{PGM}$ pulse width		0.19	0.2	0.21	ms
t_{OPW}	$\overline{PGM}$ over program pulse width		0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time		2			µs
t_{OE}	Data valid from $\overline{OE}$				150	ns

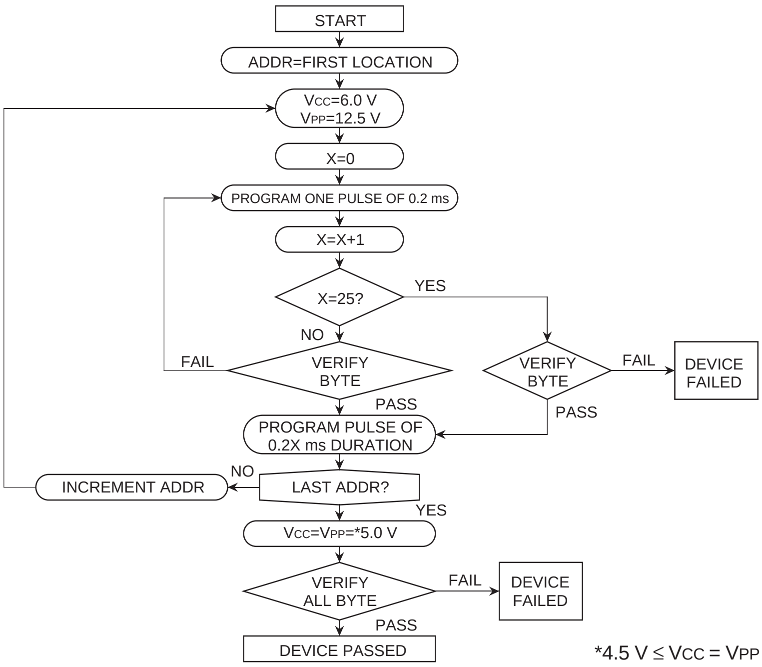
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

AC waveforms



Test conditions for A.C. characteristics
Input voltage : V_{IL} = 0.45 V, V_{IH} = 2.4 V
Input rise and fall times (10 % – 90 %) : ≤ 20 ns
Reference voltage at timing measurement : Input, Output
"L" = 0.8 V, "H" = 2 V

Programming algorithm flow chart

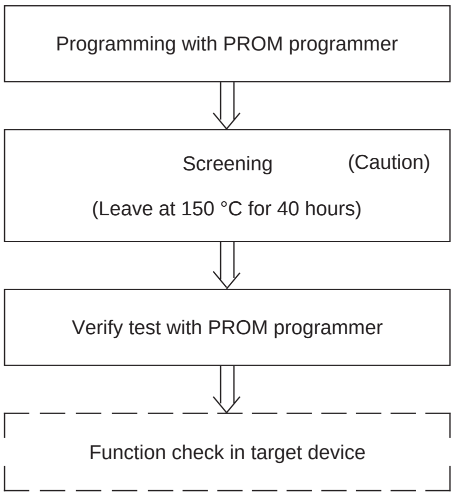


*4.5 V ≤ V_{CC} = V_{PP} ≤ 5.5 V

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SAFETY INSTRUCTIONS

(1) A high voltage is used for programming. Take care that over-voltage is not applied. Take care especially at power on.
(2) The programmable M37736EHLHP that is shipped in blank is also provided. For the M37736EHLHP, Mitsubishi Electric corp. does not perform PROM programming test and screening following the assembly processes. To improve reliability after programming, performing programming and test according to the flow below before use is recommended.



Caution : Never expose to 150 °C exceeding 100 hours.

ADDRESSING MODES

The M37736EHLXXXHP has 28 powerful addressing modes. Refer to the “7700 Family Software Manual” for the details.

MACHINE INSTRUCTION LIST

The M37736EHLXXXHP has 103 machine instructions. Refer to the “7700 Family Software Manual” for the details.

DATA REQUIRED FOR PROM ORDERING

Please send the following data for writing to PROM.
(1) M37736EHLXXXHP writing to PROM order confirmation form
(2) 100P6Q mark specification form (100P6D mark specification form is substituted.)
(3) ROM data (EPROM 3 sets)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Power source voltage		–0.3 to +7	V
AVcc	Analog power source voltage		–0.3 to +7	V
V_I	Input voltage $\overline{RESET}$, CNVss, BYTE		–0.3 to +12(Note)	V
V_I	Input voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $P9_0$ – $P9_2$, $P10_0$ – $P10_7$, V_{REF}, X_{IN}, BSEL		–0.3 to Vcc + 0.3	V
V_O	Output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $P9_0$ – $P9_7$, $P10_0$ – $P10_7$, X_{OUT}, $\overline{E}$		–0.3 to Vcc + 0.3	V
P_d	Power dissipation	Ta = 25 °C	200	mW
T_{opr}	Operating temperature		–40 to +85	°C
T_{stg}	Storage temperature		–65 to +150	°C

Note. When the EPROM is programmed, input voltage of pins CNVss and BYTE is 13 V respectively.

RECOMMENDED OPERATING CONDITIONS (Vcc = 2.7 – 5.5 V, Ta = –40 to +85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
Vcc	Power source voltage	$f(X_{IN})$: Operating	2.7		5.5	V
		$f(X_{IN})$: Stopped, $f(X_{CIN})$ = 32.768 kHz	2.7		5.5	
AVcc	Analog power source voltage			Vcc		V
Vss	Power source voltage			0		V
AVss	Analog power source voltage			0		V
V_{IH}	High-level input voltage $P0_0$ – $P0_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $P9_0$ – $P9_2$, $P10_0$ – $P10_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, BSEL, X_{CIN} (Note 3)		0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in single-chip mode)		0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in memory expansion mode and microprocessor mode)		0.5 Vcc		Vcc	V
V_{IL}	Low-level input voltage $P0_0$ – $P0_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $P9_0$ – $P9_2$, $P10_0$ – $P10_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, BSEL, X_{CIN} (Note 3)		0		0.2Vcc	V
V_{IL}	Low-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in single-chip mode)		0		0.2Vcc	V
V_{IL}	Low-level input voltage $P1_0$ – $P1_7$, $P2_0$ – $P2_7$ (in memory expansion mode and microprocessor mode)		0		0.16Vcc	V
$I_{OH(peak)}$	High-level peak output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $P9_0$ – $P9_7$, $P10_0$ – $P10_7$				–10	mA
$I_{OH(avg)}$	High-level average output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $P9_0$ – $P9_7$, $P10_0$ – $P10_7$				–5	mA
$I_{OL(peak)}$	Low-level peak output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_3$, $P5_4$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $P9_0$ – $P9_7$, $P10_4$ – $P10_7$				10	mA
$I_{OL(peak)}$	Low-level peak output current $P4_4$ – $P4_7$, $P10_0$ – $P10_3$				16	mA
$I_{OL(avg)}$	Low-level average output current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_3$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $P9_0$ – $P9_7$, $P10_4$ – $P10_7$				5	mA
$I_{OL(avg)}$	Low-level average output current $P4_4$ – $P4_7$, $P10_0$ – $P10_3$				12	mA
$f(X_{IN})$	Main-clock oscillation frequency (Note 4)				12	MHz
$f(X_{CIN})$	Sub-clock oscillation frequency			32.768	50	kHz

Notes 1. Average output current is the average value of a 100 ms interval.

2. The sum of $I_{OL(peak)}$ for ports P0, P1, P2, P3, P8, and P9 must be 80 mA or less,
the sum of $I_{OH(peak)}$ for ports P0, P1, P2, P3, P8, and P9 must be 80 mA or less,
the sum of $I_{OL(peak)}$ for ports P4, P5, P6, P7, and P10 must be 100 mA or less, and
the sum of $I_{OH(peak)}$ for ports P4, P5, P6, P7, and P10 must be 80 mA or less.

3. Limits V_{IH} and V_{IL} for X_{CIN} are applied when the sub clock external input selection bit = “1”.

4. The maximum value of $f(X_{IN})$ = 6 MHz when the main clock division selection bit = “1”.

ELECTRICAL CHARACTERISTICS (Vcc = 5 V, Vss = 0 V, Ta = –40 to +85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	High-level output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $P9_0$ – $P9_7$, $P10_0$ – $P10_7$	V_{CC} = 5 V, I_{OH} = –10 mA	3			V
		V_{CC} = 3 V, I_{OH} = –1 mA	2.5			
V_{OH}	High-level output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_3$	V_{CC} = 5 V, I_{OH} = –400 µA	4.7			V
V_{OH}	High-level output voltage $P3_0$ – $P3_2$	V_{CC} = 5 V, I_{OH} = –10 mA	3.1			V
		V_{CC} = 5 V, I_{OH} = –400 µA	4.8			
		V_{CC} = 3 V, I_{OH} = –1 mA	2.6			
V_{OH}	High-level output voltage $\overline{E}$	V_{CC} = 5 V, I_{OH} = –10 mA	3.4			V
		V_{CC} = 5 V, I_{OH} = –400 µA	4.8			
		V_{CC} = 3 V, I_{OH} = –1 mA	2.6			
V_{OL}	Low-level output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_3$, $P4_0$ – $P4_3$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $P9_0$ – $P9_7$, $P10_4$ – $P10_7$	V_{CC} = 5 V, I_{OL} = 10 mA			2	V
		V_{CC} = 3 V, I_{OL} = 1 mA			0.5	
V_{OL}	Low-level output voltage $P4_4$ – $P4_7$, $P10_0$ – $P10_3$	V_{CC} = 5 V, I_{OL} = 16 mA			1.8	V
		V_{CC} = 3 V, I_{OL} = 10 mA			1.5	
V_{OL}	Low-level output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_3$	V_{CC} = 5 V, I_{OL} = 2 mA			0.45	V
V_{OL}	Low-level output voltage $P3_0$ – $P3_2$	V_{CC} = 5 V, I_{OL} = 10 mA			1.9	V
		V_{CC} = 5 V, I_{OL} = 2 mA			0.43	
		V_{CC} = 3 V, I_{OL} = 1 mA			0.4	
V_{OL}	Low-level output voltage $\overline{E}$	V_{CC} = 5 V, I_{OL} = 10 mA			1.6	V
		V_{CC} = 5 V, I_{OL} = 2 mA			0.4	
		V_{CC} = 3 V, I_{OL} = 1 mA			0.4	
$V_{T+} - V_{T-}$	Hysteresis $\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$ – $TA4_{IN}$, $TB0_{IN}$ – $TB2_{IN}$, $\overline{INT_0}$ – $\overline{INT_2}$, $\overline{AD_{TRG}}$, $\overline{CTS_0}$, $\overline{CTS_1}$, $\overline{CTS_2}$, CLK_0, CLK_1, CLK_2, $\overline{KI_0}$ – $\overline{KI_3}$	V_{CC} = 5 V	0.4		1	V
		V_{CC} = 3 V	0.1		0.7	
$V_{T+} - V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC} = 5 V	0.2		0.5	V
		V_{CC} = 3 V	0.1		0.4	
$V_{T+} - V_{T-}$	Hysteresis X_{IN}	V_{CC} = 5 V	0.1		0.4	V
		V_{CC} = 3 V	0.06		0.26	
$V_{T+} - V_{T-}$	Hysteresis X_{CIN} (When external clock is input)	V_{CC} = 5 V	0.1		0.4	V
		V_{CC} = 3 V	0.06		0.26	
I_{IH}	High-level input current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $P9_0$ – $P9_2$, $P10_0$ – $P10_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, BSEL	V_{CC} = 5 V, V_I = 5 V			5	µA
		V_{CC} = 3 V, V_I = 3 V			4	
I_{IL}	Low-level input current $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, $P4_0$ – $P4_7$, $P5_0$ – $P5_3$, $P6_0$, $P6_1$, $P6_5$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, $P9_0$ – $P9_2$, $P10_0$ – $P10_3$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, BSEL	V_{CC} = 5 V, V_I = 0 V			–5	µA
		V_{CC} = 3 V, V_I = 0 V			–4	
I_{IL}	Low-level input current $P6_2$ – $P6_4$, $P10_4$ – $P10_7$	V_I = 0 V, without a pull-up transistor, V_{CC} = 5 V			–5	µA
		V_I = 0 V, without a pull-up transistor, V_{CC} = 3 V			–4	
		V_I = 0 V, with a pull-up transistor, V_{CC} = 5 V	–0.25	–0.5	–1.0	mA
		V_I = 0 V, with a pull-up transistor, V_{CC} = 3 V	–0.08	–0.18	–0.35	
V_{RAM}	RAM hold voltage	When clock is stopped.	2			V

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, V_{SS} = 0 V, Ta = –40 to +85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	When single-chip mode, output pins are open, and other pins are V_{SS}.	V_{CC} = 5 V, $f(X_{IN})$ = 12 MHz (square waveform), $(f(f_2)$ = 6 MHz), $f(X_{CIN})$ = 32.768 kHz, in operating (Note 1)		4.5	9	mA
			V_{CC} = 3 V, $f(X_{IN})$ = 12 MHz (square waveform), $(f(f_2)$ = 6 MHz), $f(X_{CIN})$ = 32.768 kHz, in operating (Note 1)		3	6	mA
			V_{CC} = 3 V, $f(X_{IN})$ = 12 MHz (square waveform), $(f(f_2)$ = 0.75 MHz), $f(X_{CIN})$: Stopped, in operating		0.4	0.8	mA
			V_{CC} = 3 V, $f(X_{IN})$ = 12 MHz (square waveform), $f(X_{CIN})$ = 32.768 kHz, when a WIT instruction is executed (Note 2)		6	12	µA
			V_{CC} = 3 V, $f(X_{IN})$: Stopped, $f(X_{CIN})$ = 32.768 kHz, in operating (Note 3)		30	60	µA
			V_{CC} = 3 V, $f(X_{IN})$: Stopped, $f(X_{CIN})$ = 32.768 kHz, when a WIT instruction is executed (Note 4)		3	6	µA
			Ta = 25 °C, when clock is stopped			1	µA
			Ta = 85 °C, when clock is stopped			20	µA

Notes 1. This applies when the main clock external input selection bit = “1”, the main clock division selection bit = “0”, and the signal output stop bit = “1”.
2. This applies when the main clock external input selection bit = “1” and the system clock stop bit at wait state = “1”.
3. This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.
4. This applies when the X_{COUT} drivability selection bit = “0” and the system clock stop bit at wait state = “1”.

A–D CONVERTER CHARACTERISTICS

(V_{CC} = AV_{CC} = 5 V, V_{SS} = AV_{SS} = 0 V, Ta = –40 to +85 °C, $f(X_{IN})$ = 12 MHz, unless otherwise noted (Note))

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V_{REF} = V_{CC}			10	Bits
—	Absolute accuracy	V_{REF} = V_{CC}			± 3	LSB
R_{LADDER}	Ladder resistance	V_{REF} = V_{CC}	10		25	kΩ
t_{CONV}	Conversion time		19.6			µs
V_{REF}	Reference voltage		2.7		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

Note. This applies when the main clock division selection bit = “0” and $f(f_2)$ = 6 MHz.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TIMING REQUIREMENTS (V_{CC} = 2.7 – 5.5 V, V_{SS} = 0 V, Ta = –40 to +85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted (Note 1))

Notes 1. This applies when the main clock division selection bit = “0” and f(f_2) = 6 MHz.

2. Input signal’s rise/fall time must be 100 ns or less, unless otherwise noted.

External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time (Note 3)	83		ns
$t_{w(H)}$	External clock input high-level pulse width (Note 4)	33		ns
$t_{w(L)}$	External clock input low-level pulse width (Note 4)	33		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

Notes 3. When the main clock division selection bit = “1”, the minimum value of t_c = 166 ns.

4. When the main clock division selection bit = “1”, values of $t_{w(H)}$ / t_c and $t_{w(L)}$ / t_c must be set to values from 0.45 through 0.55.

Single-chip mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(P0D-E)}$	Port P0 input setup time	200		ns
$t_{su(P1D-E)}$	Port P1 input setup time	200		ns
$t_{su(P2D-E)}$	Port P2 input setup time	200		ns
$t_{su(P3D-E)}$	Port P3 input setup time	200		ns
$t_{su(P4D-E)}$	Port P4 input setup time	200		ns
$t_{su(P5D-E)}$	Port P5 input setup time	200		ns
$t_{su(P6D-E)}$	Port P6 input setup time	200		ns
$t_{su(P7D-E)}$	Port P7 input setup time	200		ns
$t_{su(P8D-E)}$	Port P8 input setup time	200		ns
$t_{su(P10D-E)}$	Port P10 input setup time	200		ns
$t_{h(E-P0D)}$	Port P0 input hold time	0		ns
$t_{h(E-P1D)}$	Port P1 input hold time	0		ns
$t_{h(E-P2D)}$	Port P2 input hold time	0		ns
$t_{h(E-P3D)}$	Port P3 input hold time	0		ns
$t_{h(E-P4D)}$	Port P4 input hold time	0		ns
$t_{h(E-P5D)}$	Port P5 input hold time	0		ns
$t_{h(E-P6D)}$	Port P6 input hold time	0		ns
$t_{h(E-P7D)}$	Port P7 input hold time	0		ns
$t_{h(E-P8D)}$	Port P8 input hold time	0		ns
$t_{h(E-P10D)}$	Port P10 input hold time	0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(D-E)}$	Data input setup time (external bus mode A)	50		ns
$t_{su(D-RDE)}$	Data input setup time (external bus mode B)	50		ns
$t_{su(RDY-\phi1)}$	$\overline{RDY}$ input setup time	80		ns
$t_{su(HOLD-\phi1)}$	$\overline{HOLD}$ input setup time	80		ns
$t_{h(E-D)}$	Data input hold time (external bus mode A)	0		ns
$t_{h(RDE-D)}$	Data input hold time (external bus mode B)	0		ns
$t_{h(\phi1-RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(\phi1-HOLD)}$	$\overline{HOLD}$ input hold time	0		ns

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	250		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	125		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	125		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time (Note)	666		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width (Note)	333		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width (Note)	333		ns

Note. Limits change depending on f(X_{IN}). Refer to “DATA FORMULAS”.

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time (Note)	666		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	166		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	166		ns

Note. Limits change depending on f(X_{IN}). Refer to “DATA FORMULAS”.

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	166		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	166		ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} input cycle time	3333		ns
$t_{w(UPH)}$	TAi_{OUT} input high-level pulse width	1666		ns
$t_{w(UPL)}$	TAi_{OUT} input low-level pulse width	1666		ns
$t_{su(UP-T_{IN})}$	TAi_{OUT} input setup time	666		ns
$t_{h(T_{IN}-UP)}$	TAi_{OUT} input hold time	666		ns

Timer A input (Two-phase pulse input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAj_{IN} input cycle time	2000		ns
$t_{su(TAj_{IN}-TAj_{OUT})}$	TAj_{IN} input setup time	500		ns
$t_{su(TAj_{OUT}-TAj_{IN})}$	TAj_{OUT} input setup time	500		ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (one edge count)	250		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (one edge count)	125		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (one edge count)	125		ns
$t_{c(TB)}$	TBi_{IN} input cycle time (both edges count)	500		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (both edges count)	250		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (both edges count)	250		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (Note)	666		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (Note)	333		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (Note)	666		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (Note)	333		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{AD_{TRG}}$ input cycle time (minimum allowable trigger)	1333		ns
$t_{w(ADL)}$	$\overline{AD_{TRG}}$ input low-level pulse width	166		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK_i input cycle time	333		ns
$t_{w(CKH)}$	CLK_i input high-level pulse width	166		ns
$t_{w(CKL)}$	CLK_i input low-level pulse width	166		ns
$t_{d(C-Q)}$	TxD_i output delay time		100	ns
$t_{h(C-Q)}$	TxD_i hold time	0		ns
$t_{su(D-C)}$	RxD_i input setup time	65		ns
$t_{h(C-D)}$	RxD_i input hold time	75		ns

External interrupt $\overline{INT_i}$ input, key input interrupt $\overline{KI_i}$ input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT_i}$ input high-level pulse width	250		ns
$t_{w(INL)}$	$\overline{INT_i}$ input low-level pulse width	250		ns
$t_{w(KIL)}$	$\overline{KI_i}$ input low-level pulse width	250		ns

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

DATA FORMULAS

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer B input (In pulse period measurement mode or pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Note. $f(f_2)$ represents the clock f_2 frequency.
For the relation to the main clock and sub clock, refer to Table 10 in data sheet “M37736MHBXXXGP”.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SWITCHING CHARACTERISTICS

(V_{CC} = 2.7 – 5.5 V, V_{SS} = 0 V, Ta = –40 to +85°C, f(X_{IN}) = 12 MHz, unless otherwise noted (Note))

Single-chip mode

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{d(E-P0Q)}$	Port P0 data output delay time	Fig. 3		300	ns
$t_{d(E-P1Q)}$	Port P1 data output delay time			300	ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			300	ns
$t_{d(E-P3Q)}$	Port P3 data output delay time			300	ns
$t_{d(E-P4Q)}$	Port P4 data output delay time			300	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time			300	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time			300	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time			300	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time			300	ns
$t_{d(E-P9Q)}$	Port P9 data output delay time			300	ns
$t_{d(E-P10Q)}$	Port P10 data output delay time			300	ns

Note. This applies when the main clock division selection bit = “0” and f(f_2) = 6 MHz.

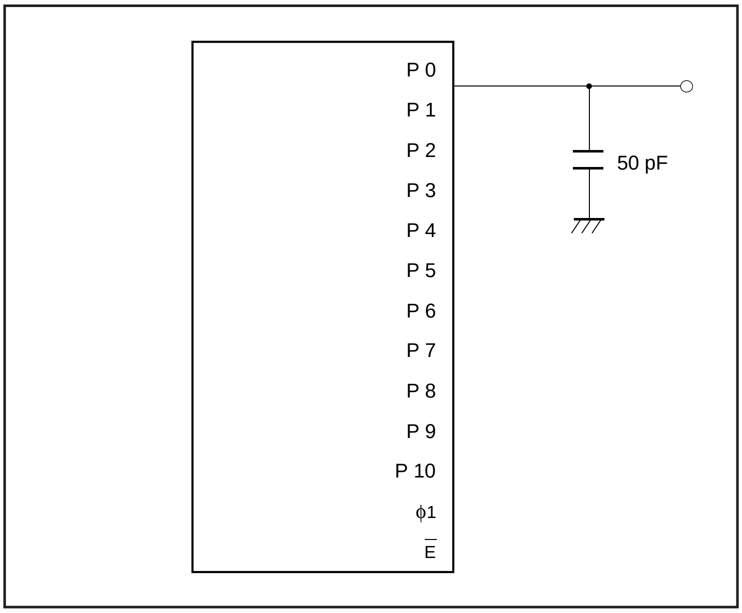


Fig. 3 Measuring circuit for ports P0 – P10 and ϕ_1

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

[External bus mode A]
Memory expansion mode and microprocessor mode

(V_{CC} = 2.7 – 5.5 V, V_{SS} = 0 V, Ta = –40 to +85°C, f(X_{IN}) = 12 MHz (Note 1), unless otherwise noted)

Symbol	Parameter	Wait mode (Note 2)	Test conditions	Limits Min.	Limits Max.	Unit
$t_{d(An-E)}$	Address output delay time	No wait Wait 1		20		ns
		Wait 0		182		ns
$t_{d(A-E)}$	Address output delay time	No wait Wait 1		20		ns
		Wait 0		162		ns
$t_{h(E-An)}$	Address hold time			40		ns
$t_{w(ALE)}$	ALE pulse width	No wait Wait 1		40		ns
		Wait 0		123		ns
$t_{su(A-ALE)}$	Address output setup time	No wait Wait 1		10		ns
		Wait 0		93		ns
$t_{h(ALE-A)}$	Address hold time	No wait Wait 1		9		ns
		Wait 0		40		ns
$t_{d(ALE-E)}$	ALE output delay time	No wait Wait 1	Fig. 3	4		ns
		Wait 0		40		ns
$t_{d(E-DQ)}$	Data output delay time				90	ns
$t_{h(E-DQ)}$	Data hold time			40		ns
$t_{w(EL)}$	$\overline{E}$ pulse width	No wait		131		ns
		Wait 1 Wait 0		298		ns
$t_{pxz(E-DZ)}$	Floating start delay time				10	ns
$t_{pzx(E-DZ)}$	Floating release delay time			53		ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time	No wait Wait 1		20		ns
		Wait 0		182		ns
$t_{d(R/W-E)}$	R/$\overline{W}$ output delay time	No wait Wait 1		20		ns
		Wait 0		182		ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time			33		ns
$t_{h(E-R/W)}$	R/$\overline{W}$ hold time			33		ns
$t_{d(E-\phi_1)}$	ϕ_1 output delay time			0	30	ns
$t_{d(\phi_1-HLDA)}$	$\overline{HLDA}$ output delay time				120	ns

Notes 1. This applies when the main clock division selection bit = “0” and f(f_2) = 6 MHz.
2. No wait : Wait bit = “1”.
Wait 1 : The external memory area is accessed with wait bit = “0” and wait selection bit = “1”.
Wait 0 : The external memory area is accessed with wait bit = “0” and wait selection bit = “0”.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

[External bus mode A]
Memory expansion mode and microprocessor mode

Bus timing data formulas (Vcc = 2.7 – 5.5 V, Vss = 0 V, Ta = –40 to +85 °C, f(XIN) = 12 MHz (Max., Note), unless otherwise noted)

Symbol	Parameter	Wait mode	Limits Min.	Limits Max.	Unit
$t_{d(An-E)}$	Address output delay time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 68$		ns
$t_{d(A-E)}$	Address output delay time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 88$		ns
$t_{h(E-An)}$	Address hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{w(ALE)}$	ALE pulse width	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{su(A-ALE)}$	Address output setup time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 73$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 73$		ns
$t_{h(ALE-A)}$	Address hold time	No wait Wait 1	9		ns
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{d(ALE-E)}$	ALE output delay time	No wait Wait 1	4		ns
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{d(E-DQ)}$	Data output delay time			90	ns
$t_{h(E-DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{w(EL)}$	$\overline{E}$ pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
		Wait 1 Wait 0	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
$t_{pxz(E-DZ)}$	Floating start delay time			10	ns
$t_{pzx(E-DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 68$		ns
$t_{d(R/W-E)}$	R/$\overline{W}$ output delay time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 68$		ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 50$		ns
$t_{h(E-R/W)}$	R/$\overline{W}$ hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 50$		ns
$t_{d(E-\phi 1)}$	ϕ_1 output delay time		0	30	ns

Notes 1. This applies when the main-clock division selection bit = “0”.
2. f(f2) represents the clock f2 frequency.
For the relation to the main clock and sub clock, refer to Table 10 in data sheet “M37736MHBXXXGP”.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

[External bus mode B]
Memory expansion mode and microprocessor mode

(V_{CC} = 2.7 – 5.5 V, V_{SS} = 0 V, Ta = –40 to +85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted (Note 1))

Symbol	Parameter	Wait mode (Note 2)	Test conditions	Limits Min.	Limits Max.	Unit
$t_{d(CS-WE)}$ $t_{d(CS-RDE)}$	Chip-select output delay time	No wait Wait 1	Fig.3	20		ns
		Wait 0		182		ns
$t_{h(WE-CS)}$ $t_{h(RDE-CS)}$	Chip-select hold time			4		ns
$t_{d(An-WE)}$ $t_{d(An-RDE)}$	Address output delay time	No wait Wait 1		20		ns
		Wait 0		182		ns
$t_{d(A-WE)}$ $t_{d(A-RDE)}$	Address output delay time	No wait Wait 1		20		ns
		Wait 0		162		ns
$t_{h(WE-An)}$ $t_{h(RDE-An)}$	Address hold time			40		ns
$t_{w(ALE)}$	ALE pulse width	No wait Wait 1		40		ns
		Wait 0		123		ns
$t_{su(A-ALE)}$	Address output setup time	No wait Wait 1		10		ns
		Wait 0		93		ns
$t_{h(ALE-A)}$	Address hold time	No wait Wait 1		9		ns
		Wait 0		40		ns
$t_{d(ALE-WE)}$ $t_{d(ALE-RDE)}$	ALE output delay time	No wait Wait 1		4		ns
		Wait 0		40		ns
$t_{d(WE-DQ)}$	Data output delay time				90	ns
$t_{h(WE-DQ)}$	Data hold time			40		ns
$t_{w(WE)}$	$\overline{\text{WEL}}$/$\overline{\text{WEH}}$ pulse width	No wait		131		ns
		Wait 1 Wait 0		298		ns
$t_{pxz(RDE-DZ)}$	Floating start delay time				10	ns
$t_{pzx(RDE-DZ)}$	Floating release delay time			53		ns
$t_{w(RDE)}$	$\overline{\text{RDE}}$ pulse width	No wait		128		ns
		Wait 1 Wait 0		295		ns
$t_{d(RSMP-WE)}$ $t_{d(RSMP-RDE)}$	$\overline{\text{RSMP}}$ output delay time			25		ns
$t_{h(\phi_1-RSMP)}$	$\overline{\text{RSMP}}$ hold time			0		ns
$t_{d(WE-\phi_1)}$ $t_{d(RDE-\phi_1)}$	ϕ_1 output delay time			0	30	ns
$t_{d(\phi_1-HLDA)}$	$\overline{\text{HLDA}}$ output delay time				120	ns

Notes 1. This applies when the main clock division selection bit = “0” and f(f_2) = 6 MHz.

2. No wait : Wait bit = “1”.
Wait 1 : The external memory area is accessed with wait bit = “0” and wait selection bit = “1”.
Wait 0 : The external memory area is accessed with wait bit = “0” and wait selection bit = “0”.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

[External bus mode B]

Bus timing data formulas (V_{CC} = 2.7 – 5.5V, V_{SS} = 0 V, Ta = –40 to +85 °C, f(X_{IN}) = 12 MHz (Max.), unless otherwise noted (Note1))

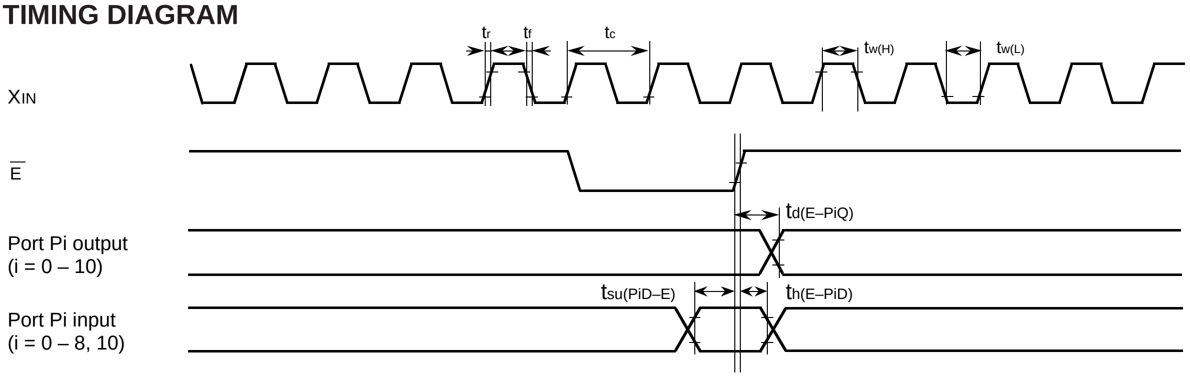
Symbol	Parameter	Wait mode	Limits Min.	Limits Max.	Unit
$t_{d(CS-WE)}$ $t_{d(CS-RDE)}$	Chip-select output delay time	No wait Wait 1	$\frac{1\times10^9}{2\cdot f(f_2)}-63$		ns
		Wait 0	$\frac{3\times10^9}{2\cdot f(f_2)}-68$		ns
$t_{h(WE-CS)}$ $t_{h(RDE-CS)}$	Chip-select hold time		4		ns
$t_{d(An-WE)}$ $t_{d(An-RDE)}$	Address output delay time	No wait Wait 1	$\frac{1\times10^9}{2\cdot f(f_2)}-63$		ns
		Wait 0	$\frac{3\times10^9}{2\cdot f(f_2)}-68$		ns
$t_{d(A-WE)}$ $t_{d(A-RDE)}$	Address output delay time	No wait Wait 1	$\frac{1\times10^9}{2\cdot f(f_2)}-63$		ns
		Wait 0	$\frac{3\times10^9}{2\cdot f(f_2)}-88$		ns
$t_{h(WE-An)}$ $t_{h(RDE-An)}$	Address hold time		$\frac{1\times10^9}{2\cdot f(f_2)}-43$		ns
$t_{w(ALE)}$	ALE pulse width	No wait Wait 1	$\frac{1\times10^9}{2\cdot f(f_2)}-43$		ns
		Wait 0	$\frac{2\times10^9}{2\cdot f(f_2)}-43$		ns
$t_{su(A-ALE)}$	Address output setup time	No wait Wait 1	$\frac{1\times10^9}{2\cdot f(f_2)}-73$		ns
		Wait 0	$\frac{2\times10^9}{2\cdot f(f_2)}-73$		ns
$t_{h(ALE-A)}$	Address hold time	No wait Wait 1	9		ns
		Wait 0	$\frac{1\times10^9}{2\cdot f(f_2)}-43$		ns
$t_{d(ALE-WE)}$ $t_{d(ALE-RDE)}$	ALE output delay time	No wait Wait 1	4		ns
		Wait 0	$\frac{1\times10^9}{2\cdot f(f_2)}-43$		ns
$t_{d(WE-DQ)}$	Data output delay time			90	ns
$t_{h(WE-DQ)}$	Data hold time		$\frac{1\times10^9}{2\cdot f(f_2)}-43$		ns
$t_{w(WE)}$	$\overline{WEL}$/$\overline{WEH}$ pulse width	No wait	$\frac{2\times10^9}{2\cdot f(f_2)}-35$		ns
		Wait 1 Wait 0	$\frac{4\times10^9}{2\cdot f(f_2)}-35$		ns
$t_{pxz(RDE-DZ)}$	Floating start delay time			10	ns
$t_{pzx(RDE-DZ)}$	Floating release delay time		$\frac{1\times10^9}{2\cdot f(f_2)}-30$		ns
$t_{w(RDE)}$	$\overline{RDE}$ pulse width	No wait	$\frac{2\times10^9}{2\cdot f(f_2)}-38$		ns
		Wait 1 Wait 0	$\frac{4\times10^9}{2\cdot f(f_2)}-38$		ns
$t_{d(RSMP-WE)}$ $t_{d(RSMP-RDE)}$	$\overline{RSMP}$ output delay time		$\frac{1\times10^9}{2\cdot f(f_2)}-58$		ns
$t_{h(\phi_1-RSMP)}$	$\overline{RSMP}$ hold time		0		ns
$t_{d(WE-\phi_1)}$ $t_{d(RDE-\phi_1)}$	ϕ_1 output delay time		0	30	ns

Notes 1. This applies when the main clock division selection bit = "0".

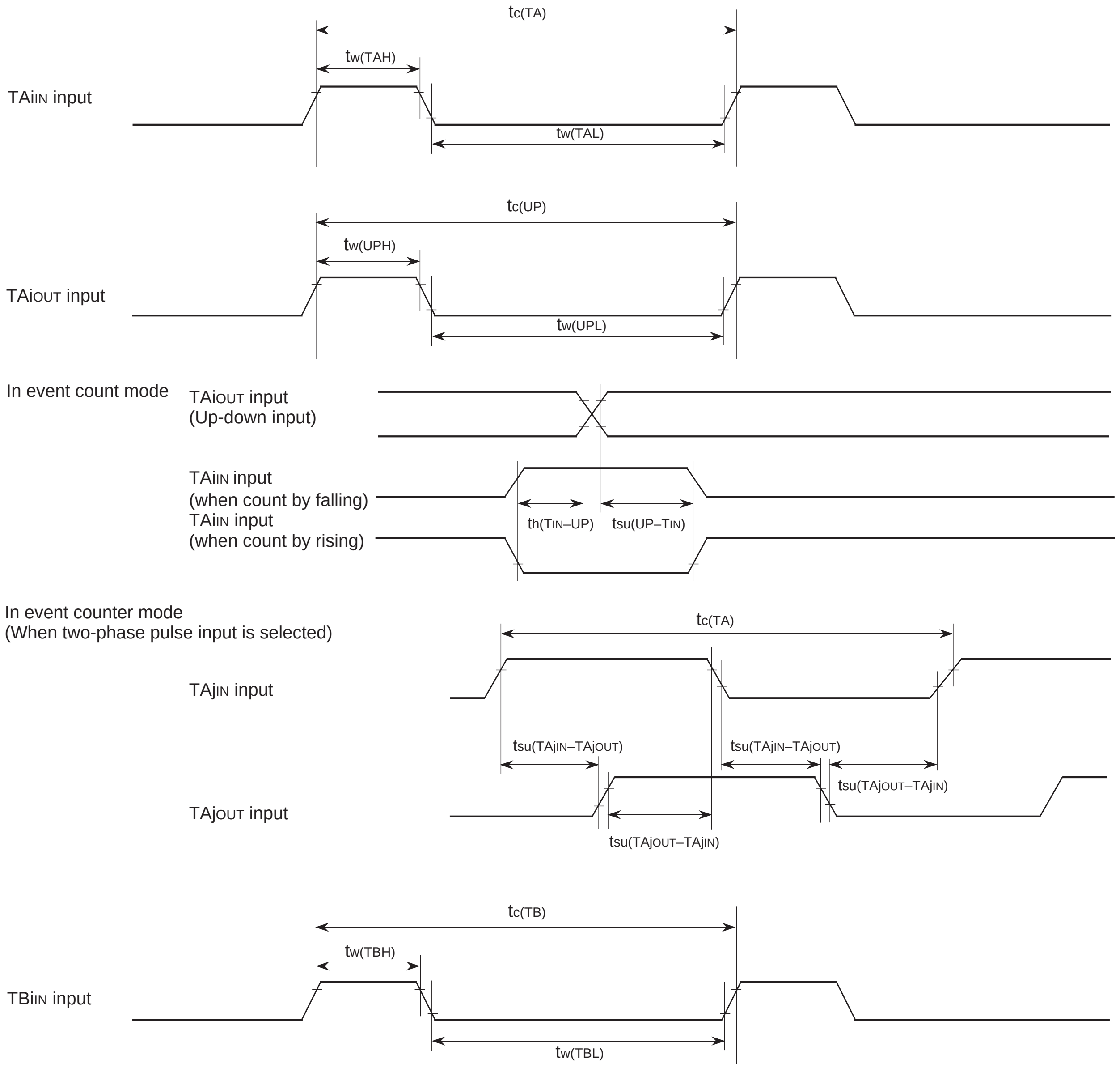
2. f(f_2) represents the clock f_2 frequency.
For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37736MHBXXXGP".

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

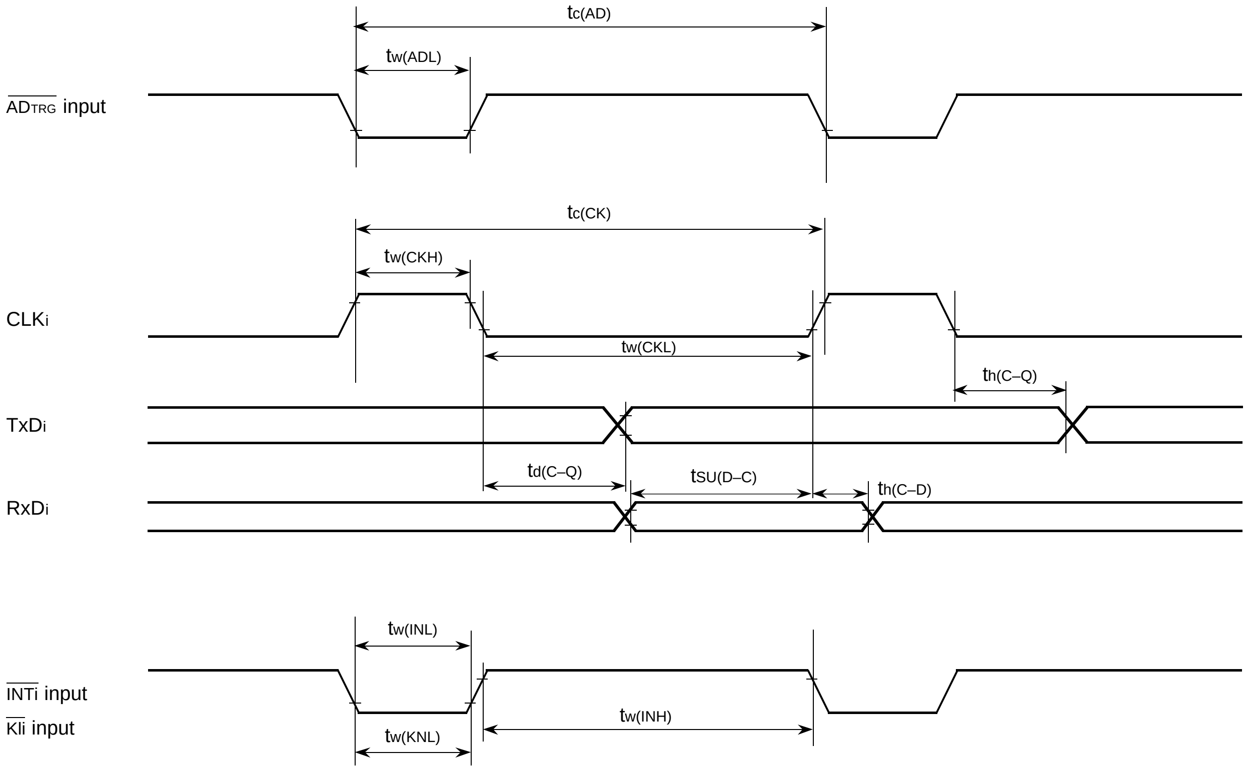
TIMING DIAGRAM



PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

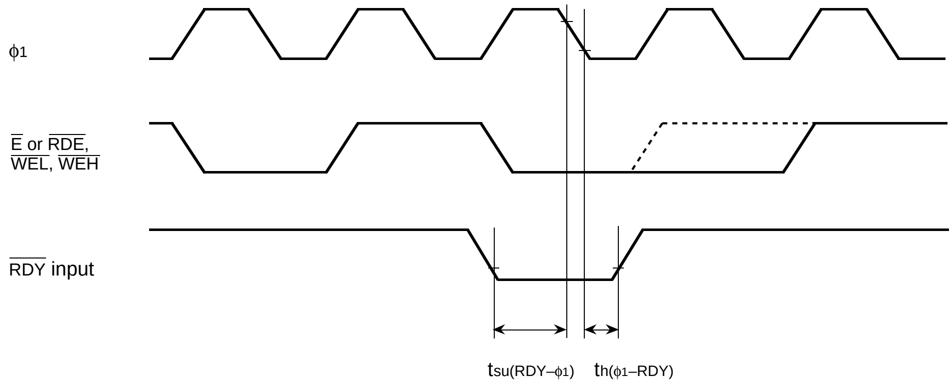


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

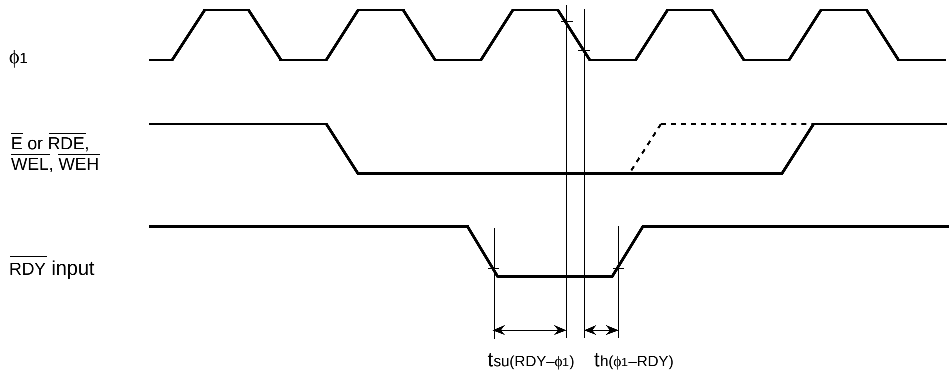


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

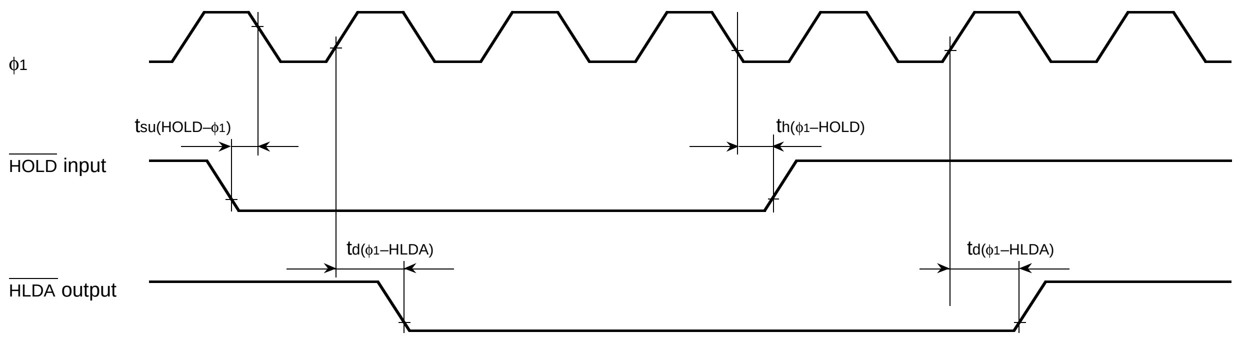
Memory expansion mode and microprocessor mode
(When wait bit = “1”)



(When wait bit = “0”)



(When wait bit = “1” or “0” in common)

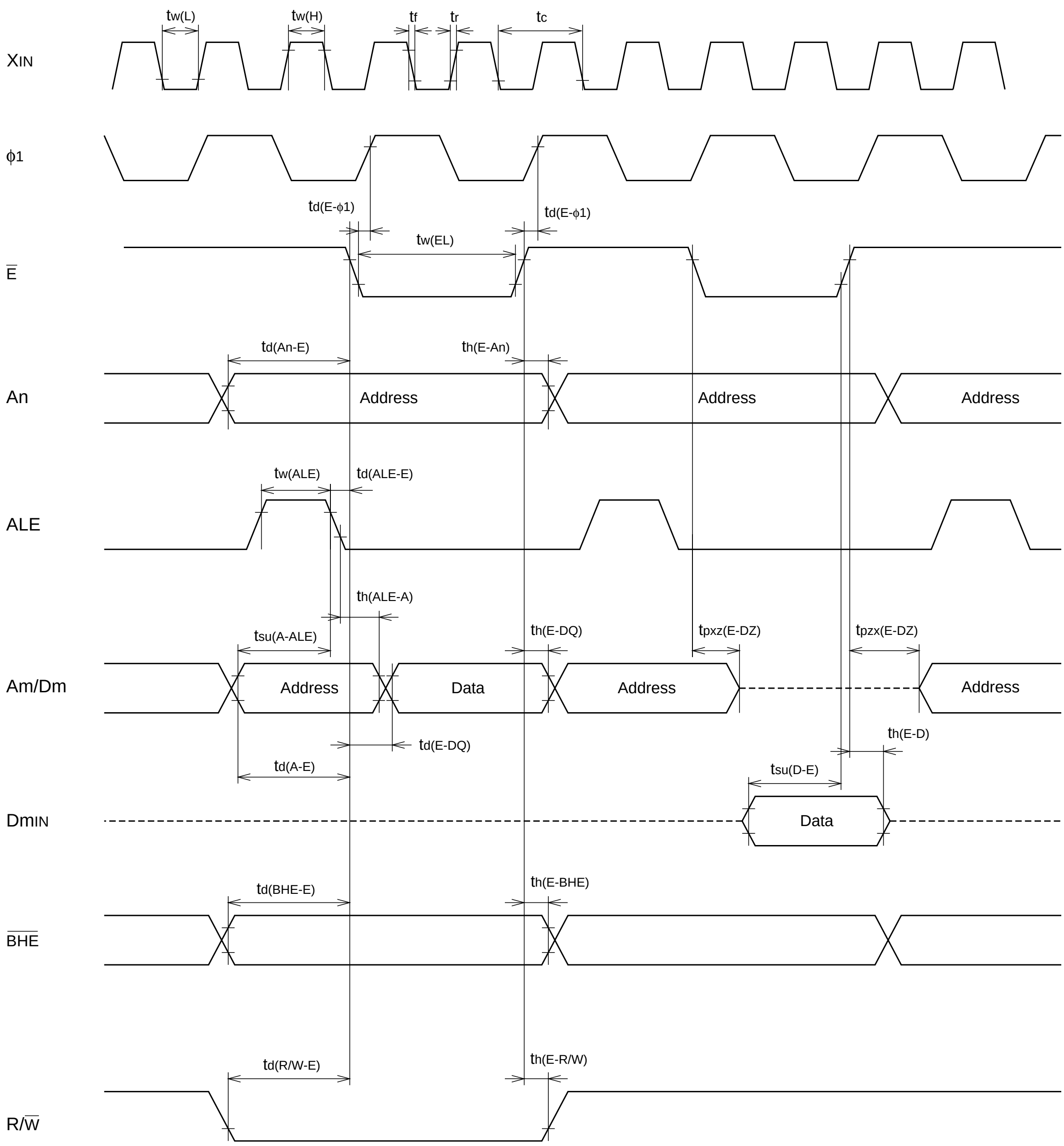


Test conditions
• V_{CC} = 2.7 – 5.5 V
• Input timing voltage : V_{IL} = 0.2 V_{CC}, V_{IH} = 0.8 V_{CC}
• Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

[External bus mode A]

Memory expansion mode and microprocessor mode
(No wait : When wait bit = “1”)

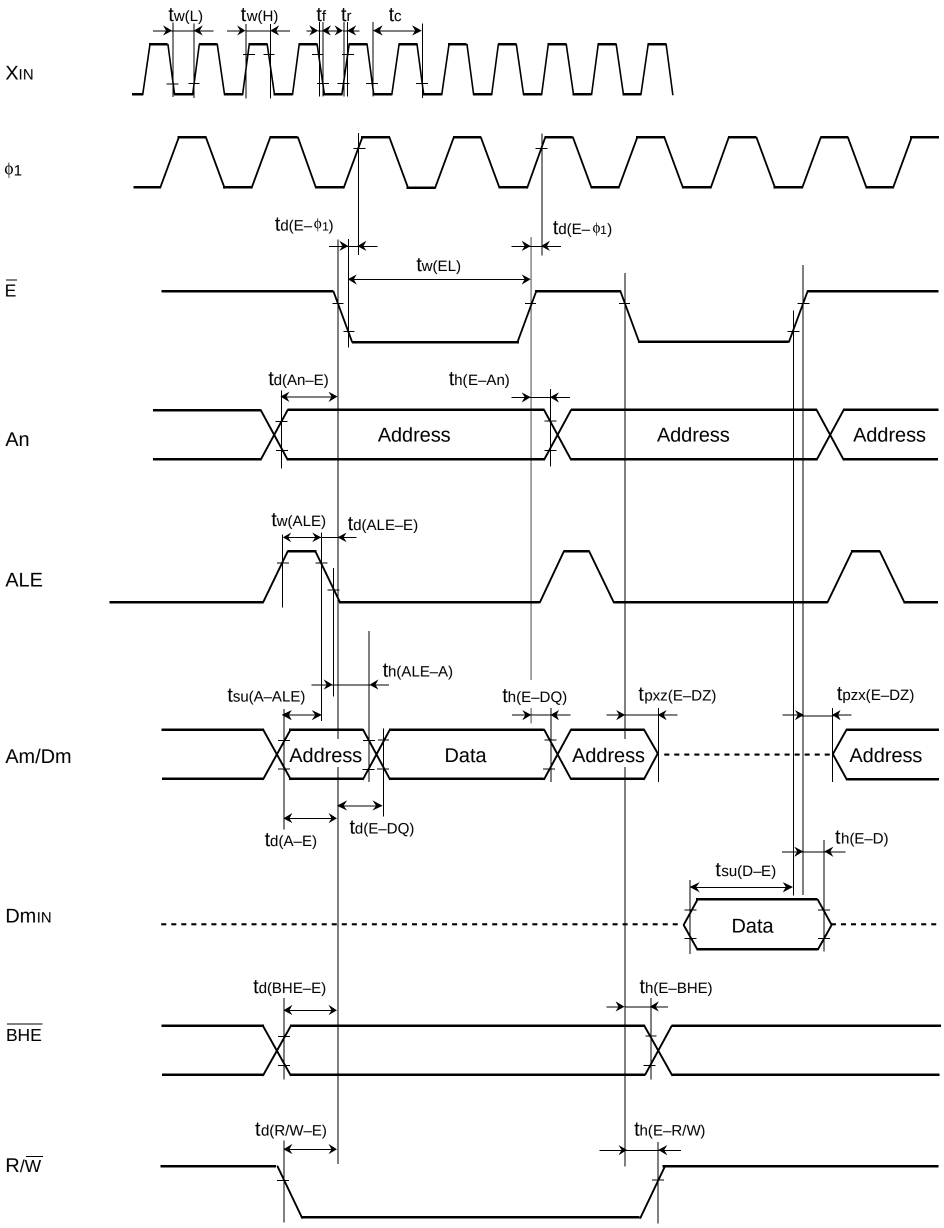


Test conditions
・V_{CC} = 2.7 – 5.5 V
・Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
・Data input Dm_{IN} : V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

[External bus mode A]

Memory expansion mode and microprocessor mode
(Wait 1 : The external area is accessed when wait bit = “0” and wait selection bit = “1”.)

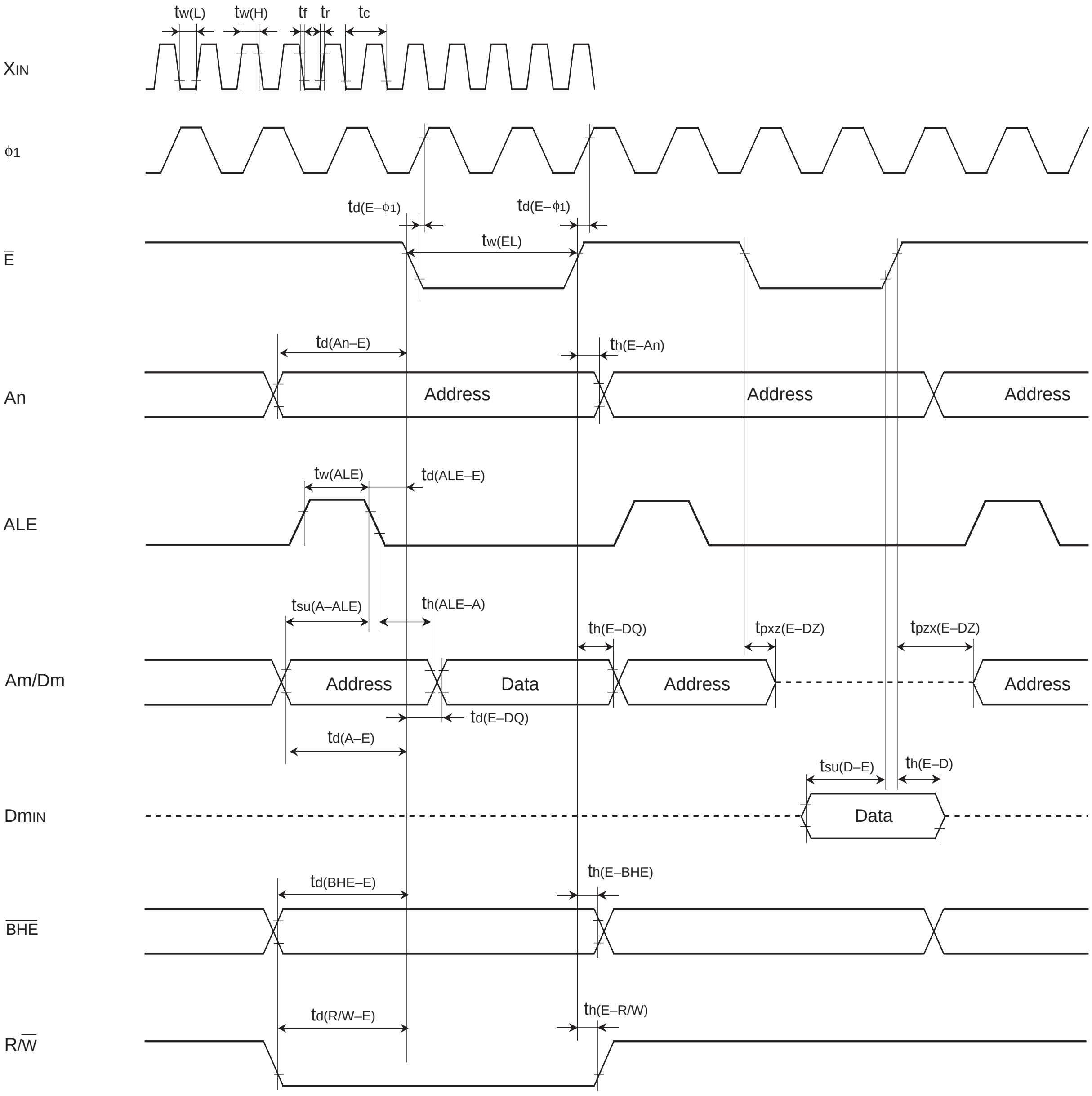


Test conditions
- Vcc = 2.7 – 5.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input Dm_{IN} : V_{IL} = 0.16 Vcc, V_{IH} = 0.5 Vcc

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

[External bus mode A]

Memory expansion mode and microprocessor mode
(Wait 0 : The external memory area is accessed when wait bit = “0” and wait selection bit = “0”.)



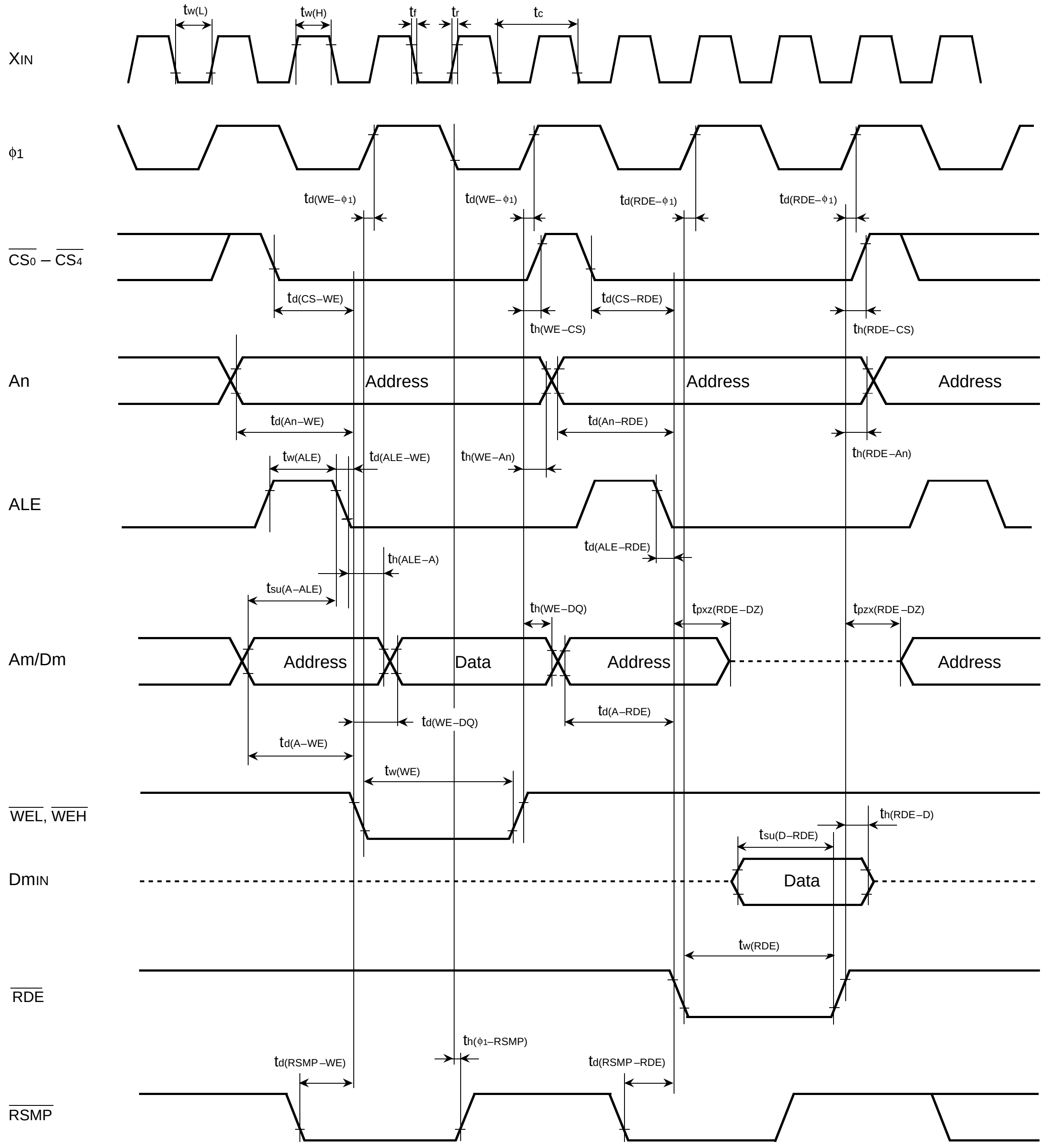
Test conditions
• Vcc = 2.7 – 5.5 V
• Output timing voltage : VOL = 0.8 V, VOH = 2.0 V
• Data input DmIN : VIL = 0.16 Vcc, VIH = 0.5 Vcc

MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

[External bus mode B]

Memory expansion and microprocessor mode
(No wait : When wait bit = “1”)

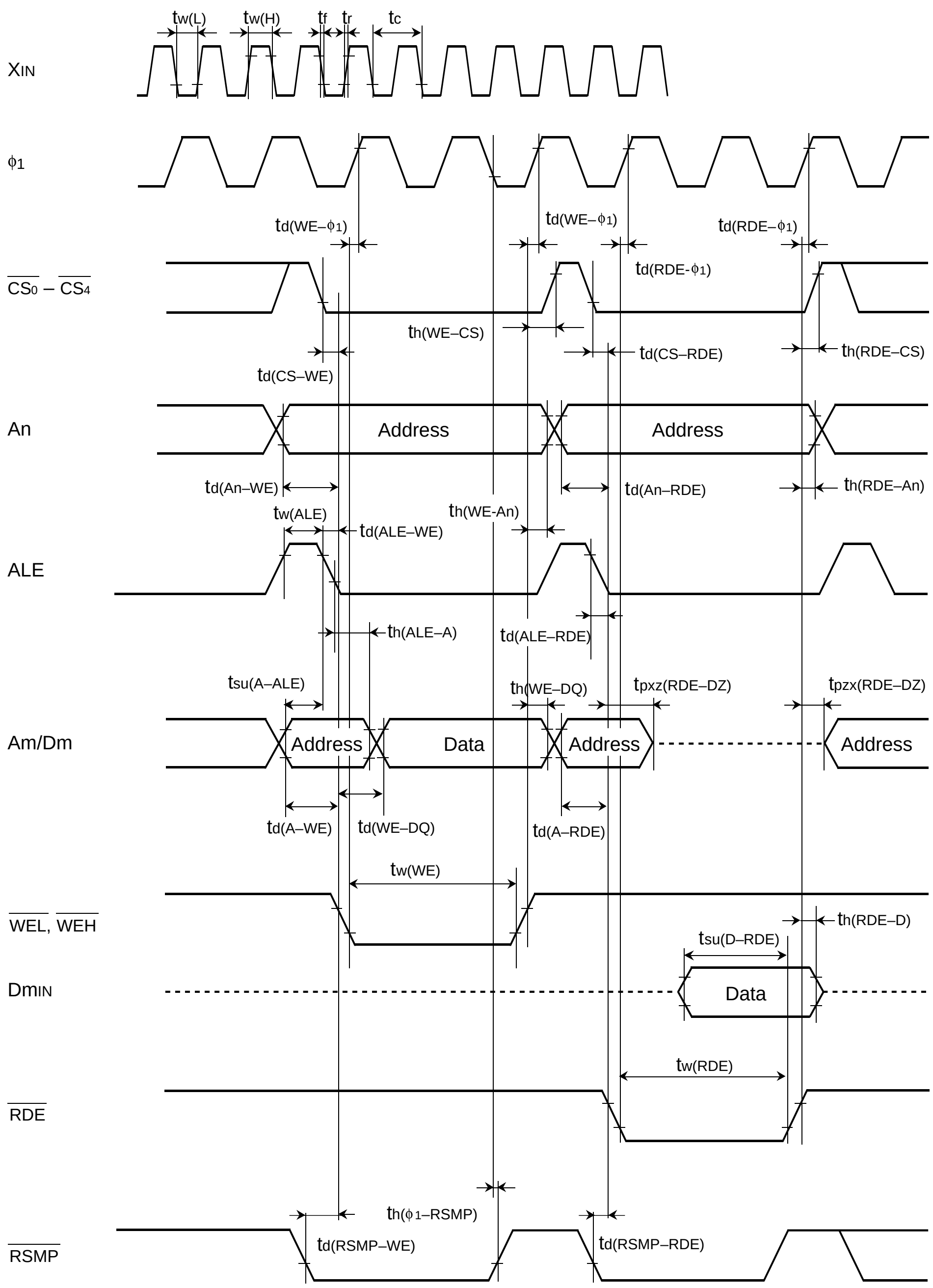


Test conditions
- V_{CC} = 2.7 – 5.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input Dm_{IN} : V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

[External bus mode B]

Memory expansion and microprocessor mode
(Wait 1 : The external area is accessed when wait bit = “0” and wait selection bit = “1”.)

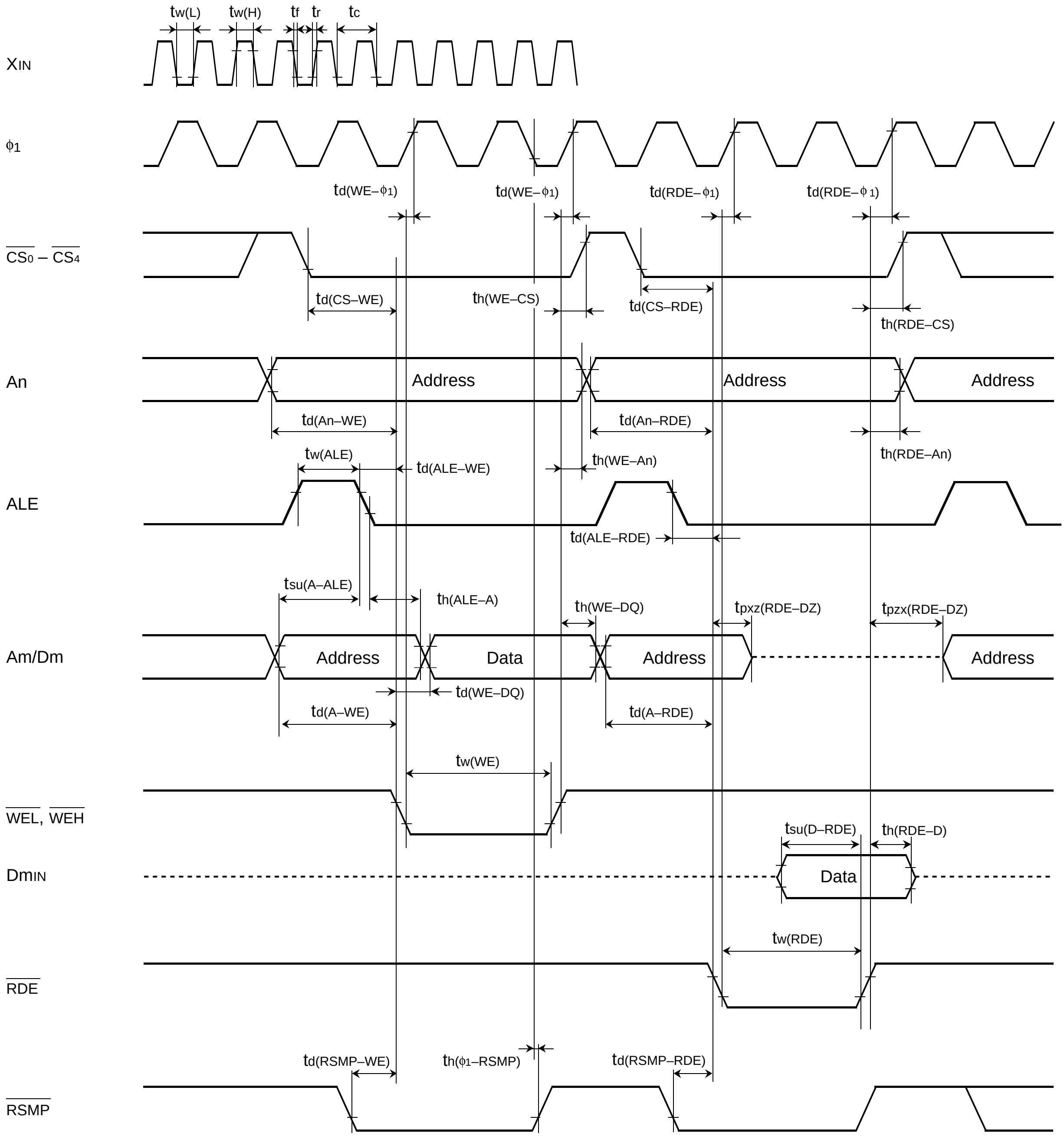


Test conditions
• Vcc = 2.7 – 5.5 V
• Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
• Data input Dm_{IN} : V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

[External bus mode B]

Memory expansion and microprocessor mode
(Wait 0 : The external memory are is accessed when wait bit = “0” and wait selection bit = “0”.)



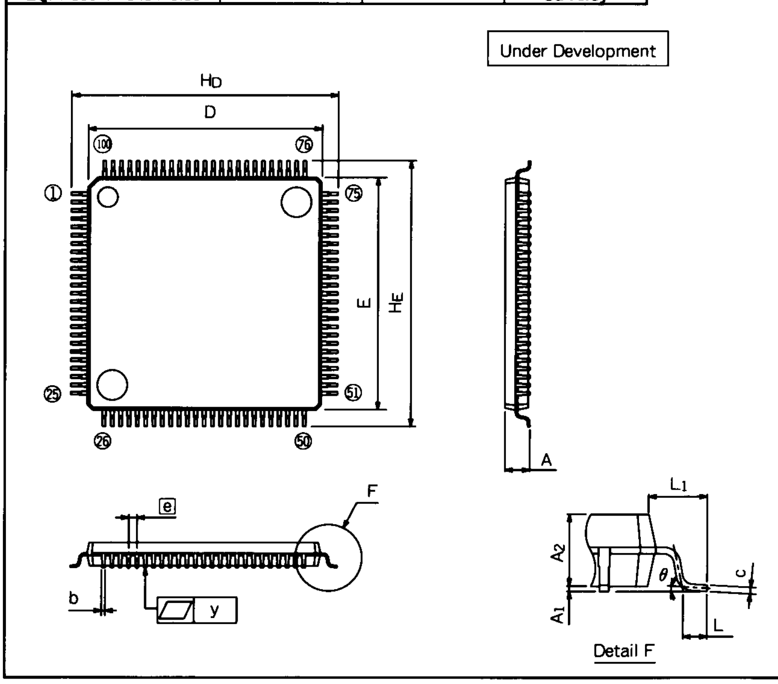
Test conditions
- Vcc = 2.7 – 5.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input Dm_{IN} : V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}

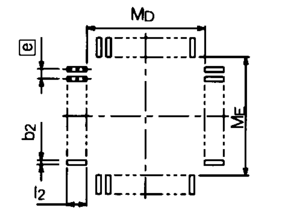
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

PACKAGE OUTLINE

100P6Q–A Plastic 100pin 14×14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	–		Cu Alloy





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0	0.1	0.2
A_2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.5	–
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
L	0.3	0.5	0.7
L_1	–	1.0	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.225	–
l_2	1.0	–	–
M_D	–	14.4	–
M_E	–	14.4	–

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

PROM VERSION OF M37736MHLXXXHP

Keep safety first in your circuit designs!

- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

- These materials are intended as a reference to assist our customers in the selection of the Mitsubishi semiconductor product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Mitsubishi Electric Corporation or a third party.
- Mitsubishi Electric Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts or circuit application examples contained in these materials.
- All information contained in these materials, including product data, diagrams and charts, represent information on products at the time of publication of these materials, and are subject to change by Mitsubishi Electric Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for the latest product information before purchasing a product listed herein.
- Mitsubishi Electric Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
- The prior written approval of Mitsubishi Electric Corporation is necessary to reprint or reproduce in whole or in part these materials.
- If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
  Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
- Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for further details on these materials or the products contained therein.

© 1997 MITSUBISHI ELECTRIC CORP.
H-LF487-A KI-9703 Printed in Japan (ROD) Ⅱ
New publication, effective Mar. 1997.
Specifications subject to change without notice.

MITSUBISHI
ELECTRIC

REVISION DESCRIPTION LIST	M37736EHLXXXHP Datasheet

Rev. No.	Revision Description	Rev. date
1.00	First Edition	970611
2.00	The following are revised:	980731

Page	Previous Version	Revised Version
P11 Right column Line 2	The M37736EHLXXXHP has 28 powerful addressing modes. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for the details of each addressing mode. **MACHINE INSTRUCTION LIST** The M37736EHLXXXHP has 103 machine instructions. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for details.	The M37736EHLXXXHP has 28 powerful addressing modes. Refer to the “7700 Family Software Manual” for the details. **MACHINE INSTRUCTION LIST** The M37736EHLXXXHP has 103 machine instructions. Refer to the “7700 Family Software Manual” for the details.

P15
Memory expansion mode and microprocessor mode

Previous Version

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(D-E)}$	Data input setup time (external bus mode A)	80		ns
$t_{su(D-RDE)}$	Data input setup time (external bus mode B)	80		ns

Revised Version

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(D-E)}$	Data input setup time (external bus mode A)	50		ns
$t_{su(D-RDE)}$	Data input setup time (external bus mode B)	50		ns