## DESCRIPTION

The M37754FFCGP and the M37754FFCHP are single-chip micro-computers designed with high-performance CMOS silicon gate tech-nology, including the internal flash memory. These are housed in 100-pin plastic molded QFP.

These microcomputers have a CPU and a bus interface unit. The CPU is a 16-bit parallel processor that can also be switched to per-form 8-bit parallel processing, and the bus interface unit enhances the memory access efficiency to execute instructions fast.

In addition to the 7700 Family basic instructions, the M37754FFCGP and the M37754FFCHP have 6 special instructions which contain in-structions for signed multiplication/division; these added instructions improve the servo arithmetic performance to control hard disk drives and so on.

These microcomputers also include the flash memory, RAM, mul-tiple-function timers, motor control function, serial I/O, A-D converter, D-A converter, and so on.

The internal flash memory can be programed and erased by using a PROM programmer or by control of the central processing unit (CPU). Therefore, these microcomputers can change the program easily even after they are mounted on the board.

## APPLICATION

Control devices for personal computer peripheral equipment such as CD-ROM drives, hard disk drives, high density FDD, printers
Control devices for office equipment such as copiers and facsimiles
Control devices for industrial equipment such as communication and measuring instruments
Control devices for equipment required for motor control such as in-verter air conditioner and general purpose inverter

## DISTINCTIVE FEATURES

<Microcomputer mode>
- Number of basic machine instructions ..................................... 109
     (103 basic instructions of 7700 Family + 6 special instructions)
- Memory size        Flash memory ................................ 120 Kbytes
                             RAM ...............................................3968 bytes
- Instruction execution time
   The fastest instruction at 40 MHz frequency ...................... 100 ns
- Single power supply ....................................................... 5V ±10 %
- Low power dissipation (at 40 MHz frequency) ....... 125 mW (Typ.)
- Interrupts ........................................................... 21 types, 7 levels
- Multiple-function 16-bit timer .................................................... 5+3
   (three-phase motor drive waveform or pulse motor control wave-form output)
- Serial I/O (UART or clock synchronous) ...................................... 2
- 10-bit A-D converter ........................................... 8-channel inputs
- 8-bit D-A converter .......................................... 2-channel outputs
- 12-bit watchdog timer
- Programmable input/output (ports P0—P11) ............................ 87
- Small package [M37754FFCHP]
     ................................. 100-pin fine pitch QFP (lead pitch : 0.5 mm)

<Flash memory mode>
- Supply voltage ................................................... $V_{CC}$ = 5 V ± 10 %
- Program/Erase voltage ...................................... $V_{PP}$ = 12 V ± 5 %
- Programming method ........................ Programming in unit of byte
- Erasing method ..........................................................................
   Batch erasing and 2-division-block erasing (in CPU reprogramming mode)
- Program/Erase control by software command
- Number of times for programming/erasing ............................. 100

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## M37754FFCGP PIN CONFIGURATION (TOP VIEW)

M37754FFCGP

Left side (pins 81–100):
- P87/TxD1 ↔ 81
- P86/RxD1 ↔ 82
- P85/CLK1 ↔ 83
- P84/CTS1/RTS1/DA1/INT4 ↔ 84
- P83/TxD0 ↔ 85
- P82/RxD0/CLKS0 ↔ 86
- P81/CLK0 ↔ 87
- P80/CTS0/RTS0/CLKS1/DA0 ↔ 88
- VCC — 89
- AVCC — 90
- VREF → 91
- AVSS — 92
- VSS — 93
- P77/AN7/ADTRG ↔ 94
- P76/AN6 ↔ 95
- P75/AN5 ↔ 96
- P74/AN4 ↔ 97
- P73/AN3 ↔ 98
- P72/AN2 ↔ 99
- P71/AN1 ↔ 100

Top side (pins 80–51):
- 80 P00/A0
- 79 P01/A1
- 78 P02/A2
- 77 P03/A3
- 76 P04/A4
- 75 P05/A5
- 74 P06/A6
- 73 P07/A7
- 72 P10/A8
- 71 P11/A9
- 70 P12/A10
- 69 P13/A11
- 68 P14/A12
- 67 P15/A13
- 66 P16/A14
- 65 P17/A15
- 64 P20/A16
- 63 P21/A17
- 62 P22/A18
- 61 P23/A19
- 60 P27/A23
- 59 P100/D0/LA0
- 58 P101/D1/LA1
- 57 P102/D2/LA2
- 56 P103/D3/LA3
- 55 P104/D4/LA4
- 54 P105/D5/LA5
- 53 P106/D6/LA6
- 52 P107/D7/LA7
- 51 P110/D8

Right side (pins 50–31):
- 50 ↔ P111/D9
- 49 ↔ P112/D10
- 48 ↔ P113/D11
- 47 ↔ P114/D12
- 46 ↔ P115/D13
- 45 ↔ P116/D14
- 44 ↔ P117/D15
- 43 ↔ P30/WR
- 42 ↔ P31/BHE
- 41 ↔ P32/ALE
- 40 ↔ P33/HLDA
- 39 VCC
- 38 VSS
- 37 → E/RD
- 36 → XOUT
- 35 XIN
- 34 ← RESET
- 33 CNVSS
- 32 ← BYTE
- 31 ↔ P40/HOLD

Bottom side (pins 1–30):
- 1 P70/AN0
- 2 P95/INT3/KI4
- 3 P94/CS4/RTP13
- 4 P93/CS3/A22/RTP12
- 5 P92/CS2/A21/U/RTP11
- 6 P91/CS1/A20/V/RTP10
- 7 P90/CS0
- 8 P67/TB2IN
- 9 P66/TB1IN
- 10 P65/TB0IN
- 11 P64/INT2
- 12 P63/INT1
- 13 P62/INT0
- 14 P61/TA4IN
- 15 P60/TA4OUT
- 16 P57/TA3IN/KI2
- 17 P56/TA3OUT/KI2
- 18 P55/TA2IN/KI1
- 19 P54/TA2OUT/KI0
- 20 P53/TA1IN/W/RTP03
- 21 P52/TA1OUT/U/RTP02
- 22 P51/TA0IN/V/RTP01
- 23 P50/TA0OUT/W/RTP00
- 24 P47
- 25 P46
- 26 P45
- 27 P44
- 28 P43
- 29 P42/φ1
- 30 P41/RDY

**Outline 100P6S-A**

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SHINGLE-CHIP 16-BIT CMOS MICROCOMPUTER FLASH MEMORY VERSION

## M37754FFCHP PIN CONFIGURATION (TOP VIEW)
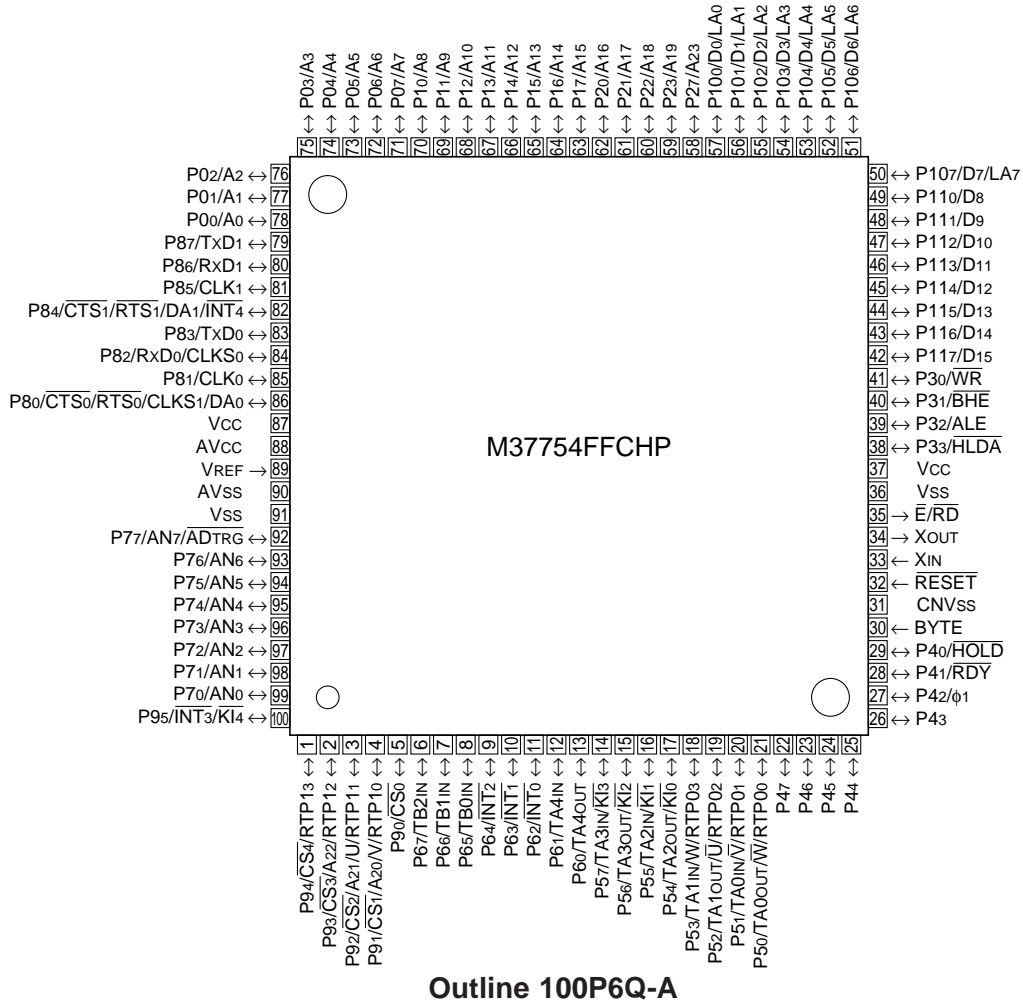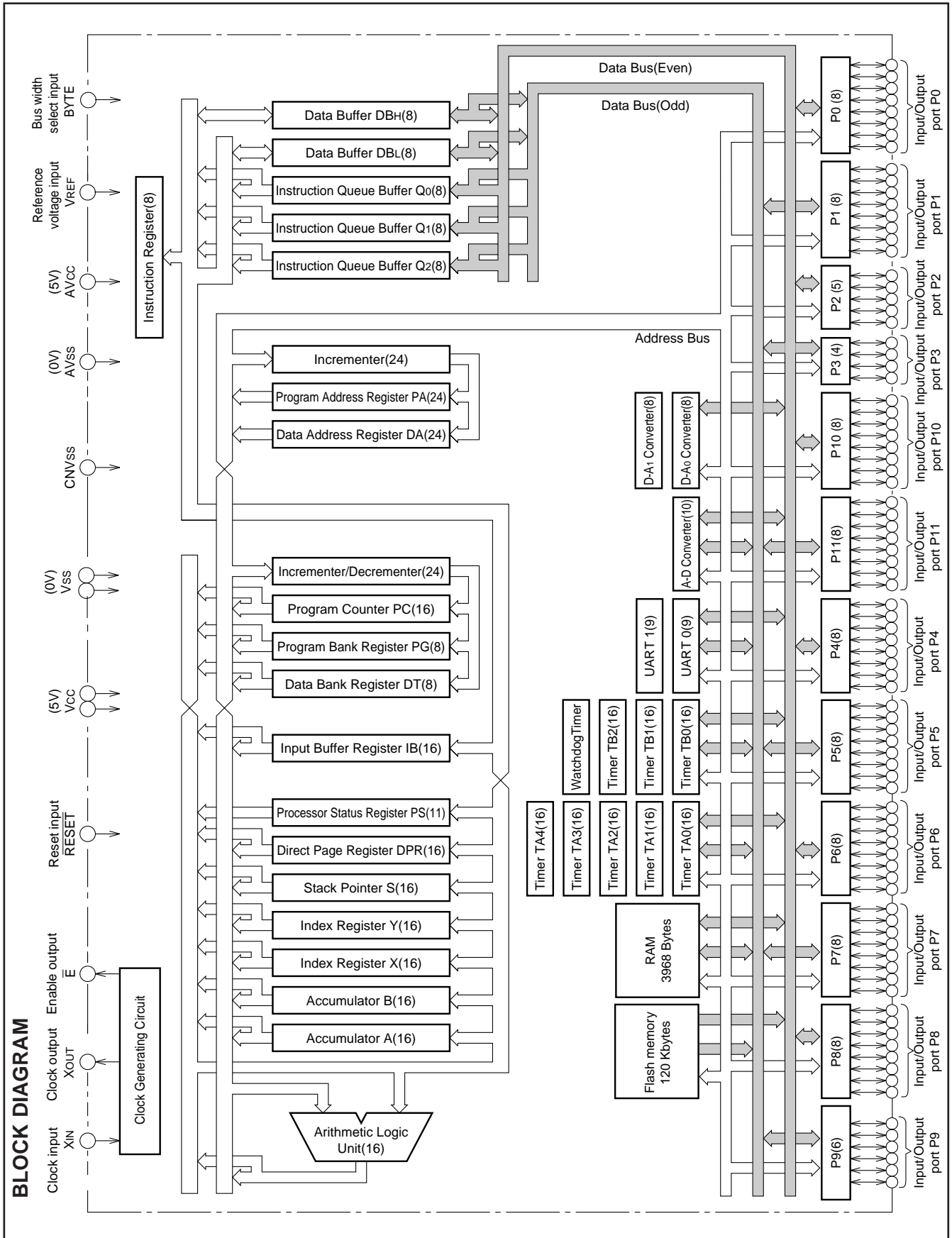


M37754FFCHP

**Outline 100P6Q-A**

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## BLOCK DIAGRAM

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## FUNCTIONS (Microcomputer mode)

| Parameter | | Functions |
|---|---|---|
| Number of basic machine instructions | | 109 (103 basic instructions of 7700 Family + 6 special instructions) |
| Instruction execution time | | 100 ns (the fastest instruction at external clock 40 MHz frequency) |
| Memory size | Flash memory | 120 Kbytes |
| | RAM | 3968 bytes |
| Input/Output ports | P0, P1, P4–P8, P10, P11 | 8-bit × 9 |
| | P2 | 5-bit × 1 |
| | P3 | 4-bit × 1 |
| | P9 | 6-bit × 1 |
| Multiple-function timers | TA0, TA1, TA2, TA3, TA4 | 16-bit × 5 |
| | TB0, TB1, TB2 | 16-bit × 3 |
| Serial I/O | | (UART or clock synchronous serial I/O) × 2 |
| A-D converter | | 10-bit × 1(8 channels) |
| D-A converter | | 8-bit × 2 |
| Watchdog timer | | 12-bit × 1 |
| Dead-time timer | | 8-bit × 3 |
| Interrupts | | 5 external types, 16 internal types (Each interrupt can be set to priority levels 0 – 7.) |
| Clock generating circuit | | Built-in (externally connected to a ceramic resonator or quartz crystal resonator) |
| Supply voltage | | 5 V±10 % |
| Power dissipation | | 125 mW (at external clock 40 MHz frequency) |
| Input/Output characteristic | Input/Output withstand voltage | 5 V |
| | Output current | 5 mA |
| Memory expansion | | Maximum 16 Mbytes |
| Operating temperature range | | –20 to 85 °C |
| Device structure | | CMOS high-performance silicon gate process |
| Package | | 100-pin plastic molded QFP |

## FUNCTIONS (Flash memory mode)

| Parameter | | Functions |
|---|---|---|
| Supply voltage | | 5 V ± 10 % |
| Program/Erase voltage | | 12 V ± 5 % |
| Flash memory mode | | 3 modes (parallel I/O, serial I/O, CPU reprogramming) |
| Programming method | Parallel I/O mode | Programming in unit of byte/120 Kbytes |
| | Serial I/O mode | Programming in unit of byte/120 Kbytes |
| | CPU reprogramming mode | Programming in unit of byte/112 Kbytes |
| Erasing method | Parallel I/O mode | Batch erasing/120 Kbytes |
| | Serial I/O mode | Batch erasing/120 Kbytes |
| | CPU reprogramming mode | Batch erasing/112 Kbytes or 2-division-block erasing 2-division-block erasing: 56-Kbyte area to be erased is selectable. |
| Program/Erase control method | | Program/Erase control by software command |
| Command number | Parallel I/O mode | 7 commands |
| | Serial IO mode | 7 commands |
| | CPU reprogramming mode | 7 commands |
| Number of times for Program/Erase | | 100 |

## PIN DESCRIPTION (MICROCOMPUTER MODE)

| Pin | Name | Input/ Output | Functions |
|---|---|---|---|
| $V_{CC}$, $V_{SS}$ | Power supply | | Supply 5 V±10 % to $V_{CC}$ and 0 V to $V_{SS}$. |
| $CNV_{SS}$ | $CNV_{SS}$ input | Input | This pin controls the processor mode. Connect to $V_{SS}$ for single-chip mode or memory expansion mode. Connect to $V_{CC}$ for microprocessor mode. |
| $\overline{RESET}$ | Reset input | Input | This is reset input pin. The microcomputer is reset when supplying "L" level to this pin. |
| $X_{IN}$ | Clock input | Input | These are I/O pins of internal clock generating circuit. Connect a ceramic or quartz-crystal resonator between $X_{IN}$ and $X_{OUT}$. When an external clock is used, the clock source should be connected to the $X_{IN}$ pin and the $X_{OUT}$ pin should be left open. |
| $X_{OUT}$ | Clock output | Output | |
| $\overline{E}$ | Enable output | Output | This pin outputs enable signal $\overline{E}$, which indicates access state of data bus for single-chip mode. This pin outputs $\overline{RD}$ signal for memory expansion mode or microprocessor mode. |
| BYTE **(Note)** | Bus width select input | Input | This pin determines whether the external data bus is 8-bit width or 16-bit width for memory expansion mode or microprocessor mode. The width is 16 bits when "L" signal inputs and 8 bits when "H" signal inputs. |
| $AV_{CC}$, $AV_{SS}$ | Analog supply input | | Power supply for the A-D converter and the D-A converter. Connect $AV_{CC}$ to $V_{CC}$ and $AV_{SS}$ to $V_{SS}$ externally. |
| $V_{REF}$ | Reference voltage input | Input | This is reference voltage input pin for the A-D converter and the D-A converter. |
| $P0_0$–$P0_7$ | I/O port P0 | I/O | In single-chip mode, port P0 is an 8-bit I/O port. This port has an I/O direction register and each pin can be programmed for input or output. These ports are in the input mode when reset. Address ($A_0$ - $A_7$) is output in memory expansion mode or microprocessor mode. |
| $P1_0$–$P1_7$ | I/O port P1 | I/O | In single-chip mode, these pins have the same functions as port P0. Address ($A_8$ - $A_{15}$) is output in memory expansion mode or microprocessor mode. |
| $P2_0$–$P2_3$, $P2_7$ | I/O port P2 | I/O | In single-chip mode, these pins have the same functions as port P0. Address ($A_{16}$ - $A_{19}$, $A_{23}$) is output in memory expansion mode or microprocessor mode. |
| $P3_0$–$P3_3$ | I/O port P3 | I/O | In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, $\overline{WR}$, $\overline{BHE}$, ALE, and HLDA signals are output. |
| $P4_0$–$P4_7$ | I/O port P4 | I/O | In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, $P4_0$, $P4_1$, and $P4_2$ become $\overline{HOLD}$ and $\overline{RDY}$ input pins, and clock $\phi_1$ output pin respectively. Functions of other pins are the same as in single-chip mode. In memory expansion mode, $P4_2$ can be programmed as I/O port. |
| $P5_0$–$P5_7$ | I/O port P5 | I/O | In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A0, timer A1, timer A2, timer A3, output pins for motor drive waveform, and input pins for key input interrupt. |
| $P6_0$–$P6_7$ | I/O port P6 | I/O | In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input $\overline{INT_0}$, $\overline{INT_1}$, and $\overline{INT_2}$, and input pins for timer B0, timer B1, and timer B2. |
| $P7_0$–$P7_7$ | I/O port P7 | I/O | In addition to having the same functions as port P0 in single-chip mode, these pins also function as input pins for A-D converter. |
| $P8_0$–$P8_7$ | I/O port P8 | I/O | In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for UART0, UART1, output pins for D-A converter, and input pin for $\overline{INT_4}$. |
| $P9_0$–$P9_5$ | I/O port P9 | I/O | In addition to having the same functions as port P0 in single-chip mode, these pins also function as input pin for $\overline{INT_3}$, output pins for motor drive waveform. In memory expansion mode and microprocessor mode, these pins can be programmed as address ($A_{20}$ - $A_{22}$) or output pins for $\overline{CS_0}$ – $\overline{CS_4}$ |

**Note:** It is impossible to change the input level of the BYTE pin in each bus cycle. In other words, bus width cannot be switched dynamically. Fix the input level of the BYTE pin to "H" or "L" according to the bus width used.

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| Pin | Name | Input/Output | Functions |
|---|---|---|---|
| P10$_0$–P10$_7$ | I/O port P10 | I/O | In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, these pins become data I/O pins and operate as follows:<br><br>(1) When using 16-bit width as external data bus width:<br>● Accessing external memory<br><When reading><br>Pins' value is input into low-order internal data bus (DB$_0$ to DB$_7$).<br><When writing><br>Value of low-order internal data bus (DB$_0$ to DB$_7$) is output to these pins.<br>● Accessing internal memory<br><When reading><br>These pins enter high impedance state.<br><When writing><br>Value of internal data bus is output to these pins.<br><br>(2) When using 8-bit width as external data bus width:<br>● Accessing external memory<br><When reading><br>Pins' value is input into internal data bus. The value is input into low-order internal data bus (DB$_0$ to DB$_7$) when accessing an even address; it is input into high-order internal data bus (DB$_8$ to DB$_{15}$) when accessing an odd address.<br><When writing><br>Value of internal data bus is output to these pins. The value of low-order internal data bus (DB$_0$ to DB$_7$) is output when accessing an even address; the value of high-order internal data bus (DB$_8$ to DB$_{15}$) is output when accessing an odd address.<br>● Accessing internal memory<br><When reading><br>These pins enter high impedance state.<br><When writing><br>Value of internal data bus is output to these pins.<br>When the external bus width is 8 bits, the mode where low-order address (LA$_0$ – LA$_7$) is output when $\overline{RD}$ or $\overline{WR}$ output is "H" and data (D$_0$ – D$_7$) is input/output when $\overline{RD}$ or $\overline{WR}$ output is "L" can be selected in specified external memory area access cycle. |
| P11$_0$–P11$_7$ | I/O port P11 | I/O | In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, these pins operate as follows:<br><br>(1) When using 16-bit width as external data bus width<br>● Accessing external memory<br><When reading><br>The value is input into high-order internal data bus (DB$_8$ to DB$_{15}$) when accessing an odd address; these pins enter high impedance state when not accessing an odd address.<br><When writing><br>Value of high-order internal data bus (DB$_8$-DB$_{15}$) is output to these pins.<br>● Accessing internal memory<br><When reading><br>These pins enter high impedance state.<br><When writing><br>Value of internal data bus is output to these pins.<br>(2) When using 8-bit width as external data bus width<br>These pins become I/O port P11$_0$ – P11$_7$. |

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

## PIN DESCRIPTION (FLASH MEMORY PARALLEL I/O MODE)

| Pin | Name | Input/Output | Functions |
|---|---|---|---|
| $V_{CC}$, $V_{SS}$ | Power supply | — | Supply 5 V ± 10 % to $V_{CC}$ and 0 V to $V_{SS}$. |
| $\overline{CNV_{SS}}$ | $V_{PP}$ input | Input | Connect to 5 V ± 10 % in read-only mode, connect to 12 V ± 5 % in read/write mode. |
| BYTE | Bus width select input | Input | Connect to $V_{SS}$. |
| $\overline{RESET}$ | Reset input | Input | Connect to $V_{SS}$. |
| $X_{IN}$ | Clock input | Input | Connect a ceramic resonator between $X_{IN}$ and $X_{OUT}$. |
| $X_{OUT}$ | Clock output | Output | |
| $\overline{E}$ | Enable output | Output | Keep it open. |
| $AV_{CC}$, $AV_{SS}$ | Analog supply input | — | Connect $AV_{CC}$ to $V_{CC}$ and $AV_{SS}$ to $V_{SS}$. |
| $V_{REF}$ | Reference voltage input | Input | Connect to $V_{SS}$. |
| $P0_0$–$P0_7$ | Address input (A0–A7) | Input | Port P0 functions as 8-bit address input (A0–A7). |
| $P1_0$–$P1_7$ | Address input (A8–A15) | Input | Port P1 functions as 8-bit address input (A8–A15). |
| $P2_0$–$P2_3$, $P2_7$ | Input port P2 | Input | Connect to $V_{SS}$. |
| $P3_0$–$P3_3$ | Input port P3 | Input | Connect to $V_{SS}$. |
| $P4_0$–$P4_7$ | Input port P4 | Input | Keep $P4_2$ open. Connect $P4_0$, $P4_1$, $P4_3$–$P4_7$ to $V_{SS}$. |
| $P5_0$–$P5_7$ | Control signal input | Input | $P5_0$, $P5_1$ and $P5_2$ function as the $\overline{WE}$, $\overline{OE}$ and $\overline{CE}$ input pins respectively. $P5_4$ functions as the A16 input pin. Connect $P5_3$ to $V_{CC}$. Connect $P5_5$, $P5_6$ and $P5_7$ to $V_{SS}$. |
| $P6_0$–$P6_7$ | Input port P6 | Input | Connect to $V_{SS}$. |
| $P7_0$–$P7_7$ | Input port P7 | Input | Connect to $V_{SS}$. |
| $P8_0$–$P8_7$ | Input port P8 | Input | Connect to $V_{SS}$. |
| $P9_0$–$P9_5$ | Input port P9 | Input | Connect to $V_{SS}$. |
| $P10_0$–$P10_7$ | Data I/O (D0–D7) | I/O | Function as 8-bit data's I/O pins (D0–D7). |
| $P11_0$–$P11_7$ | Input port P11 | Input | Connect to $V_{SS}$. |

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## PIN DESCRIPTION (FLASH MEMORY SERIAL I/O MODE)

| Pin | Name | Input /Output | Functions |
|---|---|---|---|
| $V_{CC}$, $V_{SS}$ | Power supply | — | Supply 5 V ± 10 % to $V_{CC}$ and 0 V to $V_{SS}$. |
| $CNV_{SS}$ | $V_{PP}$ input | Input | Connect to 12 V ± 5 %. |
| BYTE | Bus width select input | Input | Connect to $V_{SS}$ or $V_{CC}$. |
| $\overline{RESET}$ | Reset input | Input | Connect to $V_{SS}$. |
| $X_{IN}$ | Clock input | Input | Connect a ceramic resonator between $X_{IN}$ and $X_{OUT}$. |
| $X_{OUT}$ | Clock output | Output | |
| $\overline{E}$ | Enable output | Output | "H" is output. |
| $AV_{CC}$, $AV_{SS}$ | Analog supply input | — | Connect $AV_{CC}$ to $V_{CC}$ and $AV_{SS}$ to $V_{SS}$. |
| $V_{REF}$ | Reference voltage input | Input | Input an arbitrary level between the range of $V_{SS}$ and $V_{CC}$. |
| $P0_0$–$P0_7$ | Input port P0 | Input | Input "H" or "L", or keep them open. |
| $P1_0$–$P1_7$ | Input port P1 | Input | Input "H" or "L", or keep them open. |
| $P2_0$–$P2_3$, $P2_7$ | Input port P2 | Input | Input "H" or "L", or keep them open. |
| $P3_0$–$P3_3$ | Input port P3 | Input | Input "H" or "L", or keep them open. |
| $P4_0$–$P4_3$, $P4_7$ | Input port P4 | Input | Input "H" or "L" to $P4_0$, $P4_1$, $P4_3$, $P4_7$, or keep them open. Keep $P4_2$ open. |
| $P4_4$ | BUSY output | Output | This pin is for BUSY signal output. |
| $P4_5$ | SDA I/O | I/O | This pin is for serial data I/O. |
| $P4_6$ | SCLK input | Input | This pin is for serial clock input. |
| $P5_0$, $P5_2$–$P5_7$ | Input port P5 | Input | Input "H" or "L", or keep them open. |
| $P5_1$ | Control signal input | Input | $\overline{OE}$ input pin |
| $P6_0$–$P6_7$ | Input port P6 | Input | Input "H" or "L", or keep them open. |
| $P7_0$–$P7_7$ | Input port P7 | Input | Input "H" or "L", or keep them open. |
| $P8_0$–$P8_7$ | Input port P8 | Input | Input "H" or "L", or keep them open. |
| $P9_0$–$P9_5$ | Input port P9 | Input | Input "H" or "L", or keep them open. |
| $P10_0$–$P10_7$ | Input port P10 | Input | Input "H" or "L", or keep them open. |
| $P11_0$–$P11_7$ | Input port P11 | Input | Input "H" or "L", or keep them open. |

## BASIC FUNCTION BLOCKS

The M37754FFCGP and the M37754FFCHP have the same functions as the M37754M8C-XXXGP and the M37754M8C-XXXHP except for the following.

Therefore, refer to the section on the M37754M8C-XXXGP and the M37754M8C-XXXHP.

(1) Flash memory is included instead of ROM.

(2) The memory size is different.

(3) The memory area modification function is different.

(4) Part of the peripheral devices control registers is different.
   (Flash memory control register, flash command register, and bits 3, 4 of particular function select register 0 are added.)

## MEMORY

The memory map is shown in Figure 1.



Fig. 1  Memory map

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Notice: This is not a final specification.
Some parametric limits are subject to change.
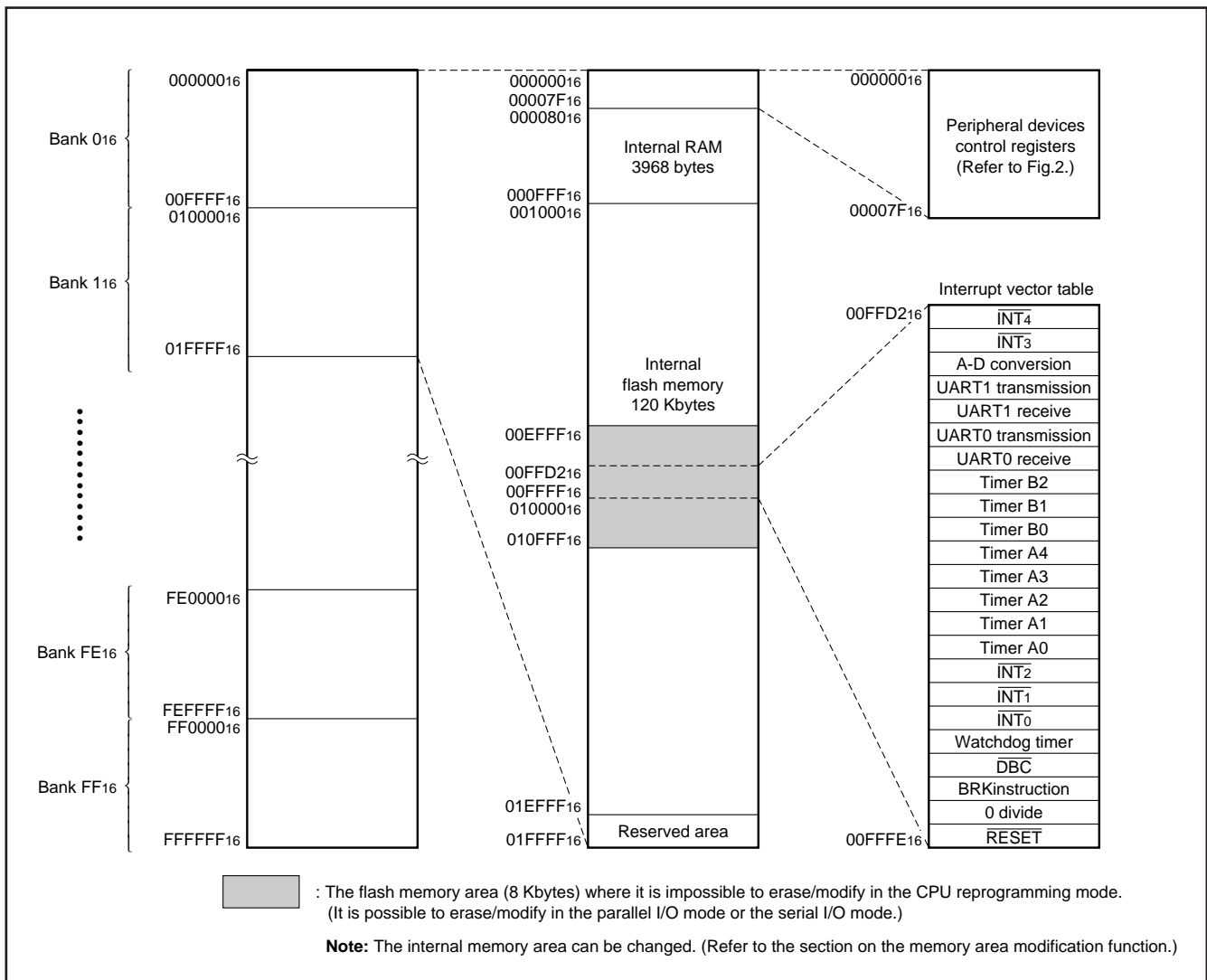
| Address (Hexadecimal notation) | |
|---|---|
| 000000 | |
| 000001 | |
| 000002 | Port P0 register |
| 000003 | Port P1 register |
| 000004 | Port P0 direction register |
| 000005 | Port P1 direction register |
| 000006 | Port P2 register |
| 000007 | Port P3 register |
| 000008 | Port P2 direction register |
| 000009 | Port P3 direction register |
| 00000A | Port P4 register |
| 00000B | Port P5 register |
| 00000C | Port P4 direction register |
| 00000D | Port P5 direction register |
| 00000E | Port P6 register |
| 00000F | Port P7 register |
| 000010 | Port P6 direction register |
| 000011 | Port P7 direction register |
| 000012 | Port P8 register |
| 000013 | Port P9 register |
| 000014 | Port P8 direction register |
| 000015 | Port P9 direction register |
| 000016 | Port P10 register |
| 000017 | Port P11 register |
| 000018 | Port P10 direction register |
| 000019 | Port P11 direction register |
| 00001A | Waveform output mode register |
| 00001B | Dead-time timer |
| 00001C | Pulse output data register 1 |
| 00001D | Pulse output data register 0 |
| 00001E | A-D control register 0 |
| 00001F | A-D control register 1 |
| 000020 | A-D register 0 |
| 000021 | |
| 000022 | A-D register 1 |
| 000023 | |
| 000024 | A-D register 2 |
| 000025 | |
| 000026 | A-D register 3 |
| 000027 | |
| 000028 | A-D register 4 |
| 000029 | |
| 00002A | A-D register 5 |
| 00002B | |
| 00002C | A-D register 6 |
| 00002D | |
| 00002E | A-D register 7 |
| 00002F | |
| 000030 | UART0 transmit/receive mode register |
| 000031 | UART0 baud rate register |
| 000032 | UART0 transmit buffer register |
| 000033 | |
| 000034 | UART0 transmit/receive control register 0 |
| 000035 | UART0 transmit/receive control register 1 |
| 000036 | UART0 receive buffer register |
| 000037 | |
| 000038 | UART1 transmit/receive mode register |
| 000039 | UART1 baud rate register |
| 00003A | UART1 transmit buffer register |
| 00003B | |
| 00003C | UART1 transmit/receive control register 0 |
| 00003D | UART1 transmit/receive control register 1 |
| 00003E | UART1 receive buffer register |
| 00003F | |

| Address (Hexadecimal notation) | |
|---|---|
| 000040 | Count start register |
| 000041 | |
| 000042 | One-shot start register |
| 000043 | |
| 000044 | Up-down register |
| 000045 | Timer A write register |
| 000046 | Timer A0 register |
| 000047 | |
| 000048 | Timer A1 register |
| 000049 | |
| 00004A | Timer A2 register |
| 00004B | |
| 00004C | Timer A3 register |
| 00004D | |
| 00004E | Timer A4 register |
| 00004F | |
| 000050 | Timer B0 register |
| 000051 | |
| 000052 | Timer B1 register |
| 000053 | |
| 000054 | Timer B2 register |
| 000055 | |
| 000056 | Timer A0 mode register |
| 000057 | Timer A1 mode register |
| 000058 | Timer A2 mode register |
| 000059 | Timer A3 mode register |
| 00005A | Timer A4 mode register |
| 00005B | Timer B0 mode register |
| 00005C | Timer B1 mode register |
| 00005D | Timer B2 mode register |
| 00005E | Processor mode register 0 |
| 00005F | Processor mode register 1 |
| 000060 | Watchdog timer register |
| 000061 | Watchdog timer frequency select regsiter |
| 000062 | Chip select control register |
| 000063 | Chip select area register |
| 000064 | Comparator function select register |
| 000065 | Flash command register |
| 000066 | Comparator result register |
| 000067 | Flash memory control register |
| 000068 | D-A register 0 |
| 000069 | |
| 00006A | D-A register 1 |
| 00006B | |
| 00006C | Particular function select register 0 |
| 00006D | Particular function select register 1 |
| 00006E | $\overline{INT_4}$ interrupt control register |
| 00006F | $\overline{INT_3}$ interrupt control register |
| 000070 | A-D interrupt control register |
| 000071 | UART0 trasmit interrupt control register |
| 000072 | UART0 receive interrupt control register |
| 000073 | UART1 trasmit interrupt control register |
| 000074 | UART1 receive interrupt control register |
| 000075 | Timer A0 interrupt control register |
| 000076 | Timer A1 interrupt control register |
| 000077 | Timer A2 interrupt control register |
| 000078 | Timer A3 interrupt control register |
| 000079 | Timer A4 interrupt control register |
| 00007A | Timer B0 interrupt control register |
| 00007B | Timer B1 interrupt control register |
| 00007C | Timer B2 interrupt control register |
| 00007D | $\overline{INT_0}$ interrupt control register |
| 00007E | $\overline{INT_1}$ interrupt control register |
| 00007F | $\overline{INT_2}$ interrupt control register |

Fig. 2  Location of peripheral devices and interrupt control registers

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| Register | Address | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| Port P0 direction register | $(04_{16})$ | | | | $00_{16}$ | | | | |
| Port P1 direction register | $(05_{16})$ | | | | $00_{16}$ | | | | |
| Port P2 direction register | $(08_{16})$ | 0 | X | X | X | 0 | 0 | 0 | 0 |
| Port P3 direction register | $(09_{16})$ | X | X | X | X | 0 | 0 | 0 | 0 |
| Port P4 direction register | $(0C_{16})$ | | | | $00_{16}$ | | | | |
| Port P5 direction register | $(0D_{16})$ | | | | $00_{16}$ | | | | |
| Port P6 direction register | $(10_{16})$ | | | | $00_{16}$ | | | | |
| Port P7 direction register | $(11_{16})$ | | | | $00_{16}$ | | | | |
| Port P8 direction register | $(14_{16})$ | | | | $00_{16}$ | | | | |
| Port P9 direction register | $(15_{16})$ | X | X | 0 | 0 | 0 | 0 | 0 | 0 |
| Port P10 direction register | $(18_{16})$ | | | | $00_{16}$ | | | | |
| Port P11 direction register | $(19_{16})$ | | | | $00_{16}$ | | | | |
| Waveform output mode register | $(1A_{16})$ | | | | $00_{16}$ | | | | |
| Pulse output data register 1 | $(1C_{16})$ | | | | $00_{16}$ | | | | |
| Pulse output data register 0 | $(1D_{16})$ | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 |
| A-D control register 0 | $(1E_{16})$ | 0 | 0 | 0 | 0 | 0 | ? | ? | ? |
| A-D control register 1 | $(1F_{16})$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| UART 0 transmit/receive mode register | $(30_{16})$ | | | | $00_{16}$ | | | | |
| UART 1 transmit/receive mode register | $(38_{16})$ | | | | $00_{16}$ | | | | |
| UART 0 transmit/receive control register 0 | $(34_{16})$ | 0 | X | X | 0 | 1 | 0 | 0 | 0 |
| UART 1 transmit/receive control register 0 | $(3C_{16})$ | 0 | X | X | 0 | 1 | 0 | 0 | 0 |
| UART 0 transmit/receive control register 1 | $(35_{16})$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| UART 1 transmit/receive control register 1 | $(3D_{16})$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Count start register | $(40_{16})$ | | | | $00_{16}$ | | | | |
| One-shot start register | $(42_{16})$ | X | X | X | 0 | 0 | 0 | 0 | 0 |
| Up-down register | $(44_{16})$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Timer A write register | $(45_{16})$ | X | X | X | X | X | 0 | 0 | 0 |
| Timer A0 mode register | $(56_{16})$ | | | | $00_{16}$ | | | | |
| Timer A1 mode register | $(57_{16})$ | | | | $00_{16}$ | | | | |
| Timer A2 mode register | $(58_{16})$ | | | | $00_{16}$ | | | | |
| Timer A3 mode register | $(59_{16})$ | | | | $00_{16}$ | | | | |
| Timer A4 mode register | $(5A_{16})$ | | | | $00_{16}$ | | | | |
| Timer B0 mode register | $(5B_{16})$ | 0 | 0 | 1 | X | 0 | 0 | 0 | 0 |
| Timer B1 mode register | $(5C_{16})$ | 0 | 0 | 1 | X | 0 | 0 | 0 | 0 |
| Timer B2 mode register | $(5D_{16})$ | 0 | 0 | 1 | X | 0 | 0 | 0 | 0 |
| Processor mode register 0 | $(5E_{16})$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Processor mode register 1 | $(5F_{16})$ | | | | $00_{16}$ | | | | |

| Register | Address | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| Watchdog timer | $(60_{16})$ | | | | $FFF_{16}$ | | | | |
| Watchdog timer frequency select register | $(61_{16})$ | X | X | X | X | X | X | 0 | 0 |
| Chip select control register | $(62_{16})$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Chip select area register | $(63_{16})$ | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 |
| Comparator function select register | $(64_{16})$ | | | | $00_{16}$ | | | | |
| Comparator result register | $(66_{16})$ | | | | $00_{16}$ | | | | |
| Flash memory control register | $(67_{16})$ | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D-A register 0 | $(68_{16})$ | | | | $00_{16}$ | | | | |
| D-A register 1 | $(6A_{16})$ | | | | $00_{16}$ | | | | |
| Particular function select register 0 | $(6C_{16})$ | | | | $00_{16}$ | | | | |
| Particular function select register 1 | $(6D_{16})$ | | | | $00_{16}$ | | | | |
| $\overline{INT4}$ interrupt control register | $(6E_{16})$ | X | X | 0 | 0 | 0 | 0 | 0 | 0 |
| $\overline{INT3}$ interrupt control register | $(6F_{16})$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| A-D interrupt control register | $(70_{16})$ | X | X | X | X | ? | 0 | 0 | 0 |
| UART 0 transmit interrupt control register | $(71_{16})$ | X | X | X | X | 0 | 0 | 0 | 0 |
| UART 0 receive interrupt control register | $(72_{16})$ | X | X | X | X | 0 | 0 | 0 | 0 |
| UART 1 transmit interrupt control register | $(73_{16})$ | X | X | X | X | 0 | 0 | 0 | 0 |
| UART 1 receive interrupt control register | $(74_{16})$ | X | X | X | X | 0 | 0 | 0 | 0 |
| Timer A0 interrupt control register | $(75_{16})$ | X | X | X | X | 0 | 0 | 0 | 0 |
| Timer A1 interrupt control register | $(76_{16})$ | X | X | X | X | 0 | 0 | 0 | 0 |
| Timer A2 interrupt control register | $(77_{16})$ | X | X | X | X | 0 | 0 | 0 | 0 |
| Timer A3 interrupt control register | $(78_{16})$ | X | X | X | X | 0 | 0 | 0 | 0 |
| Timer A4 interrupt control register | $(79_{16})$ | X | X | X | X | 0 | 0 | 0 | 0 |
| Timer B0 interrupt control register | $(7A_{16})$ | X | X | X | X | 0 | 0 | 0 | 0 |
| Timer B1 interrupt control register | $(7B_{16})$ | X | X | X | X | 0 | 0 | 0 | 0 |
| Timer B2 interrupt control register | $(7C_{16})$ | X | X | X | X | 0 | 0 | 0 | 0 |
| $\overline{INT0}$ interrupt control register | $(7D_{16})$ | X | X | 0 | 0 | 0 | 0 | 0 | 0 |
| $\overline{INT1}$ interrupt control register | $(7E_{16})$ | X | X | 0 | 0 | 0 | 0 | 0 | 0 |
| $\overline{INT2}$ interrupt control register | $(7F_{16})$ | X | X | 0 | 0 | 0 | 0 | 0 | 0 |

| Register | Value |
|---|---|
| Processor status register PS | 0 0 0 ? ? 0 0 0 1 ? ? |
| Program bank register PG | $00_{16}$ |
| Program counter PCH | Contents of $FFFF_{16}$ |
| Program counter PCL | Contents of $FFFE_{16}$ |
| Direct page register DPR | $0000_{16}$ |
| Data bank register DT | $00_{16}$ |

Contents of other registers and RAM are not initiallzed and must be in-itiallzed by software.

**Note :** Bit 0 of chip select control register (address $62_{16}$) becomes "0" when CNVss pin level is "L"; that bit becomes "1" when the pin level is "H".

Fig. 3  Microcomputer internal registers status after reset

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## MEMORY AREA MODIFICATION FUNCTION

For the M37754FFCGP and the M37754FFCHP, the internal memory's size and address area can be changed by setting bits 2, 3, 4 (memory allocation select bits) of the particular function select register 0 (see figure 5). Figure 4 shows the memory map when changing the internal memory area.
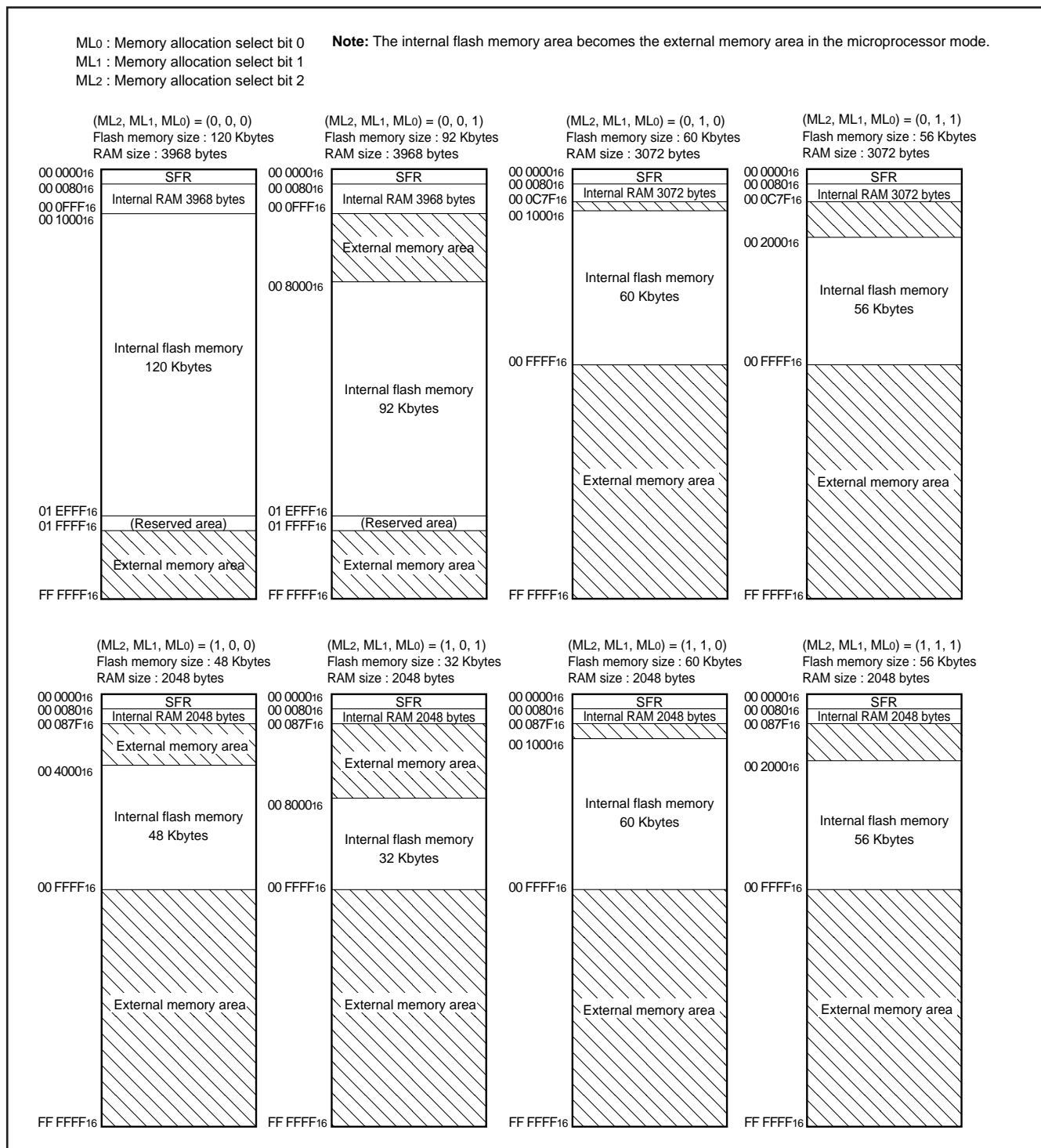


Fig. 4  Memory allocation (Internal memory area modification by memory allocation select bits)
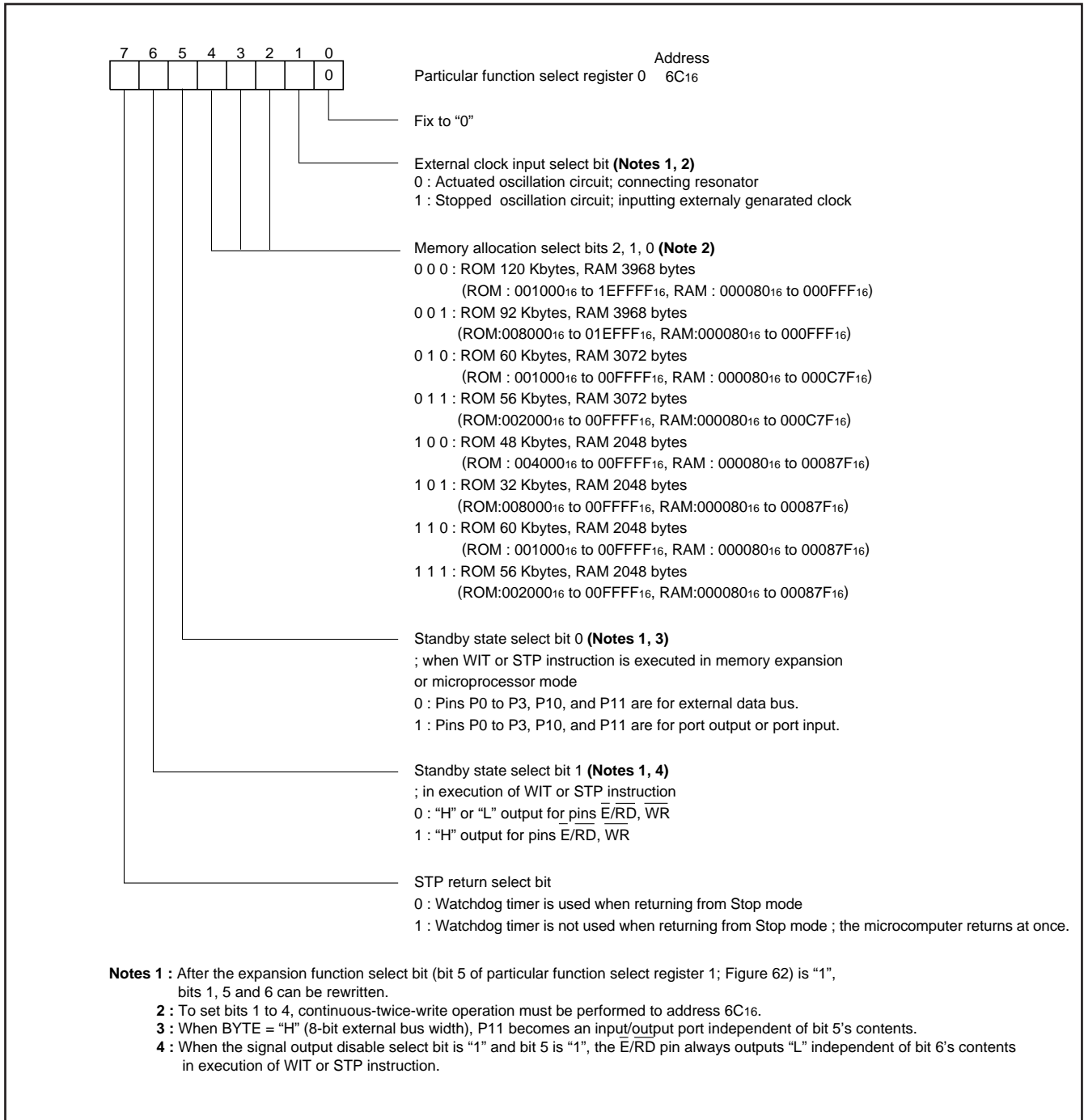
SHINGLE-CHIP 16-BIT CMOS MICROCOMPUTER FLASH MEMORY VERSION

```
  7 6 5 4 3 2 1 0
 ┌─┬─┬─┬─┬─┬─┬─┬─┐                                          Address
 └─┴─┴─┴─┴─┴─┴─┴0┘     Particular function select register 0    6C₁₆
```

Fix to "0"

**External clock input select bit (Notes 1, 2)**
0 : Actuated oscillation circuit; connecting resonator
1 : Stopped oscillation circuit; inputting externaly genarated clock

**Memory allocation select bits 2, 1, 0 (Note 2)**
0 0 0 : ROM 120 Kbytes, RAM 3968 bytes
    (ROM : 001000₁₆ to 1EFFFF₁₆, RAM : 000080₁₆ to 000FFF₁₆)
0 0 1 : ROM 92 Kbytes, RAM 3968 bytes
    (ROM:008000₁₆ to 01EFFF₁₆, RAM:000080₁₆ to 000FFF₁₆)
0 1 0 : ROM 60 Kbytes, RAM 3072 bytes
    (ROM : 001000₁₆ to 00FFFF₁₆, RAM : 000080₁₆ to 000C7F₁₆)
0 1 1 : ROM 56 Kbytes, RAM 3072 bytes
    (ROM:002000₁₆ to 00FFFF₁₆, RAM:000080₁₆ to 000C7F₁₆)
1 0 0 : ROM 48 Kbytes, RAM 2048 bytes
    (ROM : 004000₁₆ to 00FFFF₁₆, RAM : 000080₁₆ to 00087F₁₆)
1 0 1 : ROM 32 Kbytes, RAM 2048 bytes
    (ROM:008000₁₆ to 00FFFF₁₆, RAM:000080₁₆ to 00087F₁₆)
1 1 0 : ROM 60 Kbytes, RAM 2048 bytes
    (ROM : 001000₁₆ to 00FFFF₁₆, RAM : 000080₁₆ to 00087F₁₆)
1 1 1 : ROM 56 Kbytes, RAM 2048 bytes
    (ROM:002000₁₆ to 00FFFF₁₆, RAM:000080₁₆ to 00087F₁₆)

**Standby state select bit 0 (Notes 1, 3)**
; when WIT or STP instruction is executed in memory expansion
or microprocessor mode
0 : Pins P0 to P3, P10, and P11 are for external data bus.
1 : Pins P0 to P3, P10, and P11 are for port output or port input.

**Standby state select bit 1 (Notes 1, 4)**
; in execution of WIT or STP instruction
0 : "H" or "L" output for pins $\overline{E/RD}$, $\overline{WR}$
1 : "H" output for pins $\overline{E/RD}$, $\overline{WR}$

**STP return select bit**
0 : Watchdog timer is used when returning from Stop mode
1 : Watchdog timer is not used when returning from Stop mode ; the microcomputer returns at once.

**Notes 1 :** After the expansion function select bit (bit 5 of particular function select register 1; Figure 62) is "1",
bits 1, 5 and 6 can be rewritten.
   **2 :** To set bits 1 to 4, continuous-twice-write operation must be performed to address 6C₁₆.
   **3 :** When BYTE = "H" (8-bit external bus width), P11 becomes an input/output port independent of bit 5's contents.
   **4 :** When the signal output disable select bit is "1" and bit 5 is "1", the $\overline{E/RD}$ pin always outputs "L" independent of bit 6's contents
in execution of WIT or STP instruction.

Fig. 5 Particular function select register 0 bit configuration

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## FLASH MEMORY MODE

The M37754FFCGP and the M37754FFCHP have the flash memory mode in addition to the normal operation mode (microcomputer mode). The user can use this mode to perform read, program, and erase operations for the internal flash memory.

The M37754FFCGP and the M37754FFCHP have three modes the user can choose: the parallel input/output and serial input/output mode, where the flash memory is handled by using the external programmer, and the CPU reprogramming mode, where the flash memory is handled by the central processing unit (CPU). The following explains these modes.

## Flash memory mode 1 (parallel I/O mode)

The parallel I/O mode can be selected by connecting wires as shown in Figures 6, 7 and supplying power to the $V_{CC}$ and $V_{PP}$ pins. In this mode, the M37754FFCGP and the M37754FFCHP operate as an equivalent of MITSUBISHI's CMOS flash memory M5M28F101. However, because the M37754FFCGP and the M37754FFCHP's internal memory has a capacity of 120 Kbytes, programming is available for addresses $0100_{16}$ to $1EFFF_{16}$, and make sure that the data in addresses $0000_{16}$ to $00FFF_{16}$ and addresses $1F000_{16}$ to $1FFFF_{16}$ are $FF_{16}$. Note also that the M37754FFCGP and the M37754FFCHP does not contain a facility to read out a device identification code by applying a high voltage to address input (A9). Be careful not to erratically set program conditions when using a general-purpose PROM programmer.

Table 1 shows the pin assignments when operating in the parallel input/output mode.

**Table 1. Pin assignments of M37754FFCGP and  M37754FFCHP when operating in the parallel input/output mode**

|  | M37754FFCGP/CHP | M5M28F101 |
|---|---|---|
| $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| $V_{PP}$ | $CNV_{SS}$ | $V_{PP}$ |
| $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| Address input | Ports P0, P1, P5$_4$ | $A_0$–$A_{16}$ |
| Data I/O | Port P10 | $D_0$–$D_7$ |
| $\overline{CE}$ | P5$_2$ | $\overline{CE}$ |
| $\overline{OE}$ | P5$_1$ | $\overline{OE}$ |
| $\overline{WE}$ | P5$_0$ | $\overline{WE}$ |

## Functional outline (Parallel input/output mode)

In the parallel input/output mode, the M37754FFCGP and the M37754FFCHP allows the user to choose an operation mode between the read-only mode and the read/write mode (software command control mode) depending on the voltage applied to the $V_{PP}$ pin. When $V_{PP}$ = $V_{PPL}$, the read-only mode is selected, and the user can choose one of three states (e.g., read, output disable, or standby) depending on inputs to the $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ pins. When $V_{PP}$ = $V_{PPH}$, the read/write mode is selected, and the user can choose one of four states (e.g., read, output disable, standby, or write) depending on inputs to the $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ pins. Table 2 shows assignment states of control input and each state.

### Read

The microcomputer enters the read state by driving the $\overline{CE}$, and $\overline{OE}$ pins low and the $\overline{WE}$ pin high; and the contents of memory corresponding to the address to be input to address input pins ($A_0$–$A_{16}$). are output to the data input/output pins ($D_0$–$D_7$).

### Output disable

The microcomputer enters the output disable state by driving the $\overline{CE}$ pin low and the $\overline{WE}$ and $\overline{OE}$ pins high; and the data input/output pins enter the floating state.

### Standby

The microcomputer enters the standby state by driving the $\overline{CE}$ pin high. The M37754FFCGP and the M37754FFCHP are placed in a power-down state consuming only a minimal supply current. At this time, the data input/output pins enter the floating state.

### Write

The microcomputer enters the write state by driving the $V_{PP}$ pin high ($V_{PP}$ = $V_{PPH}$) and then the $\overline{WE}$ pin low when the $\overline{CE}$ pin is low and the $\overline{OE}$ pin is high. In this state, software commands can be input from the data input/output pins, and the user can choose program or erase operation depending on the contents of this software command.

**Table 2.  Assignment sates of control input and each state**

| Mode | State | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $V_{PP}$ | Data I/O |
|---|---|---|---|---|---|---|
| Read-only | Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{PPL}$ | Output |
| | Output disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{PPL}$ | Floating |
| | Standby | $V_{IH}$ | $\times$ | $\times$ | $V_{PPL}$ | Floating |
| Read/Write | Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{PPH}$ | Output |
| | Output disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{PPH}$ | Floating |
| | Standby | $V_{IH}$ | $\times$ | $\times$ | $V_{PPH}$ | Floating |
| | Write | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{PPH}$ | Input |

**Note:** $\times$ can be $V_{IL}$ or $V_{IH}$.

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PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.



∗ : Connect to the ceramic oscillation circuit.
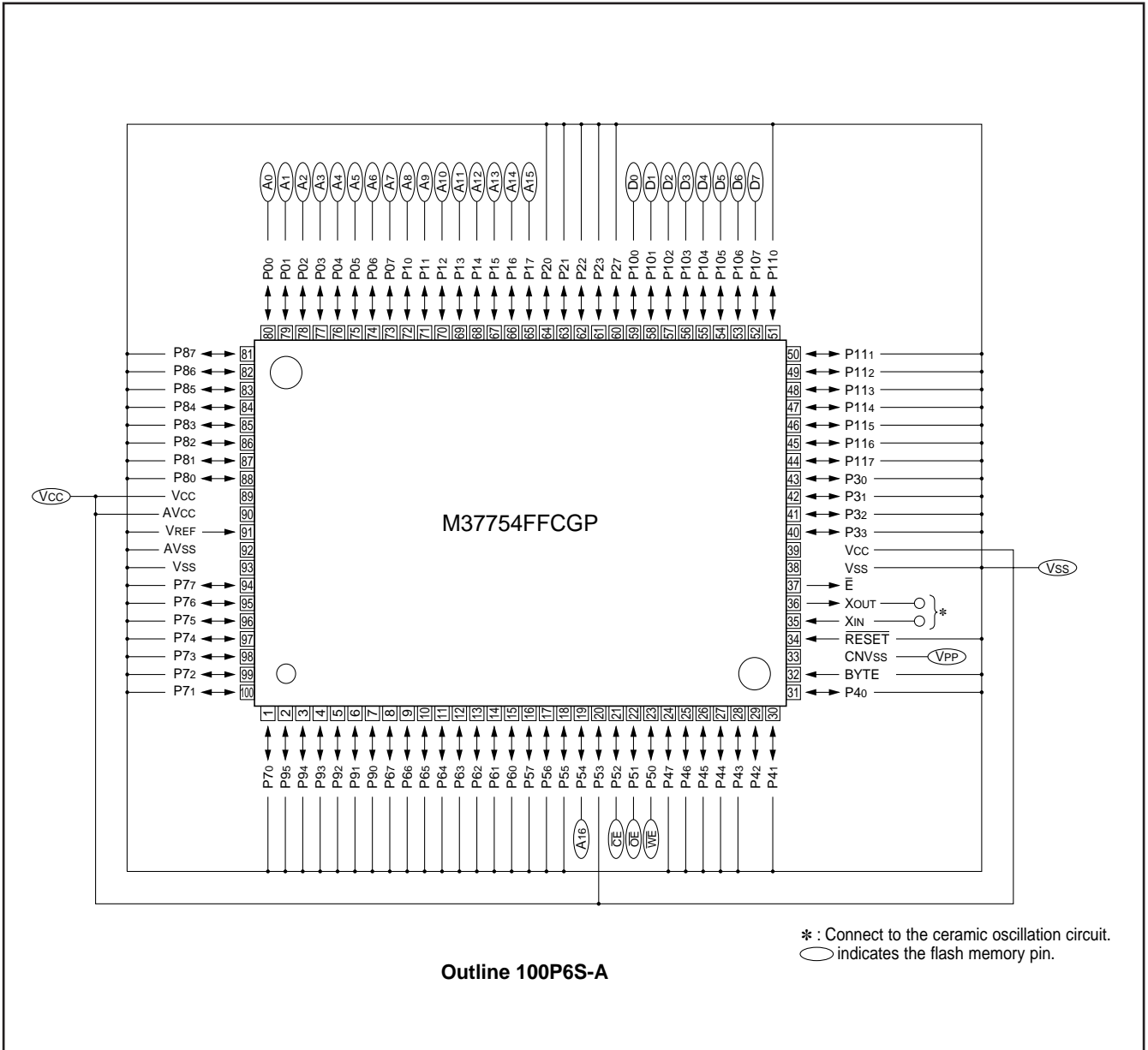⬭ indicates the flash memory pin.

**Outline 100P6S-A**

Fig. 6  Pin connection of M37754FFCGP when operating in parallel input/output mode

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Notice: This is not a final specification.
Some parametric limits are subject to change.



**Outline 100P6Q-A**

∗ : Connect to the ceramic oscillation circuit.
⬭ indicates the flash memory pin.
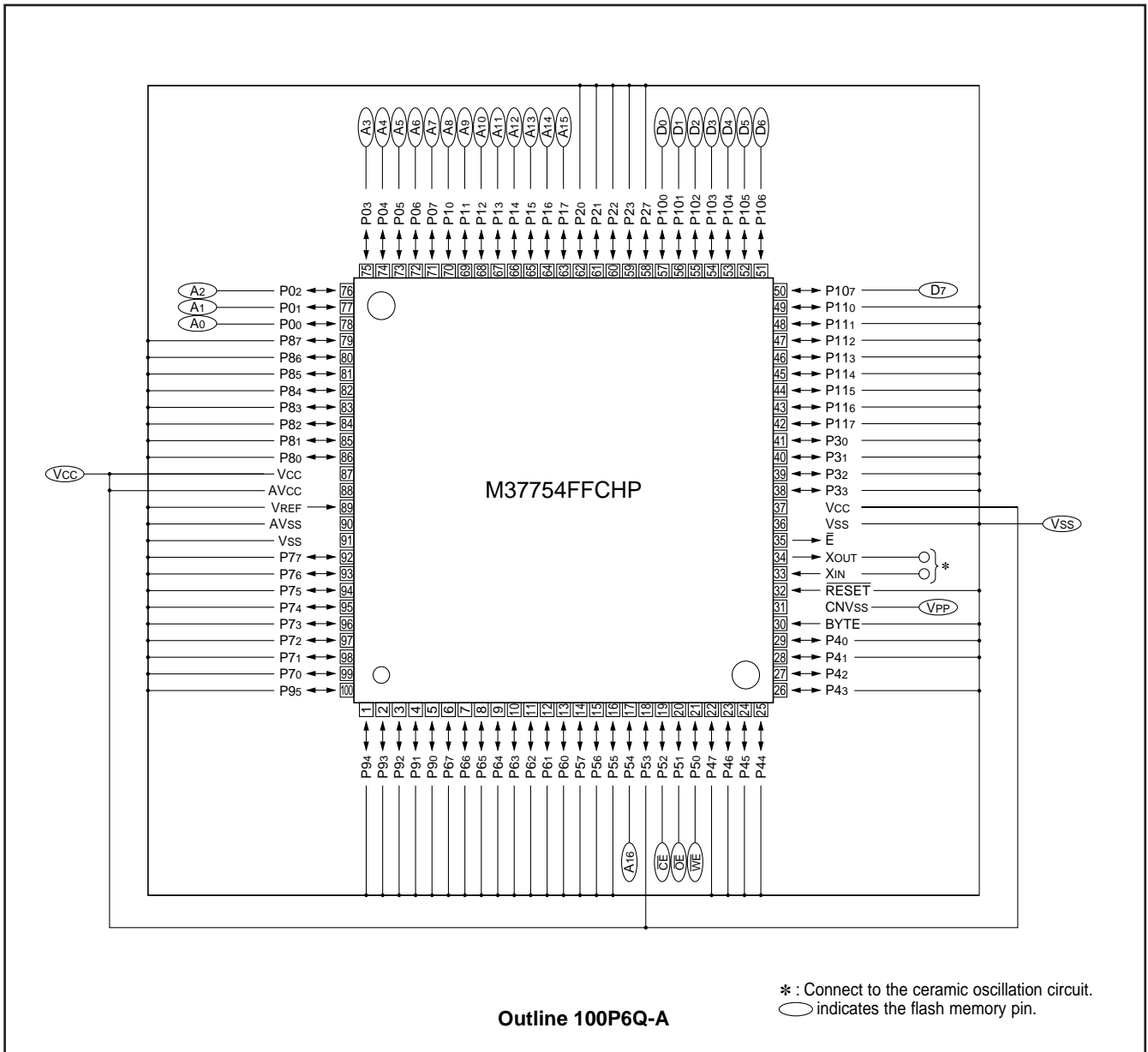
Fig. 7 Pin connection of M37754FFCHP when operating in parallel input/output mode

## Read-only mode

The microcomputer enters the read-only mode by applying $V_{PPL}$ to the $V_{PP}$ pin. In this mode, the user can input the address of a memory location to be read and the control signals at the timing shown in Figure 8, and the M37754FFCGP and the M37754FFCHP will output the contents of the user's specified address from data I/O pin to the external. In this mode, the user cannot perform any operation other than read.
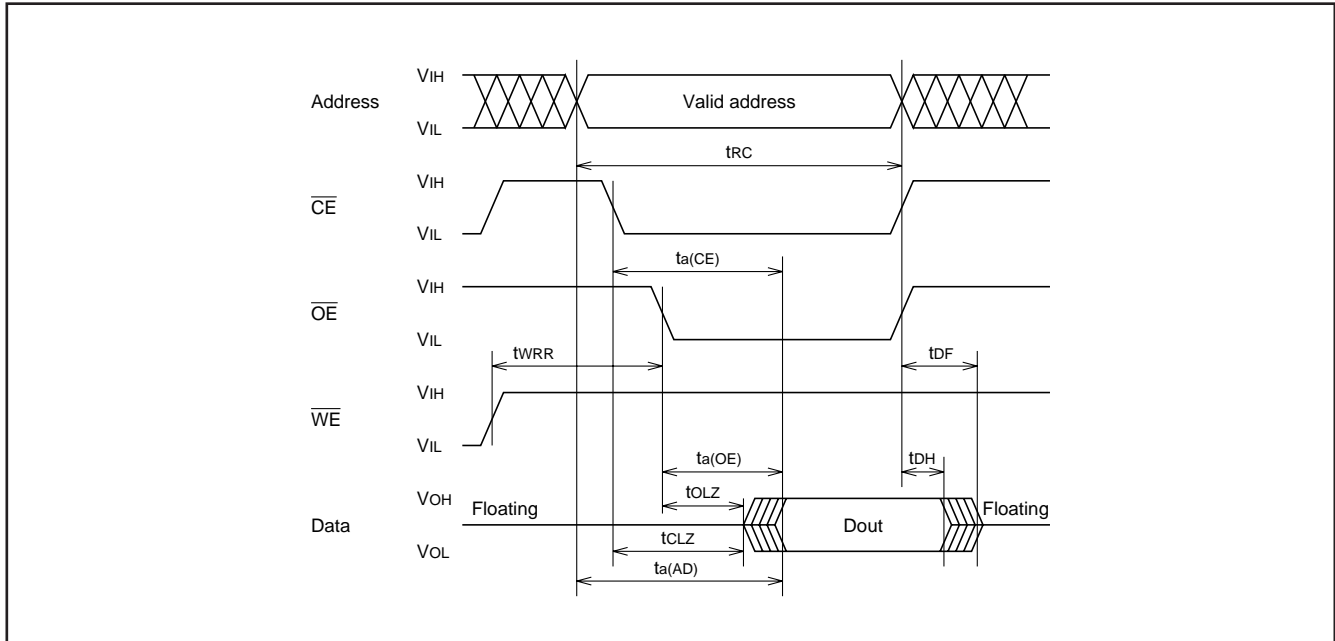


Fig. 8  Read timing

## Read/Write mode

The microcomputer enters the read/write mode by applying $V_{PPH}$ to the $V_{PP}$ pin. In this mode, the user must first input a software command to choose the operation (e. g., read, program, or erase) to be performed on the flash memory (this is called the first cycle), and then input the information necessary for execution of the command (e.g, address and data) and control signals (this is called the second cycle). When this is done, the M37754FFCGP and the M37754FFCHP execute the specified operation.

Table 3 shows the software commands and the input/output information in the first and the second cycles. The input address is latched internally at the falling edge of the $\overline{WE}$ input; software commands and other input data are latched internally at the rising edge of the $\overline{WE}$ input.

The following explains each software command. Refer to Figures 9 to 11 for details about the signal input/output timings.

**Table 3.  Software command (Parallel input/output mode)**

| Symbol | First cycle | | Second cycle | |
|---|---|---|---|---|
| | Address input | Data input | Address input | Data I/O |
| Read | $\times$ | $00_{16}$ | Read address | Read data (Output) |
| Program | $\times$ | $40_{16}$ | Program address | Program data (Input) |
| Program verify | $\times$ | $C0_{16}$ | $\times$ | Verify data (Output) |
| Erase | $\times$ | $20_{16}$ | $\times$ | $20_{16}$ (Input) |
| Erase verify | Verify address | $A0_{16}$ | $\times$ | Verify data (Output) |
| Reset | $\times$ | $FF_{16}$ | $\times$ | $FF_{16}$ (Input) |
| Device identification | $\times$ | $90_{16}$ | ADI | DDI (Output) |

**Note:** ADI = Device identification address : manufacturer's code $00000_{16}$, device code $000001_{16}$
DDI = Device identification data : manufacturer's code $1C_{16}$, device code $D0_{16}$
X can be $V_{IL}$ or $V_{IH}$.

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Notice: This is not a final specification.
Some parametric limits are subject to change.

## Read command

The microcomputer enters the read mode by inputting command code "00₁₆" in the first cycle. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. When the address of a memory location to be read is input in the second cycle, with control signals input at the timing shown in Figure 9, the M37754FFCGP and the M37754FFCHP output the contents of the specified address from the data I/O pins to the external.

The read mode is retained until any other command is latched into the command latch. Consequently, once the M37754FFCGP and the M37754FFCHP enter the read mode, the user can read out the successive memory contents simply by changing the input address and executing the second cycle only. Any command other than the read command must be input beginning from its command code over again each time the user execute it. The contents of the command latch immediately after power-on is 00₁₆.
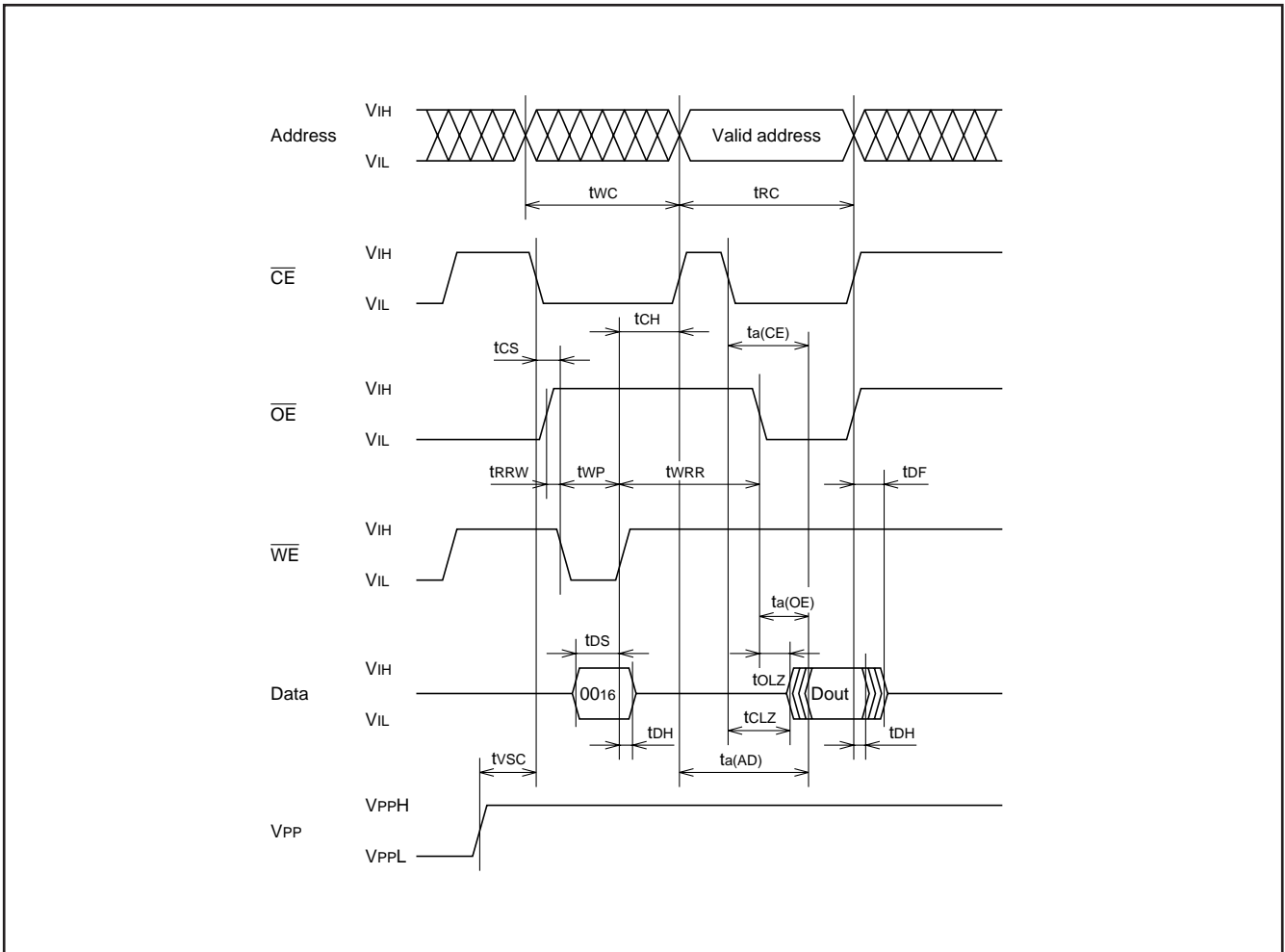


Fig. 9 Timings during reading

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## Program command

The microcomputer enters the program mode by inputting command code "$40_{16}$" in the first cycle. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. When the address which indicates a program location and data are input in the second cycle, the M37754FFCGP and the M37754FFCHP internally latch the address at the falling edge of the $\overline{WE}$ input and the data at the rising edge of the $\overline{WE}$ input. The M37754FFCGP and the M37754FFCHP start programming at the rising edge of the $\overline{WE}$ input in the second cycle and finishes programming within 10 $\mu$s as measured by its internal timer. Programming is performed in units of bytes.

**Note:** A programming operation is not completed by executing the program command once. Always be sure to execute a program verify command after executing the program command. When the failure is found in this verification, the user must repeatedly execute the program command until the pass. Refer to Figure 12 for the programming flowchart.

## Program verify command

The microcomputer enters the program verify mode by inputting command code "$C0_{16}$" in the first cycle. This command is used to verify the programmed data after executing the program command. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. When control signals are input in the second cycle at the timing shown in Figure 10, the M37754FFCGP and the M37754FFCHP output the programmed address's contents to the external. Since the address is internally latched when the program command is executed, there is no need to input it in the second cycle.
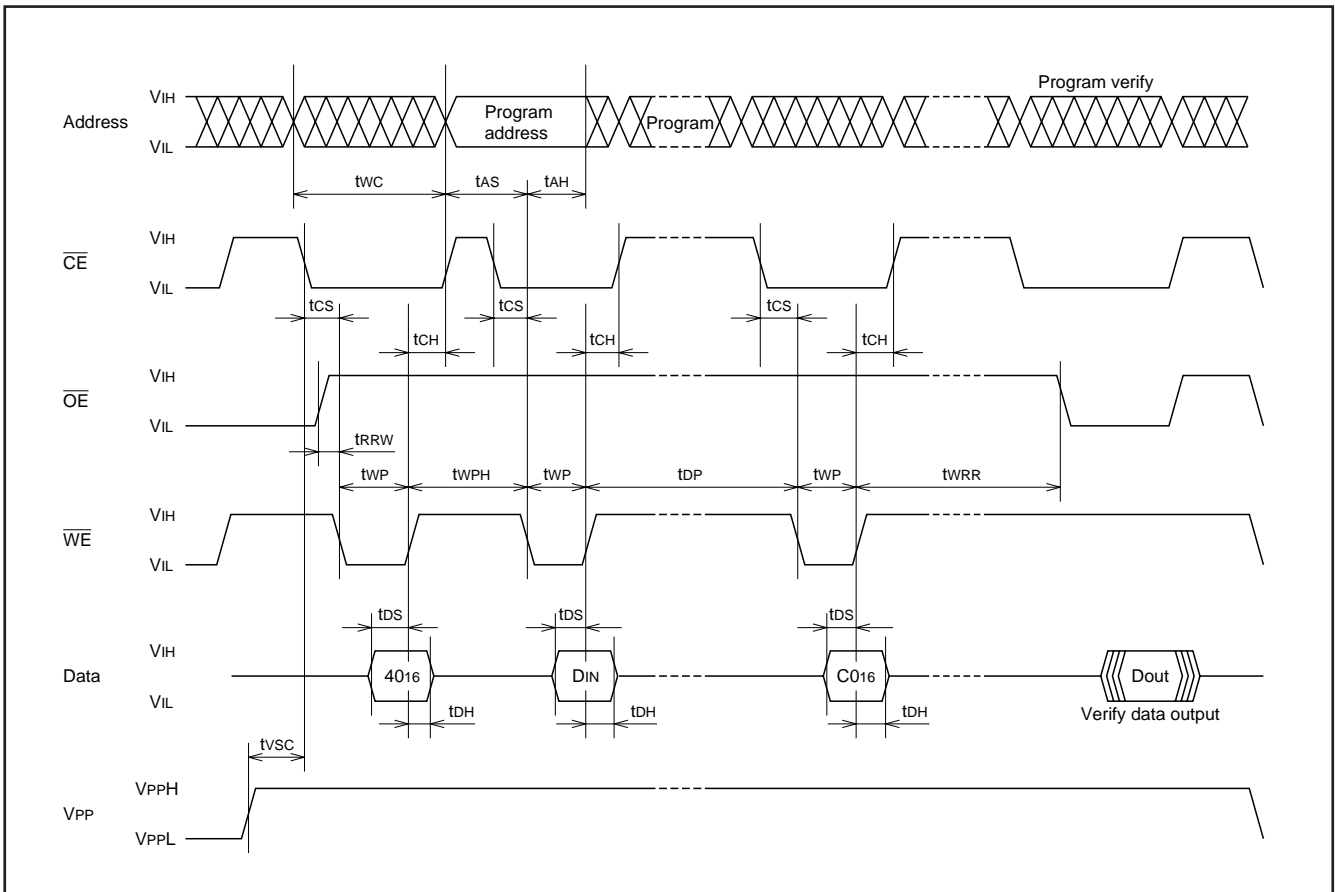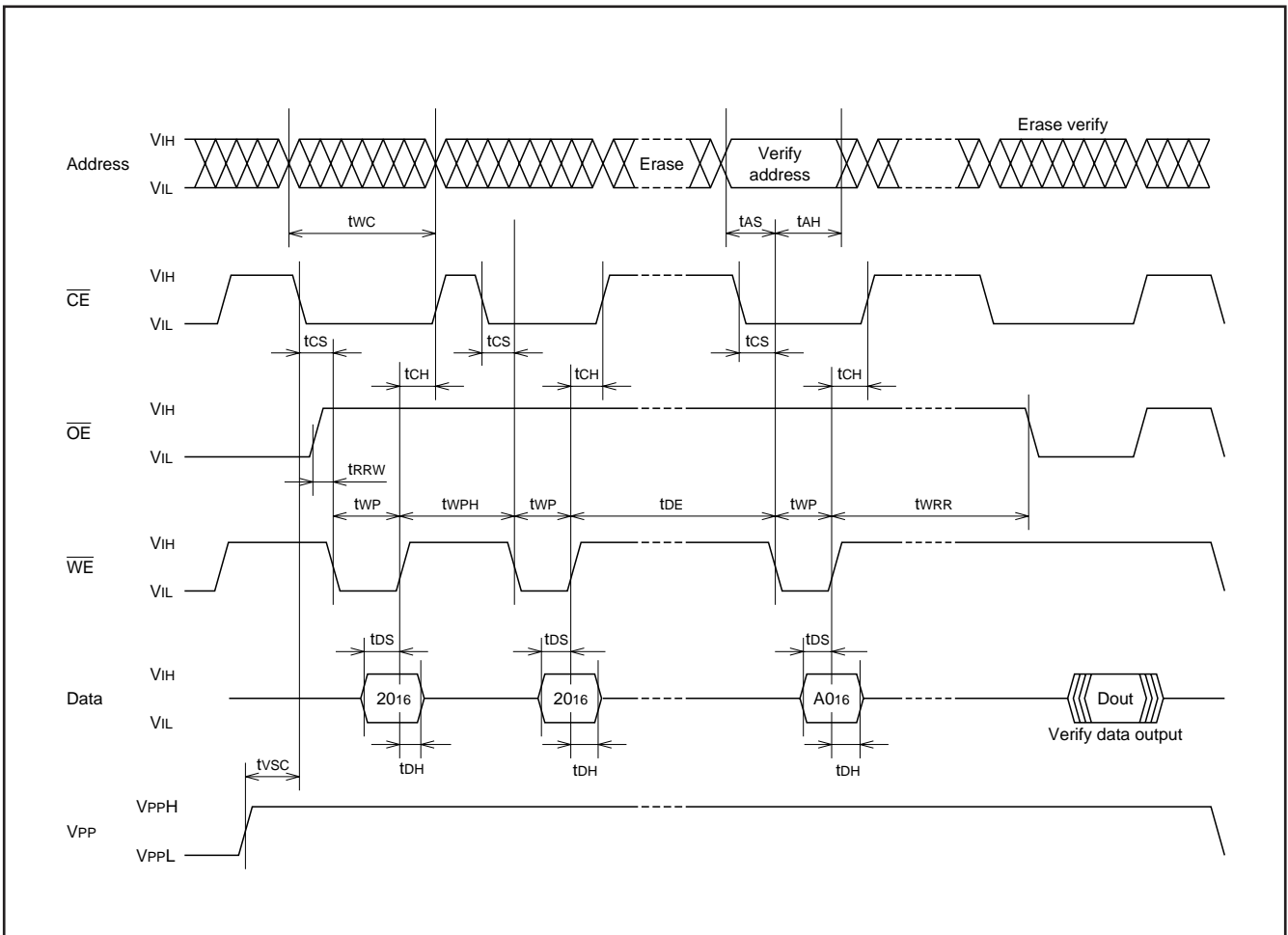


Fig. 10 Input/output timings during programming (Verify data is output at the same timing as for read.)

## Erase command

The erase command is executed by inputting command code $20_{16}$ in the first cycle and command code $20_{16}$ again in the second cycle. The command code is latched into the internal command latch at the rising edges of the $\overline{WE}$ input in the first cycle and in the second cycle, respectively. The erase operation is initiated at the rising edge of the $\overline{WE}$ input in the second cycle, and the memory contents are collectively erased within 9.5 ms as measured by the internal timer. Note that data $00_{16}$ must be written to all memory locations before executing the erase command.

**Note:** An erase operation is not completed by executing the erase command once. Always be sure to execute an erase verify command after executing the erase command. When the failure is found in this verification, the user must repeatedly execute the erase command until the pass. Refer to Figure 12 for the erase flowchart.

## Erase verify command

The user must verify the contents of all addresses after completing the erase command. The microcomputer enters the erase verify mode by inputting the verify address and command code $A0_{16}$ in the first cycle. The address is internally latched at the falling edge of the $\overline{WE}$ input, and the command code is internally latched at the rising edge of the $\overline{WE}$ input. When control signals are input in the second cycle at the timing shown in Figure 11, the M37754FFCGP and the M37754FFCHP output the contents of the specified address to the external.

**Note:** If any memory location where the contents have not been erased is found in the erase verify operation, execute the operation of "erase → erase verify" over again. In this case, however, the user does not need to write data $00_{16}$ to memory locations before erasing.



Fig. 11 Input/output timings during erasing (Verify data is output at the same timing as for read.)

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

## Reset command

The reset command provides a means of stopping execution of the erase or program command safely. If the user inputs command code $FF_{16}$ in the second cycle after inputting the erase or program command in the first cycle and again input command code $FF_{16}$ in the third cycle, the erase or program command is disabled (i.e., reset), and the M37754FFCGP and the M37754FFCHP are placed in the read mode. If the reset command is executed, the contents of the memory does not change.

## Device identification code command

By inputting command code $90_{16}$ in the first cycle, the user can read out the device identification code. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. At this time, the user can read out manufacture's code $1C_{16}$ (i.e., MITSUBISHI) by inputting $0000_{16}$ to the address input pins in the second cycle; the user can read out device code $D0_{16}$ (i. e., 1M-bit flash memory) by inputting $0001_{16}$.

These command and data codes are input/output at the same timing as for read.

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**Program**

START

$V_{CC} = 5$ V, $V_{PP} = V_{PPH}$

ADRS = first location

X = 0

WRITE PROGRAM COMMAND — $40_{16}$

WRITE PROGRAM DATA — $D_{IN}$

DURATION = 10 µs

X = X + 1

WRITE PROGRAM-VERIFY COMMAND — $C0_{16}$

DURATION = 6 µs

X = 25 ? — YES

NO → VERIFY BYTE ? — PASS → VERIFY BYTE ? — FAIL → DEVICE FAILED

FAIL

PASS → LAST ADRS ? — NO → INC ADRS

LAST ADRS ? — YES

WRITE READ COMMAND — $00_{16}$

$V_{PP} = V_{PPL}$

DEVICE PASSED

**Erase**

START

$V_{CC} = 5$ V, $V_{PP} = V_{PPH}$

ALL BYTES = $00_{16}$ ? — YES

NO → PROGRAM ALL BYTES = $00_{16}$

ADRS = first location

X = 0

WRITE ERASE COMMAND — $20_{16}$

WRITE ERASE COMMAND — $20_{16}$

DURATION = 9.5 ms

X = X + 1

WRITE ERASE-VERIFY COMMAND — $A0_{16}$

DURATION = 6 µs

X = 1000 ? — YES

NO → VERIFY BYTE ? — PASS → VERIFY BYTE ? — FAIL → DEVICE FAILED

FAIL

PASS → LAST ADRS ? — NO → INC ADRS

LAST ADRS ? — YES

WRITE READ COMMAND — $00_{16}$

$V_{PP} = V_{PPL}$

DEVICE PASSED

Fig. 12  Programming/Erasing algorithm flow chart

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.

## DC ELECTRICAL CHARACTERISTICS ($T_a$ = 25 °C, $V_{CC}$ = 5 V ± 10 %, unless otherwise noted)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SB1}$ | $V_{CC}$ supply current (at standby) | $V_{CC}$ = 5.5 V, $\overline{CE}$ = $V_{IH}$ | | | 1 | mA |
| $I_{SB2}$ | | $V_{CC}$ = 5.5 V, $\overline{CE}$ = $V_{CC}$ ± 0.2 V | | | 100 | μA |
| $I_{CC1}$ | $V_{CC}$ supply current (at read) | $V_{CC}$ = 5.5 V, $\overline{CE}$ = $V_{IL}$, $t_{RC}$ = 150 ns, $I_{OUT}$ = 0 mA | | | 30 | mA |
| $I_{CC2}$ | $V_{CC}$ supply current (at program) | $V_{PP}$ = $V_{PPH}$ | | | 30 | mA |
| $I_{CC3}$ | $V_{CC}$ supply current (at erase) | $V_{PP}$ = $V_{PPH}$ | | | 30 | mA |
| $I_{PP1}$ | $V_{PP}$ supply current (at read) | $0 \leq V_{PP} \leq V_{CC}$ | | | 10 | μA |
| | | $V_{CC} < V_{PP} \leq V_{CC} + 1.0$ V | | | 100 | μA |
| | | $V_{PP}$ = $V_{PPH}$ | | | 100 | μA |
| $I_{PP2}$ | $V_{PP}$ supply current (at program) | $V_{PP}$ = $V_{PPH}$ | | | 30 | mA |
| $I_{PP3}$ | $V_{PP}$ supply current (at erase) | $V_{PP}$ = $V_{PPH}$ | | | 30 | mA |
| $V_{PPL}$ | $V_{PP}$ supply voltage (read only) | | $V_{CC}$ | | $V_{CC}$ + 1.0 | V |
| $V_{PPH}$ | $V_{PP}$ supply voltage (read/write) | | 11.4 | 12.0 | 12.6 | V |

**Note:** $V_{IH}$, $V_{IL}$, $V_{OH}$, $V_{OL}$, $I_{IH}$, and $I_{IL}$ for the control input, address input, and data input/output pins conform to the standards for microcomputer modes (e.g., memory expansion and microprocessor modes).

## AC ELECTRICAL CHARACTERISTICS ($T_a$ = 25 °C, $V_{CC}$ = 5 V ± 10 %, unless otherwise noted)

### Read-only mode

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{RC}$ | Read cycle time | 150 | | ns |
| $t_{a(AD)}$ | Address access time | | 150 | ns |
| $t_{a(CE)}$ | $\overline{CE}$ access time | | 150 | ns |
| $t_{a(OE)}$ | $\overline{OE}$ access time | | 55 | ns |
| $t_{CLZ}$ | Output enable time (after $\overline{CE}$) | 0 | | ns |
| $t_{OLZ}$ | Output enable time (after $\overline{OE}$) | 0 | | ns |
| $t_{DF}$ | Output floating time (after $\overline{OE}$) | | 35 | ns |
| $t_{DH}$ | Output valid time (after $\overline{CE}$, $\overline{OE}$, address) | 0 | | ns |
| $t_{WRR}$ | Write recovery time (before read) | 6 | | μs |

### Read/Write mode

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{WC}$ | Write cycle time | 150 | | ns |
| $t_{AS}$ | Address set up time | 0 | | ns |
| $t_{AH}$ | Address hold time | 60 | | ns |
| $t_{DS}$ | Data setup time | 50 | | ns |
| $t_{DH}$ | Data hold time | 10 | | ns |
| $t_{WRR}$ | Write recovery time (before read) | 6 | | μs |
| $t_{RRW}$ | Read recovery time (before write) | 0 | | μs |
| $t_{CS}$ | $\overline{CE}$ setup time | 20 | | ns |
| $t_{CH}$ | $\overline{CE}$ hold time | 0 | | ns |
| $t_{WP}$ | Write pulse width | 60 | | ns |
| $t_{WPH}$ | Write pulse waiting time | 20 | | ns |
| $t_{DP}$ | Program time | 10 | | μs |
| $t_{DE}$ | Erase time | 9.5 | | ms |
| $t_{VSC}$ | $V_{PP}$ setup time | 1 | | μs |

**Note :** The read timing in the read/write mode is the same timing as in the read-only mode.

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## Flash memory mode 2 (serial I/O mode)

The M37754FFCGP and the M37754FFCHP have a function to serially input/output the software commands, addresses, and data required for operation on the internal flash memory (e. g., read, program, and erase) using only a few pins. This is called the serial I/O (input/output) mode. This mode can be selected by driving the SDA (serial data input/output), SCLK (serial clock input ), and $\overline{OE}$

pins high after connecting wires as shown in Figures 13, 14 and powering on the $V_{CC}$ pin and then applying $V_{PPH}$ to the $V_{PP}$ pin.

In the serial I/O mode, the user can use seven types of software commands: bank (0, 1) select, read, program, program verify, auto erase, and error check.

Serial input/output is accomplished synchronously with the clock, beginning from the LSB (LSB first).
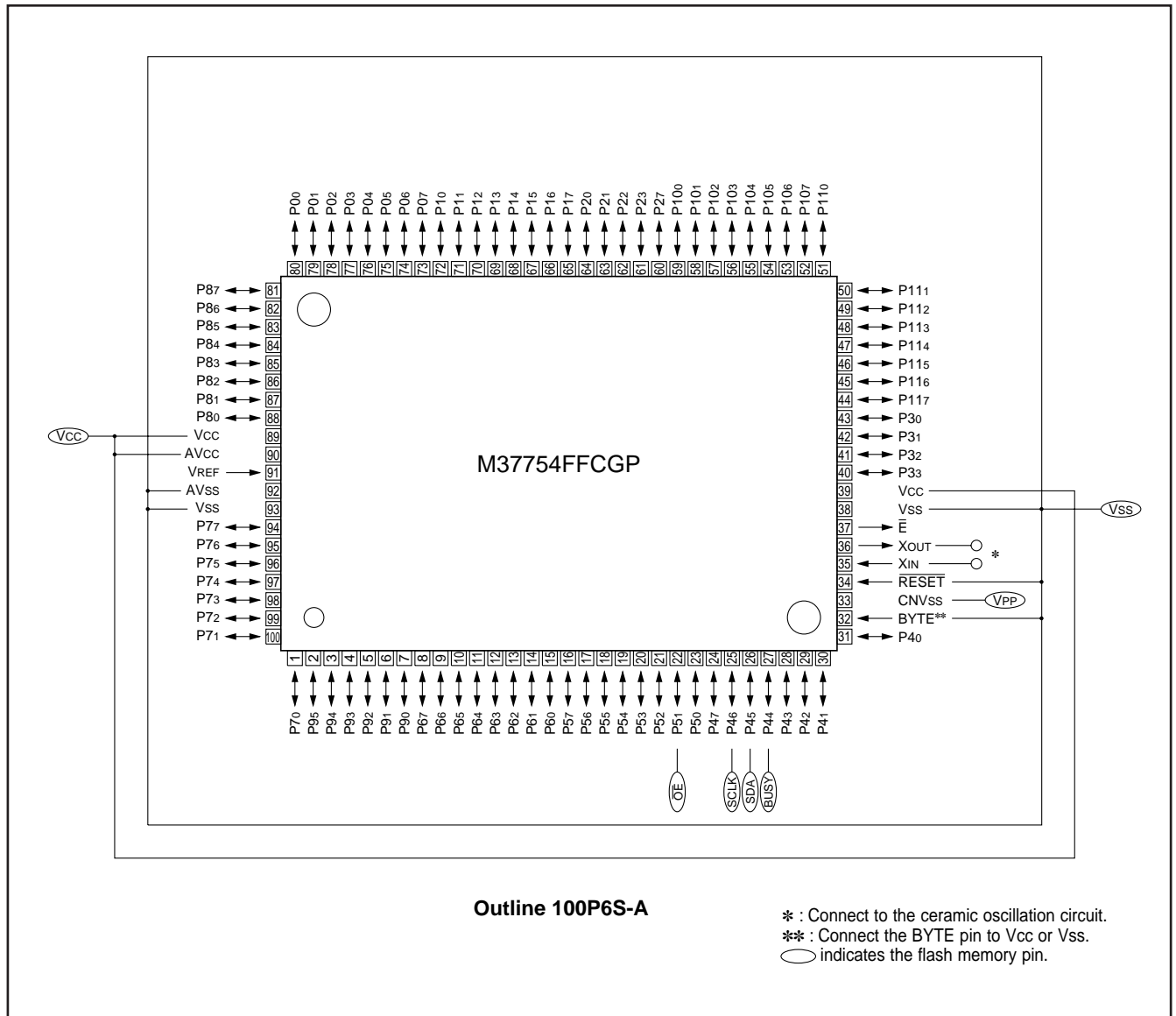


**Outline 100P6S-A**

∗ : Connect to the ceramic oscillation circuit.
∗∗ : Connect the BYTE pin to Vcc or Vss.
⬭ indicates the flash memory pin.

Fig. 13 Pin connection of M37754FFCGP when operating in serial I/O mode

✱ : Connect to the ceramic oscillation circuit.
✱✱ : Connect the BYTE pin to Vcc or Vss.
⬭ indicates the flash memory pin.

**Outline 100P6Q-A**

Fig. 14 Pin connection of M37754FFCHP when operating in serial I/O mode

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PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change.
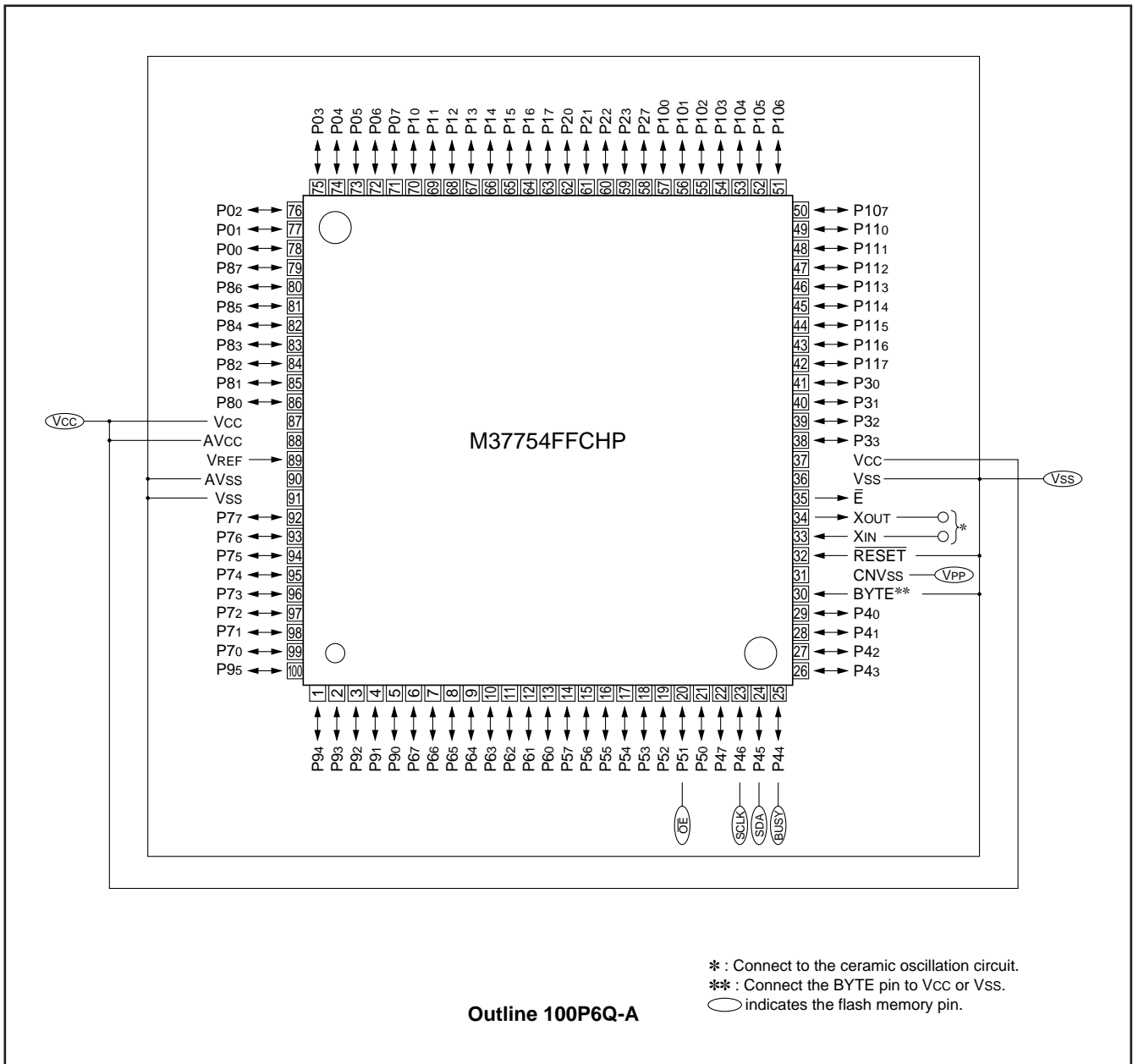
## Functional outline (Serial I/O mode)

In the serial I/O mode, data is transferred synchronously with the clock using serial input/output. The input data is read from the SDA pin into the internal circuit synchronously with the rising edge of the serial clock pulse; the output data is output from the SDA pin synchronously with the falling edge of the serial clock pulse. Data is transferred in units of eight bits.

In the first transfer, the user inputs the command code. This is followed by address input and data input/output according to the contents of the command. Table 4 shows the software commands used in the serial I/O mode. The following explains each software command.

Table 4. Software command (Serial I/O mode)

| Command \ Number of transfers | First command code input | Second | Third | Fourth |
|---|---|---|---|---|
| Bank 0 select | $E0_{16}$ | ———— | ———— | ———— |
| Bank 1 select | $E1_{16}$ | ———— | ———— | ———— |
| Read | $00_{16}$ | Read address L (Input) | Read address H (Input) | Read data (Output) |
| Program | $40_{16}$ | Program address L (Input) | Program address H (Input) | Program data (Input) |
| Program verify | $C0_{16}$ | Verify data (Output) | ———— | ———— |
| Auto erase | $30_{16}$ | $30_{16}$ (Input) | ———— | ———— |
| Error check | $80_{16}$ | Error code (Output) | ———— | ———— |

## Bank select command

This is the command which specifies the bank of the flash memory, which is to be read/programmed, before executing the read command or the program command (and the program verify command). There are the bank 0 select command (command code "$E0_{16}$"), which selects bank 0 (addresses $00000_{16}$ to $0FFFF_{16}$), and the bank 1 select command (command code "$E1_{16}$"), which selects bank 1 (addresses $10000_{16}$ to $1FFFF_{16}$).

When any bank select command is input once, specified bank is valid until the next bank select command is input. Accordingly, when the read command or the program command (and the program verify command) is executed to plural bytes in the same bank, if any bank select command is input first, it is unnecessary to input the bank select command again for the following bytes. When selecting the serial I/O mode (before bank command input), bank 0 is selected.

**Note:** Bank select command does not affect the auto erase command, that is to say, when executing the auto erase command, all flash memory is erased collectively regardless of specified bank.

And in the same way, the bank select command does not affect the error check command.
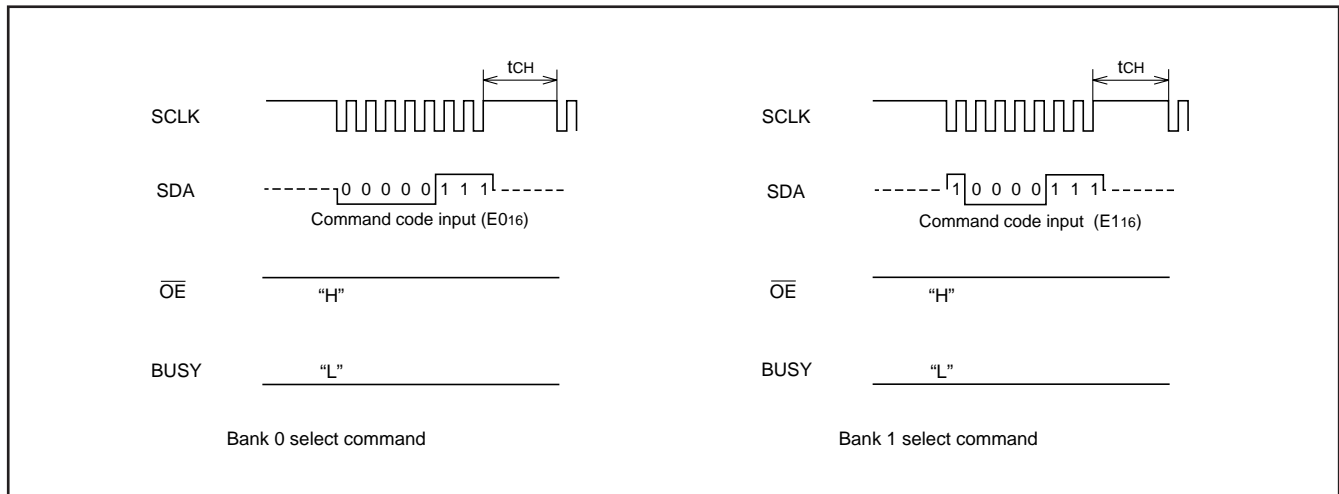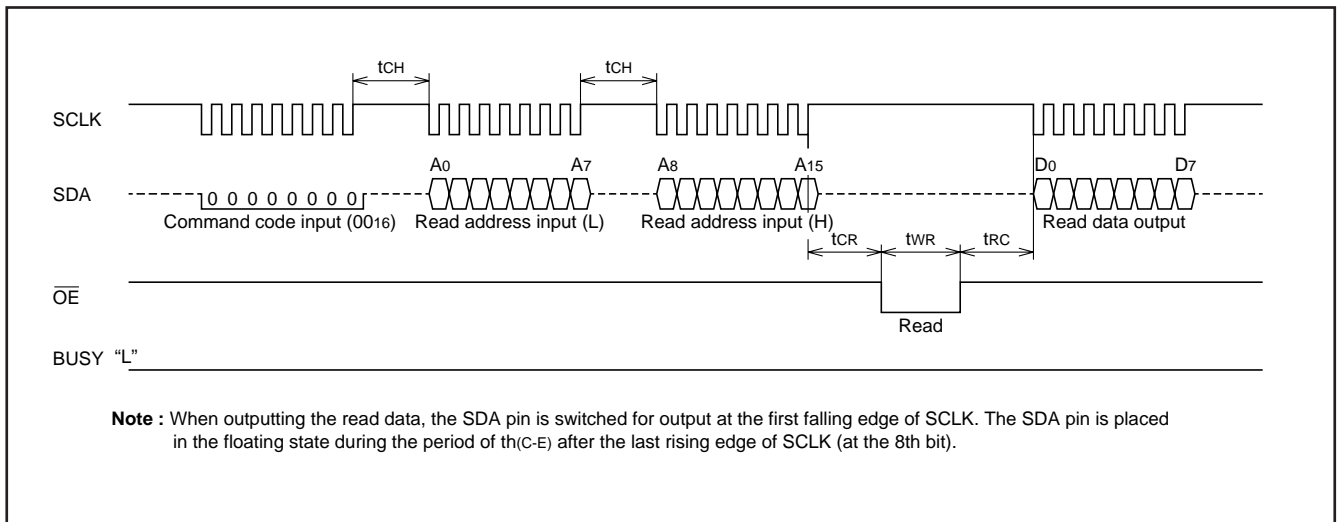


Fig. 15 Timings during bank select

## Read command

Input command code $00_{16}$ in the first transfer. Proceed and input the low-order 8 bits and the high-order 8 bits of the address and pull the $\overline{OE}$ pin low. When this is done, the M37754FFCGP and the M37754FFCHP read out the contents of the specified address, and then latch it into the internal data latch. When the $\overline{OE}$ pin is released back high and serial clock is input to the SCLK pin, the read data that has been latched into the data latch is serially output from the SDA pin.



**Note :** When outputting the read data, the SDA pin is switched for output at the first falling edge of SCLK. The SDA pin is placed in the floating state during the period of $t_{h(C-E)}$ after the last rising edge of SCLK (at the 8th bit).

Fig. 16  Timings during reading

## Program command

Input command code $40_{16}$ in the first transfer. Proceed and input the low-order 8 bits and the high-order 8 bits of the address and then program data. Programming is initiated at the last rising edge of the serial clock during program data transfer. The BUSY pin is driven high during program operation. Programming is completed within 10 $\mu$s as measured by the built-in timer, and the BUSY pin is pulled low.

**Note :** A programming operation is not completed by executing the program command once. Always be sure to execute a program verify command after executing the program command. In the case of failure in the verification, the user must repeatedly execute the program command until the pass in the verification. Refer to Figure 12 for the programming flowchart.
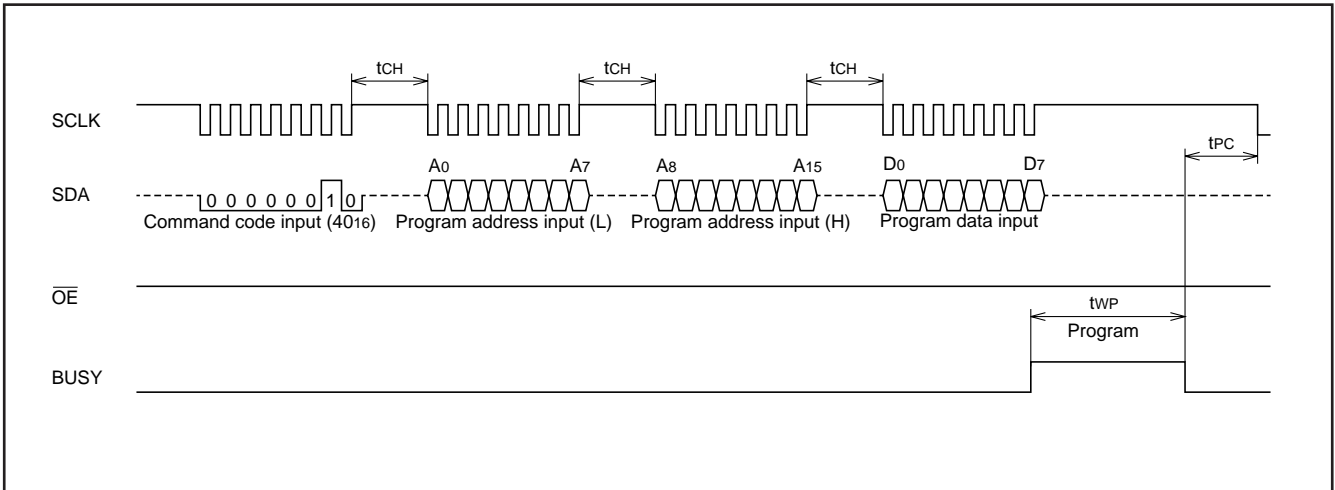


**Fig. 17  Timings during programming**

## Program verify command

Input command code $C0_{16}$ in the first transfer. Proceed and drive the $\overline{OE}$ pin low. When this is done, the M37754FFCGP and the M37754FFCHP verify-read the programmed address's contents, and then latch it into the internal data latch. When the $\overline{OE}$ pin is released back high and serial clock is input to the SCLK pin, the verify data that has been latched into the data latch is serially output from the SDA pin.
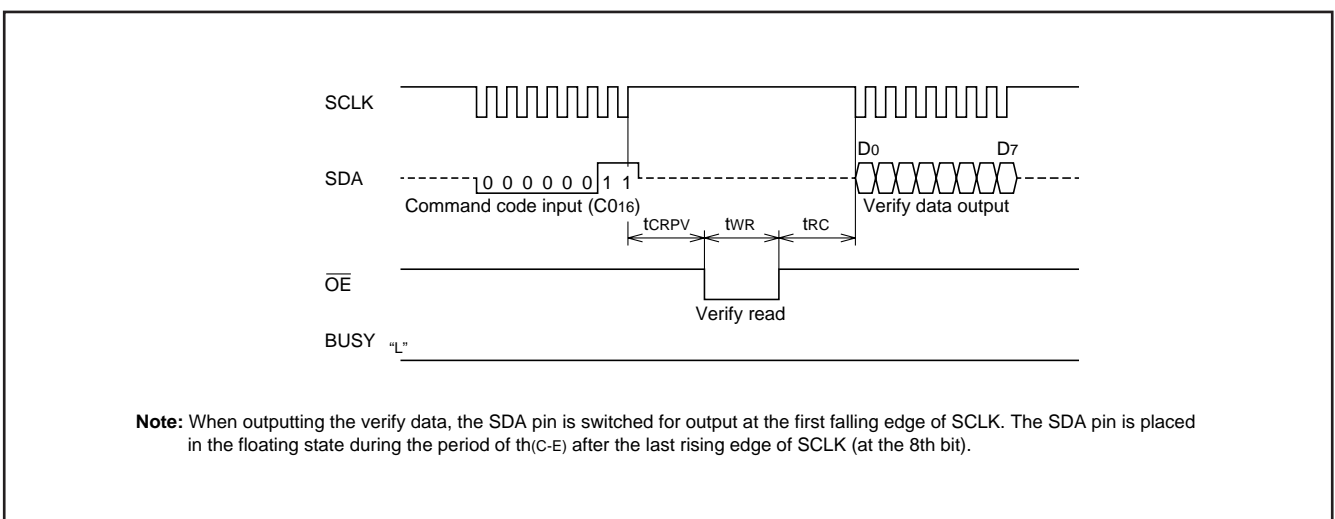


**Note:** When outputting the verify data, the SDA pin is switched for output at the first falling edge of SCLK. The SDA pin is placed in the floating state during the period of $t_{h(C-E)}$ after the last rising edge of SCLK (at the 8th bit).

Fig. 18  Timings during program verify

## Auto erase command

Input command code $30_{16}$ in the first transfer and command code $30_{16}$ again in the second transfer. When this is done, the M37754FFCGP and the M37754FFCHP execute an auto erase command. Auto erase is initiated at the last rising edge of the serial clock. The BUSY pin is driven high during the auto erase operation.

Auto erase is completed when all memory contents are erased, and the BUSY pin is pulled low.

**Note:** In the auto erase operation, the M37754FFCGP and the M37754FFCHP automatically repeat the erase and verify operations internally. Therefore, erase is completed by executing the command once.
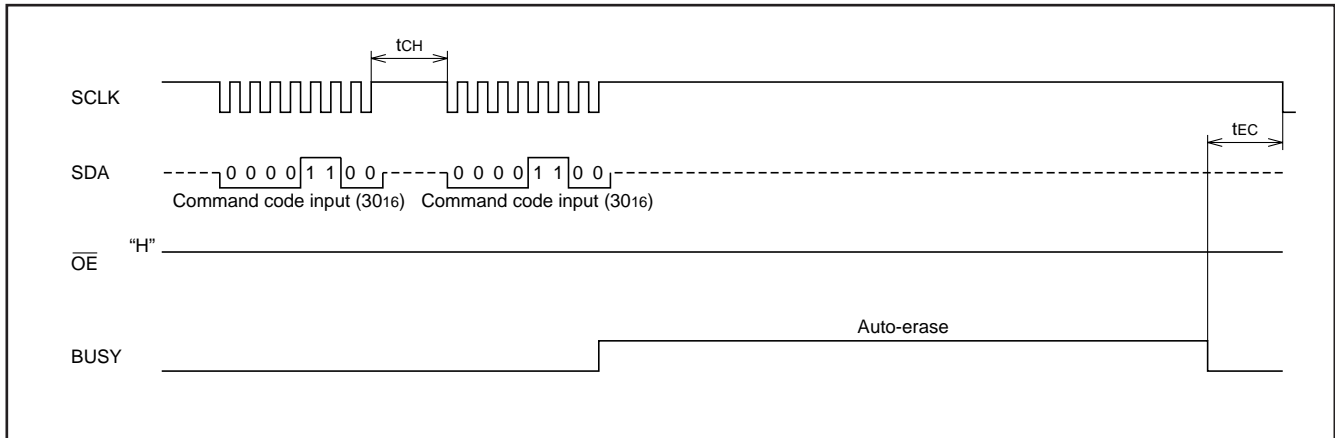


Fig. 19  Timings at auto-erasing

## Error check command

Input command code $80_{16}$ in the first transfer, and the M37754FFCGP and the M37754FFCHP output error information from the SDA pin, beginning at the next falling edge of the serial clock. If the E0 of the 8-bit error information is 1, it indicates that a command error has occurred. A command error means that some invalid commands other than commands shown in Table 4 has been input.

When a command error occurs, the serial communication circuit sets the corresponding flag and stops functioning to avoid an erroneous programming or erase. When being placed in this state, the serial communication circuit does not accept the subsequent serial clock and data (even including an error check command). Therefore, if the

user wants to execute an error check command, temporarily drop the $V_{PP}$ pin input to the $V_{PPL}$ level to terminate the serial input/output mode. Then, place the M37754FFCGP and the M37754FFCHP into the serial I/O mode back again. The serial communication circuit is reset by this operation and is ready to accept commands. The error flag alone is not cleared by this operation, so the user can examine the serial communication circuit's error conditions before reset. This examination is done by the first execution of an error check command after the reset. The error flag is cleared when the user has executed the error check command. Because the error flag is undefined immediately after power-on, always be sure to execute the error check command.



**Note:** When outputting the error flag, the SDA pin is switched for output at the first falling edge of the serial clock. The SDA pin is placed in the floating state during the period of $t_{h(C-E)}$ after the last rising edge of the serial clock (at the 8th bit).

Fig. 20  Timings at error checking

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## DC ELECTRICAL CHARACTERISTICS (Ta = 25 °C, $V_{CC}$ = 5 V ± 10 %, $V_{PP}$ = 12 V ± 5 %, unless otherwise noted)

$I_{CC}$, $I_{PP}$-relevant standards during read, program, and erase are the same as in the parallel input/output mode. $V_{IH}$, $V_{IL}$, $V_{OH}$, $V_{OL}$, $I_{IH}$, and $I_{IL}$ for the SCLK, SDA, BUSY, $\overline{OE}$ pins conform to the microcomputer modes.

## AC ELECTRICAL CHARACTERISTICS

(Ta = 25 °C, $V_{CC}$ = 5 V ± 10 %, $V_{PP}$ = 12 V ± 5 %, f($X_{IN}$) = 40 MHz, unless otherwise noted)

| Symbol | Parameter | Limits Min. | Limits Max. | Unit |
|--------|-----------|-------------|-------------|------|
| $t_{CH}$ | Serial transmission interval | 400(Note 1) | | ns |
| $t_{CR}$ | Read waiting time after transmission | 400(Note 1) | | ns |
| $t_{WR}$ | Read pulse width | 320(Note 2) | | ns |
| $t_{RC}$ | Transfer waiting time after read | 400(Note 1) | | ns |
| $t_{CRPV}$ | Waiting time before program verify | 6 | | $\mu$s |
| $t_{WP}$ | Programming time | | 10 | $\mu$s |
| $t_{PC}$ | Transfer waiting time after programming | 400(Note 1) | | ns |
| $t_{EC}$ | Transfer waiting time after erase | 400(Note 1) | | ns |
| $t_{c(CK)}$ | SCLK input cycle time | 250 | | ns |
| $t_{w(CKH)}$ | SCLK high-level pulse width | 100 | | ns |
| $t_{w(CKL)}$ | SCLK low-level pulse width | 100 | | ns |
| $t_{r(CK)}$ | SCLK rise time | 20 | | ns |
| $t_{f(CK)}$ | SCLK fall time | 20 | | ns |
| $t_{d(C-Q)}$ | SDA output delay time | 0 | 90 | ns |
| $t_{h(C-Q)}$ | SDA output hold time | 0 | | ns |
| $t_{h(C-E)}$ | SDA output hold time (only the 8th bit) | 120(Note 3) | 200(Note 4) | ns |
| $t_{su(D-C)}$ | SDA input set up time | 30 | | ns |
| $t_{h(C-D)}$ | SDA input hold time | 90 | | ns |

**Notes 1:** When f($X_{IN}$) = 25 MHz or less, calculate the minimum value according to formula 1.

Formula 1 : $\dfrac{1 \times 10}{f(X_{IN})} \times 10^9$

**2:** When f($X_{IN}$) = 25 MHz or less, calculate the minimum value according to formula 2.

Formula 2 : $\dfrac{1 \times 8}{f(X_{IN})} \times 10^9$

**3:** When f($X_{IN}$) = 25 MHz or less, calculate the minimum value according to formula 3.

Formula 3 : $\dfrac{1 \times 3}{f(X_{IN})} \times 10^9$

**4:** When f($X_{IN}$) = 25 MHz or less, calculate the minimum value according to formula 4

Formula 4 : $\dfrac{1 \times 5}{f(X_{IN})} \times 10^9$

## AC waveforms
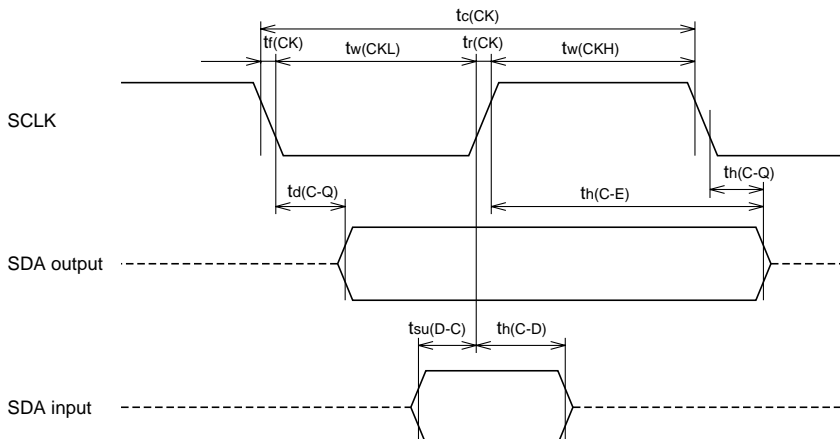


Test conditions for AC characteristics

• Output timing voltage : $V_{OL}$ = 0.8 V, $V_{OH}$ = 2.0 V

• Input timing voltage : $V_{IL}$ = 0.2 $V_{CC}$, $V_{IH}$ = 0.8 $V_{CC}$

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## Flash memory mode-3 (CPU reprogramming mode)

The M37754FFCGP and the M37754FFCHP have the CPU reprogramming mode where a built-in flash memory is handled by the central processing unit (CPU). 112 Kbytes (addresses $00100_{16}$ to $00EFFF_{16}$ and addresses $01100_{16}$ to $01EFFF_{16}$) of the 120-Kbyte flash memory shown in Figure 1 can be reprogrammed (erase and program). Remaining 8 Kbytes of the flash memory (addresses $00F000_{16}$ to $010FFF_{16}$) cannot be reprogrammed, but can be read. (It is possible to reprogram this remaining 8 Kbytes in the parallel I/O mode and the serial I/O mode). This area of 8 Kbytes can be used as an area where the control program of CPU reprogramming mode is stored.

In CPU reprogramming mode, the flash memory is handled by writing and reading to/from the flash memory control register (see Figure 21) and the flash command register (see Figure 22).

The CNVss pin is used as the Vpp power supply pin in CPU reprogramming mode. It is necessary to apply the power-supply voltage of VppH from the external to this pin.

## Functional outline (Parallel input/output mode)

Figure 21 shows the flash memory control register bit configuration.

Figure 22 shows the flash command register bit configuration.

Bit 0 of the flash memory control register is the CPU reprogramming mode select bit. When this bit is set to "1" and VppH is applied to the CNVss/Vpp pin, the CPU reprogramming mode is selected. Whether the CPU reprogramming mode is realized or not is judged by reading the CPU reprogramming mode monitor flag (bit 3 of the flash memory control register).

Bit 1 is a busy flag which becomes "1" during auto erase, erase, and program execution.

Whether these operations have been completed or not is judged by checking this flag after each command of auto erase, erase, and the program is executed.

Bits 4, 5 of the flash memory control register are the erase/program area select bits. These bits specify an area where auto erase, erase, and program is operated. When the auto erase and the erase commands are executed after an area is specified by these bits, only the specified area is erased. Only for the specified area, programming is enabled; for the other areas, programming is disabled.

Figure 23 shows the processor mode register 0 bit configuration in the CPU reprogramming mode. Set bit 1 to "0" (single-chip or memory expansion mode) in the CPU reprogramming mode. Set bit 2 (internal memory access bus cycle select bit) to "0."

Be sure to set data length select flag m to "1" (8-bit length) beforehand because writing and reading of data are operated in unit of byte.
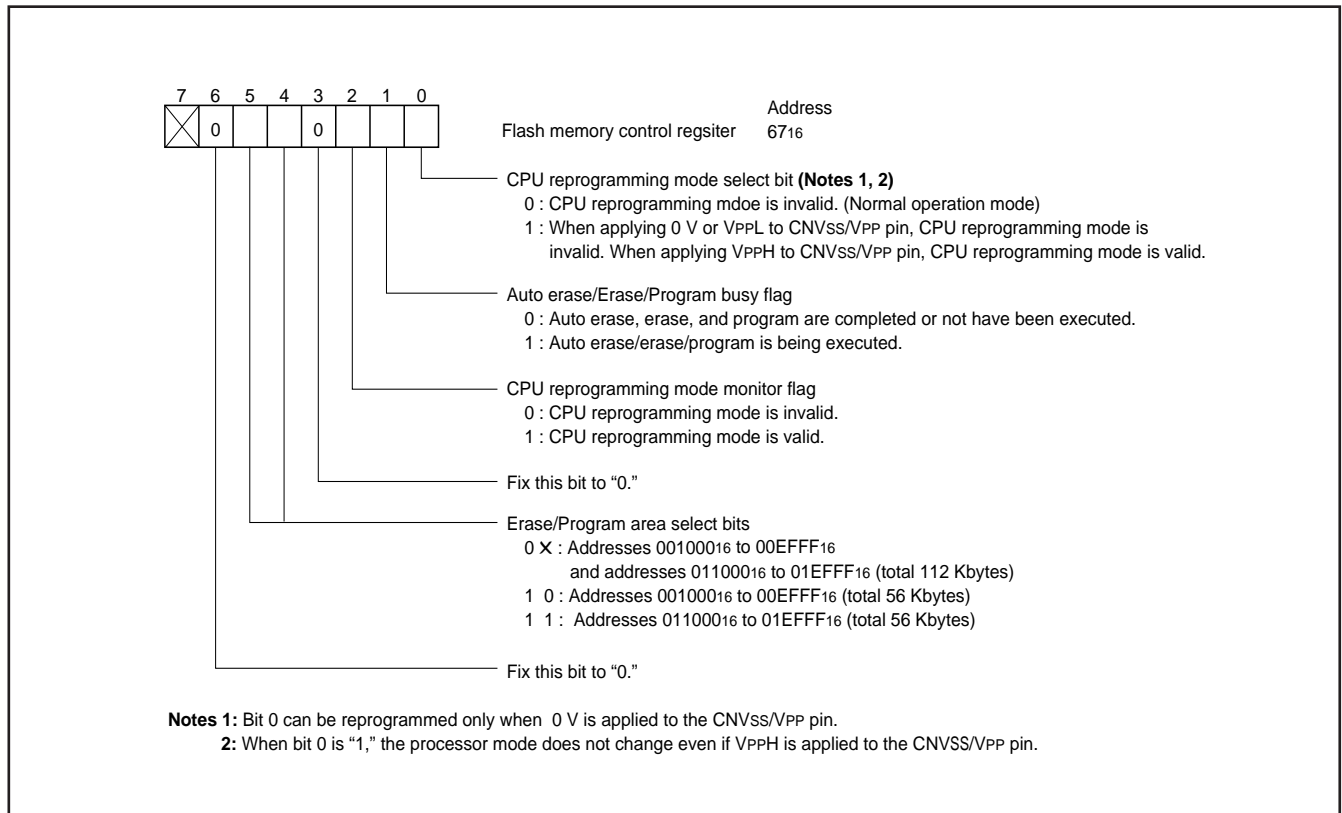


Fig. 21 Flash memory control register bit configuration

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## CPU reprogramming mode operation procedure

The operation procedure in CPU reprogramming mode is described below.

< Beginning procedure >

① Apply 0 V to the CNVss/VPP pin for reset release.

② Set the processor mode register 0 (see Figure 23).

③ After CPU reprogramming mode control program is transferred to internal RAM, jump to this control program on RAM. (The following operations are controlled by this control program).

④ Set "1" (8-bit length) to data length select flag m.

⑤ Set "1" to the CPU reprogramming mode select bit.

⑥ Apply VPPH to the CNVSS/VPP pin.

⑦ Read the CPU reprogramming mode monitor flag to confirm whether the CPU reprogramming mode is valid.

⑧ The operation of the flash memory is executed by software-command-writing to the flash command register .

**Note:** The following are necessary other than this:
  •Control for data which is input from the external (serial I/O etc.) and to be programmed to the flash memory
  •Initial setting for ports etc.
  •Writing to the watchdog timer

< Release procedure >

① Apply 0V to the CNVSS/VPP pin.

② Set the CPU reprogramming mode select bit to "0."

Each software command is explained as follows.

## Read command

When "$00_{16}$" is written to the flash command register, the M37754FFCGP and the M37754FFCHP enter the read mode. The contents of the corresponding address can be read by reading the flash memory (For instance, with the LDA instruction etc.) under this condition.

The read mode is maintained until another command code is written to the flash command register. Accordingly, after setting the read mode once, the contents of the flash memory can continuously be read.

After reset and after the reset command is executed, the read mode is set.
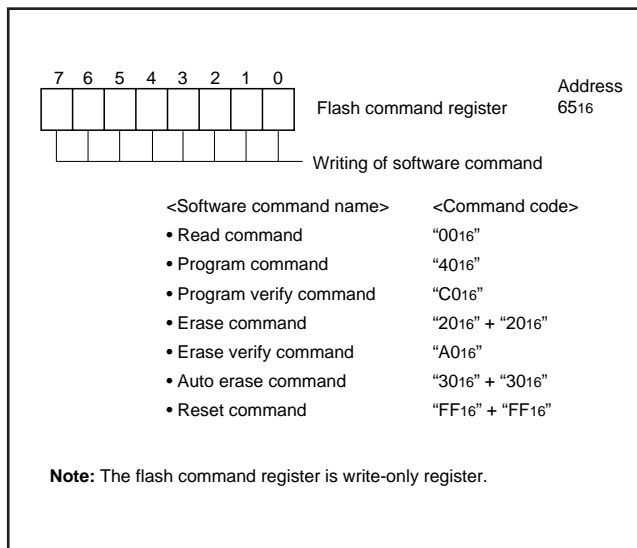


Fig. 22 Flash command register bit configuration
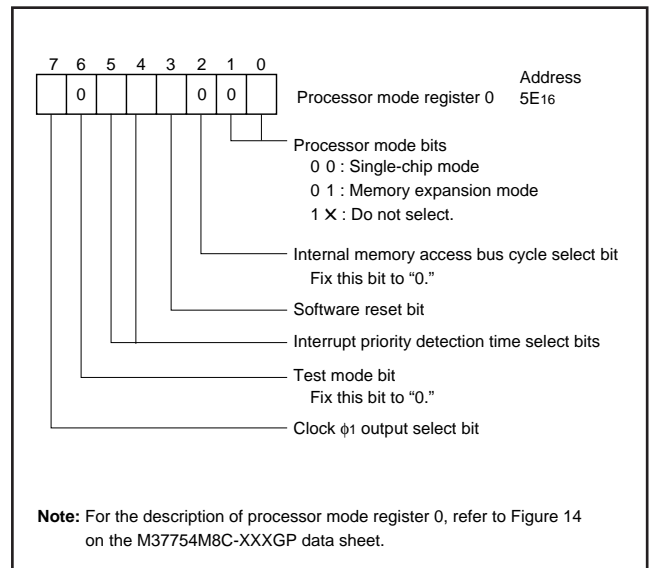


Fig. 23 Processor mode register 0 bit configuration in CPU rewriting mode

## Program command

When "$40_{16}$" is written to the flash command register, the M37754FFCGP and the M37754FFCHP enter the program mode. Subsequently to this, if the instruction (for instance, STA or LDM instruction) for writing byte data in the address to be programmed is executed, the control circuit of the flash memory executes the program. The auto erase/erase/program busy flag of the flash memory control register is set to "1" when the program starts, and becomes "0" when the program is completed. Accordingly, after the write instruction is executed, CPU can recognize the completion of the program by polling this bit.

The programmed area must be specified beforehand by the erase/program area select bits.

During programming, watchdog timer stops with "$FFF_{16}$" set.

**Note:** A programming operation is not completed by executing the program command once. Always be sure to execute a program verify command after executing the program command. When the failure is found in this verification, the user must repeatedly execute the program command until the pass. Refer to Figure 24 for the flow chart of the programming.

## Program verify command

When "$C0_{16}$" is written to the flash command register, the M37754FFCGP and the M37754FFCHP enter the program verify mode. Subsequently to this, if the instruction (for instance, LDA instruction) for reading byte data from the address to be verified (i.e., previously programmed address), the contents which has been written to the address actually is read.

CPU compares this read data with data which has been written by the previous program command. In consequence of the comparison, if not agreeing, the operation of "program $\rightarrow$ program verify" must be executed again.

## Erase command

When writing "$20_{16}$" twice continuously to the flash command register, the flash memory control circuit performs erase to the area specified beforehand by the erase/program area select bits.

Auto erase/erase/program busy flag of the flash memory control register becomes "1" when erase begins, and it becomes "0" when erase completes. Accordingly, CPU can recognize the completion of erase by polling this bit.

Data "$00_{16}$" must be written to all areas to be erased by the program and the program verify commands before the erase command is executed.

During programming, watchdog timer stops with "$FFF_{16}$" set.

**Note:** The erasing operation is not completed by executing the erase command once. Always be sure to execute an erase verify command after executing the erase command. When the failure is found in this verification, the user must repeatedly execute the erase command until the pass. Refer to Figure 24 for the erasing flowchart.

## Erase verify command

When "$A0_{16}$" is written to the flash command register, the M37754FFCGP and the M37754FFCHP enter the erase verify mode. Subsequently to this, if the instruction (for instance, LDA instruction) for reading byte data from the address to be verified, the contents of the address is read.

CPU must erase and verify to all erased areas in a unit of address.

If the address of which data is not "$FF_{16}$" (i.e., data is not erased) is found, it is necessary to discontinue erasure verification there, and execute the operation of "erase $\rightarrow$ erase verify" again.

**Note:** By executing the operation of "erase $\rightarrow$ erase verify" again when the memory not erased is found. It is unnecessary to write data "$00_{16}$" before erasing in this case.

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PRELIMINARY
Notice: This is not a final specification.
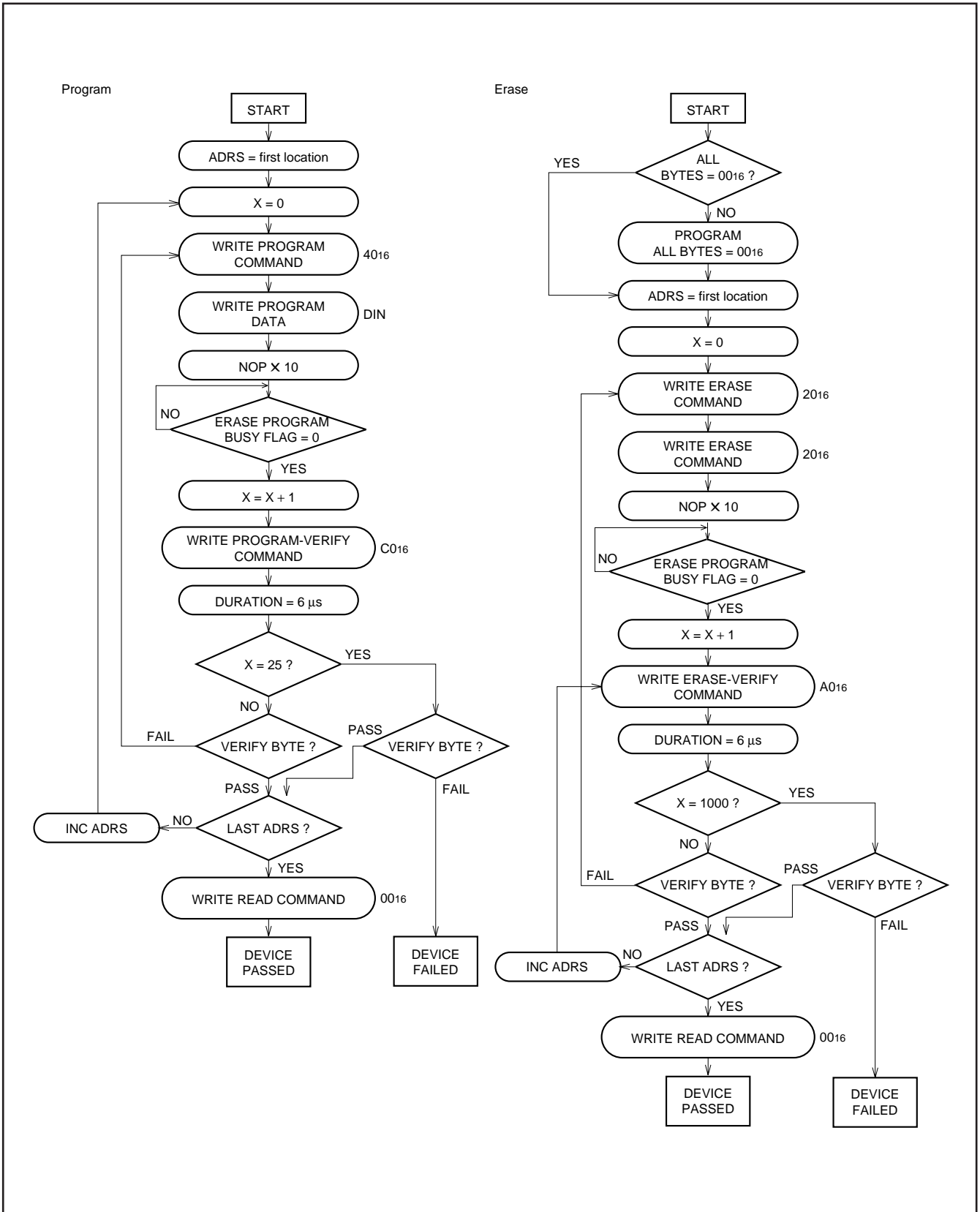Some parametric limits are subject to change.



Fig. 24 Flowchart when program/erase/auto erase is executed (1)

## Auto erase command

When writing "$30_{16}$" twice continuously to the flash command register, the flash memory control circuit executes the auto erase sequence described below for the area specified beforehand by the erase/program area select bits.

 (1) Data "$00_{16}$" is written to the area to be erased in the flash memory.

(2) The erasure is executed.

(3) The contents of the erased flash memory is erase-verified one by one. When the address which is not erased is found, verification is interrupted, and after the erase command is executed again, erase-verification is operated again.

 (4) When the erasure of all areas specified to be erased, is confirmed by erase-verify-operation, the auto erase command is ended.

The auto erase/erase/program busy flag of the flash memory control register becomes "1" when auto erase starts, and becomes "0" when auto erase completes. Accordingly, CPU can recognize the completion of auto erase by polling this bit.

During auto erase, watchdog timer stops with "$FF_{16}$" set.

**Note:** When the flash memory is erased by using the auto erase command, it is unnecessary to execute the erase and erase verify commands. Figure 25 shows the flowchart when auto erase is executed.

DC electric characteristics

**Note:** The characteristic of the flash memory part are the same as the standard of the parallel I/O mode.

AC electric characteristics

**Note:** The characteristics are the same as the standards of the microcomputer mode.

## Reset command

The reset command is a command to discontinue the program, erase, or the auto erase command on the way. When "$FF_{16}$" is written to the command register two times continuously after "$40_{16}$," "$20_{16}$," or "$30_{16}$" is written to the flash command register, the program, erase, or auto erase command becomes invalid (reset), and the M37754FFCGP and the M37754FFCHP enters the reset mode. The contents of the memory does not change even if the reset command is executed.
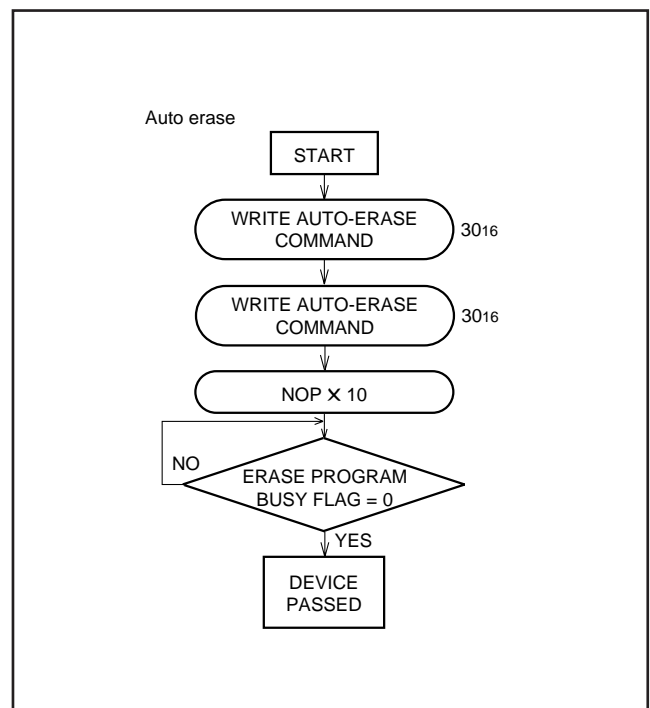


Fig. 25 Flowchart when program/erase/auto erase is executed (2)

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $V_{CC}$ | Power source voltage | −0.3 to 7 | V |
| $AV_{CC}$ | Analog power source voltage | −0.3 to 7 | V |
| $V_I$ | Input voltage $\overline{RESET}$, $CNV_{SS}$, BYTE | −0.3 to 12 **(Note)** | V |
| $V_I$ | Input voltage P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P9$_0$–P9$_5$, P10$_0$–P10$_7$, P11$_0$–P11$_7$, $V_{REF}$, $X_{IN}$ | −0.3 to $V_{CC}$+0.3 | V |
| $V_O$ | Output voltage P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P9$_0$–P9$_5$, P10$_0$–P10$_7$, P11$_0$–P11$_7$, $X_{OUT}$, $\overline{E}$ | −0.3 to $V_{CC}$+0.3 | V |
| $P_d$ | Power dissipation | 300 | mW |
| $T_{opr}$ | Operating temperature | −20 to 85 | °C |
| $T_{stg}$ | Storage temerature | −40 to 150 | °C |

**Note:** For the CNVss pin, this is 12.6 V when programming to the flash memory.

## RECOMMENDED OPERATING CONDITIONS ($V_{CC}$ = 5 V±10 %, Ta = -20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Limits Min. | Limits Typ. | Limits Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $AV_{CC}$ | Analog supply voltage | | $V_{CC}$ | | V |
| $V_{SS}$ | Supply voltage | | 0 | | V |
| $AV_{SS}$ | Analog supply voltage | | 0 | | V |
| $V_{IH}$ | High-level input voltage P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P9$_0$–P9$_5$, $X_{IN}$, $\overline{RESET}$, $CNV_{SS}$, BYTE | 0.8 $V_{CC}$ | | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage P10$_0$–P10$_7$, P11$_0$–P11$_7$ (in single-chip mode) | 0.8 $V_{CC}$ | | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage P10$_0$–P10$_7$, P11$_0$–P11$_7$ (in memory expansion mode and microprocessor mode) | 0.5 $V_{CC}$ | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P9$_0$–P9$_5$, $X_{IN}$, $\overline{RESET}$, $CNV_{SS}$, BYTE | 0 | | 0.2 $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage P10$_0$–P10$_7$, P11$_0$–P11$_7$ (in single-chip mode) | 0 | | 0.2 $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage P10$_0$–P10$_7$, P11$_0$–P11$_7$ (in memory expansion mode and microprocessor mode) | 0 | | 0.16 $V_{CC}$ | V |
| $I_{OH(peak)}$ | High-level peak output current P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P9$_0$–P9$_2$, P9$_5$, P10$_0$–P10$_7$, P11$_0$–P11$_7$ | | | −10 | mA |
| $I_{OH(peak)}$ | P9$_3$, P9$_4$ | | | −20 | mA |
| $I_{OH(avg)}$ | High-level average output current P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P9$_0$–P9$_2$, P9$_5$, P10$_0$–P10$_7$, P11$_0$–P11$_7$ | | | −5 | mA |
| $I_{OH(avg)}$ | P9$_3$, P9$_4$ | | | −15 | mA |
| $I_{OL(peak)}$ | Low-level peak output current P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_4$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P9$_0$, P9$_5$, P10$_0$–P10$_7$, P11$_0$–P11$_7$ | | | 10 | mA |
| $I_{OL(peak)}$ | P5$_0$–P5$_3$, P9$_1$–P9$_4$ | | | 20 | mA |
| $I_{OL(avg)}$ | Low-level average output current P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_4$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P9$_0$, P9$_5$, P10$_0$–P10$_7$, P11$_0$–P11$_7$ | | | 5 | mA |
| $I_{OL(avg)}$ | P5$_0$–P5$_3$, P9$_1$–P9$_4$ | | | 15 | mA |
| $f(X_{IN})$ | External clock frequency input **(Note 3)** Low-speed running | | | 25 | MHz |
| | High-speed running | | | 40 | |

**Notes 1:** Average output current is the averaage value of a 100 ms interval.
**2:** The sum of $I_{OL(peak)}$ for ports P0, P1, P2, P3, P8, P10, and P11 must be 80 mA or less, the sum of $I_{OH(peak)}$ for ports P0, P1, P2, P3, P8, P10, and P11 must be 80 mA or less, the sum of $I_{OL(peak)}$ for ports P4, P5, P6, P7, and P9 must be 110 mA or less, the sum of $I_{OH(peak)}$ for ports P4, P5, P6, P7, and P9 must be 80 mA or less.
**3:** When the clock source select bit is "1," $f(X_{IN})$'s maximum limit is 12.5 MHz at low-speed running and is 20 MHz at high-speed running.

## ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5 V, $V_{SS}$ = 0 V, Ta = –20 to 85 °C, f($X_{IN}$) = 40 MHz **(Note)**)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | High-level output voltage | P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P2$_7$, P3$_1$, P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P9$_0$–P9$_2$, P9$_5$, P10$_0$–P10$_7$, P11$_0$–P11$_7$ | $I_{OH}$ = –10 mA | 3.4 | | | V |
| $V_{OH}$ | High-level output voltage | P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P2$_7$, P3$_1$, P3$_3$, P9$_0$–P9$_2$, P10$_0$–P10$_7$, P11$_0$–P11$_7$ | $I_{OH}$ = –400 $\mu$A | 4.8 | | | V |
| $V_{OH}$ | High-level output voltage | $\overline{E}$, P3$_0$, P3$_2$ | $I_{OH}$ = –10 mA | 3.4 | | | V |
| | | | $I_{OH}$ = –400 $\mu$A | 4.8 | | | |
| $V_{OH}$ | High-level output voltage | P9$_3$, P9$_4$ | $I_{OH}$ = –15 mA | 3.4 | | | V |
| | | | $I_{OH}$ = –600 $\mu$A | 4.8 | | | |
| $V_{OL}$ | Low-level output voltage | P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P2$_7$, P3$_1$, P3$_3$, P4$_0$–P4$_7$, P5$_4$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P9$_0$, P9$_5$, P10$_0$–P10$_7$, P11$_0$–P11$_7$ | $I_{OL}$ = 10 mA | | | 2 | V |
| $V_{OL}$ | Low-level output voltage | P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P2$_7$, P3$_1$, P3$_3$, P9$_0$, P10$_0$–P10$_7$, P11$_0$–P11$_7$ | $I_{OL}$ = 2 mA | | | 0.45 | V |
| $V_{OL}$ | Low-level output voltage | $\overline{E}$, P3$_0$, P3$_2$ | $I_{OL}$ = 10 mA | | | 1.6 | V |
| | | | $I_{OL}$ = 2 mA | | | 0.4 | |
| $V_{OL}$ | Low-level output voltage | P5$_0$–P5$_3$, P9$_1$–P9$_4$ | $I_{OL}$ = 20 mA | | | 2 | V |
| | | | $I_{OL}$ = 2 mA | | | 0.4 | |
| $V_{T+}$—$V_{T-}$ | Hysteresis | $\overline{HOLD}$, $\overline{RDY}$, TA0$_{IN}$–TA4$_{IN}$, TB0$_{IN}$–TB2$_{IN}$, $\overline{INT0}$–$\overline{INT4}$, AD$_{TRG}$, $\overline{CTS0}$, $\overline{CTS1}$, CLK0, CLK1, RxD0, RxD1 | | 0.4 | | 1 | V |
| $V_{T+}$—$V_{T-}$ | Hysteresis | $\overline{RESET}$, $\overline{HOLD}$, $\overline{RDY}$ | | 0.2 | | 0.5 | V |
| $V_{T+}$—$V_{T-}$ | Hysteresis | $X_{IN}$ | | 0.1 | | 0.3 | V |
| $I_{IH}$ | High-level input current | P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P9$_0$–P9$_5$, P10$_0$–P10$_7$, P11$_0$–P11$_7$, $X_{IN}$, $\overline{RESET}$, CNV$_{SS}$, BYTE | $V_I$ = 5 V | | | 5 | $\mu$A |
| $I_{IL}$ | Low-level input current | P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_3$, P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_3$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P9$_0$–P9$_5$, P10$_0$–P10$_7$, P11$_0$–P11$_7$, $X_{IN}$, $\overline{RESET}$, CNV$_{SS}$, BYTE | $V_I$ = 0 V | | | –5 | $\mu$A |
| $I_{IL}$ | Low-level input current | P5$_4$–P5$_7$, P9$_5$ | $V_I$ = 0 V, No pull-up transistor | | | –5 | $\mu$A |
| | | | $V_I$ = 0 V, Pull-up transistor used | –0.25 | –0.5 | –1.0 | mA |
| $V_{RAM}$ | RAM hold voltage | | When clock is stoped. | 2 | | | V |
| $I_{CC}$ | Power supply current (target value) | | Output-only pin is open and other pins are Vss during reset. | f($X_{IN}$) = 40 MHz, square waveform **(Note)** | | 25 | 50 | mA |
| | | | | Ta = 25 °C when clcock is stopped. | | | 1 | $\mu$A |
| | | | | Ta = 85 °C when clcock is stopped. | | | 20 | |

**Note:** f($X_{IN}$) = 20 MHz when the clock source select bit = "1."

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## A-D CONVERTER CHARACTERISTICS

($V_{CC}$ = $AV_{CC}$ = 5 V ± 10 %, $V_{SS}$ = $AV_{SS}$ = 0 V, $T_a$ = −20 to 85 °C, the clock source select bit = 0, unless otherwise noted)

| Symbol | Parameter | Test conditions | | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| ———— | Resolution | $V_{REF}$ = $V_{CC}$ | | A-D converter selected | | | 10 | Bits |
| | | | | Comparator selected | | | $\frac{1}{256}V_{REF}$ | V |
| ———— | Absolute accuracy | $V_{REF}$ = $V_{CC}$ | 250 kHz ≤ $\phi_{AD}$ ≤ 12.5 MHz | 10-bit mode | | | ± 3 | LSB |
| | | | | 8-bit mode | | | ± 2 | LSB |
| | | | | Comparator | | | ± 40 | mV |
| | | | 250 kHz ≤ $\phi_{AD}$ ≤ 20 MHz **(Note 1)** | 8-bit mode | | | ± 3 | LSB |
| | | | | Comparator | | | ± 60 | mV |
| $R_{LADDER}$ | Ladder resistance | $V_{REF}$ = $V_{CC}$ | | | 5 | | 20 | kΩ |
| $t_{CONV}$ | Conversion time | High-speed running (f($X_{IN}$) ≤ 40 MHz) **(Note 2)** | $\phi_{AD}$ = f($X_{IN}$)/4 selected | 10-bit mode | 5.9 | | | μs |
| | | | | 8-bit mode | 4.9 | | | |
| | | | | Comparator | 1.4 | | | |
| | | | $\phi_{AD}$ = f($X_{IN}$)/2 selected | 8-bit mode | 2.45 | | | |
| | | | | Comparator | 0.7 | | | |
| | | Low-speed running (f($X_{IN}$) ≤ 25 MHz) **(Note 2)** | | 10-bit mode | 4.72 | | | |
| | | | | 8-bit mode | 3.92 | | | |
| | | | | Comparator | 1.12 | | | |
| $V_{REF}$ | Reference voltage | | | | 2.7 | | $V_{CC}$ | V |
| $V_{IA}$ | Analog input voltage | | | | 0 | | $V_{REF}$ | V |

**Notes 1**: This is valid when the high-speed running is selected.
    **2**: When the clock source select bit = 1, f($X_{IN}$) is 20 MHz or less at the high-speed running, and f($X_{IN}$) is 12.5 MHz or less at the low-speed running.

## D-A CONVERTER CHARACTERISTICS

($V_{CC}$ = 5 V, $V_{SS}$ = $AV_{SS}$ = 0 V, $V_{REF}$ = 5 V, $T_a$ = −20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| —— | Resolution | | | | 8 | Bits |
| —— | Absolute accuracy | | | | ± 1.0 | % |
| $t_{su}$ | Set time | | | | 3 | μs |
| $R_O$ | Output resistance | | 1 | 2.5 | 4 | kΩ |
| $I_{VREF}$ | Reference power supply input current | **(Note)** | | | 3.2 | mA |

**Note:** The test conditions are as follows:
- One D-A converter is used.
- The D-A register value of the unused D-A converter is "00₁₆."
- The reference power supply input current of the ladder resistance of the A-D converter is excluded.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

## PERIPHERAL DEVICE INPUT/OUTPUT TIMING (Vcc = 5 V±10 %, Vcc = 0 V, Ta = −20 to 85 °C, unless otherwise noted)

✽ If the values depends on external clock frequency f(Xin), formulas of the limits are shown below. Also, the values at f(Xin) = 40 MHz in high-speed running and at f(Xin) = 25 MHz in low-speed running are shown in ( ). At this time, the clock source select bit is "0." When the clock source select bit is "1", regard f(Xin) in tables as 2·f(Xin).

✽ The rise and fall time of input signal must be 100 ns or less respectively, unless otherwise noted.

### Timer A input (Count input in event counter mode)

| Symbol | Parameter | Limits Min. | Limits Max. | Unit |
|---|---|---|---|---|
| tc(TA) | TAiIN input cycle time | 80 | | ns |
| tw(TAH) | TAiIN input high-level pulse width | 40 | | ns |
| tw(TAL) | TAiIN input low-level pulse width | 40 | | ns |

### Timer A input (Gating input in timer mode)

| Symbol | Parameter | | Limits Min. | Limits Max. | Unit |
|---|---|---|---|---|---|
| tc(TA) | TAiIN input cycle time | f(Xin) ≤ 40 MHz | $\frac{16 \times 10^9}{f(Xin)}$ (400) | | ns |
| | | (Xin) ≤ 25 MHz | $\frac{8 \times 10^9}{f(Xin)}$ (320) | | ns |
| tw(TAH) | TAiIN input high-level pulse width | f(Xin) ≤ 40 MHz | $\frac{8 \times 10^9}{f(Xin)}$ (200) | | ns |
| | | f(Xin) ≤ 25 MHz | $\frac{4 \times 10^9}{f(Xin)}$ (160) | | ns |
| tw(TAL) | TAiIN input low-level pulse width | f(Xin) ≤ 40 MHz | $\frac{8 \times 10^9}{f(Xin)}$ (200) | | ns |
| | | f(Xin) ≤ 25 MHz | $\frac{4 \times 10^9}{f(Xin)}$ (160) | | ns |

**Note :** The TAiIN input cycle time requires 4 or more cycles of count source. The TAiIN input high-level pulse width and the TAiIN input low-level pulse width respectively require 2 or more cycles of the count source. The limits in the table are the values when the count source is f(Xin)/4 in high-speed running (f(Xin) ≤ 40 MHz) and when the count source is f(Xin)/2 in low-speed running (f(Xin) ≤ 25 MHz). At this time, the clock source select bit is "0."

### Timer A input (External trigger input in one-shot pulse mode)

| Symbol | Parameter | | Limits Min. | Limits Max. | Unit |
|---|---|---|---|---|---|
| tc(TA) | TAiIN input cycle time | f(Xin) ≤ 40 MHz | $\frac{8 \times 10^9}{f(Xin)}$ (200) | | ns |
| | | f(Xin) ≤ 25 MHz | $\frac{4 \times 10^9}{f(Xin)}$ (160) | | ns |
| tw(TAH) | TAiIN input high-level pulse width | | 80 | | ns |
| tw(TAL) | TAiIN input low-level pulse width | | 80 | | ns |

### Timer A input (External trigger input in pulse width modulation mode)

| Symbol | Parameter | Limits Min. | Limits Max. | Unit |
|---|---|---|---|---|
| tw(TAH) | TAiIN input high-level pulse width | 80 | | ns |
| tw(TAL) | TAiIN input low-level pulse width | 80 | | ns |

### Timer A input (Up-down input in event counter mode)

| Symbol | Parameter | Limits Min. | Limits Max. | Unit |
|---|---|---|---|---|
| tc(UP) | TAiOUT input cycle time | 2000 | | ns |
| tw(UPH) | TAiOUT input high-level pulse width | 1000 | | ns |
| tw(UPL) | TAiOUT input low-level pulse width | 1000 | | ns |
| tsu(UP-TIN) | TAiOUT input setup time | 400 | | ns |
| th(TIN-UP) | TAiOUT input hold time | 400 | | ns |

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## Timer A input (Two-phase pulse input in event counter mode)

| Symbol | Parameter | Limits | | Unit |
|--------|-----------|--------|--------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 800 | | ns |
| $t_{su(TAjIN-TAjOUT)}$ | TAjIN input setup time | 200 | | ns |
| $t_{su(TAjOUT-TAjIN)}$ | TAjOUT input setup time | 200 | | ns |

• Count input in event counter mode
• Gating input in timer mode
• External trigger input in one-shot pulse mode
• External trigger input in pulse width modulation mode
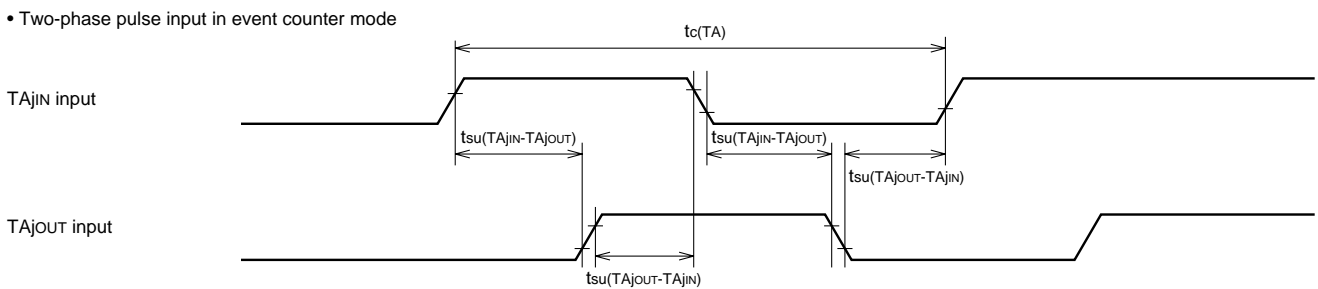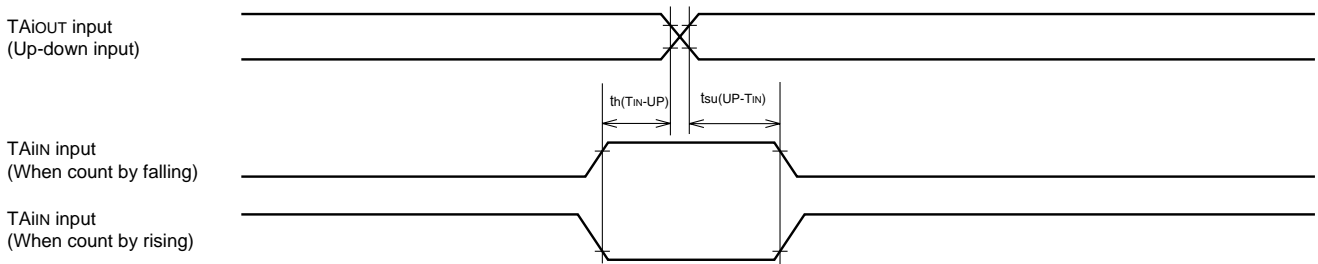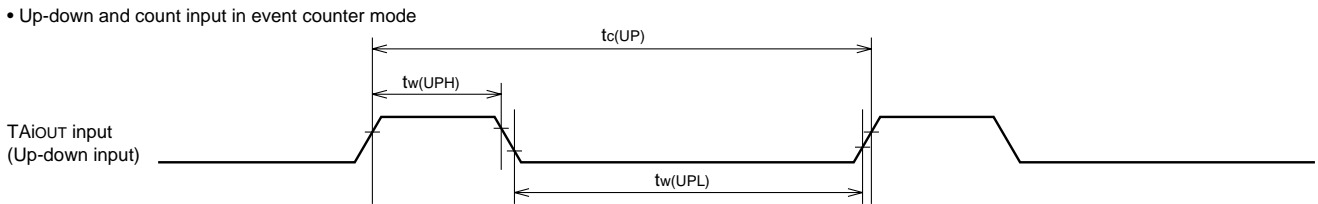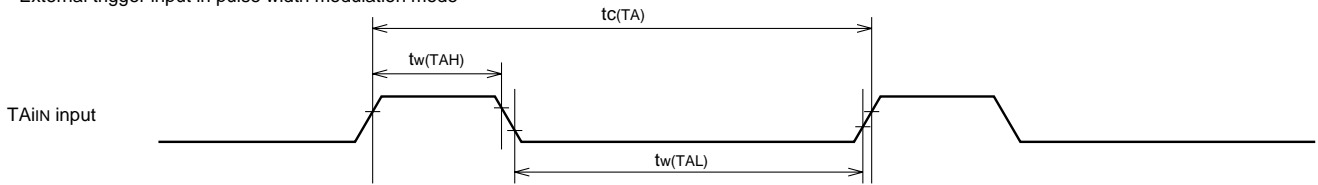


• Up-down and count input in event counter mode





• Two-phase pulse input in event counter mode



Test conditions
• $V_{CC}$ = 5 V±10 %
• Input timing voltage : $V_{IL}$ = 1.0 V, $V_{IH}$ = 4.0 V

## Timer B input (Count input in event counter mode)

| Symbol | Parameter | Limits Min. | Limits Max. | Unit |
|---|---|---|---|---|
| $t_{c(TB)}$ | TBiIN input cycle time (one edge count) | 80 | | ns |
| $t_{w(TBH)}$ | TBiIN input high-level pulse width (one edge count) | 40 | | ns |
| $t_{w(TBL)}$ | TBiIN input low-level pulse width (one edge count) | 40 | | ns |
| $t_{c(TB)}$ | TBiIN input cycle time (both edge count) | 160 | | ns |
| $t_{w(TBH)}$ | TBiIN input high-level pulse width (both edge count) | 80 | | ns |
| $t_{w(TBL)}$ | TBiIN input low-level pulse width (both edge count) | 80 | | ns |

## Timer B input (Pulse period measurement mode)

| Symbol | Parameter | | Limits Min. | Limits Max. | Unit |
|---|---|---|---|---|---|
| $t_{c(TB)}$ | TBiIN input cycle time | $f(X_{IN}) \leq 40$ MHz | $\dfrac{16 \times 10^9}{f(X_{IN})}$ (400) | | ns |
| | | $f(X_{IN}) \leq 25$ MHz | $\dfrac{8 \times 10^9}{f(X_{IN})}$ (320) | | ns |
| $t_{w(TBH)}$ | TBiIN input high-level pulse width | $f(X_{IN}) \leq 40$ MHz | $\dfrac{8 \times 10^9}{f(X_{IN})}$ (200) | | ns |
| | | $f(X_{IN}) \leq 25$ MHz | $\dfrac{4 \times 10^9}{f(X_{IN})}$ (160) | | ns |
| $t_{w(TBL)}$ | TBiIN input low-level pulse width | $f(X_{IN}) \leq 40$ MHz | $\dfrac{8 \times 10^9}{f(X_{IN})}$ (200) | | ns |
| | | $f(X_{IN}) \leq 25$ MHz | $\dfrac{4 \times 10^9}{f(X_{IN})}$ (160) | | ns |

Note : The TBiIN input cycle time requires 4 or more cycles of count source. The TBiIN input high-level pulse width and the TBiIN input low-level pulse width respectively require 2 or more cycles of the count source. The limits in the table are the values when the count source is $f(X_{IN})/4$ in high-speed running ($f(X_{IN}) \leq 40$ MHz) and when the count source is $f(X_{IN})/2$ in low-speed running ($f(X_{IN}) \leq 25$ MHz). At this time, the clock source select bit is "0."

## Timer B input (Pulse width measurement mode)

| Symbol | Parameter | | Limits Min. | Limits Max. | Unit |
|---|---|---|---|---|---|
| $t_{c(TB)}$ | TBiIN input cycle time | $f(X_{IN}) \leq 40$ MHz | $\dfrac{16 \times 10^9}{f(X_{IN})}$ (400) | | ns |
| | | $f(X_{IN}) \leq 25$ MHz | $\dfrac{8 \times 10^9}{f(X_{IN})}$ (320) | | ns |
| $t_{w(TBH)}$ | TBiIN input high-level pulse width | $f(X_{IN}) \leq 40$ MHz | $\dfrac{8 \times 10^9}{f(X_{IN})}$ (200) | | ns |
| | | $f(X_{IN}) \leq 25$ MHz | $\dfrac{4 \times 10^9}{f(X_{IN})}$ (160) | | ns |
| $t_{w(TBL)}$ | TBiIN input low-level pulse width | $f(X_{IN}) \leq 40$ MHz | $\dfrac{8 \times 10^9}{f(X_{IN})}$ (200) | | ns |
| | | $f(X_{IN}) \leq 25$ MHz | $\dfrac{4 \times 10^9}{f(X_{IN})}$ (160) | | ns |

Note : The TBiIN input cycle time requires 4 or more cycles of count source. The TBiIN input high-level pulse width and the TBiIN input low-level pulse width respectively require 2 or more cycles of the count source. The limits in the table are the values when the count source is $f(X_{IN})/4$ in high-speed running ($f(X_{IN}) \leq 40$ MHz) and when the count source is $f(X_{IN})/2$ in low-speed running ($f(X_{IN}) \leq 25$ MHz). At this time, the clock source select bit is "0."

## A-D trigger input

| Symbol | Parameter | Limits Min. | Limits Max. | Unit |
|---|---|---|---|---|
| $t_{c(AD)}$ | $\overline{AD}_{TRG}$ input cycle time (minimum allowable trigger) | 1000 | | ns |
| $t_{w(ADL)}$ | $\overline{AD}_{TRG}$ input low-level pulse width | 125 | | ns |

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## Serial I/O

| Symbol | Parameter | Limits Min. | Limits Max. | Unit |
|--------|-----------|------|------|------|
| $t_{c(CK)}$ | CLKi input cycle time | 200 | | ns |
| $t_{w(CKH)}$ | CLKi input high-level pulse width | 100 | | ns |
| $t_{w(CKL)}$ | CLKi input low-level pulse width | 100 | | ns |
| $t_{d(C-Q)}$ | TxDi output delay time | | 80 | ns |
| $t_{h(C-Q)}$ | TxDi hold time | 0 | | ns |
| $t_{su(D-C)}$ | RxDi input setup time | 20 | | ns |
| $t_{h(C-D)}$ | RxDi input hold time | 90 | | ns |

## External interrupt $\overline{INT}$i input

| Symbol | Parameter | Limits Min. | Limits Max. | Unit |
|--------|-----------|------|------|------|
| $t_{w(INH)}$ | $\overline{INT}$i input high-level pulse width | 250 | | ns |
| $t_{w(INL)}$ | $\overline{INT}$i input low-level pulse width | 250 | | ns |
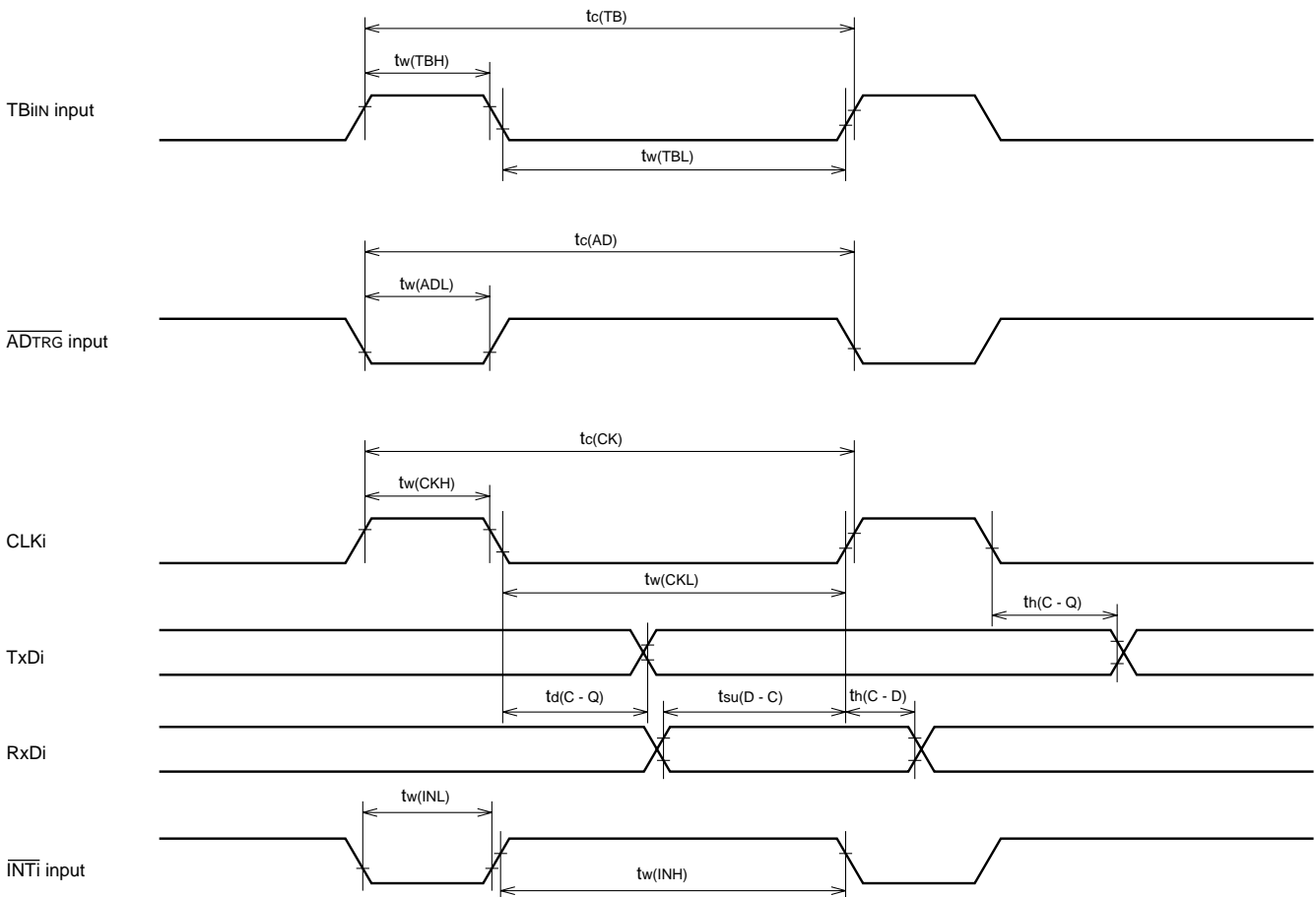
Test conditions
- Vcc = 5 V±10 %
- Input timing voltage    : VIL = 1.0 V, VIH = 4.0 V
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V, CL = 100 pF

## READY, HOLD TIMING

**Timing requirements** (Vcc = 5 V±10 %, Vss = 0 V, Ta = –20 to 85 °C, f(XIN) = 40 MHz when the clock source select bit = "0"[*], unless otherwise noted)

✳ The rise and fall time of input signal must be 100 ns or less respectively, unless otherwise noted.

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| tsu(RDY-$\phi$1) | $\overline{\text{RDY}}$ input setup time | 42 | | ns |
| tsu(HOLD-$\phi$1) | $\overline{\text{HOLD}}$ input setup time | 42 | | ns |
| th($\phi$1-RDY) | $\overline{\text{RDY}}$ input hold time | 0 | | ns |
| th($\phi$1-HOLD) | $\overline{\text{HOLD}}$ input hold time | 0 | | ns |

✳: f(XIN) = 20 MHz when the clock source select bit = "1".

## Switching characteristics (Vcc = 5 V±10 %, Vss = 0 V, Ta = –20 to 85 °C, f(XIN) = 40 MHz when the clock source select bit = "0"[*], unless otherwise noted)

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| td($\phi$1-HLDA) | $\overline{\text{HLDA}}$ output delay time | | 50 | ns |
| tpxz(HLDA-RDZ) | Floating start delay time (at hold state) | | 50 | ns |
| tpxz(HLDA-WRZ) | Floating start delay time (at hold state) | | 50 | ns |
| tpxz(HLDA-BHEZ) | Floating start delay time (at hold state) | | 50 | ns |
| tpxz(HLDA-AZ) | Floating start delay time (at hold state) | | 50 | ns |
| tpxz(HLDA-DLZ/DHZ) | Floating start delay time (at hold state) | | 50 | ns |
| tpzx(HLDA-RDZ) | Floating release delay time (at hold state) | 0 | | ns |
| tpzx(HLDA-WRZ) | Floating release delay time (at hold state) | 0 | | ns |
| tpzx(HLDA-BHEZ) | Floating release delay time (at hold state) | 0 | | ns |
| tpzx(HLDA-AZ) | Floating release delay time (at hold state) | 0 | | ns |
| tpzx(HLDA-DLZ/DHZ) | Floating release delay time (at hold state) | 0 | | ns |

✳: f(XIN) = 20 MHz when the clock source select bit = "1".

## $\overline{\text{RDY}}$ input (when 3-$\phi$ access in high-speed running)
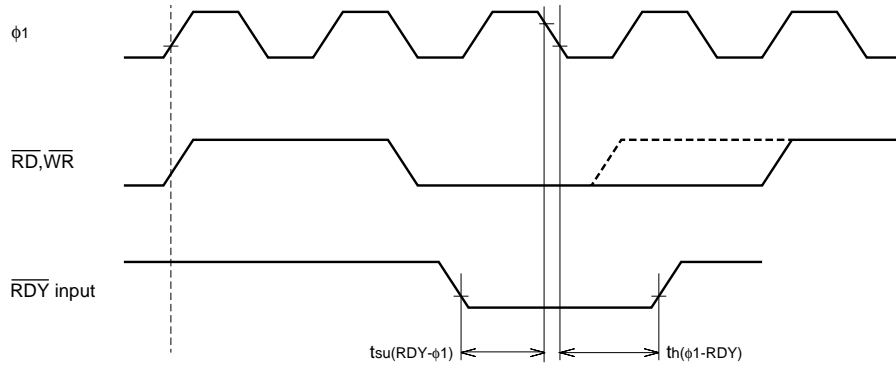


✳ $\overline{\text{RDY}}$ input is always sampled at the falling edge of $\phi1$ just before the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals' rise regardless of the bus mode and the number of waits.

## $\overline{\text{HOLD}}$ input
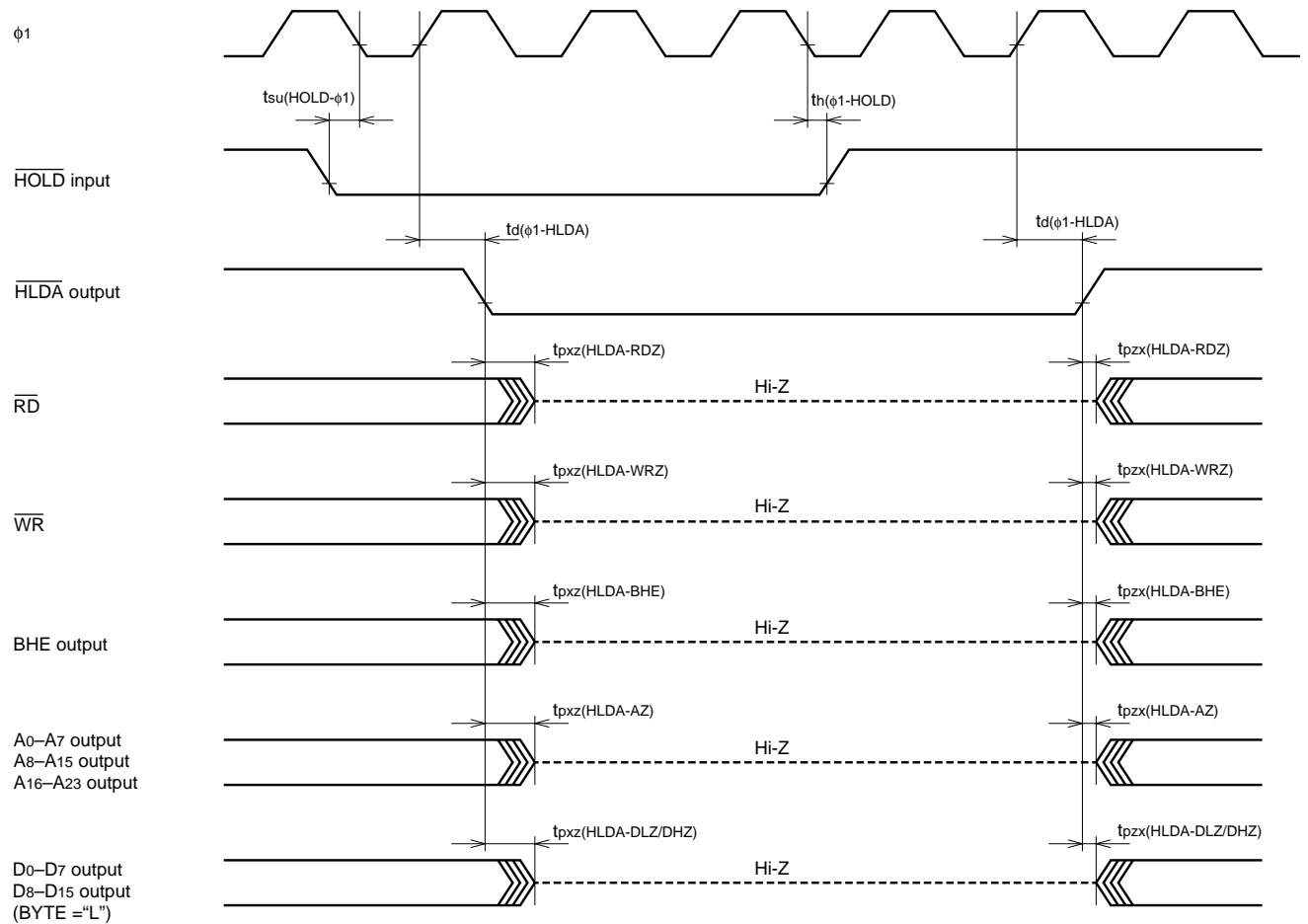


Test conditions
- $V_{CC}$ = 5 V±10 %
- $\overline{\text{RDY}}$ input, $\overline{\text{HOLD}}$ input : $V_{IL}$ = 1.0 V, $V_{IH}$ = 4.0 V
- $\overline{\text{HLDA}}$ output : $V_{OL}$ = 0.8 V, $V_{OH}$ = 2.0 V, $C_L$ = 100 pF

## Timing requirements (Vcc = 5 V±10 %, Vss = 0 V, Ta = −20 to 85 °C, f(XIN) = 40 MHz when the clock source select bit = "0"✻, unless otherwise noted)

✻ The rise and fall time of input signal must be 100 ns or less respectively, unless otherwise noted.

**Single-chip mode**

| Symbol | Parameter | Limits | | Unit |
|--------|-----------|--------|------|------|
| | | Min. | Max. | |
| tc | External clock input cycle time **(Note 1)** | 25 | | ns |
| tw(H) | External clock input high-level pulse width **(Note 2)** | $t_c/2 - 8$ | | ns |
| tw(L) | External clock input low-level pulse width **(Note 2)** | $t_c/2 - 8$ | | ns |
| tr | External clock rise time | | 8 | ns |
| tf | External clock fall time | | 8 | ns |
| tsu(PiD–E) | Port Pi input setup time (i = 0—11) | 60 | | ns |
| th(E–PiD) | Port Pi input hold time (i = 0—11) | 0 | | ns |

✻: f(XIN) = 20 MHz when the clock source select bit = "1"

**Notes 1:** When the clock source select bit = "1", tc's minimum limit is 50 ns.

**2:** When the clock source select bit = "1", set tw(H)/tc and tw(L)/tc ratios to 45 to 55 %.

## Switching characteristics (Vcc = 5 V±10 %, Vss = 0 V, Ta = −20 to 85 °C, f(XIN) = 40 MHz when the clock source select bit = "0"✻, unless otherwise noted)

(Single-chip mode)

| Symbol | Parameter | Limits | | Unit |
|--------|-----------|--------|------|------|
| | | Min. | Max. | |
| td(E–PiQ) | Port Pi data output delay time (i = 0—11) | | 60 | ns |

✻: f(XIN) = 20 MHz when the clock source select bit = "1"



Test conditions
• Vcc = 5 V±10 %
• Intput timing voltage : VIL = 1.0 V, VIH = 4.0 V
• Output timing voltage : VOL = 0.8 V, VOH = 2.0 V, CL = 100 pF

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## Timing requirements (Vcc = 5 V±10 %, Vss = 0 V, Ta = –20 to 85 °C, f(XIN) = 25 MHz when the clock source select bit = "0"[*], unless otherwise noted)

✱ The rise and fall time of input signal must be 100 ns or less respectively, unless otherwise noted.

**Memory expansion and Microprocessor mode : Low-speed running**

| Symbol | Parameter | Limits Min. | Limits Max. | Unit |
|---|---|---|---|---|
| $t_c$ | External clock input cycle time **(Note 1)** | 40 | | ns |
| $t_{w(H)}$ | External clock input high-level pulse width **(Note 2)** | $t_c/2 - 8$ | | ns |
| $t_{w(L)}$ | External clock input low-level pulse width **(Note 2)** | $t_c/2 - 8$ | | ns |
| $t_r$ | External clock rise time | | 8 | ns |
| $t_f$ | External clock fall time | | 8 | ns |
| $t_{su(DH-RD)}$ | High-order data input setup time (BYTE = "L") | 30 | | ns |
| $t_{su(DL-RD)}$ | Low-order data input setup time | 30 | | ns |
| $t_{su(PiD-RD)}$ | Port Pi input setup time (i = 4—9, 11) | 60 | | ns |
| $t_{h(RD-DH)}$ | High-order data input hold time (BYTE = "L") | 0 | | ns |
| $t_{h(RD-DL)}$ | Low-order data input hold time | 0 | | ns |
| $t_{h(RD-PiD)}$ | Port Pi input hold time (i = 4—9, 11) | 0 | | ns |
| $t_{su(A-DL/DH)}$ | Data setup time with address stabilized  **(Note 3)** | | 60 (2-$\phi$ access) / 140 (3-$\phi$ access) / 220 (4-$\phi$ access) | ns |
| $t_{su(CS-DL/DH)}$ | Data setup time with chip select stabilized  **(Note 3)** | | 60 (2-$\phi$ access) / 140 (3-$\phi$ access) / 220 (4-$\phi$ access) | ns |
| $t_{su(LA-DL)}$ | Data setup time with address stabilized  **(Note 3)** | | 55 (2-$\phi$ access) / 135 (3-$\phi$ access) / 215 (4-$\phi$ access) | ns |

✱: f(XIN) = 12.5 MHz when the clock source selet bit =  "1"

**Notes 1:** When the clock source select bit = "1", $t_c$'s minimum limit is 80 ns.

**2:** When the clock source select bit = "1", set $t_{w(H)}/t_c$ and $t_{w(L)}/t_c$ ratios to 45 to 55 %.

**3:** Since the values depend on external clock input frequency f(XIN), calculate them using the bus timing data formula on the page after the next page.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

## Switching characteristics (Vcc = 5 V±10 %, Vss = 0 V, Ta = –20 to 85 °C, f(XIN) = 25 MHz when the clock source select bit = "0"*, unless otherwise noted)

**Memory expansion and Microprocessor mode : Low-speed running**

| Symbol | Parameter | 2-$\phi$ access | | 3-$\phi$ access | | 4-$\phi$ access | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| tw($\phi$H), tw($\phi$L) | $\phi$ high-level pulse width, $\phi$ low-level pulse width **(Note)** | 20 | | 20 | | 20 | | ns |
| td($\phi$1–WR) | $\overline{WR}$ output delay time | –7 | 12 | –7 | 12 | –7 | 12 | ns |
| td($\phi$1–RD) | $\overline{RD}$ output delay time | –7 | 12 | –7 | 12 | –7 | 12 | ns |
| tw($\overline{WR}$) | $\overline{WR}$ low-level pulse width **(Note)** | 60 | | 140 | | 140 | | ns |
| tw(RD) | RD low-level pulse width **(Note)** | 60 | | 140 | | 140 | | ns |
| td(A–WR) | Address output delay time **(Note)** | 15 | | 15 | | 95 | | ns |
| td(A–RD) | Address output delay time **(Note)** | 15 | | 15 | | 95 | | ns |
| td(A–ALE) | Address output delay time **(Note)** | 8 | | 8 | | 55 | | ns |
| td(BHE–WR) | $\overline{BHE}$ output delay time **(Note)** | 15 | | 15 | | 95 | | ns |
| td(BHE–RD) | $\overline{BHE}$ output delay time **(Note)** | 15 | | 15 | | 95 | | ns |
| td(BHE–ALE) | $\overline{BHE}$ output delay time **(Note)** | 8 | | 8 | | 55 | | ns |
| td(CS–WR) | Chip select output delay time **(Note)** | 15 | | 15 | | 95 | | ns |
| td(CS–RD) | Chip select output delay time **(Note)** | 15 | | 15 | | 95 | | ns |
| td(CS–ALE) | Chip select output delay time **(Note)** | 8 | | 8 | | 55 | | ns |
| td(WR–DLQ/DHQ) | Data output delay time | | 35 | | 35 | | 35 | ns |
| tpxz(WR–DLZ/DHZ) | Floating start delay time **(Note)** | | 30 | | 30 | | 30 | ns |
| td(ALE–WR) | ALE output delay time | 4 | | 4 | | 4 | | ns |
| td(ALE–RD) | ALE output delay time | 4 | | 4 | | 4 | | ns |
| tw(ALE) | ALE pulse width **(Note)** | 22 | | 22 | | 62 | | ns |
| th(WR–A) | Address hold time **(Note)** | 10 | | 10 | | 10 | | ns |
| th(RD–A) | Address hold time **(Note)** | 10 | | 10 | | 10 | | ns |
| th(WR–BHE) | $\overline{BHE}$ hold time **(Note)** | 10 | | 10 | | 10 | | ns |
| th(RD–BHE) | $\overline{BHE}$ hold time **(Note)** | 10 | | 10 | | 10 | | ns |
| th(WR–CS) | Chip select hold time **(Note)** | 10 | | 10 | | 10 | | ns |
| th(RD–CS) | Chip select hold time **(Note)** | 10 | | 10 | | 10 | | ns |
| th(WR–DLQ/DHQ) | Data hold time **(Note)** | 15 | | 15 | | 15 | | ns |
| tpzx(WR–DLZ/DHZ) | Floating release delay time | 0 | | 0 | | 0 | | ns |
| td(LA–WR) | Address output delay time **(Note)** | 12 | | 12 | | 92 | | ns |
| td(LA–RD) | Address output delay time **(Note)** | 12 | | 12 | | 92 | | ns |
| td(LA–ALE) | Address output delay time **(Note)** | 5 | | 5 | | 52 | | ns |
| th(ALE–LA) | Address hold time | 9 | | 9 | | 25 **(Note)** | | ns |
| tpxz(RD–DLZ) | Floating start delay time | | 5 | | 5 | | 5 | ns |
| tpzx(RD–DLZ) | Floating release delay time **(Note)** | 18 | | 18 | | 18 | | ns |
| td(WR–PiQ) | Port Pi data output delay time (i = 4—9, 11) | | 60 | | 60 | | 60 | ns |

✻: f(XIN) = 12.5 MHz when the clock source selet bit = "1"

**Note:** Since the values depend on external clock input frequency f(XIN), calculate them using the bus timing data formula on the next page.

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## Bus timing data formulas

**Memory expansion and Microprocessor mode : Low-speed running** ($V_{CC}$ = 5 V±10 %, $V_{SS}$ = 0 V, Ta = −20 to 85 °C, f($X_{IN}$) ≤ 25 MHz when the clock source select bit = "0"*, unless otherwise noted)

| Symbol | Parameter | 2-$\phi$ access | 3-$\phi$ access | 4-$\phi$ access | Unit |
|---|---|---|---|---|---|
| $t_{su(A-DL/DH)}$ | Data setup time with address stabilized | $\dfrac{3 \times 10^9}{f(X_{IN})} - 60$ | $\dfrac{5 \times 10^9}{f(X_{IN})} - 60$ | $\dfrac{7 \times 10^9}{f(X_{IN})} - 60$ | ns |
| $t_{su(CS-DL/DH)}$ | Data setup time with chip select stabilized | $\dfrac{3 \times 10^9}{f(X_{IN})} - 60$ | $\dfrac{5 \times 10^9}{f(X_{IN})} - 60$ | $\dfrac{7 \times 10^9}{f(X_{IN})} - 60$ | ns |
| $t_{w(\phi H)}$, $t_{w(\phi L)}$ | $\phi$ high-level pulse width, f low-level pulse width | $\dfrac{1 \times 10^9}{f(X_{IN})} - 20$ | ← | ← | ns |
| $t_{w(\overline{WR})}$, $t_{w(\overline{RD})}$ | $\overline{WR}$, $\overline{RD}$ low-level pulse width | $\dfrac{2 \times 10^9}{f(X_{IN})} - 20$ | $\dfrac{4 \times 10^9}{f(X_{IN})} - 20$ | ← | ns |
| $t_{d(A-WR)}$ | Address output delay time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 25$ | ← | $\dfrac{3 \times 10^9}{f(X_{IN})} - 25$ | ns |
| $t_{d(A-RD)}$ | Address output delay time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 25$ | ← | $\dfrac{3 \times 10^9}{f(X_{IN})} - 25$ | ns |
| $t_{d(A-ALE)}$ | Address output delay time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 32$ | ← | $\dfrac{3 \times 10^9}{f(X_{IN})} - 65$ | ns |
| $t_{d(BHE-WR)}$ | $\overline{BHE}$ output delay time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 25$ | ← | $\dfrac{3 \times 10^9}{f(X_{IN})} - 25$ | ns |
| $t_{d(BHE-RD)}$ | $\overline{BHE}$ outupt delay time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 25$ | ← | $\dfrac{3 \times 10^9}{f(X_{IN})} - 25$ | ns |
| $t_{d(BHE-ALE)}$ | $\overline{BHE}$ output delay time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 32$ | ← | $\dfrac{3 \times 10^9}{f(X_{IN})} - 65$ | ns |
| $t_{d(CS-WR)}$ | Chip select output delay time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 25$ | ← | $\dfrac{3 \times 10^9}{f(X_{IN})} - 25$ | ns |
| $t_{d(CS-RD)}$ | Chip select output delay time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 25$ | ← | $\dfrac{3 \times 10^9}{f(X_{IN})} - 25$ | ns |
| $t_{d(CS-ALE)}$ | Chip select output delay time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 32$ | ← | $\dfrac{3 \times 10^9}{f(X_{IN})} - 65$ | ns |
| $t_{w(ALE)}$ | ALE pulse width | $\dfrac{1 \times 10^9}{f(X_{IN})} - 18$ | ← | $\dfrac{2 \times 10^9}{f(X_{IN})} - 18$ | ns |
| $t_{h(WR-A)}$ | Address hold time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 30$ | ← | ← | ns |
| $t_{h(RD-A)}$ | Address hold time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 30$ | ← | ← | ns |
| $t_{d(WR-BHE)}$ | $\overline{BHE}$ hold time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 30$ | ← | ← | ns |
| $t_{d(RD-BHE)}$ | $\overline{BHE}$ hold time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 30$ | ← | ← | ns |
| $t_{d(WR-CS)}$ | Chip select hold time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 30$ | ← | ← | ns |
| $t_{d(RD-CS)}$ | Chip select holt time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 30$ | ← | ← | ns |
| $t_{h(WR-DLQ/DHQ)}$ | Data hold time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 25$ | ← | ← | ns |
| $t_{pxz(WR-DLZ/DHZ)}$ | Floating start delay time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 10$ | ← | ← | ns |
| $t_{su(LA-DL)}$ | Data setup time with address stabilized | $\dfrac{3 \times 10^9}{f(X_{IN})} - 65$ | $\dfrac{5 \times 10^9}{f(X_{IN})} - 65$ | $\dfrac{7 \times 10^9}{f(X_{IN})} - 65$ | ns |
| $t_{d(LA-WR)}$ | Address output delay time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 28$ | ← | $\dfrac{3 \times 10^9}{f(X_{IN})} - 28$ | ns |
| $t_{d(LA-RD)}$ | Address output delay time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 28$ | ← | $\dfrac{3 \times 10^9}{f(X_{IN})} - 28$ | ns |
| $t_{d(LA-ALE)}$ | Address output delay time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 35$ | ← | $\dfrac{2 \times 10^9}{f(X_{IN})} - 28$ | ns |
| $t_{h(ALE-LA)}$ | Address hold time | — | — | $\dfrac{1 \times 10^9}{f(X_{IN})} - 15$ | ns |
| $t_{pzx(RD-DLZ)}$ | Floating release delay time | $\dfrac{1 \times 10^9}{f(X_{IN})} - 22$ | ← | ← | ns |

∗: f($X_{IN}$) ≤ 12.5 MHz when the clock source select bit = "1"

**Note:** When the clock source select bit is "1", regard f($X_{IN}$) in tables as 2·f($X_{IN}$).

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(when 2-$\phi$ access in low-speed running <Write>)



**Note:** These become a multiplex bus only when all of the following conditions are satisfied:
- BYTE = "H"
- Multiplex bus select bit = "1"
- While the address which corresponds to chip select signal $\overline{CS_4}$ is accessed
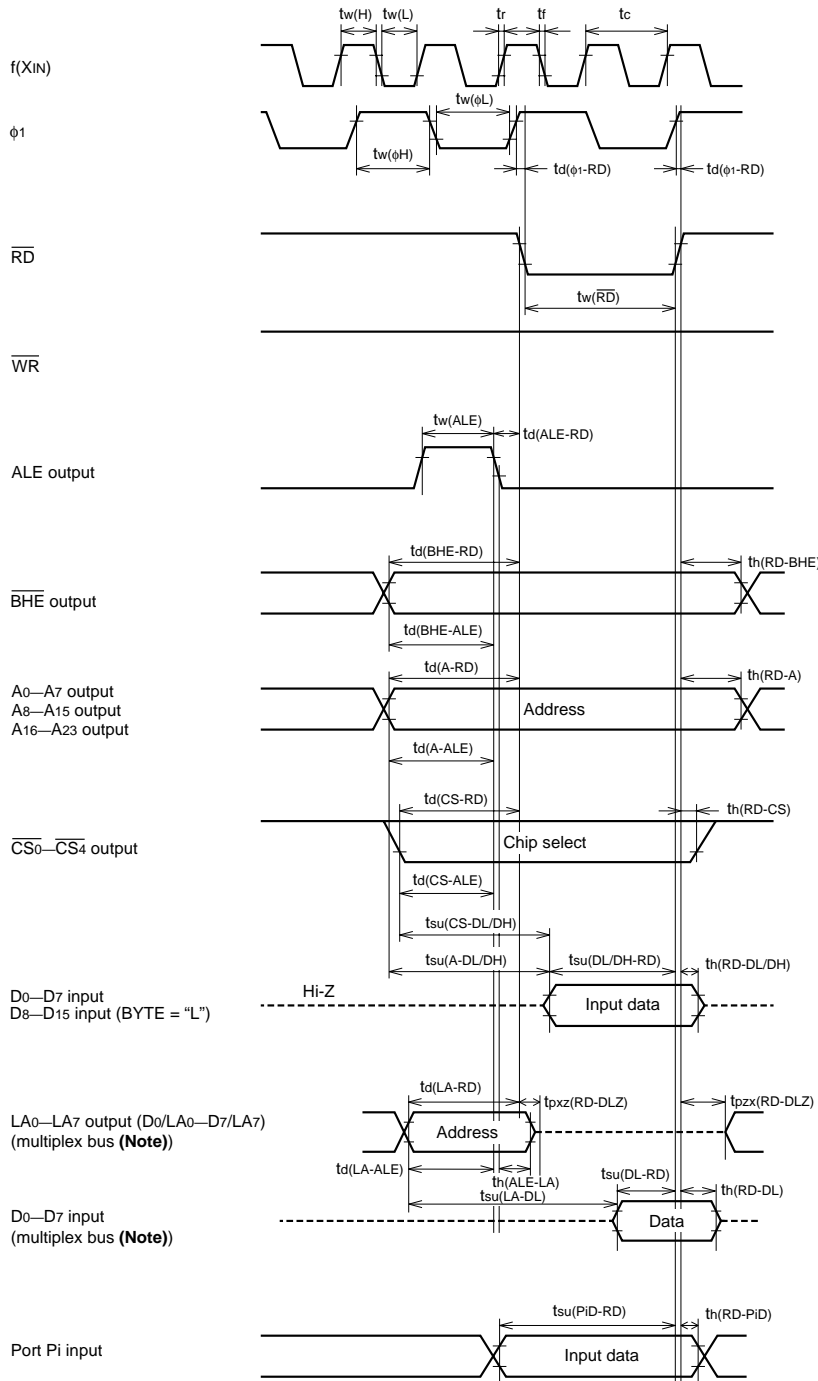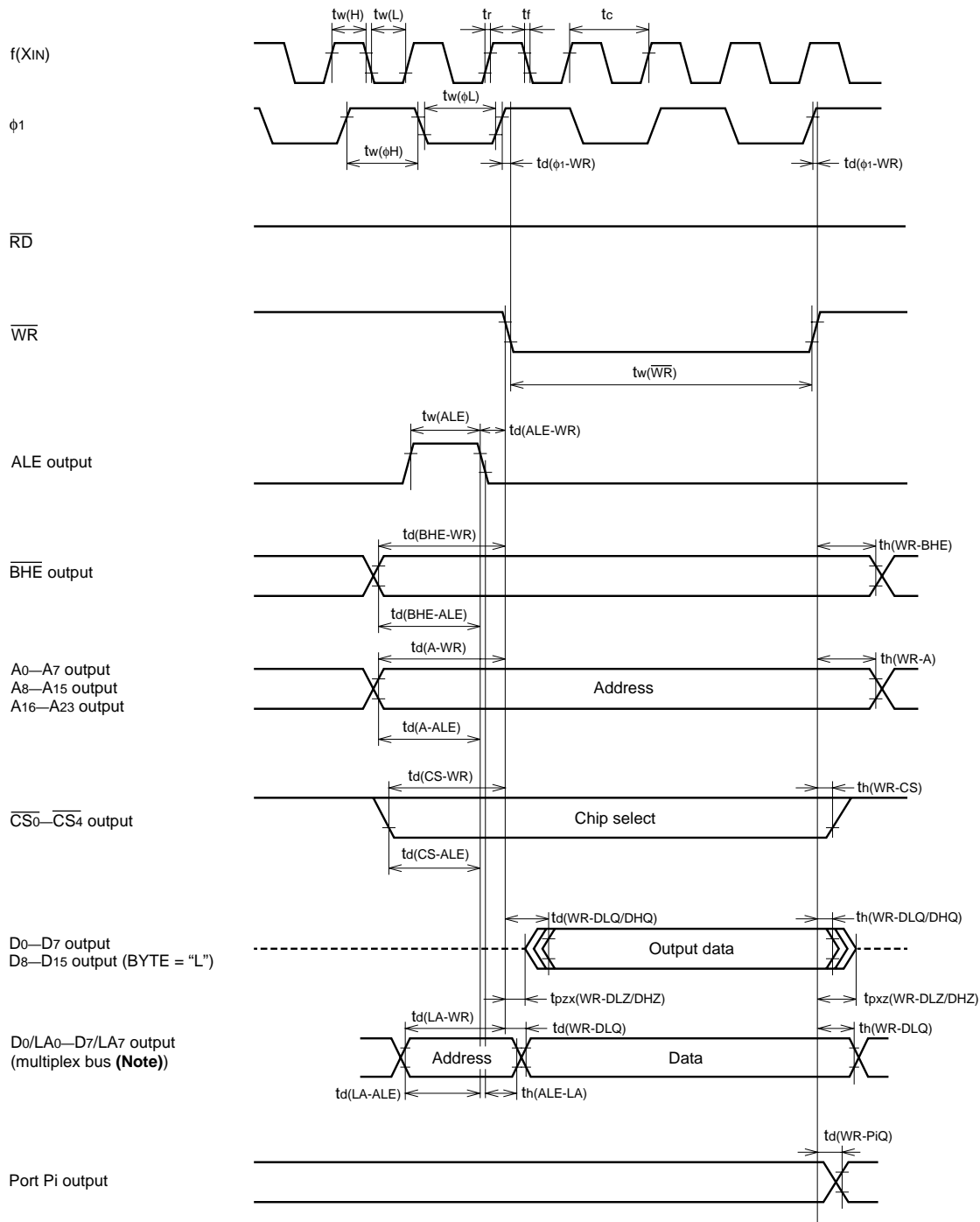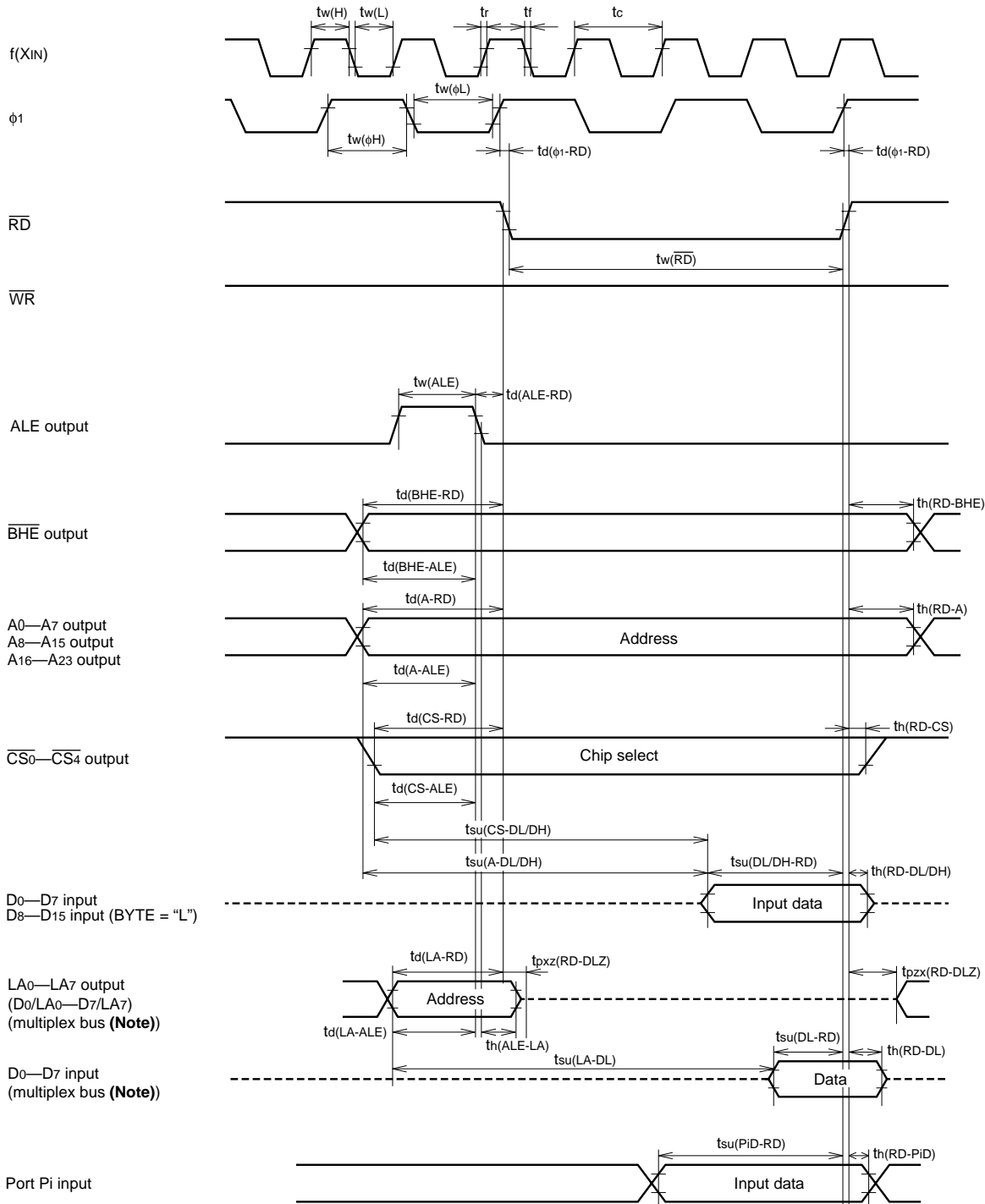
Test conditions (except Port Pi, f($X_{IN}$))
- $V_{CC}$ = 5 V±10 %
- Output timing voltage : $V_{OL}$ = 0.8 V, $V_{OH}$ = 2.0 V, $C_L$ = 100 pF
- Data input : $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.5 V

Test conditions (Port Pi, f($X_{IN}$))
- $V_{CC}$ = 5 V±10 %
- Input timing voltage : $V_{IL}$ = 1.0 V, $V_{IH}$ = 4.0 V
- Output timing voltage : $V_{OL}$ = 0.8 V, $V_{OH}$ = 2.0 V, $C_L$ = 100 pF

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(when 2-$\phi$ access in low-speed running <Read>)



**Note:** These become a multiplex bus only when all of the following conditions are satisfied:
  • BYTE = "H"
  • Multiplex bus select bit = "1"
  • While the address which corresponds to chip select signal $\overline{CS}_4$ is accessed
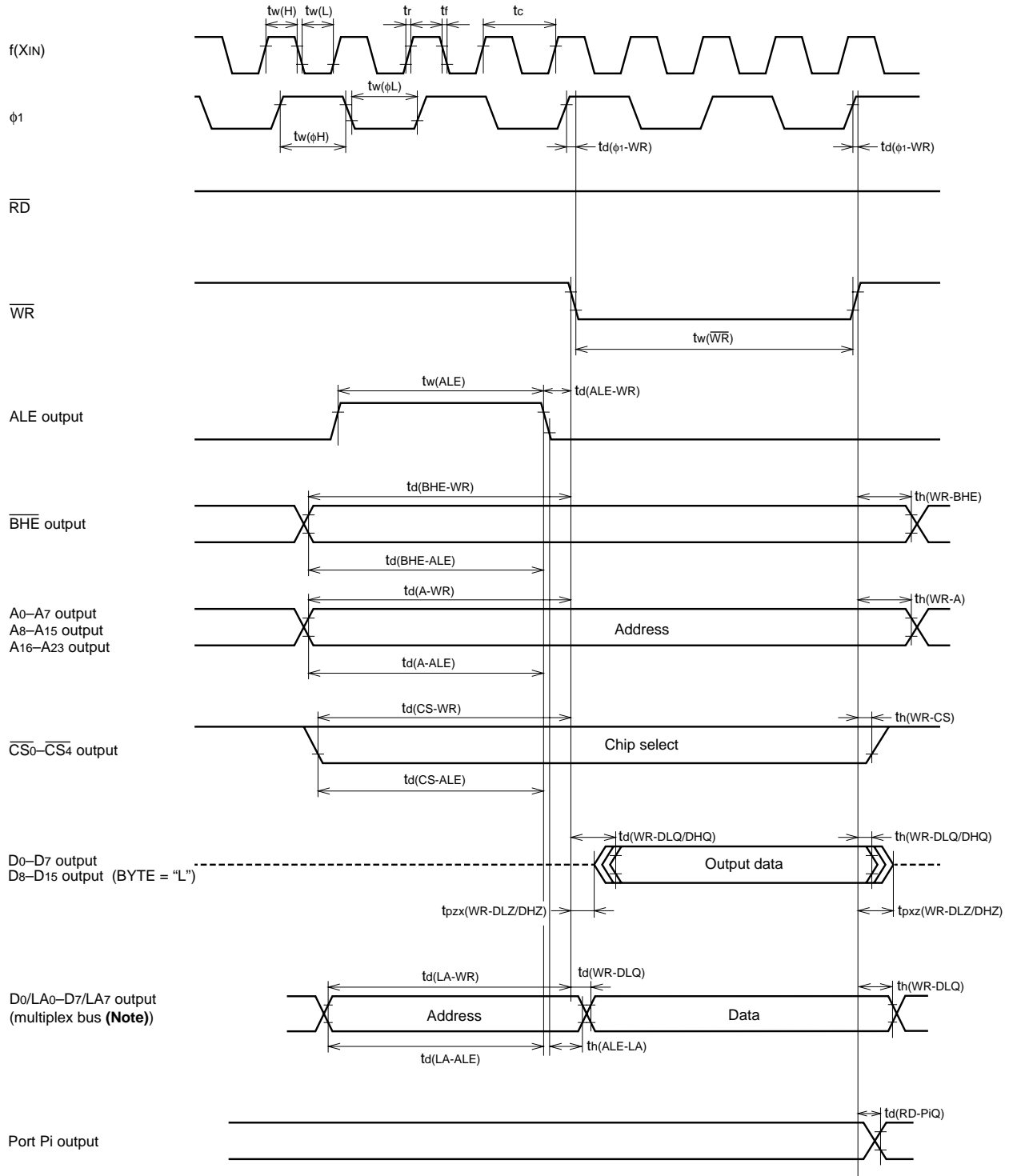
Test conditions (except Port Pi, f(XIN))
  • $V_{CC}$ = 5 V±10 %
  • Output timing voltage : $V_{OL}$ = 0.8 V, $V_{OH}$ = 2.0 V, $C_L$ = 100 pF
  • Data input : $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.5 V

Test conditions (Port Pi, f(XIN))
  • $V_{CC}$ = 5 V±10 %
  • Input timing voltage : $V_{IL}$ = 1.0 V, $V_{IH}$ = 4.0 V
  • Output timing voltage : $V_{OL}$ = 0.8 V, $V_{OH}$ = 2.0 V, $C_L$ = 100 pF

SHINGLE-CHIP 16-BIT CMOS MICROCOMPUTER FLASH MEMORY VERSION

(when 3-$\phi$ access in low-speed running <Write>)



**Note:** These become a multiplex bus only when all of the following conditions are satisfied:
- BYTE = "H"
- Multiplex bus select bit = "1"
- While the address which corresponds to chip select signal $\overline{CS_4}$ is accessed
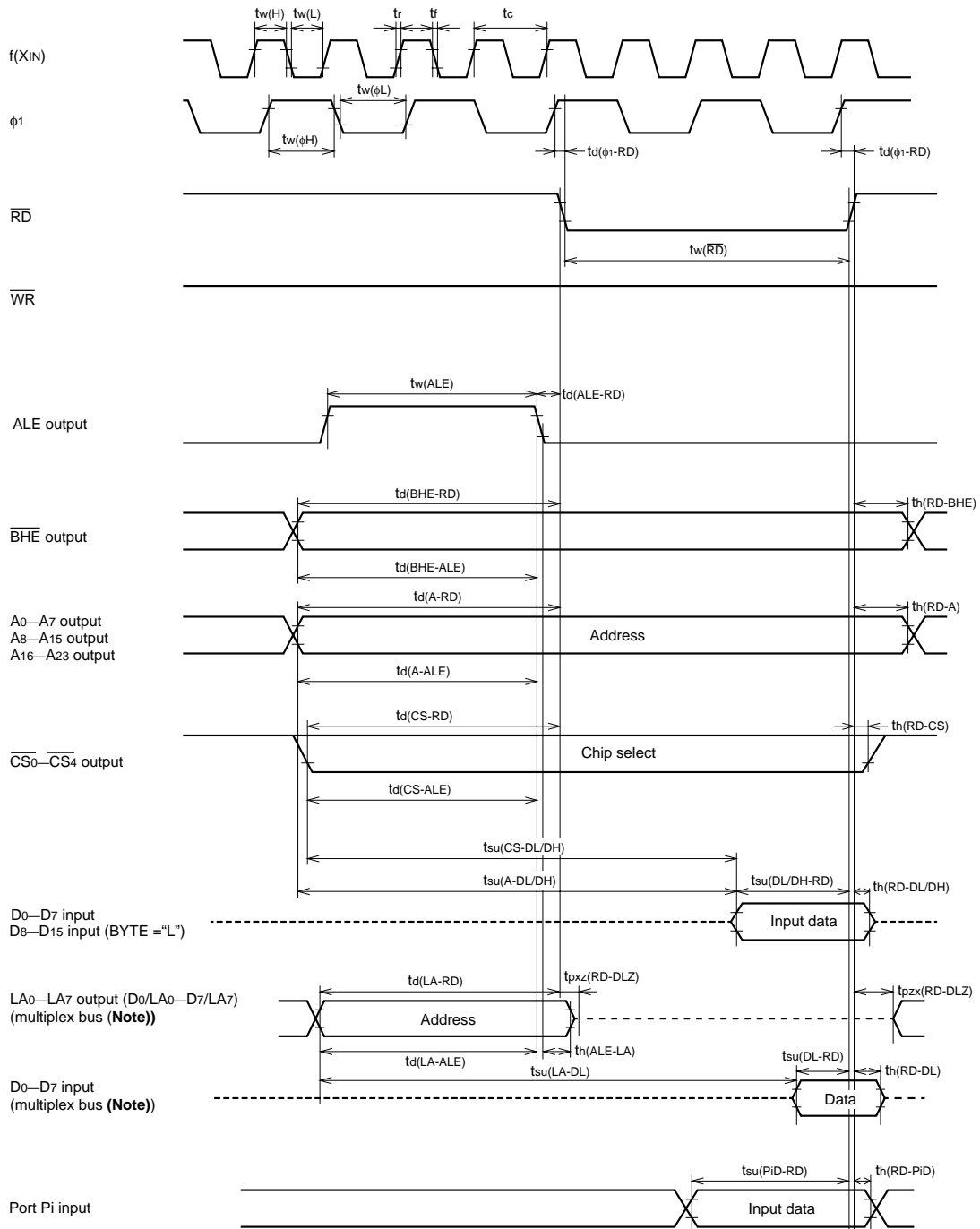
Test conditions (except Port Pi, f(X$_{IN}$))
- V$_{CC}$ = 5 V±10 %
- Output timing voltage : V$_{OL}$ = 0.8 V, V$_{OH}$ = 2.0 V, C$_L$ = 100 pF
- Data input : V$_{IL}$ = 0.8 V, V$_{IH}$ = 2.5 V

Test conditions (Port Pi, f(X$_{IN}$))
- V$_{CC}$ = 5 V±10 %
- Input timing voltage : V$_{IL}$ = 1.0 V, V$_{IH}$ = 4.0 V
- Output timing voltage : V$_{OL}$ = 0.8 V, V$_{OH}$ = 2.0 V, C$_L$ = 100 pF

MITSUBISHI ELECTRIC

(when 3-$\phi$ access in low-speed running <Read>)



**Note:** These become a multiplex bus only when all of the following conditions are satisfied:
- BYTE = "H"
- Multiplex bus select bit = "1"
- While the address which corresponds to chip select signal $\overline{CS4}$ is accessed

Test conditions (except Port Pi, f(XIN))
- VCC = 5 V±10 %
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V, CL = 100 pF
- Data input : VIL = 0.8 V, VIH = 2.5 V

Test conditions (Port Pi, f(XIN))
- VCC = 5 V±10 %
- Input timing voltage : VIL = 1.0 V, VIH = 4.0 V
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V, CL = 100 pF

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(when 4-$\phi$ access in low-speed running <Write>)



**Note:** These become a multiplex bus only when all of the following conditions are satisfied:
- BYTE = "H"
- Multiplex bus select bit = "1"
- While the address which corresponds to chip select signal $\overline{CS_4}$ is accessed

Test conditions (except Port Pi, f(XIN))
- VCC = 5 V±10 %
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V, CL = 100 pF
- Data input : VIL = 0.8 V, VIH = 2.5 V

Test conditions (Port Pi, f(XIN))
- VCC = 5 V±10 %
- Input timing voltage : VIL = 1.0 V, VIH = 4.0 V
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V, CL = 100 pF

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(when 4-$\phi$ access in low-speed running <Read>)

tw(H)  tw(L)  tr  tf  tc

f(XIN)

tw($\phi$L)

$\phi$1

tw($\phi$H)    td($\phi$1-RD)    td($\phi$1-RD)

RD

tw(RD)

WR

tw(ALE)    td(ALE-RD)

ALE output

td(BHE-RD)    th(RD-BHE)

BHE output

td(BHE-ALE)

td(A-RD)    th(RD-A)

A0—A7 output
A8—A15 output    Address
A16—A23 output

td(A-ALE)

td(CS-RD)    th(RD-CS)

CS0—CS4 output    Chip select

td(CS-ALE)

tsu(CS-DL/DH)

tsu(A-DL/DH)    tsu(DL/DH-RD)  th(RD-DL/DH)

D0—D7 input
D8—D15 input (BYTE ="L")    Input data

td(LA-RD)    tpxz(RD-DLZ)    tpzx(RD-DLZ)

LA0—LA7 output (D0/LA0—D7/LA7)
(multiplex bus (**Note**))    Address

td(LA-ALE)    th(ALE-LA)    tsu(DL-RD)  th(RD-DL)
tsu(LA-DL)

D0—D7 input
(multiplex bus (**Note**))    Data

tsu(PiD-RD)    th(RD-PiD)

Port Pi input    Input data

**Note:** These become a multiplex bus only when all of the following conditions are satisfied:
• BYTE = "H"
• Multiplex bus select bit = "1"
• While the address which corresponds to chip select signal CS4 is accessed

Test conditions (except Port Pi, f(XIN))
• VCC = 5 V±10 %
• Output timing voltage : VOL = 0.8 V, VOH = 2.0 V, CL = 100 pF
• Data input : VIL = 0.8 V, VIH = 2.5 V

Test conditions (Port Pi, f(XIN))
• VCC = 5 V±10 %
• Input timing voltage : VIL = 1.0 V, VIH = 4.0 V
• Output timing voltage : VOL = 0.8 V, VOH = 2.0 V, CL = 100 pF

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## Timing requirements

(Vcc = 5 V±10 %, Vss = 0 V, Ta = –20 to 85 °C, f(XIN)=40 MHz when the clock source select bit = "0"[*], unless otherwise noted)

[*] The rise and fall time of input signal must be 100 ns or less respectively, unless otherwise noted.

**Memory expansion and Microprocessor mode : High-speed running**

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_c$ | External clock input cycle time **(Note 1)** | 25 | | ns |
| $t_{w(H)}$ | External clock input high-level pulse width **(Note 2)** | $t_c/2 - 8$ | | ns |
| $t_{w(L)}$ | External clock input low-level pulse width **(Note 2)** | $t_c/2 - 8$ | | ns |
| $t_r$ | External clock rise time | | 8 | ns |
| $t_f$ | External clock fall time | | 8 | ns |
| $t_{su(DH-RD)}$ | High-order data input setup time (BYTE = "L") | 30 | | ns |
| $t_{su(DL-RD)}$ | Low-order data input setup time | 30 | | ns |
| $t_{su(PiD-RD)}$ | Port Pi input setup time (i = 4—9, 11) | 60 | | ns |
| $t_{h(RD-DH)}$ | High-order data input hold time (BYTE = "L") | 0 | | ns |
| $t_{h(RD-DL)}$ | Low-order data input hold time | 0 | | ns |
| $t_{h(RD-PiD)}$ | Port Pi input hold time (i = 4—9, 11) | 0 | | ns |
| $t_{su(A-DL/DH)}$ | Data setup time with address stabilized **(Note 3)** | | 65 (3-$\phi$ access) | ns |
| | | | 110 (4-$\phi$ access) | |
| | | | 160 (5-$\phi$ access) | |
| $t_{su(CS-DL/DH)}$ | Data setup time with chip select stabilized **(Note 3)** | | 65 (3-$\phi$ access) | ns |
| | | | 110 (4-$\phi$ access) | |
| | | | 160 (5-$\phi$ access) | |
| $t_{su(LA-DL)}$ | Data setup time with address stabilized **(Note 3)** | | 50 (3-$\phi$ access) | ns |
| | | | 100 (4-$\phi$ access) | |
| | | | 150 (5-$\phi$ access) | |

[*]: f(XIN) = 20 MHz when the clock source selet bit = "1"

**Notes 1:** When the clock source select bit = "1", $t_c$'s minimum limit is 50 ns.

**2:** When the clock source select bit = "1", set $t_{w(H)}/t_c$ and $t_{w(L)}/t_c$ ratios to 45 to 55 %.

**3:** Since the values depend on external clock input frequency f(XIN), calculate them using the bus timing data formula on the page after the next page.

## Switching characteristics (Vcc = 5 V±10 %, Vss = 0 V, Ta = –20 to 85 °C, f(XIN) = 40 MHz when the clock source select bit = "0"*, unless otherwise noted)

**Memory expansion and Microprocessor mode : High-speed running**

| Symbol | Parameter | | 3-$\phi$ access Min. | 3-$\phi$ access Max. | 4-$\phi$ access Min. | 4-$\phi$ access Max. | 5-$\phi$ access Min. | 5-$\phi$ access Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| tw($\phi$H), tw($\phi$L) | $\phi$ high-level pulse width, $\phi$ low-level pulse width | **(Note)** | 5 | | 5 | | 5 | | ns |
| td($\phi$1–WR) | WR output delay time | | –7 | 12 | –7 | 12 | –7 | 12 | ns |
| td($\phi$1–RD) | RD output delay time | | –7 | 12 | –7 | 12 | –7 | 12 | ns |
| tw(WR) | WR low-level pulse width | **(Note)** | 55 | | 80 | | 130 | | ns |
| tw(RD) | RD low-level pulse width | **(Note)** | 55 | | 80 | | 130 | | ns |
| td(A–WR) | Address output delay time | **(Note)** | 25 | | 45 | | 45 | | ns |
| td(A–RD) | Address output delay time | **(Note)** | 25 | | 45 | | 45 | | ns |
| td(A–ALE) | Address output delay time | **(Note)** | 10 | | 35 | | 35 | | ns |
| td(BHE–WR) | BHE output delay time | **(Note)** | 25 | | 45 | | 45 | | ns |
| td(BHE–RD) | BHE output delay time | **(Note)** | 25 | | 45 | | 45 | | ns |
| td(BHE–ALE) | BHE output delay time | **(Note)** | 10 | | 35 | | 35 | | ns |
| td(CS–WR) | Chip select output delay time | **(Note)** | 25 | | 45 | | 45 | | ns |
| td(CS–RD) | Chip select output delay time | **(Note)** | 25 | | 45 | | 45 | | ns |
| td(CS–ALE) | Chip select output delay time | **(Note)** | 10 | | 35 | | 35 | | ns |
| td(WR–DLQ/DHQ) | Data output delay time | | | 35 | | 35 | | 35 | ns |
| tpxz(WR–DLZ/DHZ) | Floating start delay time | **(Note)** | | 30 | | 30 | | 30 | ns |
| td(ALE–WR) | ALE output delay time | | 4 | | 4 | | 4 | | ns |
| td(ALE–RD) | ALE output delay time | | 4 | | 4 | | 4 | | ns |
| tw(ALE) | ALE pulse width | **(Note)** | 10 | | 35 | | 35 | | ns |
| th(WR–A) | Address hold time | **(Note)** | 10 | | 10 | | 10 | | ns |
| th(RD–A) | Address hold time | **(Note)** | 10 | | 10 | | 10 | | ns |
| th(WR–BHE) | BHE hold time | **(Note)** | 10 | | 10 | | 10 | | ns |
| th(RD–BHE) | BHE hold time | **(Note)** | 10 | | 10 | | 10 | | ns |
| th(WR–CS) | Chip select hold time | **(Note)** | 10 | | 10 | | 10 | | ns |
| th(RD–CS) | Chip select hold time | **(Note)** | 10 | | 10 | | 10 | | ns |
| th(WR–DLQ/DHQ) | Data hold time | **(Note)** | 15 | | 15 | | 15 | | ns |
| tpzx(WR–DLZ/DHZ) | Floating release delay time | | 0 | | 0 | | 0 | | ns |
| td(LA–WR) | Address output delay time | **(Note)** | 15 | | 40 | | 40 | | ns |
| td(LA–RD) | Address output delay time | **(Note)** | 15 | | 40 | | 40 | | ns |
| td(LA–ALE) | Address output delay time | **(Note)** | 5 | | 30 | | 30 | | ns |
| th(ALE–LA) | Address hold time | **(Note)** | 10 | | 10 | | 10 | | ns |
| tPXZ(RD–DLZ) | Floating start delay time | | | 5 | | 5 | | 5 | ns |
| tPZX(RD–DLZ) | Floating release delay time | **(Note)** | 15 | | 15 | | 15 | | ns |
| td(WR–PiQ) | Port Pi data output delay time (i = 4—9, 11) | | | 60 | | 60 | | 60 | ns |

✳: f(XIN) = 20 MHz when the clock source selet bit = "1"
**Note:** Since the values depend on external clock frequency f(XIN), calculate them by using the bus timing data formulas on the next page.

## Bus timing data formulas

**Memory expansion and Microprocessor mode : High-speed running** ($V_{CC}$ = 5 V±10 %, $V_{SS}$ = 0 V, $T_a$ = –20 to 85 °C, f($X_{IN}$) ≤ 40 MHz when the clock source select bit = "0"[*], unless otherwise noted)

| Symbol | Parameter | 3-$\phi$ access | 4-$\phi$ access | 5-$\phi$ access | Unit |
|---|---|---|---|---|---|
| tsu(A–DL/DH) | Data setup time with address stabilized | $\frac{5 \times 10^9}{f(X_{IN})} - 60$ | $\frac{7 \times 10^9}{f(X_{IN})} - 65$ | $\frac{9 \times 10^9}{f(X_{IN})} - 65$ | ns |
| tsu(CS–DL/DH) | Data setup time with chip select stabilized | $\frac{5 \times 10^9}{f(X_{IN})} - 60$ | $\frac{7 \times 10^9}{f(X_{IN})} - 65$ | $\frac{9 \times 10^9}{f(X_{IN})} - 65$ | ns |
| tw($\phi$H), tw($\phi$L) | $\phi$ high-level pulse width, $\phi$ low-level pulse width | $\frac{1 \times 10^9}{f(X_{IN})} - 20$ | ← | ← | ns |
| tw($\overline{WR}$), tw($\overline{RD}$) | $\overline{WR}$, $\overline{RD}$ low-level pulse width | $\frac{3 \times 10^9}{f(X_{IN})} - 20$ | $\frac{4 \times 10^9}{f(X_{IN})} - 20$ | $\frac{6 \times 10^9}{f(X_{IN})} - 20$ | ns |
| td(A–WR) | Address output delay time | $\frac{2 \times 10^9}{f(X_{IN})} - 25$ | $\frac{3 \times 10^9}{f(X_{IN})} - 30$ | ← | ns |
| td(A–RD) | Address output delay time | $\frac{2 \times 10^9}{f(X_{IN})} - 25$ | $\frac{3 \times 10^9}{f(X_{IN})} - 30$ | ← | ns |
| td(A–ALE) | Address output delay time | $\frac{1 \times 10^9}{f(X_{IN})} - 15$ | $\frac{2 \times 10^9}{f(X_{IN})} - 15$ | ← | ns |
| td(BHE–WR) | $\overline{BHE}$ outuput delay time | $\frac{2 \times 10^9}{f(X_{IN})} - 25$ | $\frac{3 \times 10^9}{f(X_{IN})} - 30$ | ← | ns |
| td(BHE–RD) | $\overline{BHE}$ outuput delay time | $\frac{2 \times 10^9}{f(X_{IN})} - 25$ | $\frac{3 \times 10^9}{f(X_{IN})} - 30$ | ← | ns |
| td(BHE–ALE) | $\overline{BHE}$ outuput delay time | $\frac{1 \times 10^9}{f(X_{IN})} - 15$ | $\frac{2 \times 10^9}{f(X_{IN})} - 15$ | ← | ns |
| td(CS–WR) | Chip select output delay time | $\frac{2 \times 10^9}{f(X_{IN})} - 25$ | $\frac{3 \times 10^9}{f(X_{IN})} - 30$ | ← | ns |
| td(CS–RD) | Chip select output delay time | $\frac{2 \times 10^9}{f(X_{IN})} - 25$ | $\frac{3 \times 10^9}{f(X_{IN})} - 30$ | ← | ns |
| td(CS–ALE) | Chip select output delay time | $\frac{1 \times 10^9}{f(X_{IN})} - 15$ | $\frac{2 \times 10^9}{f(X_{IN})} - 15$ | ← | ns |
| tw(ALE) | ALE pulse width | $\frac{1 \times 10^9}{f(X_{IN})} - 15$ | $\frac{2 \times 10^9}{f(X_{IN})} - 15$ | ← | ns |
| th(WR–A) | Address hold time | $\frac{1 \times 10^9}{f(X_{IN})} - 15$ | ← | ← | ns |
| th(RD–A) | Address hold time | $\frac{1 \times 10^9}{f(X_{IN})} - 15$ | ← | ← | ns |
| td(WR–BHE) | $\overline{BHE}$ hold time | $\frac{1 \times 10^9}{f(X_{IN})} - 15$ | ← | ← | ns |
| td(RD–BHE) | $\overline{BHE}$ hold time | $\frac{1 \times 10^9}{f(X_{IN})} - 15$ | ← | ← | ns |
| td(WR–CS) | Chip select hold time | $\frac{1 \times 10^9}{f(X_{IN})} - 15$ | ← | ← | ns |
| td(RD–CS) | Chip select hold time | $\frac{1 \times 10^9}{f(X_{IN})} - 15$ | ← | ← | ns |
| th(WR–DLQ/DHQ) | Data hold time | $\frac{1 \times 10^9}{f(X_{IN})} - 10$ | ← | ← | ns |
| tpxz(WR–DLZ/DHZ) | Floating start delay time | $\frac{1 \times 10^9}{f(X_{IN})} + 5$ | ← | ← | ns |
| tsu(LA–DL) | Data setup time with address stabilized | $\frac{5 \times 10^9}{f(X_{IN})} - 75$ | $\frac{7 \times 10^9}{f(X_{IN})} - 75$ | $\frac{9 \times 10^9}{f(X_{IN})} - 75$ | ns |
| td(LA–WR) | Address output delay time | $\frac{2 \times 10^9}{f(X_{IN})} - 35$ | $\frac{3 \times 10^9}{f(X_{IN})} - 35$ | ← | ns |
| td(LA–RD) | Address output delay time | $\frac{2 \times 10^9}{f(X_{IN})} - 35$ | $\frac{3 \times 10^9}{f(X_{IN})} - 35$ | ← | ns |
| td(LA–ALE) | Address output delay time | $\frac{1 \times 10^9}{f(X_{IN})} - 20$ | $\frac{2 \times 10^9}{f(X_{IN})} - 20$ | ← | ns |
| td(ALE–LA) | Address hold time | $\frac{1 \times 10^9}{f(X_{IN})} - 15$ | ← | ← | ns |
| tpzx(RD–DLZ) | Floating release delay time | $\frac{1 \times 10^9}{f(X_{IN})} - 10$ | ← | ← | ns |

✱: f($X_{IN}$) ≤ 20 MHz when the clock source select bit = "1"

**Note:** When the clock source select bit is "1", regard f($X_{IN}$) in tables as 2·f($X_{IN}$).

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(when 3-$\phi$ access in high-speed running <Write>)



**Note:** These become a multiplex bus only when all of the following conditions are satisfied:
- BYTE = "H"
- Multiplex bus select bit = "1"
- While the address which corresponds to chip select signal $\overline{CS_4}$ is accessed
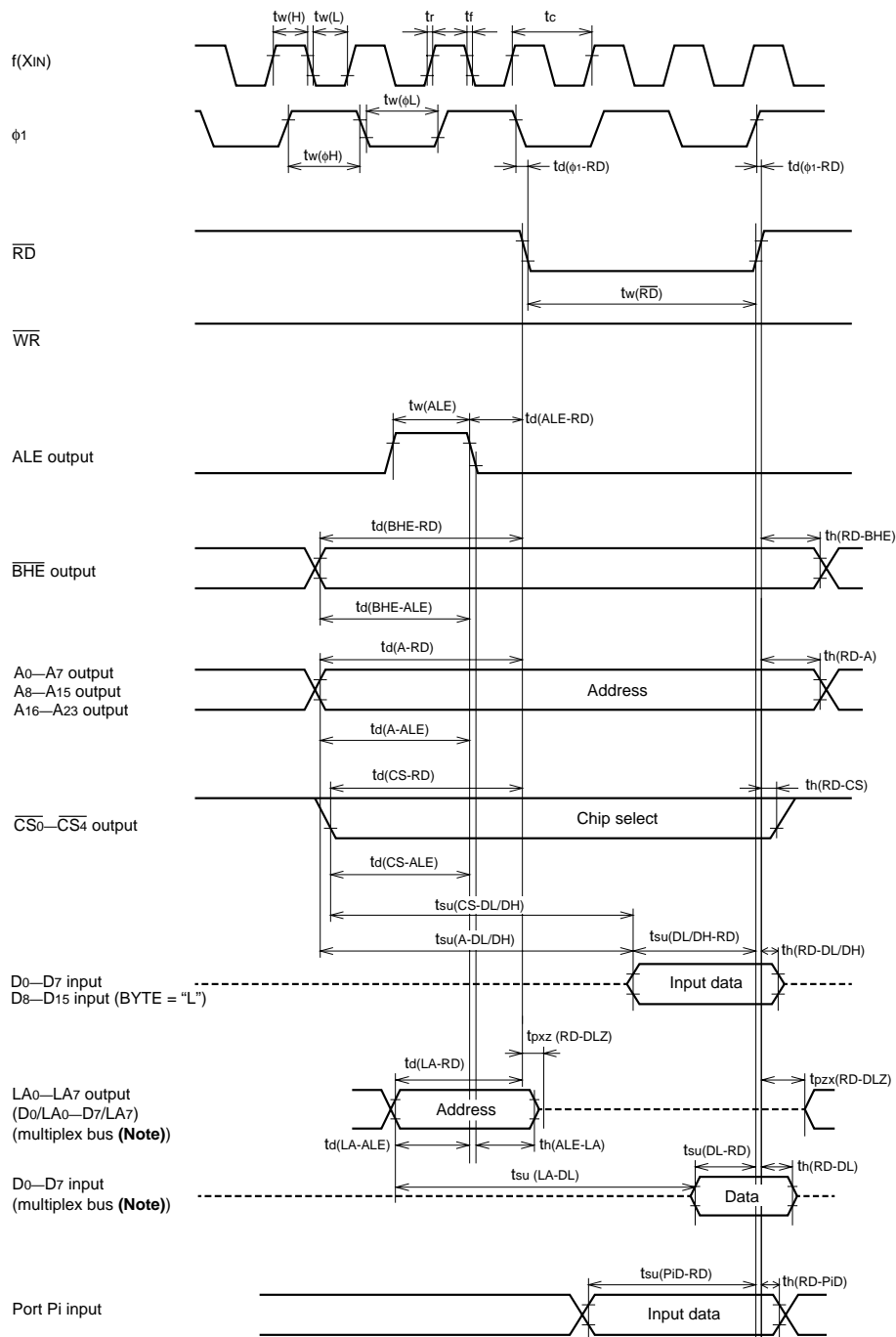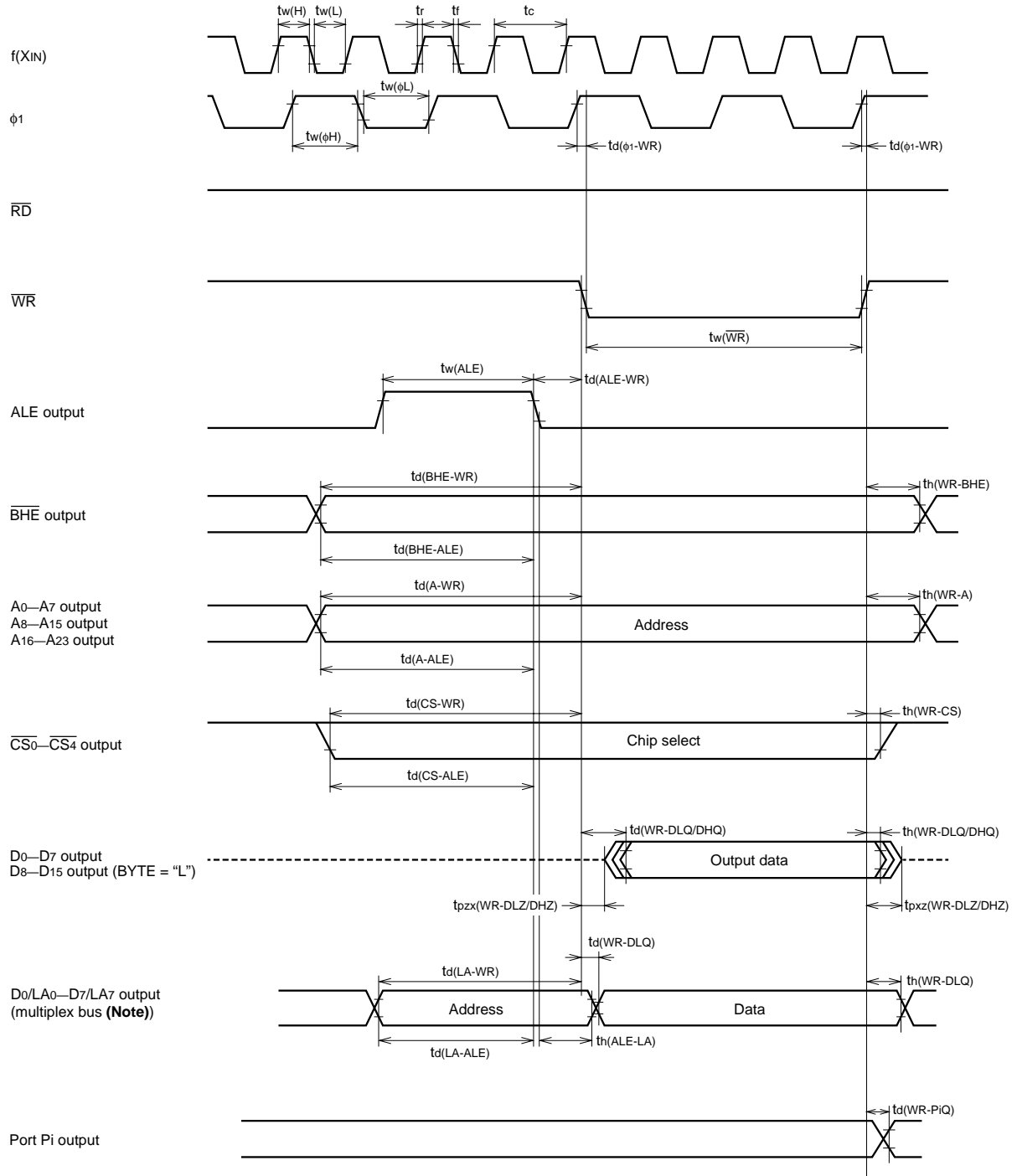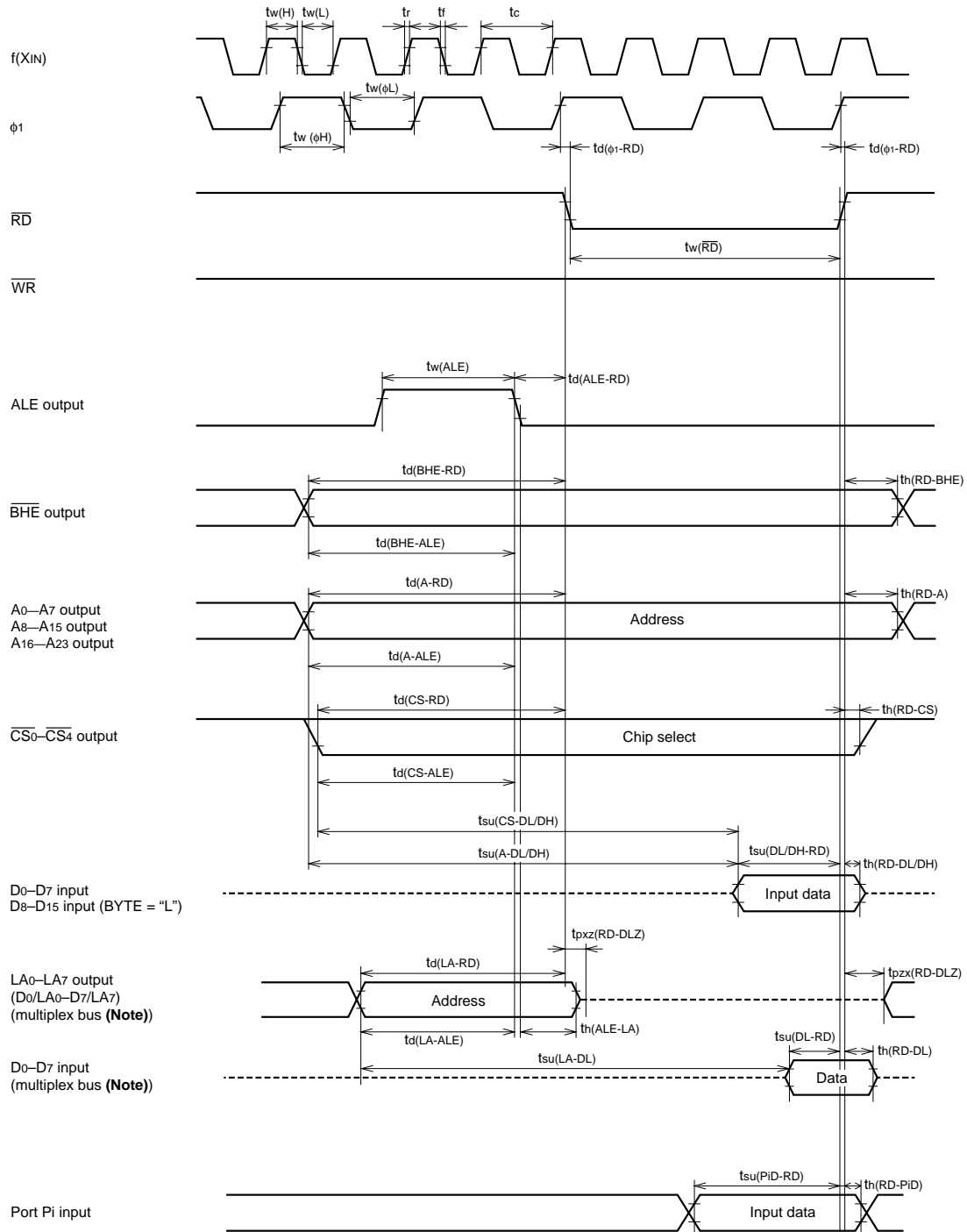
Test conditions (except Port Pi, f(XIN))
- VCC = 5 V±10 %
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V, CL = 100 pF
- Data input : VIL = 0.8 V, VIH = 2.5 V

Test conditions (Port Pi, f(XIN))
- VCC = 5 V±10 %
- Input timing voltage : VIL = 1.0 V, VIH = 4.0 V
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V, CL = 100 pF

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

(when 3-$\phi$ access in high-speed running <Read>)

f(XIN)

$\phi 1$

$\overline{RD}$

$\overline{WR}$

ALE output

$\overline{BHE}$ output

A0—A7 output
A8—A15 output
A16—A23 output

$\overline{CS0}$—$\overline{CS4}$ output

D0—D7 input
D8—D15 input (BYTE = "L")

LA0—LA7 output
(D0/LA0—D7/LA7)
(multiplex bus **(Note)**)

D0—D7 input
(multiplex bus **(Note)**)

Port Pi input

tw(H) tw(L)  tr tf  tc
tw($\phi$L)
tw($\phi$H)
td($\phi$1-RD)
tw($\overline{RD}$)
tw(ALE)  td(ALE-RD)
td(BHE-RD)  th(RD-BHE)
td(BHE-ALE)
td(A-RD)  th(RD-A)
Address
td(A-ALE)
td(CS-RD)  th(RD-CS)
Chip select
td(CS-ALE)
tsu(CS-DL/DH)
tsu(A-DL/DH)  tsu(DL/DH-RD)  th(RD-DL/DH)
Input data
tpxz (RD-DLZ)
td(LA-RD)  tpzx(RD-DLZ)
Address
td(LA-ALE)  th(ALE-LA)  tsu(DL-RD)  th(RD-DL)
tsu(LA-DL)  Data
tsu(PiD-RD)  th(RD-PiD)
Input data

**Note:** These become a multiplex bus only when all of the following conditions are satisfied:
- BYTE = "H"
- Multiplex bus select bit = "1"
- While the address which corresponds to chip select signal $\overline{CS4}$ is accessed
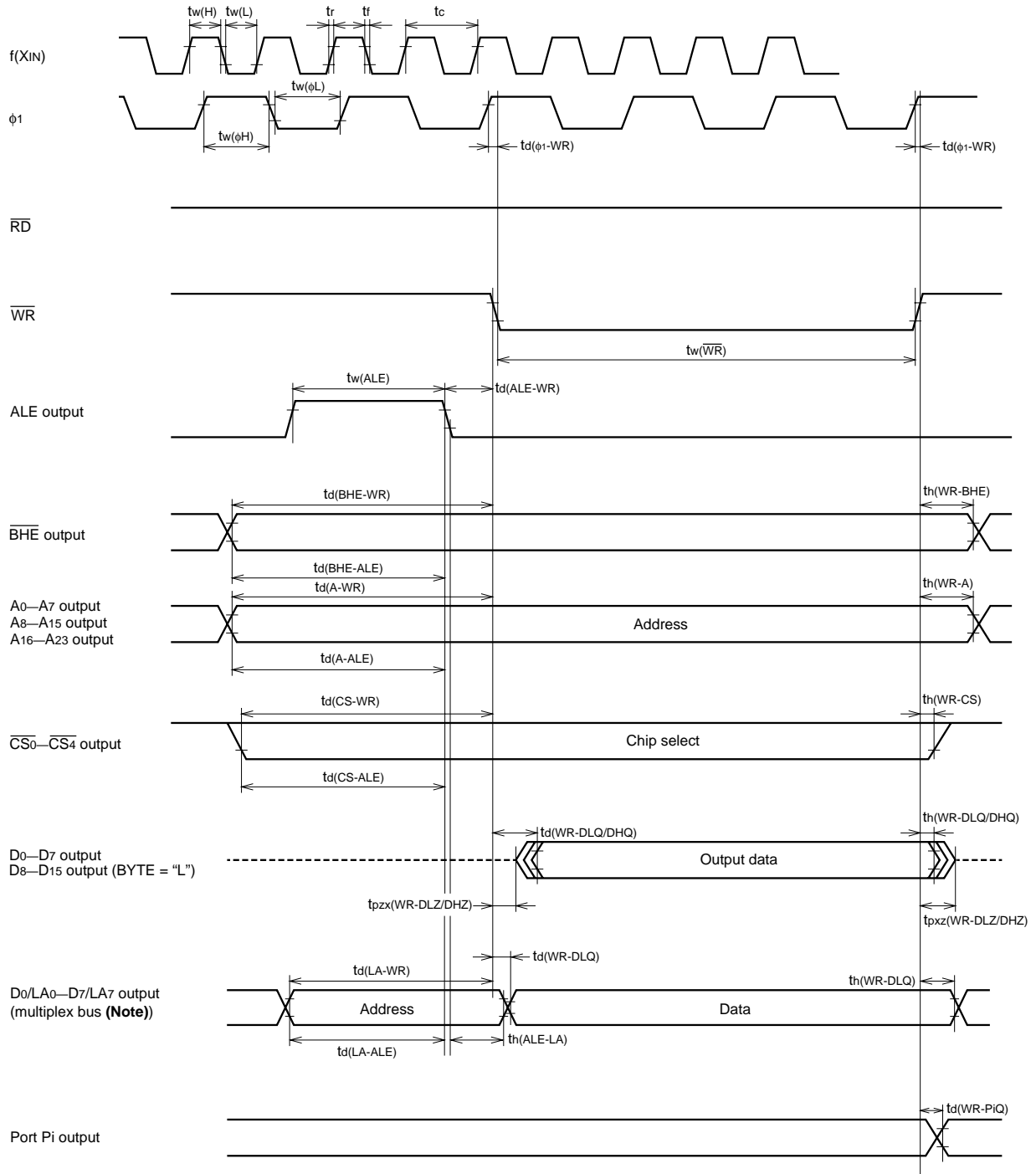
Test conditions (except Port Pi, f(XIN))
- Vcc = 5 V±10 %
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V, CL = 100 pF
- Data input : VIL = 0.8 V, VIH = 2.5 V

Test conditions (Port Pi, f(XIN))
- Vcc = 5 V±10 %
- Input timing voltage : VIL = 1.0 V, VIH = 4.0 V
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V, CL = 100 pF

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(when 4-$\phi$ access in high-speed running <Write>)



**Note:** These become a multiplex bus only when all of the following conditions are satisfied:
- BYTE = "H"
- Multiplex bus select bit = "1"
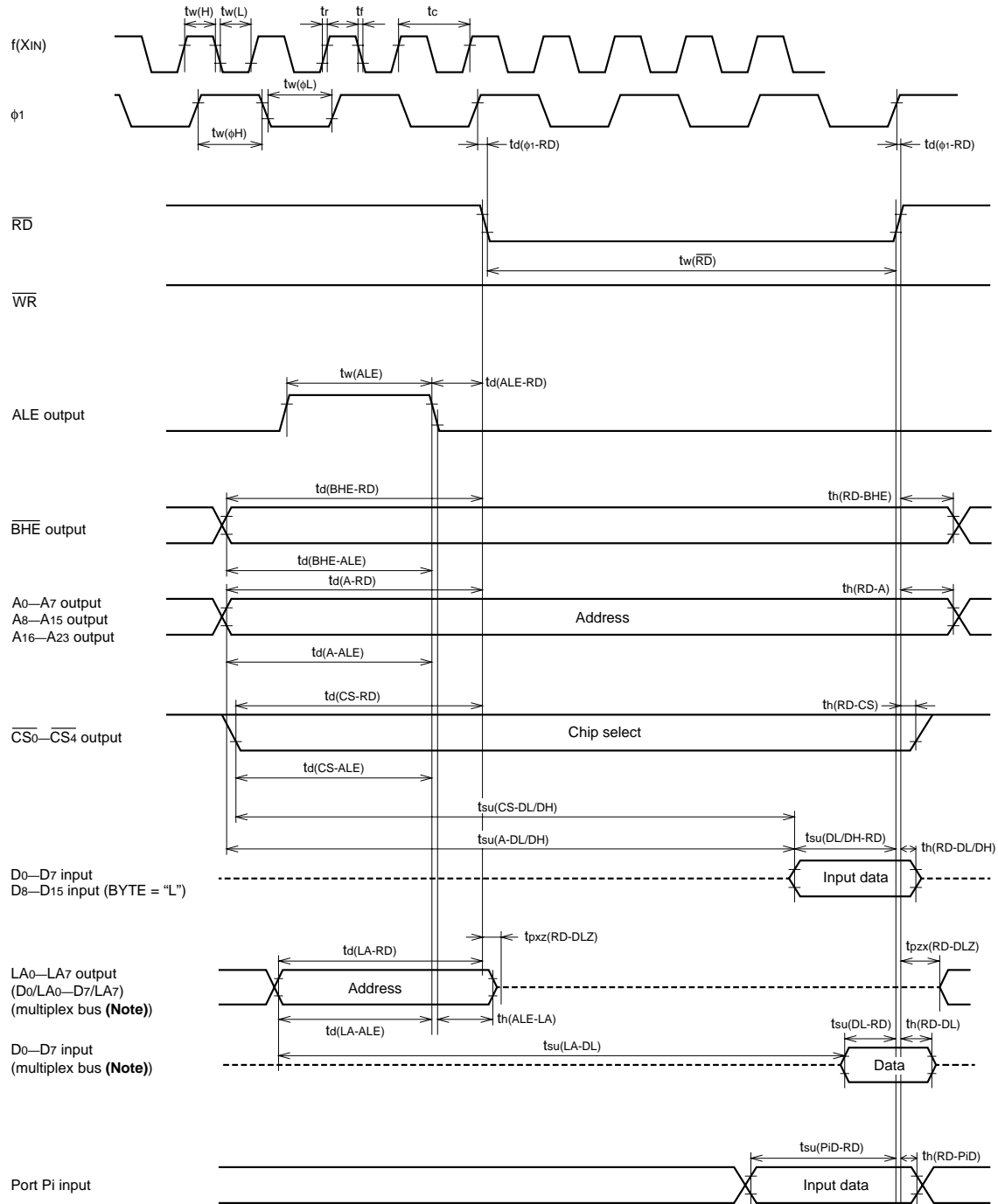- While the address which corresponds to chip select signal $\overline{CS_4}$ is accessed

Test conditions (except Port Pi, f(X$_{IN}$))
- $V_{CC}$ = 5 V±10 %
- Output timing voltage : $V_{OL}$ = 0.8 V, $V_{OH}$ = 2.0 V, $C_L$ = 100 pF
- Data input : $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.5 V

Test conditions (Port Pi, f(X$_{IN}$))
- $V_{CC}$ = 5 V±10 %
- Input timing voltage : $V_{IL}$ = 1.0 V, $V_{IH}$ = 4.0 V
- Output timing voltage : $V_{OL}$ = 0.8 V, $V_{OH}$ = 2.0 V, $C_L$ = 100 pF

(when 4-$\phi$ access in high-speed running <Read>)



f(XIN)
$\phi$1
$\overline{RD}$
$\overline{WR}$
ALE output
$\overline{BHE}$ output
A0—A7 output
A8—A15 output
A16—A23 output
$\overline{CS0}$–$\overline{CS4}$ output
D0–D7 input
D8–D15 input (BYTE = "L")
LA0–LA7 output
(D0/LA0–D7/LA7)
(multiplex bus **(Note)**)
D0–D7 input
(multiplex bus **(Note)**)
Port Pi input

Address · Chip select · Input data · Data

Timing parameters shown: tw(H), tw(L), tr, tf, tc, tw($\phi$L), tw($\phi$H), td($\phi$1-RD), tw($\overline{RD}$), tw(ALE), td(ALE-RD), td(BHE-RD), th(RD-BHE), td(BHE-ALE), td(A-RD), th(RD-A), td(A-ALE), td(CS-RD), th(RD-CS), td(CS-ALE), tsu(CS-DL/DH), tsu(A-DL/DH), tsu(DL/DH-RD), th(RD-DL/DH), tpxz(RD-DLZ), td(LA-RD), tpzx(RD-DLZ), th(ALE-LA), td(LA-ALE), tsu(LA-DL), tsu(DL-RD), th(RD-DL), tsu(PiD-RD), th(RD-PiD)

**Note:** These become a multiplex bus only when all of the following conditions are satisfied:
- BYTE = "H"
- Multiplex bus select bit = "1"
- While the address which corresponds to chip select signal $\overline{CS4}$ is accessed

Test conditions (except Port Pi, f(XIN))
- VCC = 5 V±10 %
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V, CL = 100 pF
- Data input : VIL = 0.8 V, VIH = 2.5 V

Test conditions (Port Pi, f(XIN))
- VCC = 5 V±10 %
- Input timing voltage : VIL = 1.0 V, VIH = 4.0 V
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V, CL = 100 pF

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

(when 5-$\phi$ access in high-speed running <Write>)



**Note:** These become a multiplex bus only when all of the following conditions are satisfied:
- BYTE = "H"
- Multiplex bus select bit = "1"
- While the address which corresponds to chip select signal $\overline{CS_4}$ is accessed

Test conditions (except Port Pi, f(XIN))
- $V_{CC}$ = 5 V±10 %
- Output timing voltage : $V_{OL}$ = 0.8 V, $V_{OH}$ = 2.0 V, $C_L$ = 100 pF
- Data input : $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.5 V

Test conditions (Port Pi, f(XIN))
- $V_{CC}$ = 5 V±10 %
- Input timing voltage : $V_{IL}$ = 1.0 V, $V_{IH}$ = 4.0 V
- Output timing voltage : $V_{OL}$ = 0.8 V, $V_{OH}$ = 2.0 V, $C_L$ = 100 pF

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(when 5-$\phi$ access in high-speed running <Read>)



**Note:** These become a multiplex bus only when all of the following conditions are satisfied:
- BYTE = "H"
- Multiplex bus select bit = "1"
- While the address which corresponds to chip select signal $\overline{CS_4}$ is accessed

Test conditions (except Port Pi, f(XIN))
- $V_{CC}$ = 5 V±10 %
- Output timing voltage : $V_{OL}$ = 0.8 V, $V_{OH}$ = 2.0 V, $C_L$ = 100 pF
- Data input : $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.5 V

Test conditions (Port Pi, f(XIN))
- $V_{CC}$ = 5 V±10 %
- Input timing voltage : $V_{IL}$ = 1.0 V, $V_{IH}$ = 4.0 V
- Output timing voltage : $V_{OL}$ = 0.8 V, $V_{OH}$ = 2.0 V, $C_L$ = 100 pF

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PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

## <NOTE> External bus timing when internal memory area is accessed (2-$\phi$ access) in high-speed running

($V_{CC}$ = 5 V±10 %, $V_{SS}$ = 0 V, $T_a$ = −20 to 85 °C, f($X_{IN}$) ≤ 40 MHz when the clock source select bit = "0"*)

| Symbol | Parameter | f ($X_{IN}$) = 40 MHz** | | Bus timing data formula | Unit |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $t_{w(\phi H)}$, $t_{w(\phi L)}$ | $\phi$ high-level pulse width, $\phi$ low-level pulse width | 5 | | $\dfrac{1 \times 10^9}{f(X_{IN})} - 20$ | ns |
| $t_{d(\phi1-WR)}$ | $\overline{WR}$ output delay time | −7 | 12 | | ns |
| $t_{d(\phi1-RD)}$ | $\overline{RD}$ output delay time | −7 | 12 | | ns |
| $t_{w(\overline{WR})}$ | $\overline{WR}$ low-level pulse width | 5 | | $\dfrac{1 \times 10^9}{f(X_{IN})} - 20$ | ns |
| $t_{w(\overline{RD})}$ | $\overline{RD}$ low-level pulse width | 5 | | $\dfrac{1 \times 10^9}{f(X_{IN})} - 20$ | ns |
| $t_{d(A-WR)}$ | Address output delay time | 25 | | $\dfrac{2 \times 10^9}{f(X_{IN})} - 25$ | ns |
| $t_{d(A-RD)}$ | Address output delay time | 25 | | $\dfrac{2 \times 10^9}{f(X_{IN})} - 25$ | ns |
| $t_{d(A-ALE)}$ | Address output delay time | 10 | | $\dfrac{2 \times 10^9}{f(X_{IN})} - 40$ | ns |
| $t_{d(BHE-WR)}$ | $\overline{BHE}$ output delay time | 25 | | $\dfrac{2 \times 10^9}{f(X_{IN})} - 25$ | ns |
| $t_{d(BHE-RD)}$ | $\overline{BHE}$ output delay time | 25 | | $\dfrac{2 \times 10^9}{f(X_{IN})} - 25$ | ns |
| $t_{d(BHE-ALE)}$ | $\overline{BHE}$ output delay time | 10 | | $\dfrac{2 \times 10^9}{f(X_{IN})} - 40$ | ns |
| $t_{d(CS-WR)}$ | Chip select output delay time | 25 | | $\dfrac{2 \times 10^9}{f(X_{IN})} - 25$ | ns |
| $t_{d(CS-RD)}$ | Chip select output delay time | 25 | | $\dfrac{2 \times 10^9}{f(X_{IN})} - 25$ | ns |
| $t_{d(CS-ALE)}$ | Chip select output delay time | 10 | | $\dfrac{2 \times 10^9}{f(X_{IN})} - 40$ | ns |
| $t_{d(WR-DLQ/DHQ)}$ | Data output delay time | | 35 | ——— | ns |
| $t_{pxz(WR-DLZ/DHZ)}$ | Floating start delay time | 30 | | $\dfrac{1 \times 10^9}{f(X_{IN})} + 5$ | ns |
| $t_{d(ALE-WR)}$ | ALE output delay time | 4 | | ——— | ns |
| $t_{d(ALE-RD)}$ | ALE output delay time | 4 | | ——— | ns |
| $t_{w(ALE)}$ | ALE pulse width | 10 | | $\dfrac{1 \times 10^9}{f(X_{IN})} - 15$ | ns |
| $t_{h(WR-A)}$ | Address hold time | 10 | | $\dfrac{1 \times 10^9}{f(X_{IN})} - 15$ | ns |
| $t_{h(RD-A)}$ | Address hold time | 10 | | $\dfrac{1 \times 10^9}{f(X_{IN})} - 15$ | ns |
| $t_{d(WR-BHE)}$ | $\overline{BHE}$ hold time | 10 | | $\dfrac{1 \times 10^9}{f(X_{IN})} - 15$ | ns |
| $t_{d(RD-BHE)}$ | $\overline{BHE}$ hold time | 10 | | $\dfrac{1 \times 10^9}{f(X_{IN})} - 15$ | ns |
| $t_{d(WR-CS)}$ | Chip select hold time | 10 | | $\dfrac{1 \times 10^9}{f(X_{IN})} - 15$ | ns |
| $t_{d(RD-CS)}$ | Chip select hold time | 10 | | $\dfrac{1 \times 10^9}{f(X_{IN})} - 15$ | ns |
| $t_{h(WR-DLQ/DHQ)}$ | Data hold time | 15 | | $\dfrac{1 \times 10^9}{f(X_{IN})} - 10$ | ns |
| $t_{pzx(WR-DLZ/DHZ)}$ | Floating release delay time | 0 | | ——— | ns |

∗: f($X_{IN}$) ≤ 20 MHz when the clock source select bit = "1".
∗∗: f($X_{IN}$) = 20 MHz when the clock source select bit = "1".

SHINGLE-CHIP 16-BIT CMOS MICROCOMPUTER FLASH MEMORY VERSION

(External bus timing on internal RAM access (2-$\phi$ access) in high-speed running)

f(X$_{IN}$)

$\phi$1

$\overline{RD}$

$\overline{WR}$

ALE output

$\overline{BHE}$ output

A$_0$—A$_7$ output
A$_8$—A$_{15}$ output
A$_{16}$—A$_{23}$ output

Address

$\overline{CS_0}$—$\overline{CS_4}$ output

D$_0$—D$_7$ output
D$_8$—D$_{15}$ output (BYTE = "L")

Hi-Z    Data    Hi-Z
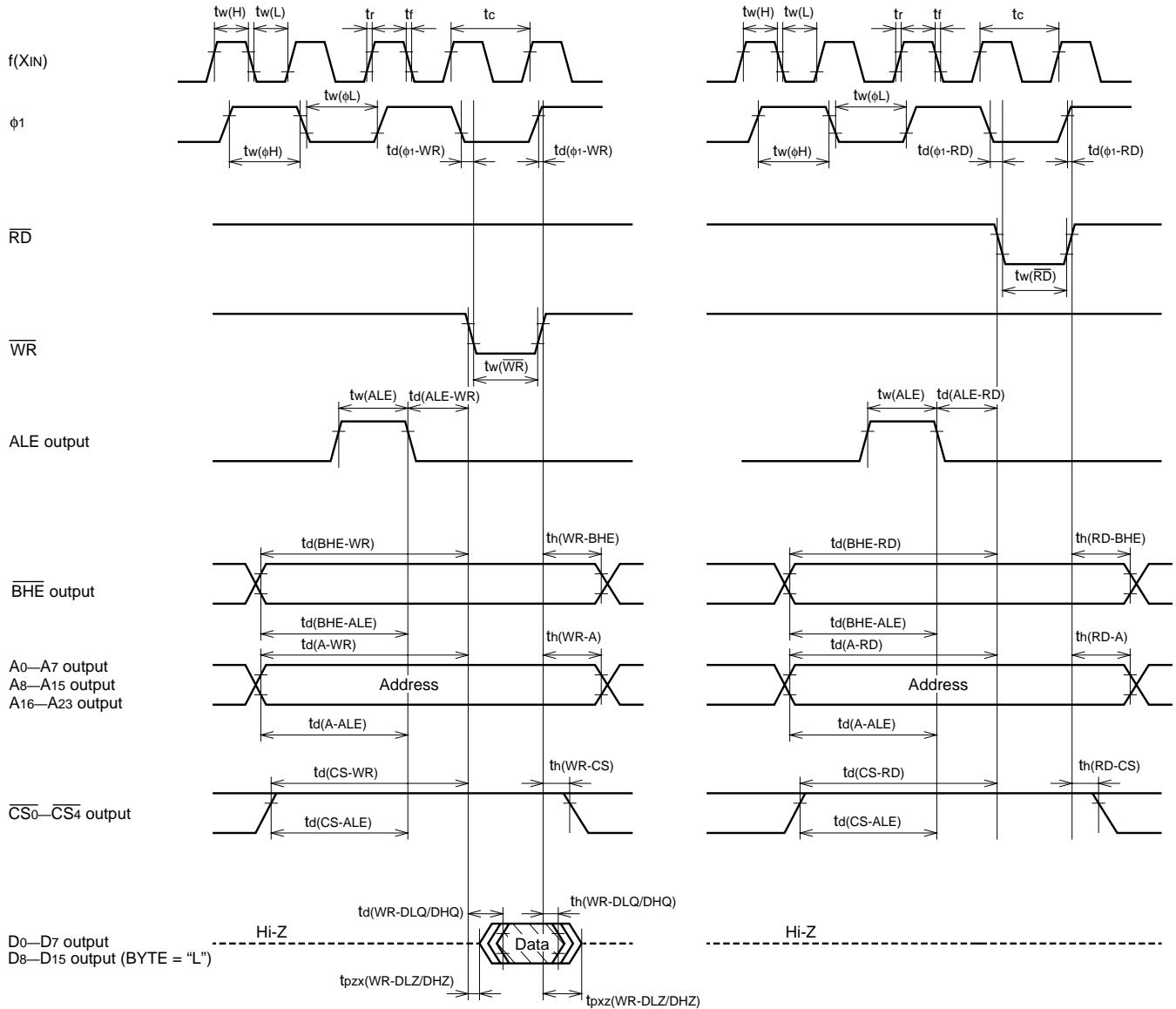
＊ The value of output data is undefined.

Test conditions
• V$_{CC}$ = 5 V±10 %
• Output timing voltage : V$_{OL}$ = 0.8 V, V$_{OH}$ = 2.0 V, C$_L$ = 100 pF

**MITSUBISHI ELECTRIC**

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| REVISION DESCRIPTION LIST | M37754FFCGP, M37754FFCHP DATA SHEET | |
|---|---|---|

| Rev. No. | Revision Description | Rev. date |
|---|---|---|
| 1.0 | First Edition | 971114 |
| 2.00 | (1) For the "timer A write flag (address $45_{16}$)", it's name is corrected:<br><br>• New register name: timer A write <u>register</u><br>• Related pages: pages 11, 12<br><br>(2) For the following register, it's internal status after reset is corrected:<br>• Target register: processor mode register 0 (address $5E_{16}$)<br>• Correction: the status of bit 1 is "0". (Not "1".)<br>• Related page: page 12 | 990428 |