M64403FP

PRELIMINARY

Notice:This is not a final specification.
Some parametric limits are subject to change.

ERROR CORRECTION WITH VARIABLE LENGTH AND DISTANCE

DESCRIPTION

The M64403FP performs the decoding for RS (Reed Solomon) code which primitive polynomial:P (X)=$X^8+X^4+X^3+X^2+1$ and its generation polynomial:G (X)=$\prod_{j=0}^{d-2}(X-\alpha^j)$.
M64403FP can set the code length and check byte length, so it is able to be adopted to various systems.

FEATURES

- It adopts three stages pipe line operation (Syndrome stage, Euclidean stage, Chen search & error value stage), so it realizes high speed error correction operation.
- Capable of erasure correcting function and it improves error correction performance.
  - Where error counts (e), erasure counts (ε) and design distance (d) have followed restriction.

$$2e + \varepsilon < d$$

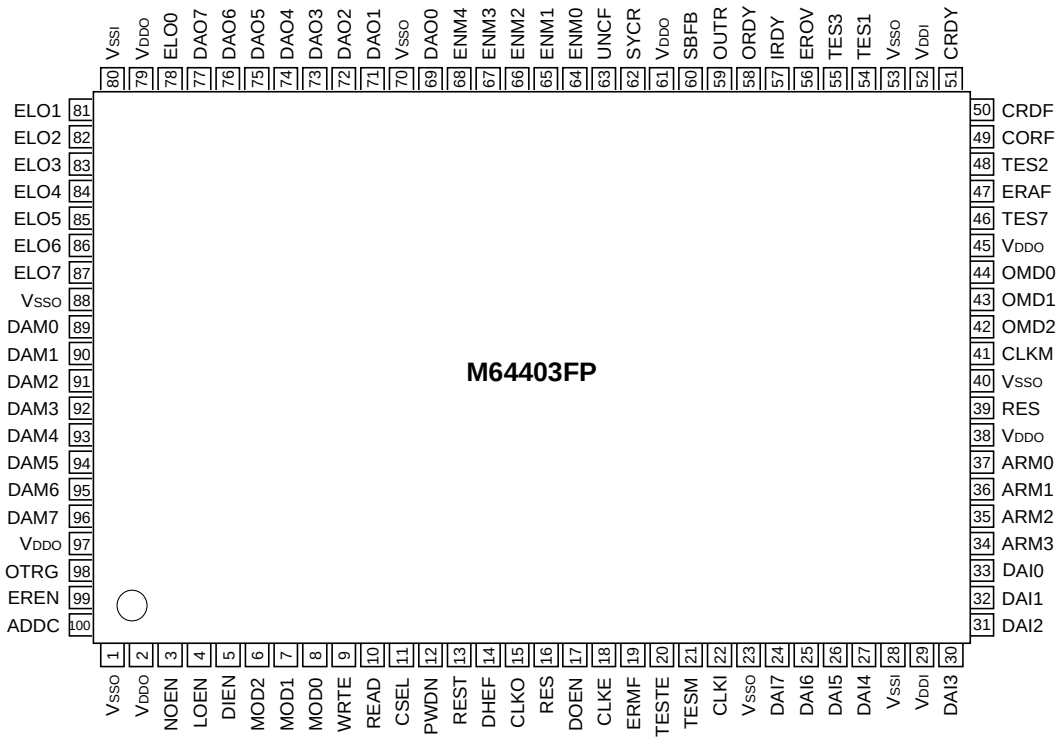
- Capable of parameter register programing.
  (1) Four kinds of code parameter which code length and check byte length are programmable.
  (Good for the product code that has plural code parameters.)
  - Where, maximum code length (L) are 255 bytes and maximum check byte length (d-1) are 16 bytes.

  (2) Programmable for erasure threshold.
  (3) Programmable for four kinds of decoding mode.

APPLICATION

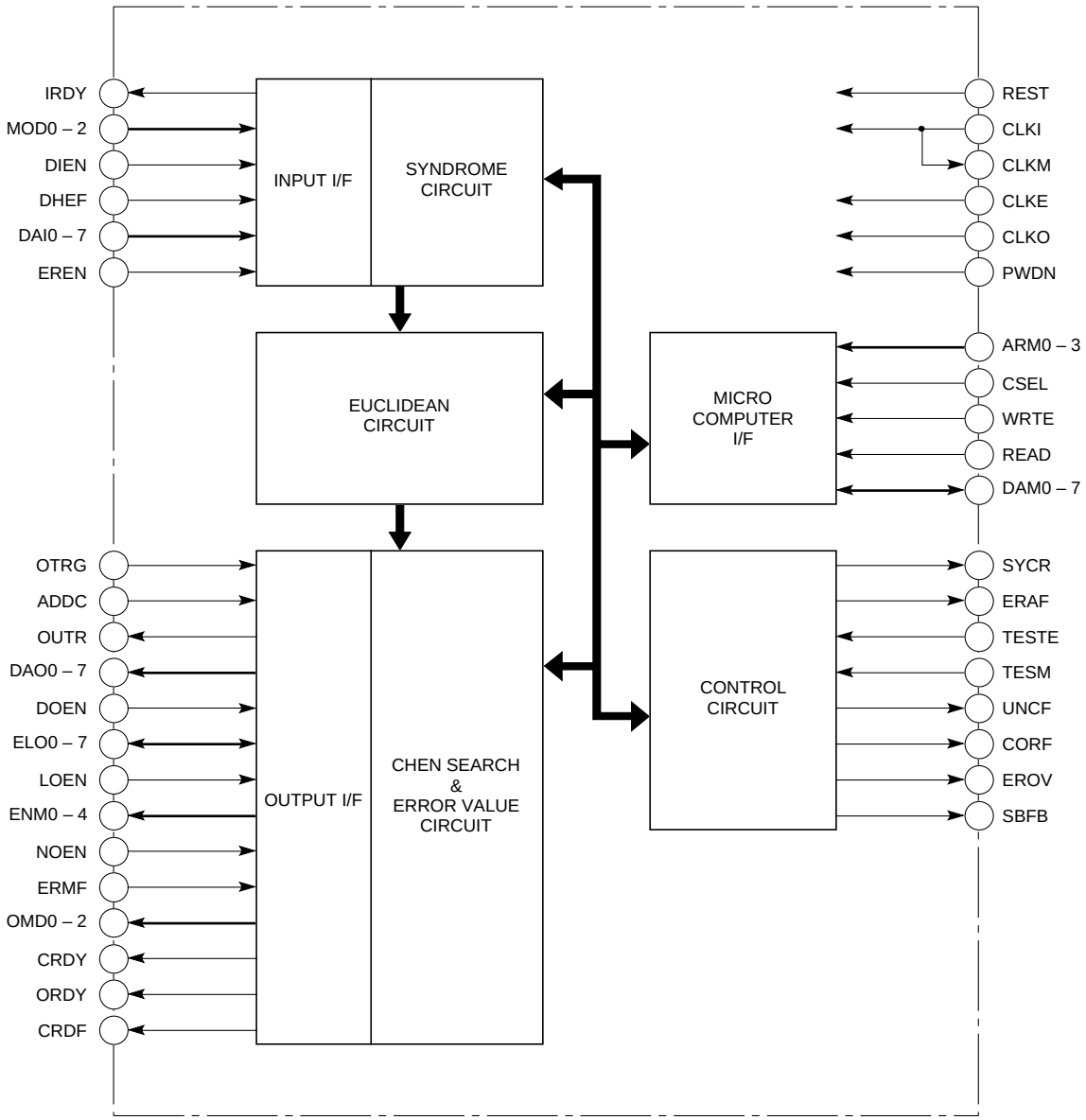
DVD player, DVD-ROM (DVD:Digital Video Disc), DBS (Direct Broadcasting by Satellite), High density floppy disk, Hard disk, CATV (Cable TV), MD (Mini Disc), DVC (Digital Video Cassette), DAT (Digital Audio Cassette), DCC (DIgital Compact Cassette), DVB (Digital Video Broadcast), CD-DA (Compact Disc-Digital Audio), CD-ROM (Compact Disc-Read Only Memory), other communication systems and storage media etc.

PIN CONFIGURATION (TOP VIEW)



Outline 100P6S-C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Ratings		Unit
			Min.	Max	
V_{DD}	Supply voltage		-0.3	+6.5	V
V_I	Input voltage		-0.3	V_{DD}+0.3	V
V_O	Output voltage		-0.3	V_{DD}+0.3	V
I_{IK}	Input protection diode current			±20	mA
I_{OK}	Output parasitic diode current			±20	mA
I_O	Output current			I_{OL}=20 I_{OH}=-26	mA
I_{DD}	V_{DD} supply current			81	mA
I_{SS}	V_{SS} supply current			81	mA
T_{stg}	Storage temperature		-55	150	˚C
PdOUT	Output load	Output buffer@I_{OL}=4mA		2200	MHz•pF
		Output buffer@I_{OL}=1mA		760	

RECOMMENDED OPERATING CONDITION

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage		4.75	5.0	5.25	V
Ta	Operating temperature		-20	+25	+70	˚C
VI	Input voltage		0		V_{DD}	V
tr, tf	Input rise & fall time	Normal input			500	nsec
		Schmit input			5	msec

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{IL}	Input voltage (TTL interface)	V_{DD}=5.0V	0		0.8	V
V_{IH}		V_{DD}=5.0V	2.2		5.25	V
VT-	Schmitt input voltage (TTL interface)	V_{DD}=5.0V	0.7		1.35	V
VT+			1.4		2.2	V
VH			0.3		1.2	V
V_{OL}	Output voltage	V_{DD}=5.0V, |IO|<1µA			0.05	V
V_{OH}			4.95			V
I_{OL}	Output current	V_{DD}=4.5V, V_{OL}=0.4V	4(*1)			mA
			1(*2)			mA
I_{OH}		V_{DD}=4.5V, V_{OH}=4.1V			-4(*3)	mA
					-1(*4)	mA
I_{IL}	Input current	V_{DD5}=5.5V, V_I=0V	-1		+1	µA
I_{IH}		V_{DD5}=5.5V, V_I=5.5V	-1		+1	µA
IOZL	Output leak current	V_{DD5}=5.5V, V_I=0V	-1		+1	µA
IOZH		V_{DD5}=5.5V, V_I=5.5V	-1		+1	µA
RD	Pull down resistance	V_{DD5}=5.0V, V_I=5.0V	3		16	kΩ
CI	Input terminal capacitance	f=1MHz, V_{DD}=0V		7	15	pF
CO	Output terminal capacitance			7	15	pF
CIO	I/O terminal capacitance			7	15	pF
I_{DD}	Supply current	V_{DD5}=5.0V, V_I=5.0V			2	mA

(* 1) : Rating for 4mA output buffer
(* 2) : Rating for 1mA output buffer

MICRO COMPUTER INTERFACE

Parameter register setting method (write) is described as follows. (See page7 about sequence chart : See below diagram about micro computer I/F and register table.)

1. Perform power on reset.
2. Set various parameters (code length-1, check byte length, erasure correction threshold) to below parameter register table.
3. Set decode operation mode parameters to address-E. (See address-E description)

See sequence chart page7 (micro computer I/F sequence) as for read from parameter register, see below table as for register table.

Parameter register table

address (Hex)	R/W	Initial (Hex)	set data (Hex)	description
0	R/W	00	≤FE	code (0) code length-1
1	R/W	00	≤FE	code (1) code length-1
2	R/W	00	≤FE	code (2) code length-1
3	R/W	00	≤FE	code (3) code length-1
4	R/W	00	≤10	code (0) check byte length
5	R/W	00	≤10	code (1) check byte length
6	R/W	00	≤10	code (2) check byte length
7	R/W	00	≤10	code (3) check byte length
8	R/W	00	≤10	code (0) erasure threshold
9	R/W	00	≤10	code (1) erasure threshold
A	R/W	00	≤10	code (2) erasure threshold
B	R/W	00	≤10	code (3) erasure threshold
C	R	—	—	real erasure counts which is derived from syndrome calculation
D	—	—	—	reserve
E	R/W	—	—	decode operation mode
F	—	—	—	reserve

Address-E description

address (Hex)	data							
E	D7	D6	D5	D4	D3	D2	D1	D0

▒ means "0" fixed.

D0 (bit0) 0:constrained error correction mode 1:erasure correction priority mode
D3 (bit3) 0:error value output mode 1:internal correction mode

DECODE MODE SETTING METHOD

Decode mode is able to set at IRDY=H. Decode mode table is as follows. Decode mode should be changed after all operations that are set before changing.

Decode mode table

MOD0	MOD1	MOD2	mode
0	0	0	code (0) error correction
1	0	0	code (1) error correction
0	1	0	code (2) error correction
1	1	0	code (3) error correction
0	0	1	code (0) erasure correction
1	0	1	code (1) erasure correction
0	1	1	code (2) erasure correction
1	1	1	code (3) erasure correction

CODE WORD INPUT METHOD

Code word is able to input at IRDY=H. IRDY changes H to L when head symbol for code word is input. And IRDY changes L to H when the last symbol of code word is input.

DHEF should be H and DIEN should be L when the head symbol of code word is input. DIEN is input enable signal for code word and while it's L, input data is recognized as valid data and latched to the internal circuit at rising edge of CLKI.

If the syndrome calculation for the 2nd code word finishes while the 1st code word is executed at Euclidean calculation stage, the syndrome data that is latched internally is overwritten (called syndrome collision) and the correcting operation for the 1st code word is impossible. In this case, SYCR changes to H and informs external of its status. (If the last symbol of code word is input at SBFB=H, decoding is operated safely.)

SYCR which changes to H is reset by system reset (REST=L).

ERASURE FLAG INPUT METHOD AND ERASURE CORRECTION MODE

Erasure correcting mode is set by the setting of erasure threshold to address 8 to B for parameter register and the setting of MOD2=H for decode mode signal. Erasure flag (EREN) should input H by synchronization with symbol data of code word.

Follows are about erasure threshold.

(1) Constrained error correction mode is derived when the bit0 (D0) of the parameter register address-E is set to L.
If the input erasure count is over the erasure threshold value(*3), the operation is adopted ordinary error correction mode by force.

(2) Erasure correction priority mode is derived when the bit0 (D0) of the parameter register address-E is set to H.
If the error is detected at syndrome calculation and erasure count is over the erasure threshold value(*4), M64403FP regards its operation as uncorrectable and correcting operation doesn't execute.

In any cases ((*3),(*4)), EROV (erasure over flag) changes to H.

CORRECTED DATA OUTPUT METHOD

When the decode operation finishes and correction result is able to output to a code word, OUTR changes to H for one period for CLKO. In this case, error location data is shown on ELO0 to ELO7, error value is shown on DAO0 to DAO7 and error correction count or erasure count is shown on ENM0 to ENM7. (Details are described later.)

When output enable signals (LOEN, DOEN, NOEN) are set to L (active mode), respective data (error location, error value, error or erasure count) are able to output. When these output enable signals are set to H, respective data bus change to high impedance status.

Error location data (ELO0 to ELO7) 00 hex means the location of head data for input code word.

Error value data (DAO0 to DAO7) corresponds with error location data (ELO0 to ELO7).

ADDC should be L for one period of CLKO in order to output next error location and next error value.

(See page10 : Correction data operation sequence chart)

ENM0 to ENM4 outputs error correcting count at ERMF=L, erasure count at ERMF=H. This erasure count means real error count at constrained error correction mode, total count for real error and erasure at erasure correction priority mode. And this erasure count includes empty erasure (it means error value is zero). If erasure count excesses 31 dec, ENM0 to ENM4 shows 31 dec.

After the external circuit read error count/error location/error value for a code word, OTRG should change L to H only one time by synchronization with CLKO clock. Data shift for internal pipe line circuit is executed by this operation. If this operation is so late, registers in the internal pipe line become full. And data collision may occur if code word is input more and its syndrome data is generated. In this case, M64403FP informs external of its status and SYCR changes to H. (If the last symbol of code word is input at SBFB=H, decoding is operated safely.)

SYCR which changes to H is reset by system reset (REST=L).

OUTPUT CONTROL SIGNAL

When OUTR changes to H, CORF (error detected flag), UNCF (uncorrectable flag) and EROV (erasure over flag) are output.

CORF changes to L when M64403FP regards input code word as no error. CORF changes to H when M64403FP detects error.

UNCF changes to H when M64403FP regards the error correction as impossible. If the input erasure flag count excesses erasure threshold value with erasure correction priority mode, UNCF changes to H also.

OMD0 to OMD2 show the current operated code word's decode mode which was set by MOD0 to MOD2.

INTERNALCORRECTION MODE

The internal correction mode is active when the bit3 (D3) of parameter register address-E is set to H. In this internal correction mode, the code word that was input already and shown by OMD0 to OMD2 input to ELO0 to ELO7.

In order to recognize the header symbol of input data, OTRG should be H by synchronization with the header symbol of code word. ADDC should be L while valid code word is input.

Corrected data is output from DAO0 to DAO7 after three clocks delay. OUTR changes to H by synchronization with header symbol in order to show the header symbol of corrected code word. CRDY changes to L by synchronization with output code word. CRDF changes to H for corrected portion. In addition, ORDY changes to H while output period of information symbol in order to distinguish from code word from information symbol and check symbol.

MISOPERATION FOR ODD CHECK BYTE NUMBER

M64403FP have no good operation when check byte number are just d/2 (d=check byte number+1) as UNCF don't to change to H, and misdata is output.

But we can judge the misoperation when ENM<4:0> indicates d/2 in error correction mode, and ENM<4:0> indicates d/2 when erasure number=0 or EROV=H in erasure correction mode.

ERROR CORRECTION TIME

M64403FP is able to perform consecutive error correction operation by bellowed three stage pipeline architecture.

- 1st stage.....Syndrome calculation
  (operation step:A1=code length+20)
- 2nd stage..... Euclidean calculation
  (operation step:A2=See table.2)
- 3rd stage..... Chen search & error value calculation
  (operation step:A1=code length+20)

Table. 1

	pipe1	pipe2	pipe3	pipe4	pipe5	pipe6	pipe7
1st code	1st stage	2nd stage	3rd stage	correction			
2nd code		1st stage	2nd stage	3rd stage	correction		
3rd code			1st stage	2nd stage	3rd stage	correction	
4th code				1st stage	2nd stage	3rd stage	correction

Table. 1 shows the operation flow in pipe line. As for the 1st code, M64403FP output error correction data at pipe4 after 1st stage is operated at pipe1, 2nd stage is operated at pipe2 and 3rd stage is operated at pipe3. Therefore, the error correction has a latency of three stages. The maximum step count for each pipe means the maximum steps among above mentioned 1st stage to 3rd stage. Where, the design distance decides the step count at the 2nd stage. (See Table. 2)

(Ex.1) In the case of code length=100, design distance=11
A1=100+20=120, A2=160 A2>A1
So maximum operation step for one pipe is 160.
Therefore, correction data is obtained 480 steps (160 x 3) later from the input of 1st code word.

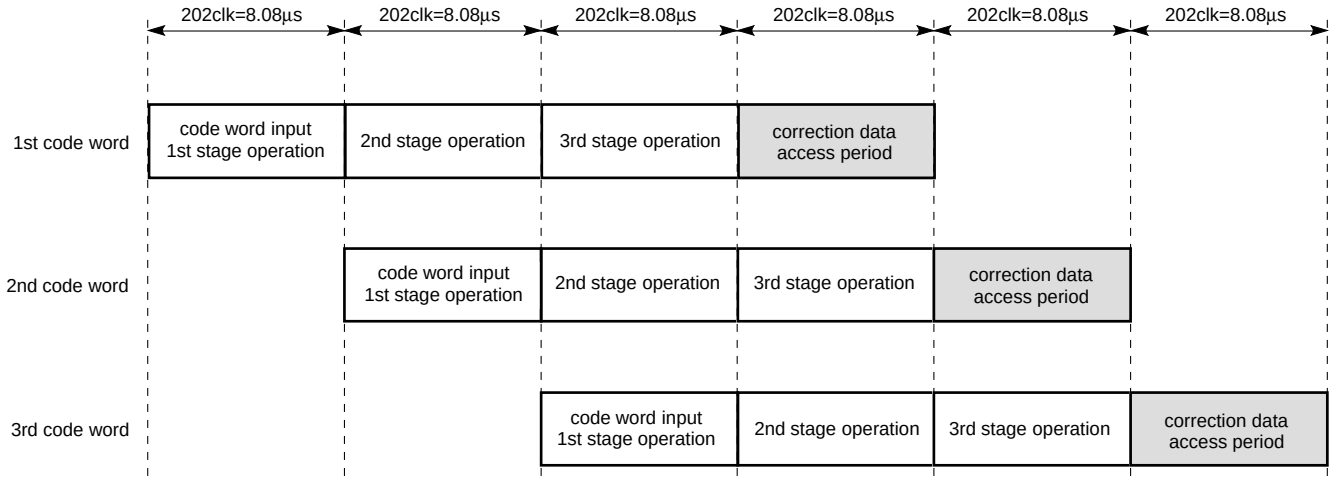
Table. 2

Design distance	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2
Euclidean calculation steps (erasure correction)	330	290	260	230	210	190	160	140	120	110	90	80	70	60	50	30
Euclidean calculation steps (error correction)	290	270	250	220	190	180	150	140	110	100	80	80	60	60	40	30

CORRECTING OPERATION STEPS IN PIPE LINE

(Ex.1) code length=182, design distance=11

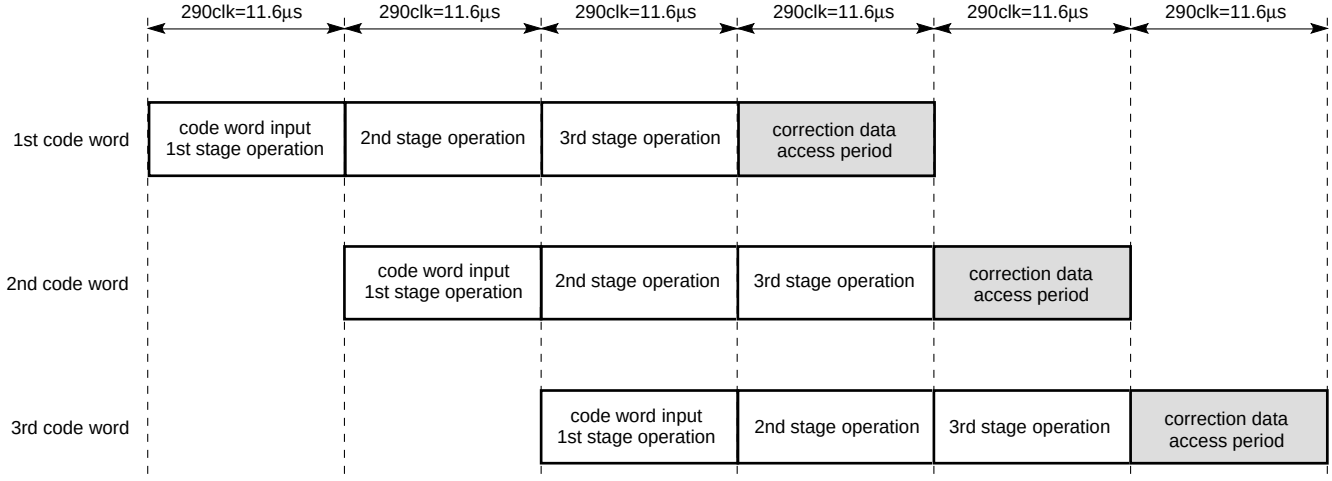
CLKI=CLKE=CLKO=25MHz error correction (no erasure)



Correction data is obtained three stages later (In this case, 202∗3=606clk 24.24µs) by input of consecutive code words.

(Ex.2) code length=208, design distance=17

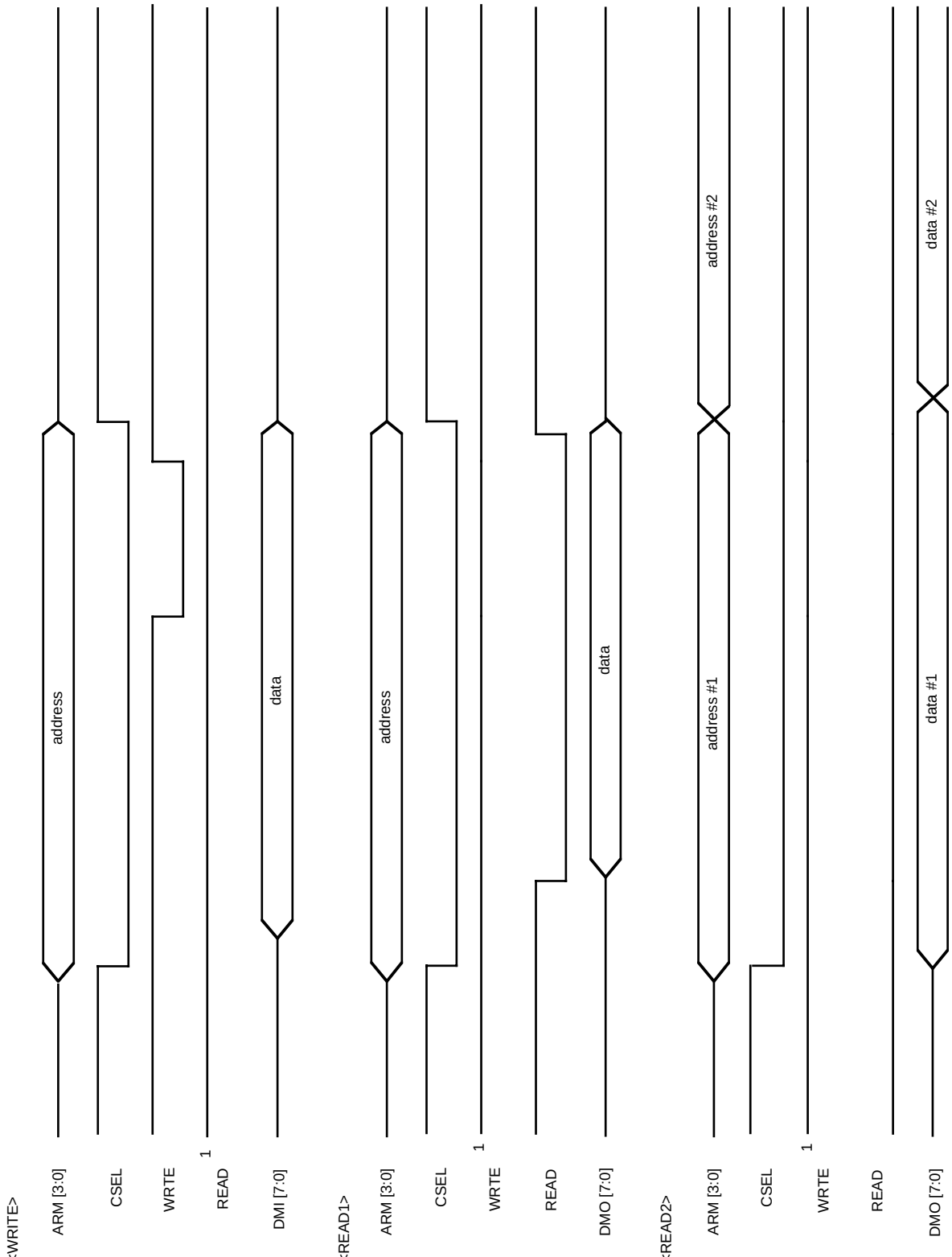
CLKI=CLKE=CLKO=25MHz erasure correction



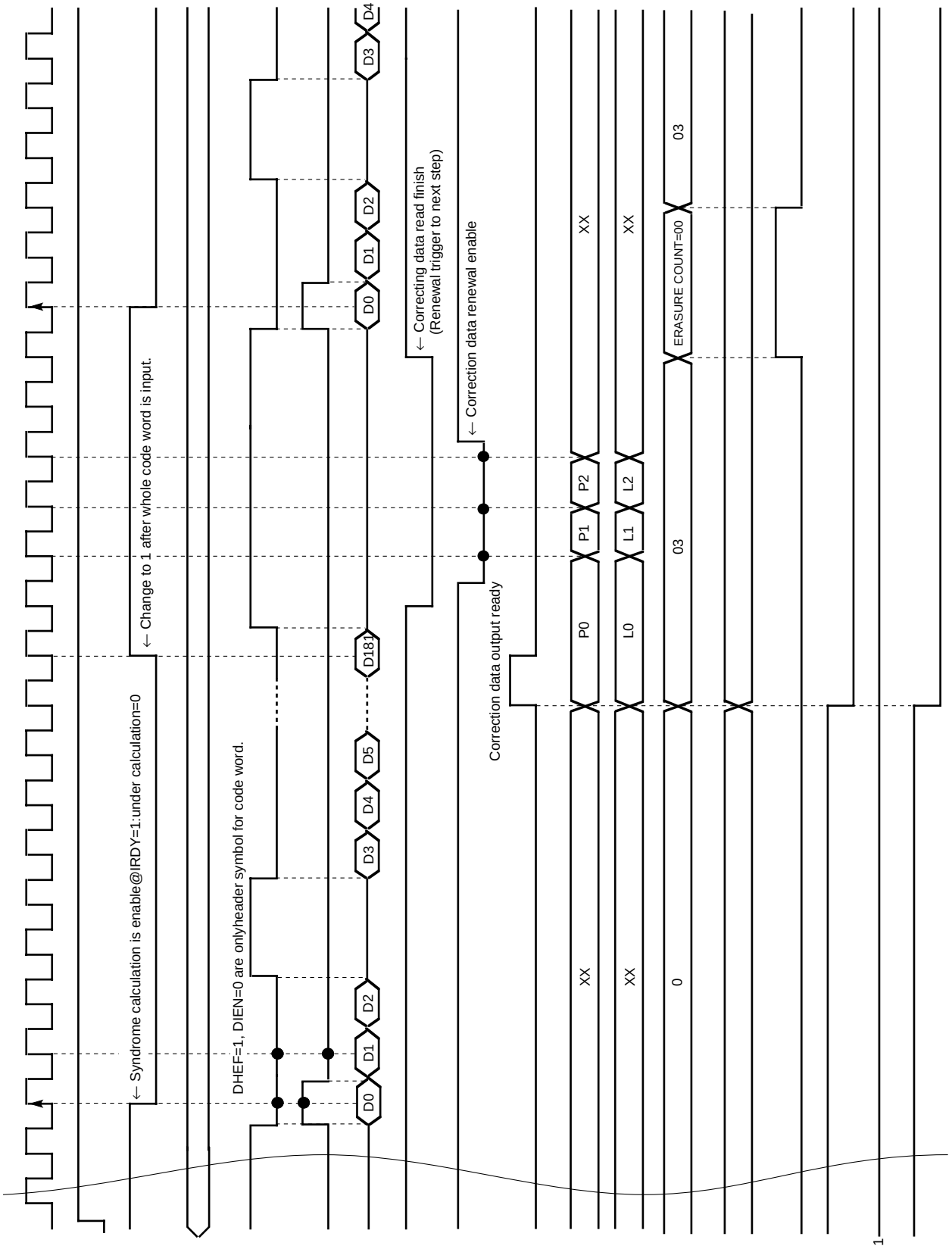
Correction data is obtained three stages later (In this case, 290∗3=870clk 34.8µs) by input of consecutive code words.

MICRO COMPUTER I/F R/W SEQUENCE CHART

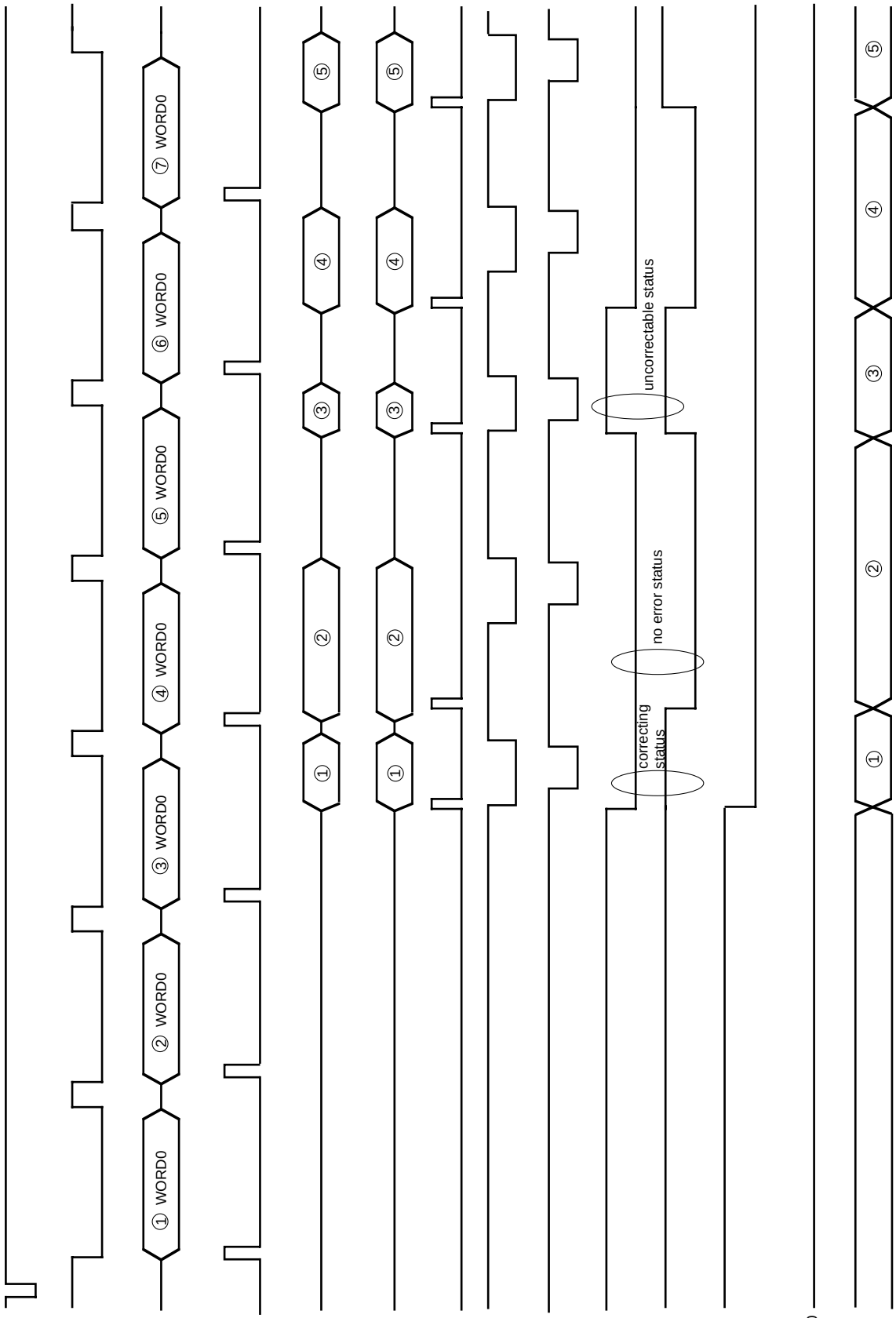
Note. READ=0 and WRTE=0 is inhibited at same time



CORRECTING DATA OPERATION SEQUENCE CHART
(Where necessary parameter is set already.)

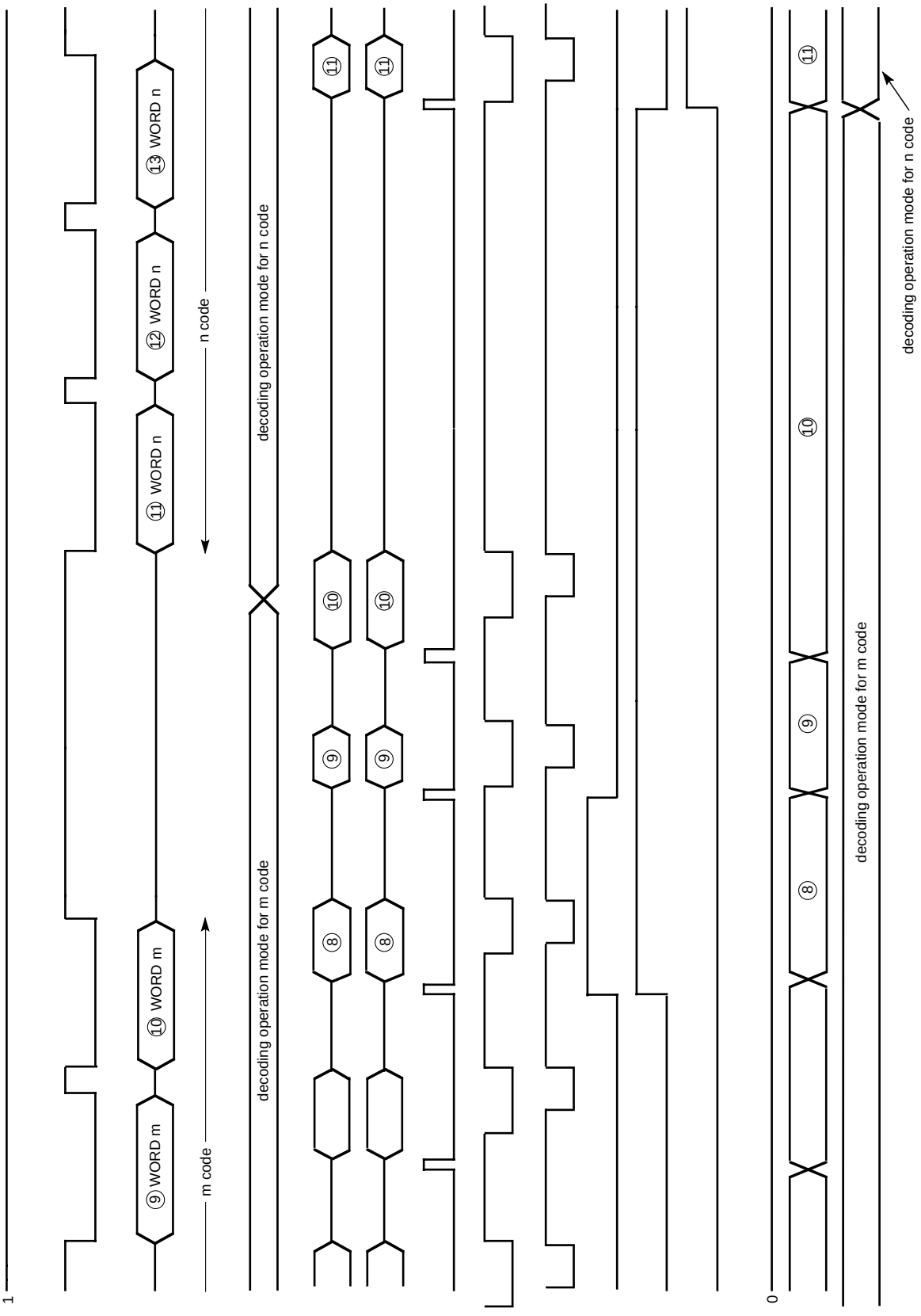


CONSECUTIVE DECODE SEQUENCE CHART (1)
(Only one kind of code exists)



Note. DAO and LOE output first error value/location @ OUTR=H. After all of error value/location for error count are output, they output zero.
Error value/location output zero at no error and uncorrectable state.

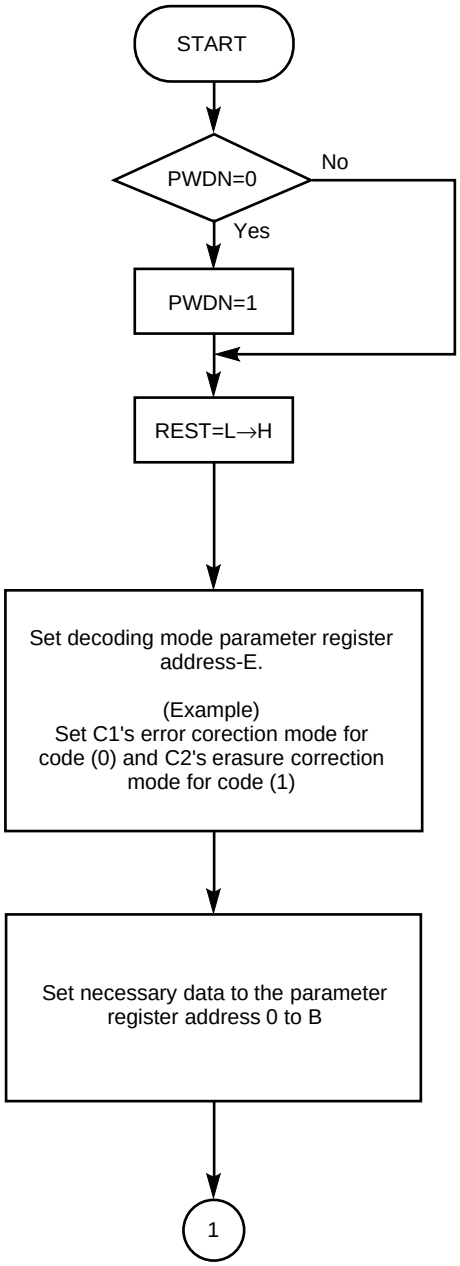
CONSECTIVE DECODE SEQUENCE CHART (2)
(Ex : Two kinds of code parameter exist (Product code))



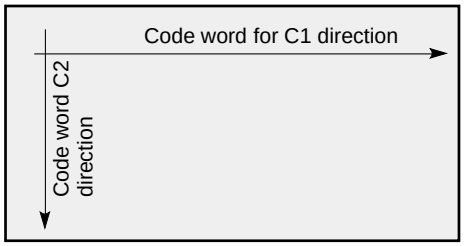
Note. DAO and LOE output first error value/location @ OUTR=H. After all of error value/location for error count are output, they output zero.
Error value/location output zero at no error and uncorrectable state.

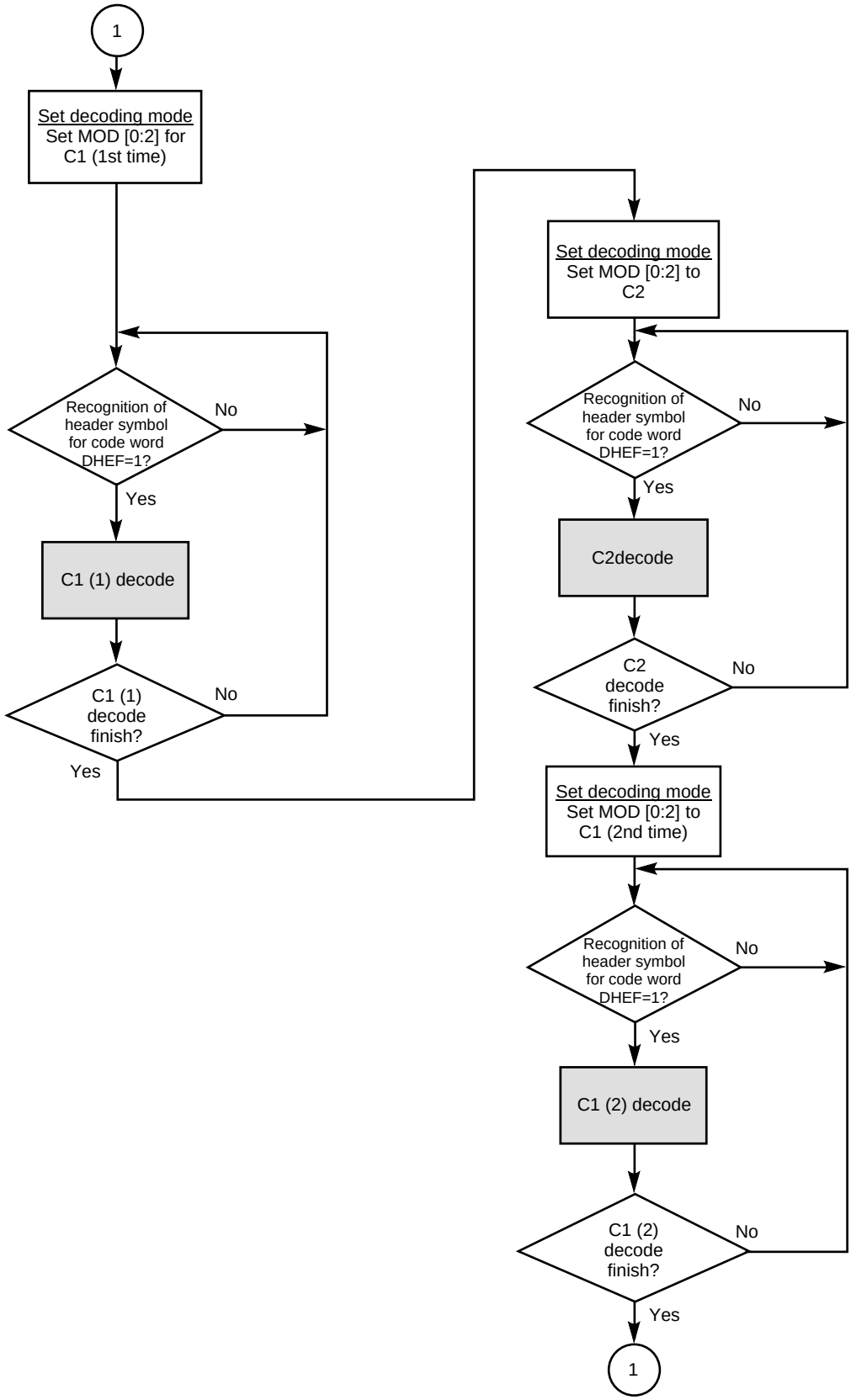
EXAMPLE FLOW CHART FOR GENERAL PRODUCT CODE DECODING

In the case of C1→C2→C1 repeat correction as a decoding method

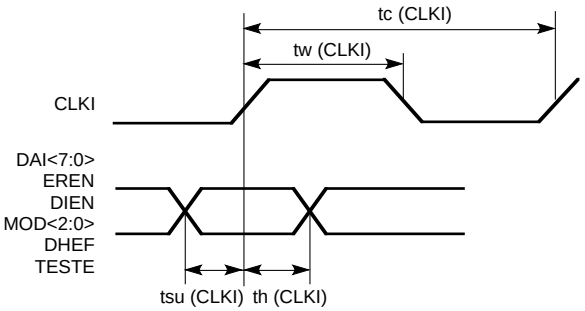


-Example for product code constitution-

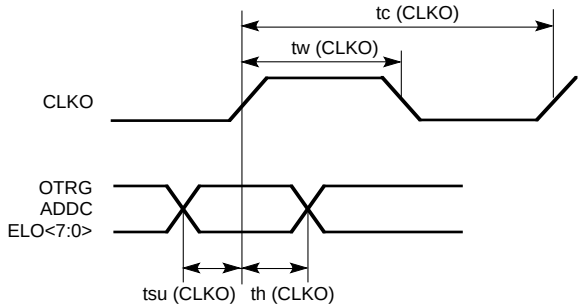



1
Set decoding mode
Set MOD [0:2] for
C1 (1st time)
Recognition of
header symbol
for code word
DHEF=1?
No
Yes
C1 (1) decode
C1 (1)
decode
finish?
No
Yes
Set decoding mode
Set MOD [0:2] to
C2
Recognition of
header symbol
for code word
DHEF=1?
No
Yes
C2decode
C2
decode
finish?
No
Yes
Set decoding mode
Set MOD [0:2] to
C1 (2nd time)
Recognition of
header symbol
for code word
DHEF=1?
No
Yes
C1 (2) decode
C1 (2)
decode
finish?
No
Yes
1

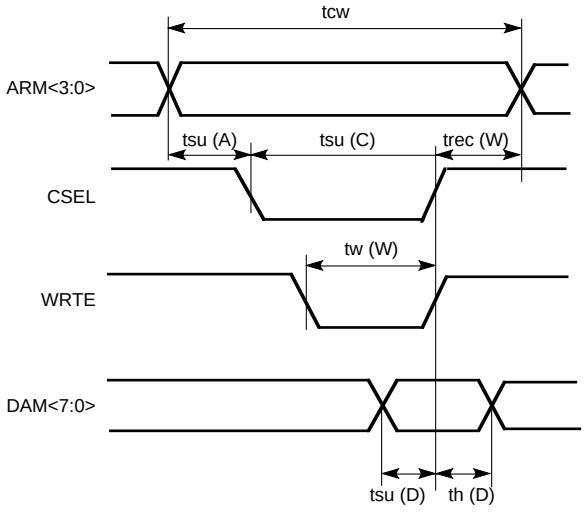
INPUT TIMING



Symbol	Parameter	Limits (Min.)	Unit
tc (CLKI)	CLKI clock period	40	ns
tw (CLKI)	CLKI clock pulse width	16	ns
tsu (CLKI)	CLKI setup time	5	ns
th (CLKI)	CLKI hold time	10	ns



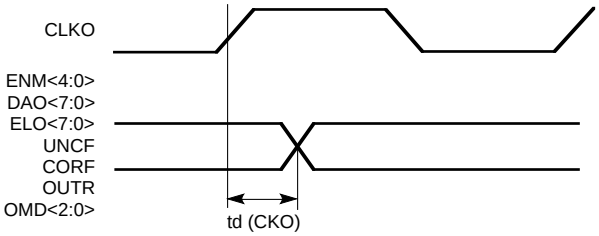
Symbol	Parameter	Limits (Min.)	Unit
tc (CLKO)	CLKO clock period	40	ns
tw (CLKO)	CLKO clock pulse width	16	ns
tsu (CLKO)	CLKO setup time	5	ns
th (CLKO)	CLKO hold time	10	ns



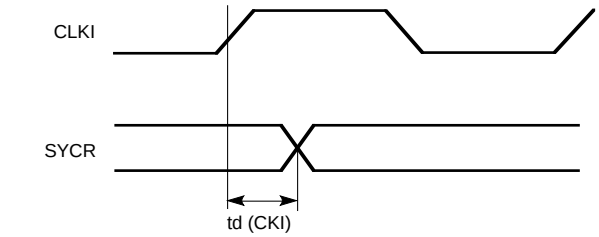
Symbol	Parameter	Limits (Min.)	Unit
tcw	Write cycle time	40	ns
tsu (A)	Address setup time	10	ns
tsu (C)	Chip select setup time	10	ns
trec (W)	Write recovery time	10	ns
tw (W)	Write ulse width	10	ns
tsu (D)	Data setup time	5	ns
th (D)	data hold time	10	ns

OUTPUT TIMING

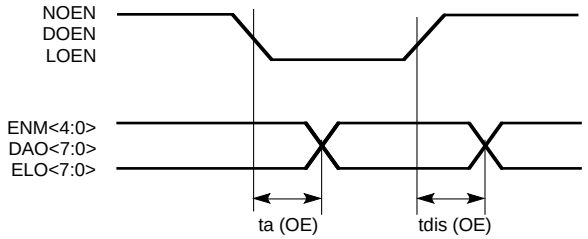
At output load capacity=50pF



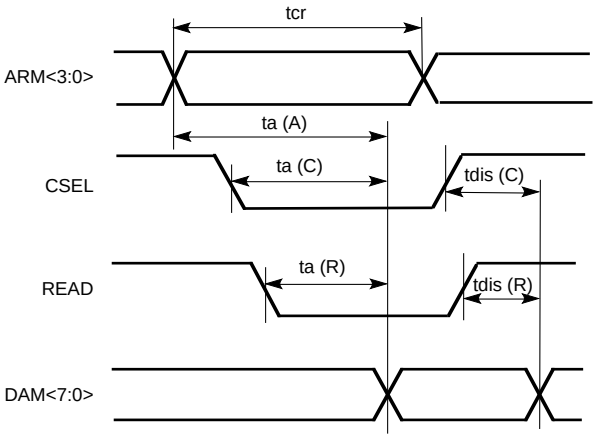
Symbol	Parameter	Limits (Max.)	Unit
td (CKO)	CLKO output propagation time	20	ns



Symbol	Parameter	Limits (Max.)	Unit
td (CKI)	CLKI output propagation time	20	ns



Symbol	Parameter	Limits (Max.)	Unit
ta (OE)	Output enable time	15	ns
tdis (OE)	Output disable time	15	ns



Symbol	Parameter	Limits	Unit
tcr	Read cycle time	40 (min)	ns
ta (A)	Address access time	10 (max)	ns
ta (C)	Chip select access time	10 (max)	ns
ta (R)	Output enable access time	10 (max)	ns
tdis (C)	Output disable access time (from CSEL)	10 (max)	ns
tdis (R)	Output disable access time (from READ)	10 (max)	ns

DESCRIPTION OF PIN

Pin No.	Name	I/O	I/O structure	I/O type	Description of function
1, 23, 40, 53, 70, 88	V_{SSO}	—	—	—	GND for output
2, 38, 45, 61, 79, 97	V_{DDO}	—	—	—	+5V for output
16, 39	RES	—	—	—	reserve
28, 80	V_{SSI}	—	—	—	GND for input
29, 52	V_{DDI}	—	—	—	+5V for input
3	NOEN	I	TTL input	T22N	output enable for ENM0 to 4 0:Enable 1:HiZ
4	LOEN	I	TTL input	T22N	output enable for ELO0 to 7 0:Enable 1:HiZ
5	DIEN	I	TTL input	T22N	Symbol data input enable 0:Enable
6 to 8	MOD2 to MOD0	I	TTL input	T22N	decoding mode setting MOD2:MSB MOD0:LSB
9	WRTE	I	TTL schmitt trigger input	U22N	micro computer I/F write enable 0:Enable
10	READ	I	TTL schmitt trigger input	U22N	micro computer I/F read enable 0:Enable
11	CSEL	I	TTL schmitt trigger input	U22N	micro computer I/F chip select 0:Select
12	PWDN	I	TTL schmitt trigger input	U22N	power save 0:power save
13	REST	I	TTL schmitt trigger input	U22N	system reset 0:Reset
14	DHEF	I	TTL input	T22N	symbol data header 1:Data head
15	CLKO	I	TTL schmitt trigger input	U22N	data output clock (Typ.13.5MHz)
17	DOEN	I	TTL input	T22N	output enable for DAO0 to 7 0:Enable 1:HiZ
18	CLKE	I	TTL input	T22N	internal operation clock (Typ.13.5MHz)
19	ERMF	I	TTL input	T22N	output enable for ENM0 to 7 1:erasure counts 0:correcting counts
20	TESTE	I	TTL input	T22N	test mode selection 0:decoding 1:testing
21	TESM	I	TTL input	T22N	test mode selection 0:decoding 1:testing
22	CLKI	I	TTL schmitt trigger input	U22N	symbol data input clock (Typ.13.5MHz)
24 to 27	DAI7 to DAI4	I	TTL input	T22N	symbol data input bus DAI7:MSB
30 to 33	DAI3 to DAI0	↓	↓	↓	↓ DAI0:LSB
34 to 37	ARM3 to ARM0	I	TTL input	T22N	micro computer I/F address bus ARM3:MSB ARM0:LSB
41	CLKM	O	TTL output (4mA)	O65T	CLKI monitor (Typ.13.5MHz)
42 to 44	OMD2 to OMD0	O	TTL output (4mA)	O65T	decoded operation mode (relative to MOD0 to 2)
46	TES7	O	TTL output (1mA)	O63T	test monitor output
47	ERAF	O	TTL output (4mA)	O65T	erasure flag output 1:Enable
48	TES2	O	TTL output (4mA)	O65T	test monitor output
49	CORF	O	TTL output (4mA)	O65T	error detection flag 0:No Error 1:detected
50	CRDF	O	TTL output (4mA)	O65T	correction flag 1:corrected data
51	CRDY	O	TTL output (4mA)	O65T	output valid flag 0:valid
54	TES1	O	TTL output (4mA)	O65T	test monitor output
55	TES3	O	TTL output (4mA)	O65T	test monitor output
56	EROV	O	TTL output (4mA)	O65T	erasure over flag 1:over
57	IRDY	O	TTL output (4mA)	O65T	symbol data input ready 1:Ready
58	ORDY	O	TTL output (4mA)	O65T	data flag 0:data
59	OUTR	O	TTL output (4mA)	O65T	output ready 1:Ready/output data header (@ internal correction mode) 1:header
60	SBFB	O	TTL output (4mA)	O65T	syndrome data collision prevention signal
62	SYCR	O	TTL output (4mA)	O65T	syndrome data collision alarm 1:alarm (collision)
63	UNCF	O	TTL output (4mA)	O65T	uncorrectable flag 1:Uncorrect
64 to 68	ENM0 to ENM4	O	TTL3 state output (4mA)	Z65T	error correction counts/erasure counts output bus ENM4:MSB ENM0:LSB
69, 71 to 77	DAO0 to DAO7	O	TTL3 state output (4mA)	Z65T	error value output bus DAO7:MSB DAO0:LSB
78, 81 to 87	ELO0 to ELO7	I/O	TTL I/O (Pull down Rd=2kΩ)	TH2N	data input (for correction) /error location output bus ELO7:MSB ELO0:LSB
89 to 96	DAM0 to DAM7	I/O	TTL I/O (Pull down Rd=2kΩ)	TH2N	micro computer I/F bus DAM7:MSB DAM0:LSB
98	OTRG	I	TTL input	T22N	renewal trigger 0→1:renewal/input data (@internal correction mode) 1:header
99	EREN	I	TTL output (4mA)	O65T	erasure flag input 1:@erasure input
100	ADDC	I	TTL input	T22N	output data renewal 0:Next/code word valid (@internal correction mode) 0:valid