M66009FP

8-BIT I/O EXPANDER WITH 5-BIT ADDRESS

DESCRIPTION

M66009 silicon gate CMOS (complementary metal oxide semiconductor) integrated circuit converts 8-bit data from serial to parallel and vice versa.
This IC has 5 address setting bits, which enable users to set a distinctive address.
This IC offers a wide range of applications, such as for microcomputer input/output port extension.

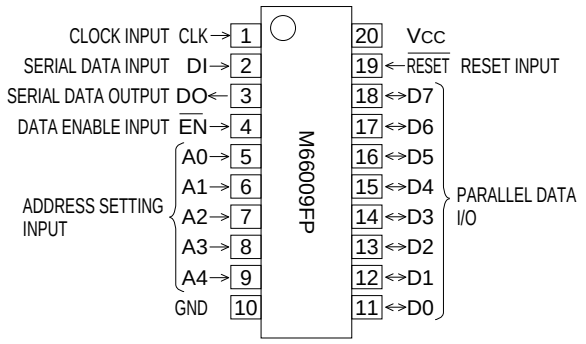
FEATURES

- Has 5 bits for address setting
- Connected to microcomputer via 4 pins ($\overline{EN}$,CLK, DI and DO)
- Input/output setting possible by the bit
- Schmitt input ($\overline{RESET}$, $\overline{EN}$ and CLK)
- Wide operating temperature range (Ta = –20˚C to 75˚C)

APPLICATION

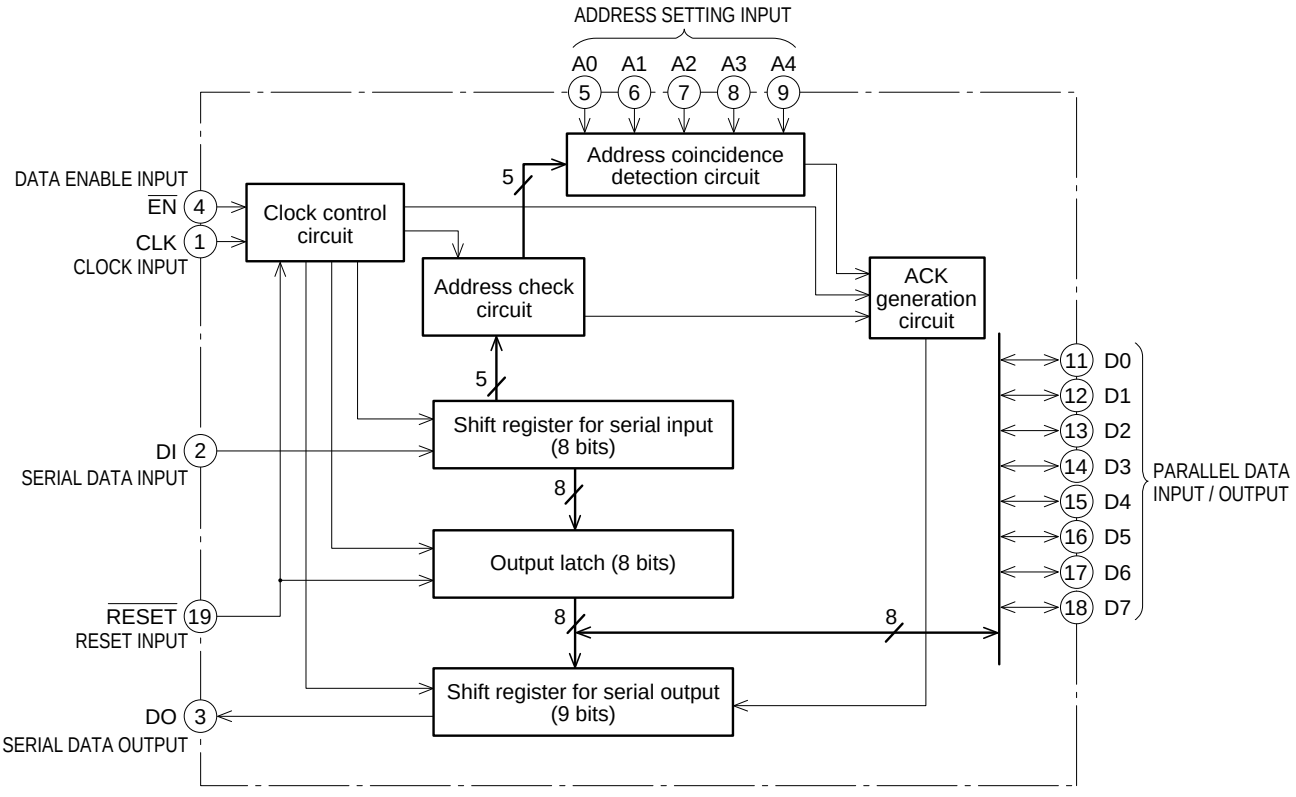
Microcomputer I/O port extension, etc.

PIN CONFIGURATION (TOP VIEW)



Outline 20P2N-A

BLOCK DIAGRAM



FUNCTION

M66009 semiconductor circuit converts data from serial to parallel and vice versa. Address can be set freely at users' option.

It communicates with microcomputer via 4 signals lines: $\overline{EN}$, CLK, DI and DO.

It has 5-bit address setting input. Connect each address input pin to Vcc or GND, then the address can be determined from among 32 patterns. When serial data arrives from microcomputer, this IC compares the address in the data to the address set with these pins. If the two addresses are the same, the given command is executed.

To output serial input data in parallel, this IC converts the lower 8 bits of the 16-bit serial data into parallel, and outputs each to pins D0 to D7. The upper 8 bits are processed as address bits and command bits.

To output parallel input data in series, this IC prefixes one acknowledge bit to the 8 parallel bits which respectively refer to the status of pins D0 to D7, and then outputs 9 bits in series.

PIN DESCRIPTIONS

Pin	Name	Input/Output	Functions
$\overline{RESET}$	Reset input	Input	"L" level: M66009 is reset to initial state.
$\overline{EN}$	Data enable input	Input	"L" level: M66009 becomes accessible.
CLK	Serial clock input	Input	Serial data that arrives at pin DI from microcomputer is taken into M66009 shift register at CLK rise edge. serial data is output from pin DO synchronously with CLK fall edge. Pin DO status stays at "H" level except during serial data output.
DI	Serial data input	Input	
DO	Serial data output	Output	
A0~A4	Address setting input	Input	Connect each to Vcc or GND to set distinctive address. Command is executed only when serial data from microcomputer includes the same address as that set by these pins. When connected to Vcc, pin status is "1". When connected to GND, pin status is "0".
D0~D7	Parallel data input/ output	Input/Output	Used to input/output parallel data. Because pull-down resistor is built in and output transistor is P-ch open drain, pins in "L" output status (equals to P-ch transistor OFF) function as input pins.
Vcc	Positive supply pin	—	Connected positive supply (5V).
GND	Grounding pin	—	Used for grounding (0V).

INPUT/OUTPUT DATA LOGIC

Serial data input from pin DI is output in parallel from pins D0 thru D7, being inverted in logic. Parallel data input from pins D0 thru D7 is output in series from pin DO in the same logic. Therefore, to set I/O pins to input, DI input data should be set to "H".

DATA SENDING/RECEIVING PROTOCOL AND OPERATION PROCEDURE

The timing at which microcomputer communicates with M66009 is as shown in the diagram below. When microcomputer accesses to M66009, it declares the start of access by lowering pin $\overline{EN}$ status from "H" to "L". It then sends data to pins CLK and DI at the timing shown below. The access stops as pin $\overline{EN}$ status rises from "L" to "H". Given below is more detailed explanation of data sending/receiving procedure:

(1) At $\overline{EN}$ fall edge, 8-bit parallel data that arrives at input/output pins D0 thru D7 is loaded into shift register for serial output.

(2) At CLK rise edge, data at pin DI is taken into serial input shift register, and internal clock counter starts counting up.

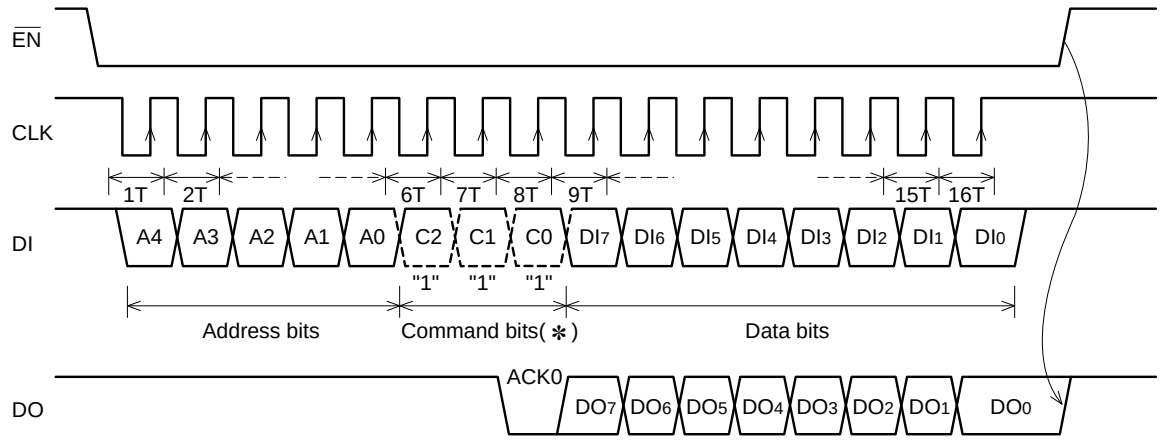
(3) When 5-bit address is taken in, it is compared to address set by pins A0 thru A4. If they are the same, acknowledge bit "0" is output to pin DO synchronously with CLK 8T fall edge.
(When the addresses are not the same, pin DO output status stays at the "H" level.)

(4) When command bits C2, C1 and C0 are all "1", operation proceeds to (5) and (6) described below.
If any of these command bits are not "1" while the addresses are the same, pin DO output is fixed to "H" synchronously with CLK 9T rise, and operation is halted until $\overline{EN}$ rises. When $\overline{EN}$ rises, clock counter is reset, and M66009 becomes ready to accept a next access.

(5) When the addresses are the same and the command bits are all "1", serial output operation starts. Eight-bit data latched at step (1) as described above is output in series, starting from the bit at pin D7, through pin DO synchronously with the fall edges of CLK 9T thru 16T. No operation is performed for CLK inputs after 16T, except the count up of CLK.

(6) When $\overline{EN}$ rises: Output pin DO status is fixed to "H", and only when clock counter has counted 16 CLK rise edges (counter output =10H), the lower 8 bits of the 16-bit serial data is sent to output latch synchronously with the $\overline{EN}$ rise edge. The latched data is inverted in logic, and output to pins D0 thru D7 in parallel. Clock counter is then reset, completing one sequence.

(Note) If the clock counter output is not 10 H when $\overline{EN}$ rises, data is not sent to output latch. Output pin DO is fixed to "H", clock counter is reset, and M66009 becomes ready to accept a next access.



(✻) Command bits (C2, C1, C0) = (1, 1, 1)

Data Communication protocol

ACKNOWLEDGE BIT ACK0

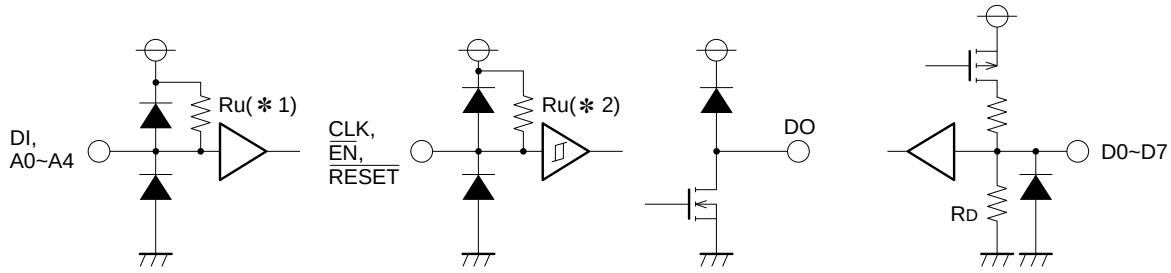
Acknowledge bit ACK0 is output only when address in serial input data is the same as that set by pins A0 thru A4. It is output from pin DO as ACK0 =“0” (“L”) synchronously with CLK 8T fall.

INITIAL STATUS AFTER RESET

If “L” is input to $\overline{\text{RESET}}$, M66009 is put in the conditions specified below:

I/O pins D0 thru D7	Input state (“L” output state) (Output p-channel transistor off)
DO output	“H” output state (Output n-channel transistor off)

INPUT AND OUTPUT EQUIVALENT CIRCUITS



(✻1) Pull-up resistor Ru is built in pin DI.

(✻2) Pull-up resistor Ru is built in pin CLK and $\overline{\text{EN}}$.

RD: Pull-down resistor

Input Configuration 1 | Input Configuration 2 | Output Configuration | Input/Output Configuration

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		conditions	Ratings	Unit
V_{CC}	Supply voltage			–0.5 ~ +7.0	V
V_I	Input voltage			–0.5 ~ V_{CC} + 0.5	V
V_O	Output voltage	DO, D0~D7		–0.5 ~ V_{CC} + 0.5	V
P_d	Power dissipation			500	mW
T_{stg}	Storage temperature			–65 ~ 150	°C

RECOMMENDED OPERATIONAL CONDITIONS

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage	DO, D0~D7	0		V_{CC}	V
T_{opr}	Operating temperature		–20		75	°C

ELECTRICAL CHARACTERISTICS (T_a = –20 ~ 75°C, V_{CC} = 5V ± 10% and GND = 0V unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
V_{IH}	"H" input voltage		DI, A0~A4		2.0			V
V_{IL}	"L" input voltage						0.8	V
V_{IH}	"H" input voltage		D0~D7		3.8			V
V_{IL}	"L" input voltage						1.2	V
V_{T+}	Positive threshold voltage		CLK, $\overline{EN}$, $\overline{RESET}$				2.4	V
V_{T-}	Negative threshold voltage				0.7			V
V_h	Hysteresis width					0.6		V
V_{OL}	"L" output voltage	DO	V_I=V_{T+},V_{T-}, V_{CC}=4.5V, I_{OL}=4mA				0.4	V
V_{OH}	"H" output voltage	D0~D7	V_I=V_{T+}, V_{T-}, V_{CC}=4.5V, I_{OH}=–2mA		3.0			V
R_D	Pull-down resistance		V_O=0~V_{CC}		20			kΩ
R_U	Pull-up resistance	$\overline{EN}$, CLK, DI	V_I=0~V_{CC}		20			kΩ
I_{OSH}	"H" output short circuit current	D0~D7	V_O=0V, V_{CC}=5V				–25	mA
I_I	Input current	$\overline{RESET}$, A0~A4	V_I=0~V_{CC}, V_{CC}=5.5V				±5.0	µA
I_O	Output leak current	DO	V_O=0~V_{CC}, V_{CC}=5.5V				±10.0	µA
I_{CC}	Static supply current		V_{CC}=5.5V, output open D0~D7: ("L" output)	V_I=V_{CC}			0.4	mA
				V_I=GND			1.2	

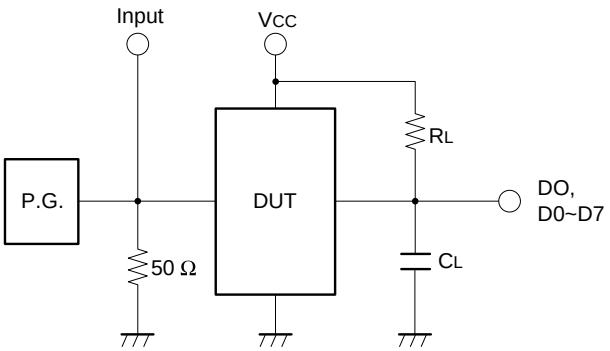
SWITCHING CHARACTERISTICS (T_a = –20 ~ 75°C, V_{CC} = 5V ± 10% and GND = 0V)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
t_{PZH}	Output "Z-H" propagation time	$\overline{EN}$–D0~D7	C_L=50pF (Note 1)			1.0	µs
t_{PHZ}	Output "H-Z" propagation time					2.0	µs
t_{PZL}	Output "Z-L" propagation time	CLK–D0	C_L=50pF, R_L=2kΩ (Note 1)			350	ns
t_{PLZ}	Output "L-Z" propagation time					350	ns
t_{PHZ}	Output "H-Z" propagation time	$\overline{RESET}$–D0~D7	C_L=50pF (Note 1)			2.0	µs

TIMING CONDITIONS

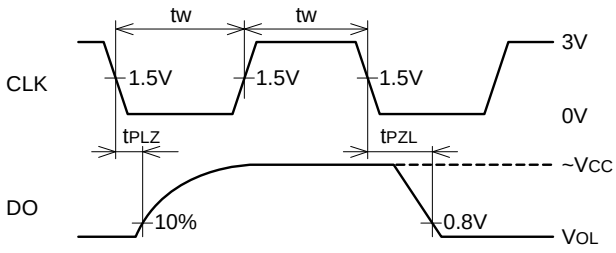
Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
tw	CLK, $\overline{EN}$, $\overline{RESET}$ pulse width		(Note 1)	250			ns
tsu	Setup time	DI-CLK		120			ns
		$\overline{EN}$-CLK		120			
		D0~D7-$\overline{EN}$		120			
th	Hold time	DI-CLK		120			ns
		$\overline{EN}$-CLK		120			
		D0~D7-$\overline{EN}$		120			
trec	Recovery time	EN-$\overline{RESET}$		120			ns

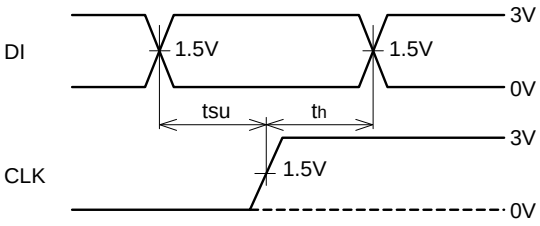
NOTE 1: TEST CIRCUIT

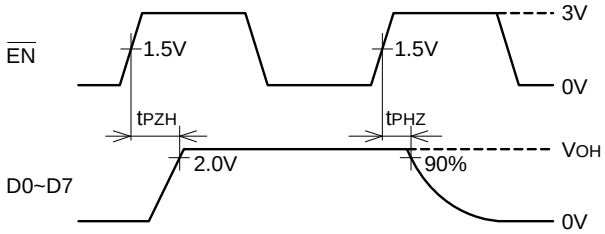


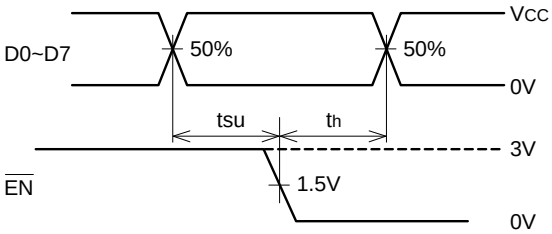
(1) Pulse generator (PG) characteristics: $t_r = t_f$ = 6ns (10%–90%)
(2) Capacitance C_L includes connection floating capacitance and probe input capacitance.

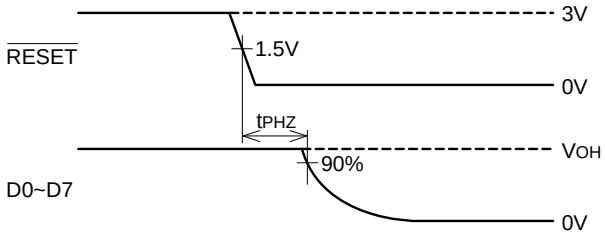
TIMING CHARTS

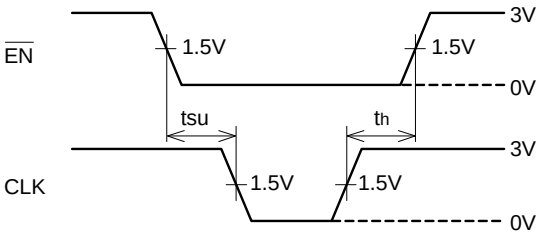


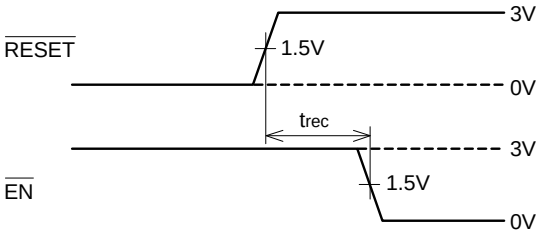












APPLICATION EXAMPLE