M66013FP

8-BIT I/O EXPANDER WITH ADDRESS

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

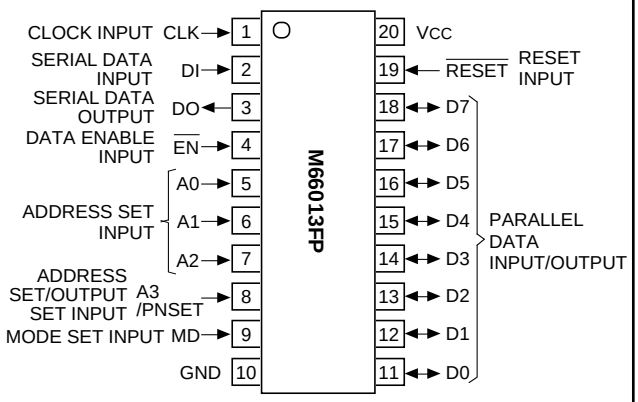
DESCRIPTION

The M66013FP is a semiconductor IC that is capable of performing serial-parallel conversion of data. This IC can set addresses.
The microcomputer uses the four signal lines of $\overline{EN}$, CLK, DI and DO to send and receive data.
The IC adopts the two types of operation modes: echo-back mode and normal mode. In the echo-back mode, data received in serial can be sent to the sender within the same sequence (*1) as it is.
In the normal mode, restriction is given to the data to be sent to the sender. However, the normal mode supports the same communication protocol as that of the M66009FP. (*1): one of the higher order command bits is excluded.
Three bits in the echo-back mode and four bits in the normal mode are available for addresses. The echo-back mode and the normal mode have 8 types and 16 types of address, respectively, and any address can be set.
Receiving serial data from the microcomputer, the M66013 compares address data included in the data with an address entered in address setting. Only when these addresses match each other, a specified command provided are to be executed.
For serial input-parallel output operation, low order 8 bits of the received 16 bit serial data is converted to parallel data to output to pins D0 to D7. High order 8 bits are handled as address or command bits. Since the writing operation to the data register for parallel output and the outputting operation of register contents to pins D0 to D7 are performed with different commands and can be controlled independently, the register contents must be checked before output of the specified data to pins D0 to D7.
For parallel input-serial output operation, parallel data of pins D0 to D7 are outputted to low order 8 bits of the sended 16 bit serial data. The contents of high order 8 bits of the sended 16 bit serial data differs in the using operation mode.
In echo mode, the I/O port output format is capable of setting to either N-ch or P-ch open drain. In normal mode, the I/O port output format is fixed to P-ch open drain.

FEATURES

- Is capable of providing high speed serial communication at 8 MHz.
- Provides two modes: echo back mode and normal mode.
- Is capable of reading serial input data in echo back mode. (However, 3 bits are available for the address.)
- Is capable of achieving communication protocol of current M66009FP in the normal mode. (However, 4 bits are available for the address.)
- Uses different commands in operations for output of data to I/O port: command for writing data into an output register and command for output operation to the I/O port.
- Provides an I/O port data read only command.
- Is capable of reading an output register.
- Adopts a decision by majority by reading three types of data when serial data is received.
- Is capable of setting the I/O port output format to either N-ch or P-ch open drain. (In echo mode)

PIN CONFIGURATION (TOP VIEW)

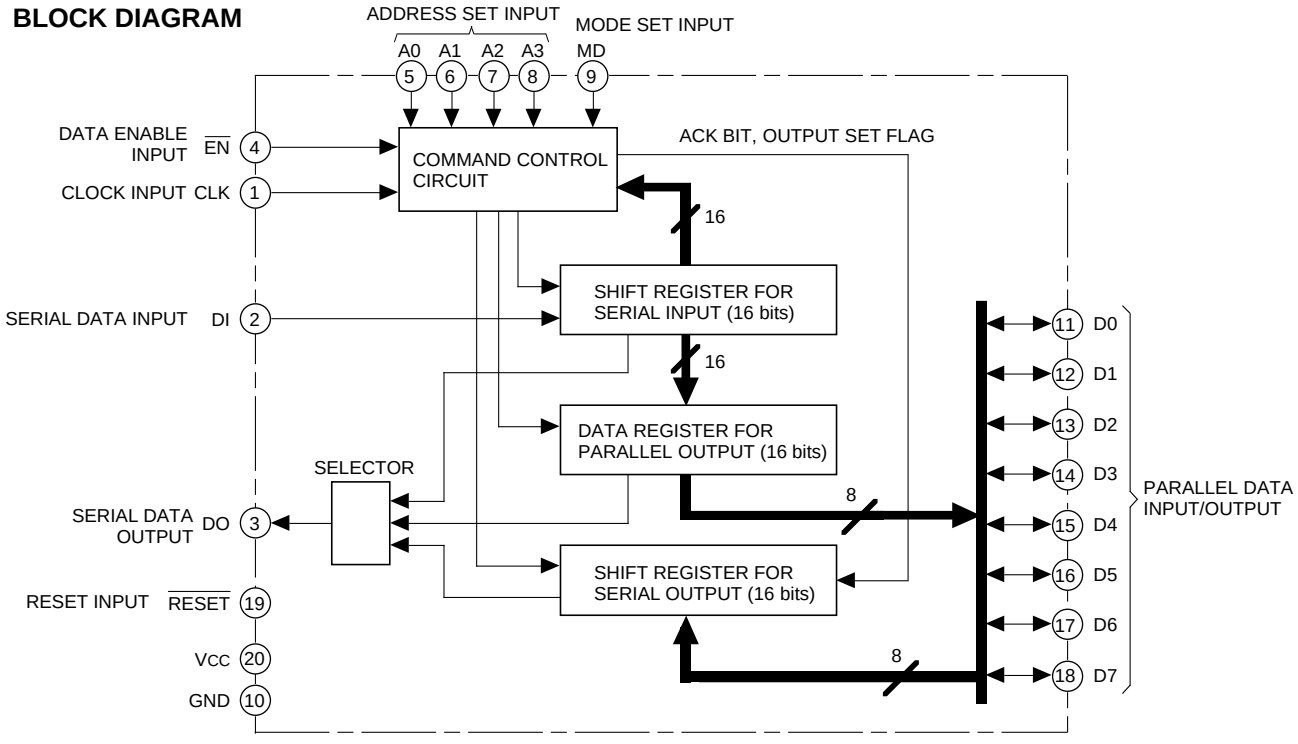


Outline 20P2N-A (20 pin SOP)

APPLICATIONS

Inter board communication in VTR, AV and OA equipment, expansion of microcomputer I/O port, etc.

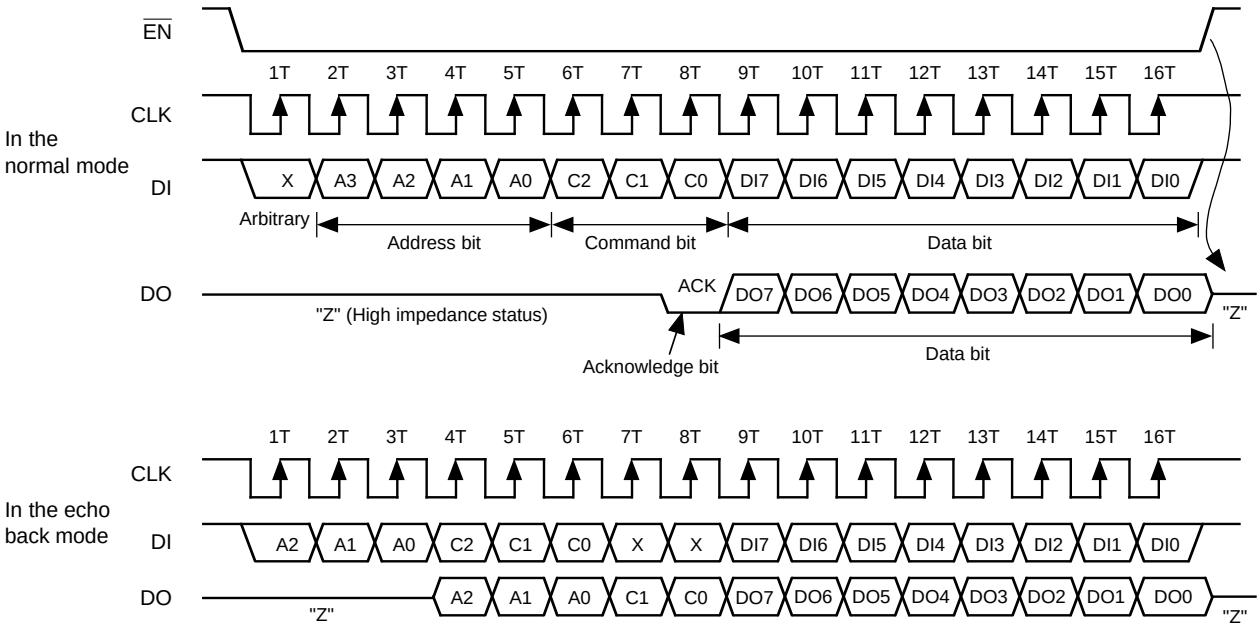
BLOCK DIAGRAM



BASIC PROTOCOL FOR SENDING AND RECEIVING DATA

The following diagram shows the basic protocol for sending and receiving data between the microcomputer and the M66013.
Falling of $\overline{EN}$ from "H" to "L" starts a series of sequence and rising of $\overline{EN}$ from "L" to "H" terminates the sequence. The concrete operation sequence is as follows:

(1) At a falling edge of $\overline{EN}$, 8-bit parallel data of I/O pins D0 to D7 are loaded into the shift register for serial output.
(2) At a rising edge of CLK, DI pin input data is read into the shift register for serial input and the counter for CLK counts up.
(3) When all address bits are read, a received address is compared with an address set in the address set pin to start the specified operation only when these addresses matches each other. The DO pin is kept in a high impedance status until the address comparison is complete.
When these addresses do not match, the DO pin keeps the high impedance status until the next sequence.
(4) When the addresses match each other, the operation for reading serial data from the DI pin and the operation for output serial data from the D0 pin in synchronization with a falling edge of CLK is carried out.
(5) When 16-bit data has been completely sent or received, the following operations are carried out in synchronization with a rising edge of $\overline{EN}$.
 (a) The DO output pin is placed in a high impedance status.
 (b) When the CLK counter does not count 16 CLK rising edges, operation (c) below is skipped and the counter is reset to wait for the next access.
 (c) When the counter value is 16, operation for writing to the data register for parallel output, operation for output to the I/O port or operation for setting/resetting the data setting flag is carried out, and the counter is then reset to wait for the next address.



Basic Protocol (The actual protocol differs depending on the command.)