

DESCRIPTION

The M66222 is a mail box that incorporates two complete CMOS shared memory cells of 128 × 8-bit configuration using high-performance silicon gate CMOS process technology, and are equipped with two access ports of A and B.

Access ports A and B are equipped with independent addresses \overline{CS} , \overline{WE} and \overline{OE} control pins and I/O pins to allow independent and asynchronous read/write operations individually. This product exclusively performs a write operation from A port and a read operation from B port for one memory, and a read operation from A port and a write operation from B port for the other memory.

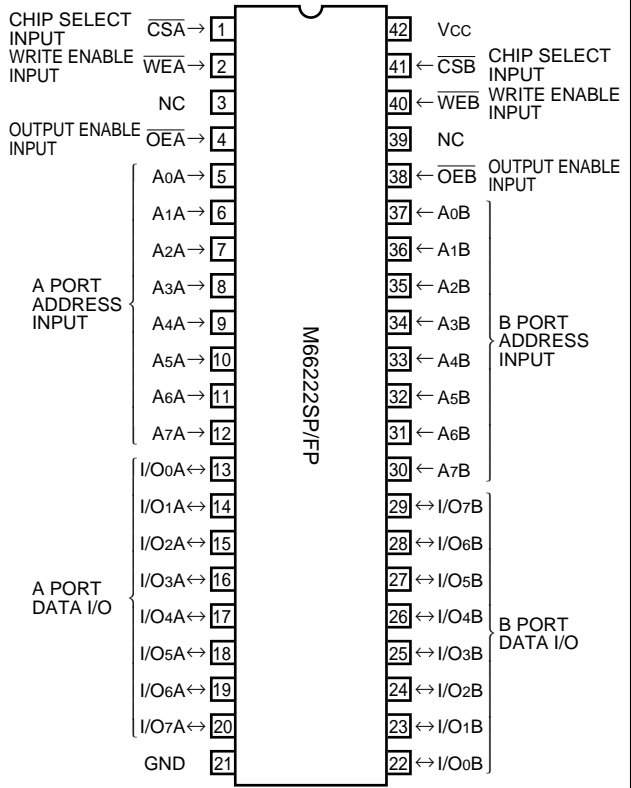
FEATURES

- Memory configuration of 128 × 8 bits × 2 memory areas
- High-speed access, address access time 40ns (typ.)
- Complete asynchronous accessibility from ports A and B
- Fixed read/write access ports for memory
- Completely static operation
- Low power dissipation CMOS design
- 5V single power supply
- TTL direct-coupled I/O
- 3-state output for I/O pins

APPLICATION

Inter-MCU data transfer memory, communication buffer memory

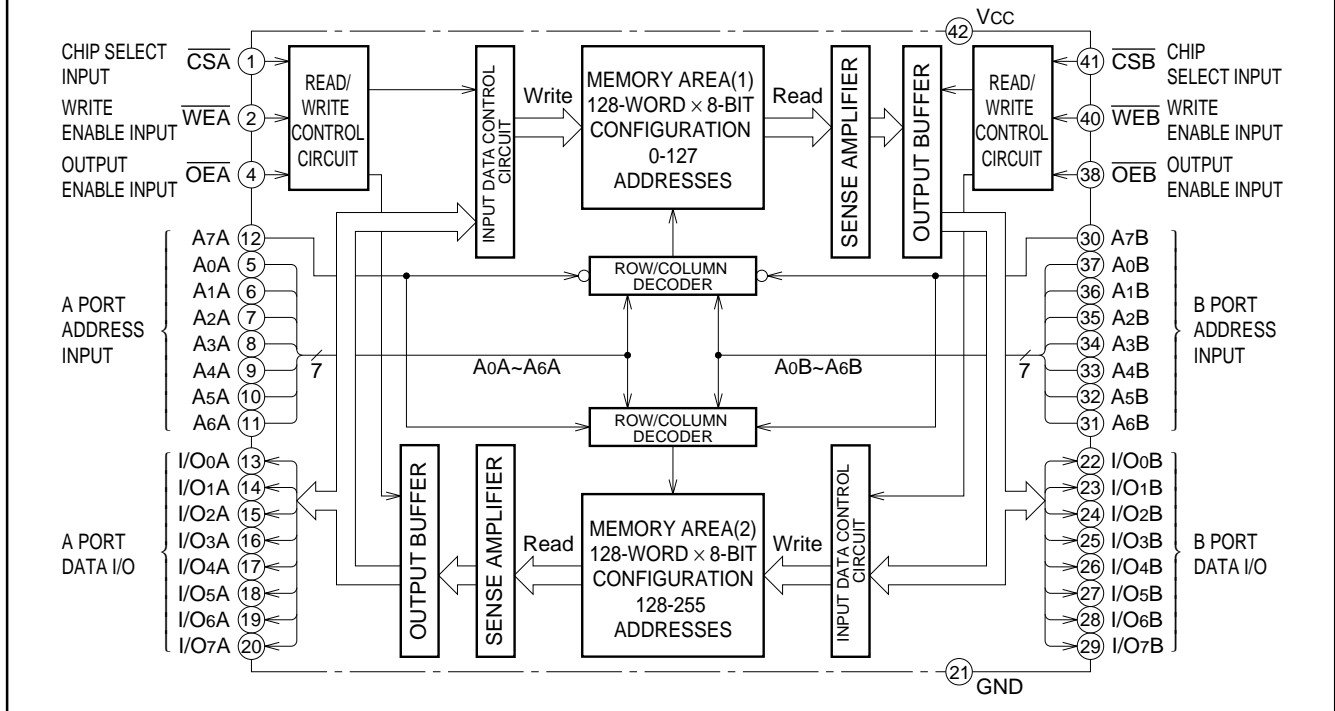
PIN CONFIGURATION (Top view)



Outline 42P4B
 42P2R-A

NC: No Connection

BLOCK DIAGRAM



FUNCTION

The M66222 is a mail box most suitable for inter-MCU data communication interface. Provision of two pairs of addresses and data buses in its shared memory cell of 128 × 8-bit configuration allows independent and asynchronous read/write operations from/to two access ports of A and B individually.

Two memory areas of 128 × 8-bit configuration are incorporated in the chip. Memory area (1) is used only to perform a write operation from A port and a read operation from B port, and memory area (2) only to perform a read operation from A port and a write operation from B port.

In this case, address A7A should be set to "L" when writing data from A port in memory area (1), and address A7B should be set to "L" when reading data from B port in memory area (1). Also, address A7B should be set to "H" when writing data from B port in memory area (2), and address A7A should be set to "H" when reading data from A port in memory area (2).

Therefore, an attempt to set addresses A7A and A7B from each port in a mode other than the above setting invalidates any read/write operation from the corresponding port (See Table 1 and Fig 1).

As a basic write operation to memory, one of addresses A0 to A7 is specified. The \overline{CS} signal is set to "L" to place one of I/O pins in the input mode. Also, the \overline{WE} signal is set to "L". Data at the I/O pin is written into memory.

As a read operation, the \overline{WE} signal is set to "H". Both \overline{CS} signal and \overline{OE} signal are set to "L" to place one of I/O pins in the output mode. One of addresses A0 to A7 is specified. Data at the specified address is thus output to the I/O pin.

When the \overline{CS} signal is set to "H", the chip enters a non-select state which inhibits a read and write operation. At this time, the output is placed in the floating state (high impedance state), thus allowing OR tie with another chip. When the \overline{OE} signal is set to "H", the output enters the floating state. In the I/O bus mode, setting the \overline{OE} signal to "H" at a write time avoids contention of I/O bus data. When the \overline{CS} signal is set to Vcc, the output enters the full stand-by state to minimize supply current (See Tables 2 and 3).

Table 1 Port Operations and Address A7 Setting Conditions

| Access port | A port | B port |
|-------------|-----------|-----------|
| Write | A7A = "L" | A7B = "H" |
| Read | A7A = "H" | A7B = "L" |

Note 1: No input data is written into any port having address A7 set under any condition other than Table 1. Undefined data is read to an output pin during a read operation.

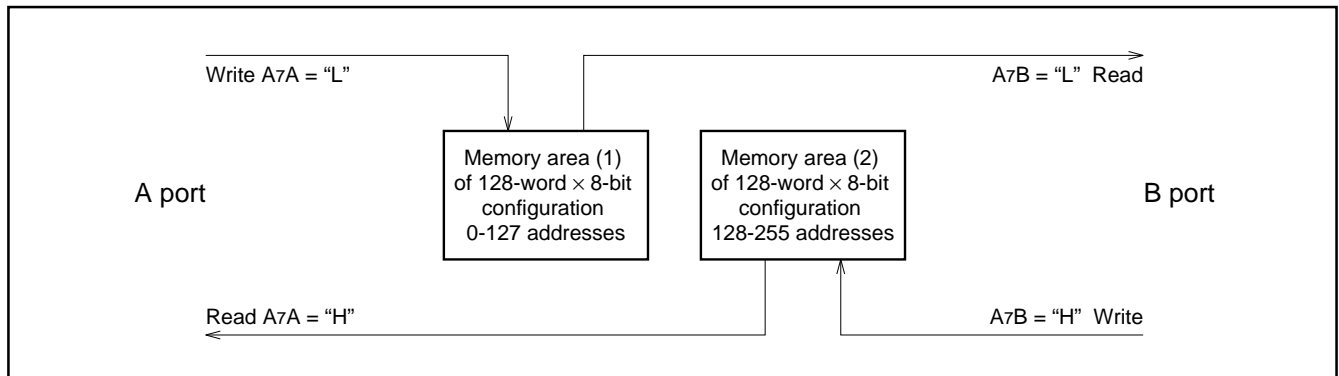


Fig 1 Access from Ports

Table 2 A Port Function Table

| CSA | WEA | OEA | A7A | Mode | I/O pin | Icc |
|-----|-----|-----|-----|------------|----------------|-----------|
| L | L | x | L | Write | DIN | Operation |
| | | | H | Invalid | DIN | Operation |
| L | H | L | L | Invalid | DOUT | Operation |
| | | | H | Read | DOUT | Operation |
| L | H | H | x | — | High impedance | Operation |
| H | x | x | x | Non-select | High impedance | Stand-by |

Note 2: x indicates "L" or "H". (Irrelevant)
 "H" = High level, "L" = Low level

Table 3 B Port Function Table

| CSB | WEB | OEB | A7B | Mode | I/O pin | Icc |
|-----|-----|-----|-----|------------|----------------|-----------|
| L | L | x | L | Invalid | DIN | Operation |
| | | | H | Write | DIN | Operation |
| L | H | L | L | Read | DOUT | Operation |
| | | | H | Invalid | DOUT | Operation |
| L | H | H | x | — | High impedance | Operation |
| H | x | x | x | Non-select | High impedance | Stand-by |

FUNCTIONAL DESCRIPTION

The M66222 with independent and asynchronous accessibility from two ports has the following four basic operations depending on an address and mode set from both ports:

- (1) A port Write B port Write
- (2) A port Write B port Read
- (3) A port Read B port Write
- (4) A port Read B port Read

In this case, the same address is not selected when the same read/write instruction is being executed at both ports as given in (1) and

(4). There is no concern about uncertainty of read/write data at an active address. If one port operates in the write mode and the other does in the read mode as given in (2) and (3), however, the same address may be selected. In this case, data of the port operating in the write mode is written. If the port in the read mode comes first, read data of the first-in port becomes uncertain until write data of the last-in port is determined (If the same address is selected, data of the port operating in the write mode is written into memory. Therefore, data of the port in the read mode may change from previously written data to newly written ones during the same cycle) (See Fig 2).

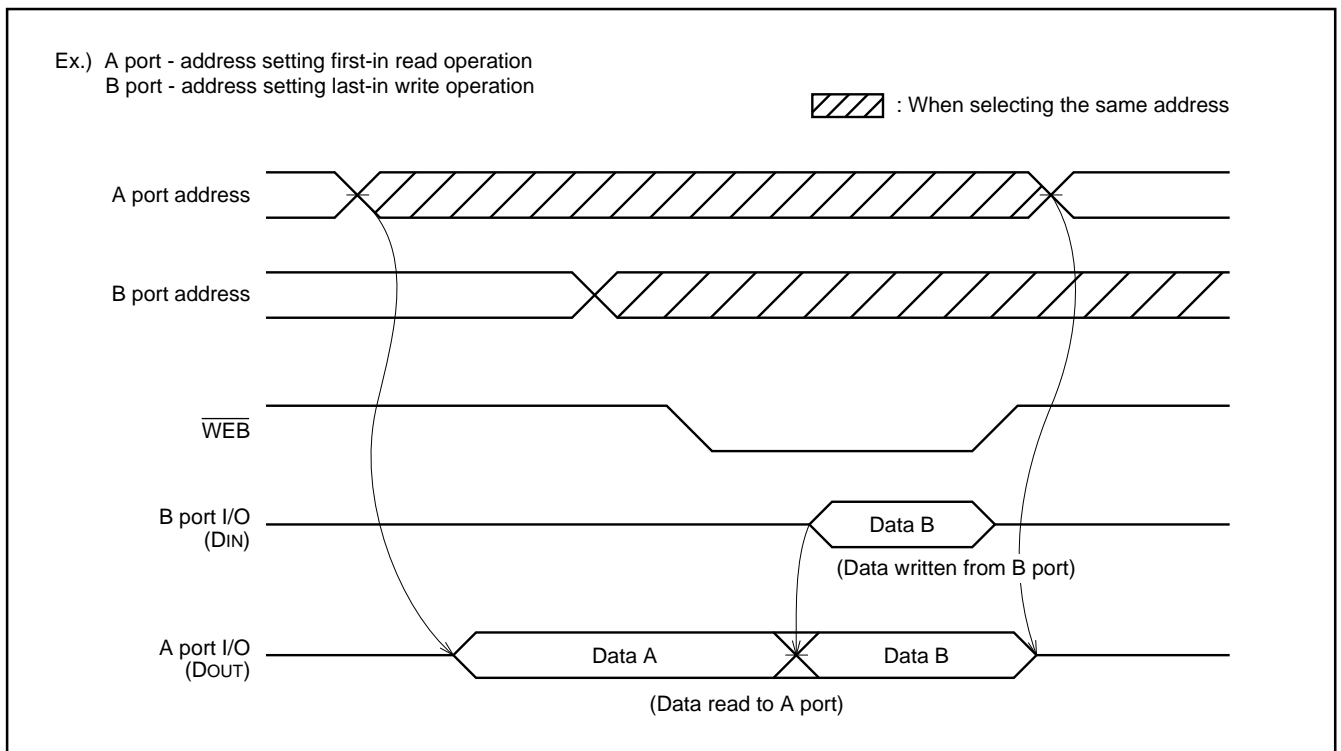


Fig 2 Example of Read Data Transition at Selection of Same Address

ABSOLUTE MAXIMUM RATINGS (Ta = 0 ~ 70°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Ratings | Unit |
|--------|---------------------------|---------------------------------------|------------------|------|
| Vcc | Supply voltage | When defining GND pin as a reference. | -0.3 ~ +7.0 | V |
| Vi | Input voltage | | -0.3 ~ Vcc + 0.3 | V |
| Vo | Output voltage | | 0 ~ Vcc | V |
| Pd | Maximum power dissipation | Ta = 25°C | 700 | mW |
| Tstg | Storage temperature range | | -65 ~ 150 | °C |

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Limits | | | Unit |
|--------|-----------------------------|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| Vcc | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Ground | | 0 | | V |
| Vi | Input voltage | 0 | | Vcc | V |
| Topr | Operating temperature range | 0 | | 70 | °C |

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, Vcc=5V±10%, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit | |
|--------|-------------------------------------|--|---|------|---------|------|----|
| | | | Min. | Typ. | Max. | | |
| VIH | "H" input voltage | | 2.2 | | Vcc+0.3 | V | |
| VIL | "L" input voltage | | -0.3 | | 0.8 | V | |
| VOH | "H" output voltage | IOH = -2mA | 2.4 | | | V | |
| VOL | "L" output voltage | IOL = 4mA | | | 0.5 | V | |
| IiH | "H" input current | Vi = Vcc | | | 10.0 | µA | |
| IiL | "L" input current | Vi = GND | | | -10.0 | µA | |
| IOZH | Off state "H" output current | CS = VIH or OE = VIH Vo = Vcc | | | 10.0 | µA | |
| IOZL | Off state "L" output current | CS = VIH or OE = VIH Vo = GND | | | -10.0 | µA | |
| Icc | Static current dissipation (active) | CS < 0.2V, Another input VIN > Vcc - 0.2V or VIN < 0.2V, Output pin open | | | 60 | mA | |
| ISB1 | Stand-by current | Two-port stand-by | | | 5 | mA | |
| ISB2 | | One-port stand-by | CSA or CSB = VIH IOUT = 0mA (Active port output pin open) | | | 60 | mA |
| ISB3 | | Two-port full stand-by | CSA, CSB > Vcc - 0.2V Another input VIN > Vcc - 0.2V or VIN < 0.2V | | | 0.1 | mA |
| ISB4 | | One-port full stand-by | CSA or CSB > Vcc - 0.2V Another input VIN > Vcc - 0.2V or VIN < 0.2V, IOUT = 0mA (Active port output pin open) | | | 30 | mA |
| CI | Input capacitance | | | | 10 | pF | |
| CO | Output capacitance in off state | | | | 15 | pF | |

Notes 3: The direction in which current flows into the IC is defined as positive (no sign).

4: The above typical values are standard values for Vcc=5V and Ta=25°C.

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, Vcc = 5V±10%, unless otherwise noted)

Read cycle

| Symbol | Parameter | Limits | | | Unit |
|-----------------------|--|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| tCR | Read cycle time | 70 | | | ns |
| ta(A) | Address access time | | | 70 | ns |
| ta(CS) | Chip select access time | | | 70 | ns |
| ta(OE) | Output enable access time | | | 35 | ns |
| t _{dis} (CS) | Output disable time after \overline{CS} (Note 5) | | | 35 | ns |
| t _{dis} (OE) | Output disable time after \overline{OE} (Note 5) | | | 35 | ns |
| t _{en} (CS) | Output enable time after \overline{CS} (Note 5) | 5 | | | ns |
| t _{en} (OE) | Output enable time after \overline{OE} (Note 5) | 5 | | | ns |
| t _v (A) | Data effective time after Address | 10 | | | ns |

TIMING REQUIREMENTS (Ta = 0 ~ 70°C, Vcc = 5V±10%, unless otherwise noted)

Write cycle

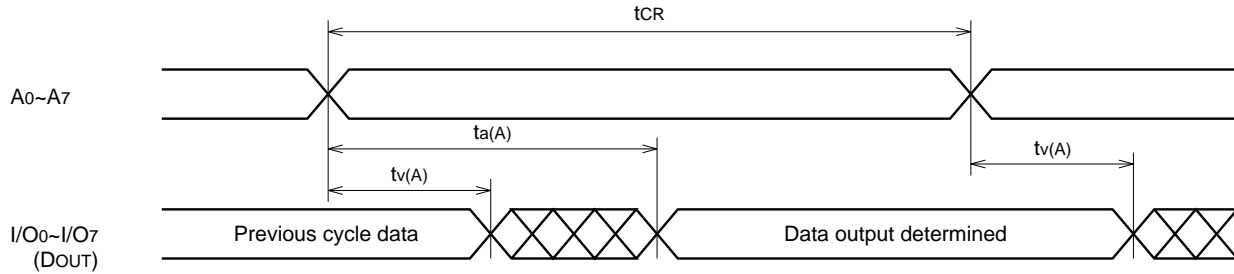
| Symbol | Parameter | Limits | | | Unit |
|-------------------------|--|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| tCW | Write cycle time | 70 | | | ns |
| t _w (WE) | Write pulse width | 45 | | | ns |
| t _{su} (A)1 | Address setup time (for \overline{WE}) | 0 | | | ns |
| t _{su} (A)2 | Address setup time (for \overline{CS}) | 0 | | | ns |
| t _{su} (A-WEH) | Address setup time for rise of \overline{WE} | 65 | | | ns |
| t _{su} (CS) | Chip select setup time | 65 | | | ns |
| t _{su} (D) | Data setup time | 40 | | | ns |
| t _h (D) | Data hold time | 0 | | | ns |
| t _{rec} (WE) | Write recovery time | 0 | | | ns |
| t _{dis} (WE) | Output disable time after \overline{WE} (Note 5) | | | 35 | ns |
| t _{dis} (OE) | Output disable time after \overline{OE} (Note 5) | | | 35 | ns |
| t _{en} (WE) | Output enable time after \overline{WE} (Note 5) | 0 | | | ns |
| t _{en} (OE) | Output enable time after \overline{OE} (Note 5) | 5 | | | ns |

Note 5: The time required for the output to change from a steady state to ±500mV under the load conditions shown in Figure 4.
This parameter is guaranteed but is not tested at shipment.

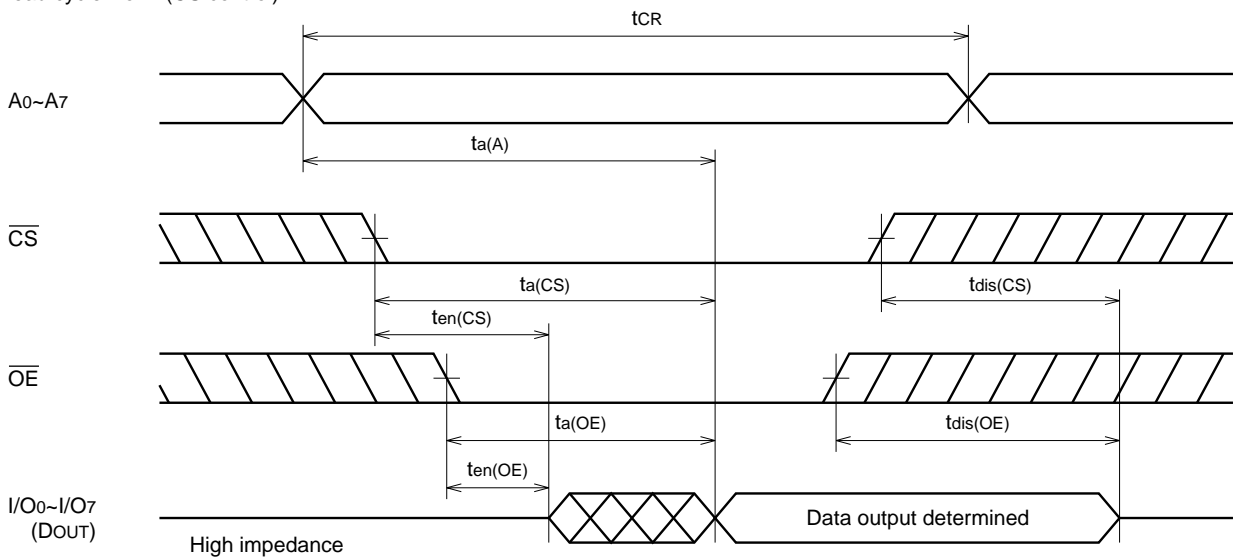
TIMING DIAGRAM

Read Cycle ($\overline{WE} = V_{IH}$)

Read cycle No. 1 (Address control) ($\overline{CS} = \overline{OE} = V_{IL}$)

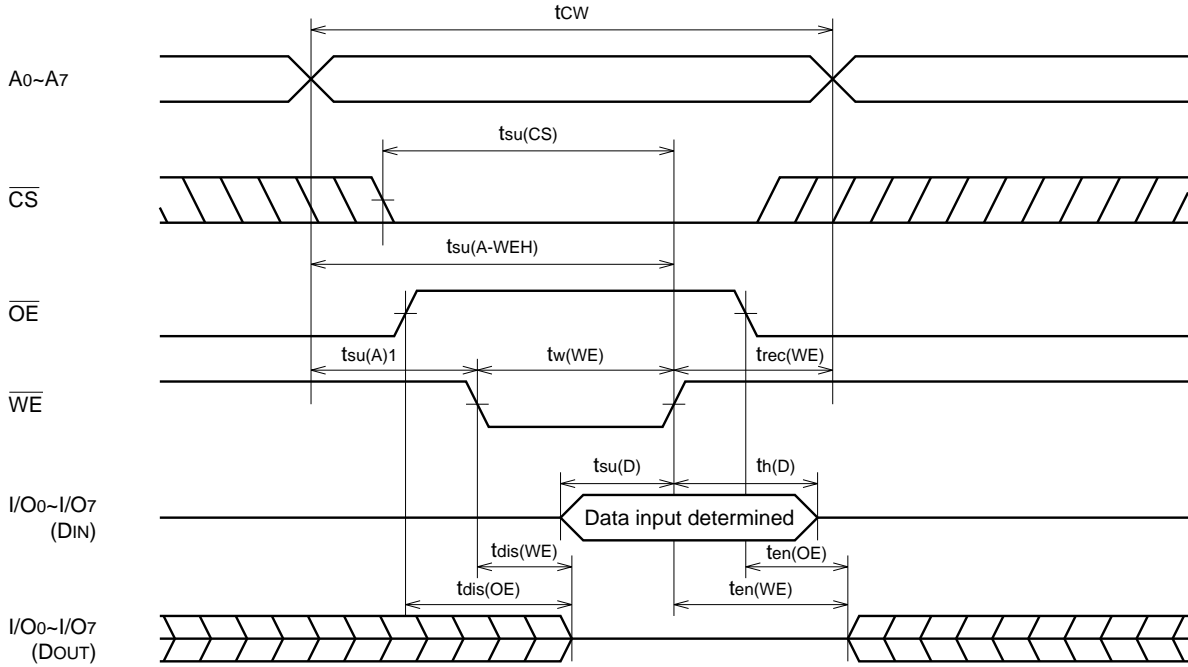


Read cycle No. 2 (\overline{CS} control)

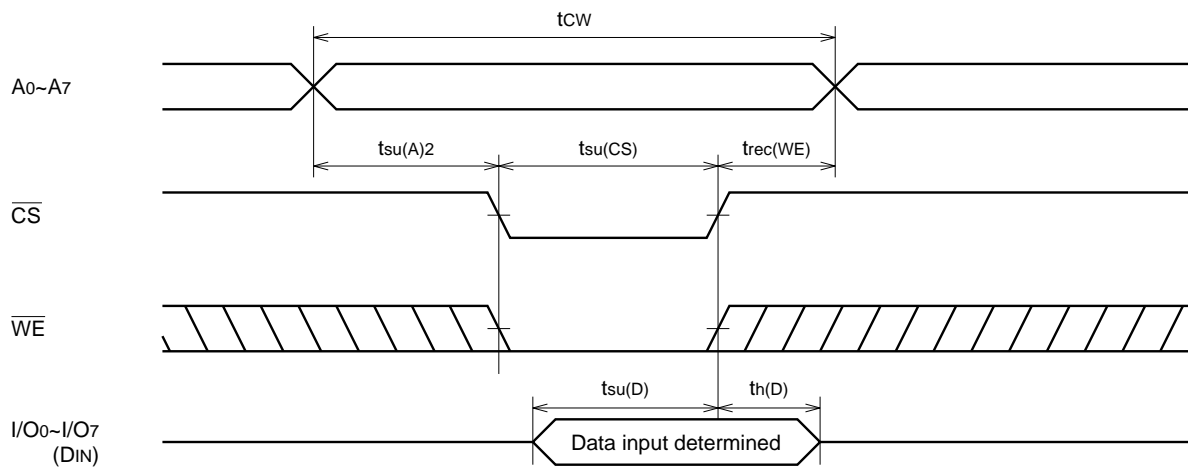


Write Cycle

Write cycle No.1 (\overline{WE} control) See Notes 6, 7 and 8.



Write cycle No.2 (\overline{CS} control) See Notes 7 and 8.



- Notes 6: The \overline{WE} of the port must be set to "H" when an address input changes.
- 7: A write operation is performed during the overlap period when both \overline{CS} and \overline{WE} are "L".
- 8: Do not apply any negative-phase signal from outside when an I/O pin is in output state.
- 9: The shaded part means a state in which a signal can be "H" or "L".

SWITCHING CHARACTERISTICS MEASUREMENT CIRCUIT

Input pulse level : $V_{IH} = 3.0V, V_{IL} = 0V$

Input pulse rise/fall time : $t_r/t_f = 5ns$

Input timing reference voltage : 1.5V

Output timing decision voltage : 1.5V

Output load : Figure 3 ~ 4 (The capacitance includes stray wiring capacitance and the probe input capacitance.)

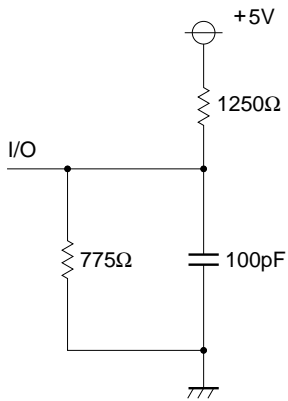


Fig 3. Output Load

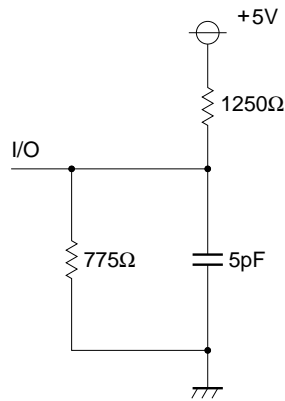


Fig 4. Output Load (to ten, tdis)