# MH1S64CWXTJ-12,-15,-1539

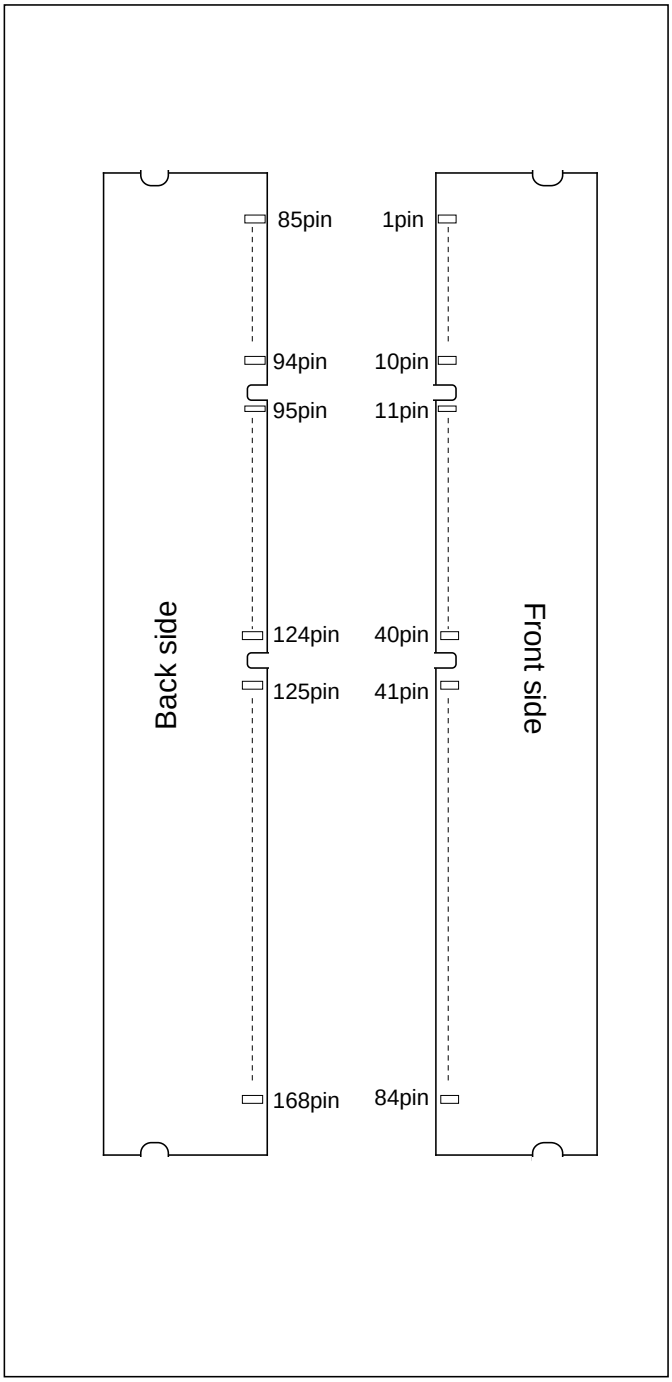
67108864-BIT (1048576-WORD BY 64-BIT)SynchronousDRAM

## DESCRIPTION

The MH1S64CWXTJ is 1048576-word by 64-bit Synchronous DRAM module. This consists of four industry standard 1Mx16 Synchronous DRAMs in TSOP and one industory standard EEPROM in TSSOP.

The mounting of TSOP on a card edge Dual Inline package provides any application where high densities and large quantities of memory are required.

This is a socket type - memory modules, suitable for easy interchange or addition of modules.




## FEATURES

| | Frequency | CLK Access Time (Component SDRAM) |
|---|---|---|
| -12 | 83MHz | 8ns(CL=3) |
| -15 | 67MHz | 9.5ns (CL=2) |
| -1539 | 67MHz | 9ns (CL=3) |

- Utilizes industry standard 1M x 16 Synchronous DRAMs TSOP and industry standard EEPROM in TSSOP
- 168-pin (84-pin dual in-line package)
- single 3.3V±0.3V power supply
- Clock frequency 83MHz/67MHz
- Fully synchronous operation referenced to clock rising edge
- Dual bank operation controlled by BA(Bank Address)
- /CAS latency- 1/2/3(programmable)
- Burst length- 1/2/4/8(programmable)
- Burst type- sequential / interleave(programmable)
- Column access - random
- Auto precharge / All bank precharge controlled by A10
- Auto refresh and Self refresh
- 4096 refresh cycle /64ms
- LVTTL Interface

## APPLICATION

main memory or graphic memory in computer systems

SPD table

| Byte No. | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 126 | 127 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MH1S64CWXTJ-12 | 80 | 08 | 04 | 0C | 08 | 01 | 40 | 00 | 01 | C0 | 80 | 00 | 80 | 00 | 06 | 01 | 05 | 02 | 06 | 01 | 01 | 83 | 06 |
| MH1S64CWXTJ-15 | 80 | 08 | 04 | 0C | 08 | 01 | 40 | 00 | 01 | F0 | 95 | 00 | 80 | 00 | 06 | 01 | 05 | 02 | 06 | 01 | 01 | 66 | 06 |
| MH1S64CWXTJ-1539 | 80 | 08 | 04 | 0C | 08 | 01 | 40 | 00 | 01 | F0 | 90 | 00 | 80 | 00 | 04 | 01 | 05 | 02 | 04 | 01 | 01 | 66 | 04 |

**PIN CONFIGURATION**

| PIN NO. | PIN NAME | PIN NO. | PIN NAME | PIN NO. | PIN NAME | PIN NO. | PIN NAME |
|---|---|---|---|---|---|---|---|
| 1 | VSS | 43 | VSS | 85 | VSS | 127 | VSS |
| 2 | DQ0 | 44 | NC | 86 | DQ32 | 128 | CKE |
| 3 | DQ1 | 45 | /S2 | 87 | DQ33 | 129 | NC |
| 4 | DQ2 | 46 | DQMB2 | 88 | DQ34 | 130 | DQMB6 |
| 5 | DQ3 | 47 | DQMB3 | 89 | DQ35 | 131 | DQMB7 |
| 6 | VDD | 48 | NC | 90 | VDD | 132 | NC |
| 7 | DQ4 | 49 | VDD | 91 | DQ36 | 133 | VDD |
| 8 | DQ5 | 50 | NC | 92 | DQ37 | 134 | NC |
| 9 | DQ6 | 51 | NC | 93 | DQ38 | 135 | NC |
| 10 | DQ7 | 52 | NC | 94 | DQ39 | 136 | NC |
| 11 | DQ8 | 53 | NC | 95 | DQ40 | 137 | NC |
| 12 | VSS | 54 | VSS | 96 | VSS | 138 | VSS |
| 13 | DQ9 | 55 | DQ16 | 97 | DQ41 | 139 | DQ48 |
| 14 | DQ10 | 56 | DQ17 | 98 | DQ42 | 140 | DQ49 |
| 15 | DQ11 | 57 | DQ18 | 99 | DQ43 | 141 | DQ50 |
| 16 | DQ12 | 58 | DQ19 | 100 | DQ44 | 142 | DQ51 |
| 17 | DQ13 | 59 | VDD | 101 | DQ45 | 143 | VDD |
| 18 | VDD | 60 | DQ20 | 102 | VDD | 144 | DQ52 |
| 19 | DQ14 | 61 | NC | 103 | DQ46 | 145 | NC |
| 20 | DQ15 | 62 | NC | 104 | DQ47 | 146 | NC |
| 21 | NC | 63 | NC | 105 | NC | 147 | NC |
| 22 | NC | 64 | VSS | 106 | NC | 148 | VSS |
| 23 | VSS | 65 | DQ21 | 107 | VSS | 149 | DQ53 |
| 24 | NC | 66 | DQ22 | 108 | NC | 150 | DQ54 |
| 25 | NC | 67 | DQ23 | 109 | NC | 151 | DQ55 |
| 26 | VDD | 68 | VSS | 110 | VDD | 152 | VSS |
| 27 | /WE | 69 | DQ24 | 111 | /CAS | 153 | DQ56 |
| 28 | DQMB0 | 70 | DQ25 | 112 | DQMB4 | 154 | DQ57 |
| 29 | DQMB1 | 71 | DQ26 | 113 | DQMB5 | 155 | DQ58 |
| 30 | /S0 | 72 | DQ27 | 114 | NC | 156 | DQ59 |
| 31 | NC | 73 | VDD | 115 | /RAS | 157 | VDD |
| 32 | VSS | 74 | DQ28 | 116 | VSS | 158 | DQ60 |
| 33 | A0 | 75 | DQ29 | 117 | A1 | 159 | DQ61 |
| 34 | A2 | 76 | DQ30 | 118 | A3 | 160 | DQ62 |
| 35 | A4 | 77 | DQ31 | 119 | A5 | 161 | DQ63 |
| 36 | A6 | 78 | VSS | 120 | A7 | 162 | VSS |
| 37 | A8 | 79 | NC | 121 | A9 | 163 | NC |
| 38 | A10 | 80 | NC | 122 | BA | 164 | NC |
| 39 | NC | 81 | NC | 123 | NC | 165 | SA0 |
| 40 | VDD | 82 | SDA | 124 | VDD | 166 | SA1 |
| 41 | VDD | 83 | SCL | 125 | NC | 167 | SA2 |
| 42 | CK0 | 84 | VDD | 126 | NC | 168 | VDD |

NC = No Connection

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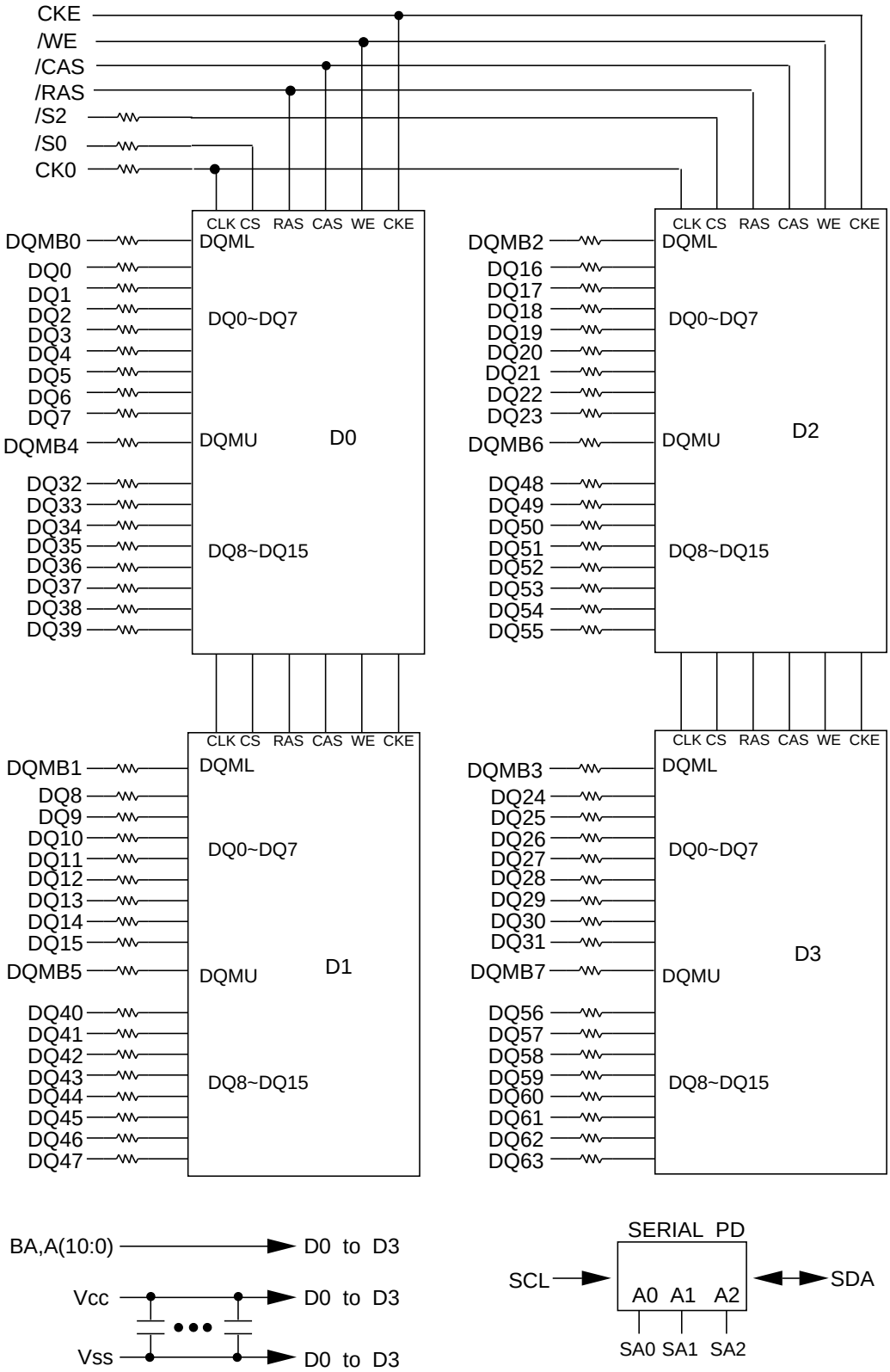
**Block Diagram**



## PIN FUNCTION

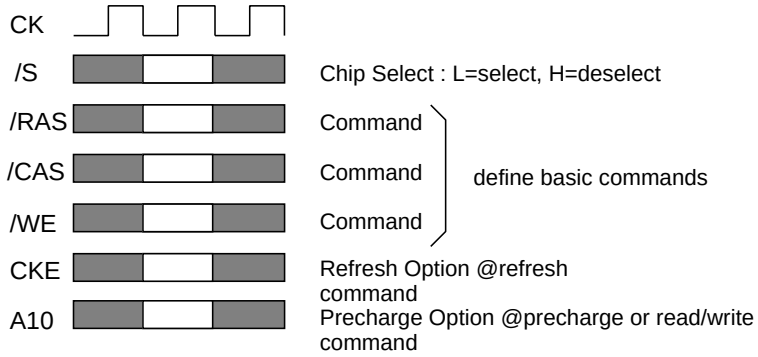
| | | |
|---|---|---|
| CK<br>(CK0) | Input | Master Clock:All other inputs are referenced to the rising edge of CK |
| CKE | Input | Clock Enable:CKE controls internal clock.When CKE is low,internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE E becomes asynchronous input.Self refresh is maintained as long as CKE is low. |
| /S<br>(/S0 &/S2) | Input | Chip Select: When /S is high,any command means No Operation. |
| /RAS,/CAS,/WE | Input | Combination of /RAS,/CAS,/WE defines basic commands. |
| A0-10 | Input | A0-10 specify the Row/Column Address in conjunction with BA.The Row Address is specified by A0-10.The Column Address is specified by A0-7.A10 is also used to indicate precharge option.When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, both banks are precharged. |
| BA | Input | Bank Address:BA is not simply BA.BA specifies the bank to which a command is applied.BA must be set with ACT,PRE,READ,WRITE commands |
| DQ0-63 | Input/Output | Data In and Data out are referenced to the rising edge of CK |
| DQMB0-7 | Input | Din Mask/Output Disable:When DQMB is high in burst write.Din for the current cycle is masked.When DQMB is high in burst read,Dout is disabled at the next but one cycle. |
| Vdd,Vss | Power Supply | Power Supply for the memory mounted module. |
| SLA | Input | Serial clock for serial PD |
| SDA | Output | Serial data for serial PD |

# BASIC FUNCTIONS

The MH1S64CWXTJ provides basic functions,bank(row)activate,burst read / write, bank(row)precharge,and auto / self refresh.

Each command is defined by control signals of /RAS,/CAS and /WE at CK rising edge. In addition to 3 signals,/S,CKE and A10 are used as chip select,refresh option,and precharge option,respectively.

To know the detailed definition of commands please see the command truth table.




**Activate(ACT) [/RAS =L, /CAS = /WE =H]**

ACT command activates a row in an idle bank indicated by BA.

**Read(READ) [/RAS =H,/CAS =L, /WE =H]**

READ command starts burst read from the active bank indicated by BA.First output data appears after /CAS latency. When A10 =H at this command,the bank is deactivated after the burst read(auto-precharge,**READA**).

**Write(WRITE) [/RAS =H, /CAS = /WE =L]**

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 =H at this command, the bank is deactivated after the burst write(auto-precharge,**WRITEA**).

**Precharge(PRE) [/RAS =L, /CAS =H,/WE =L]**

PRE command deactivates the active bank indicated by BA. This command also terminates burst read / write operation. When A10 =H at this command, both banks are deactivated(precharge all, **PREA**).

**Auto-Refresh(REFA) [/RAS =/CAS =L, /WE =CKE =H]**

PEFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

# COMMAND TRUTH TABLE

| COMMAND | MNEMONIC | CK n-1 | CK n | /S | /RAS | /CAS | /WE | BA | A10 | A0-9 |
|---|---|---|---|---|---|---|---|---|---|---|
| Deselect | DESEL | H | X | H | X | X | X | X | X | X |
| No Operation | NOP | H | X | L | H | H | H | X | X | X |
| Row Adress Entry & Bank Activate | ACT | H | X | L | L | H | H | V | V | V |
| Single Bank Precharge | PRE | H | X | L | L | H | L | V | L | X |
| Precharge All Bank | PREA | H | X | L | L | H | L | V | H | X |
| Column Address Entry & Write | WRITE | H | X | L | LH | H | L | V | L | V |
| Column Address Entry & Write with Auto-Precharge | WRITEA | H | X | L | H | L | L | V | H | V |
| Column Address Entry & Read | READ | H | X | L | H | L | H | V | L | V |
| Column Address Entry & Read with Auto Precharge | READA | H | X | L | H | L | H | V | H | V |
| Auto-Refresh | REFA | H | H | L | HL | L | H | X | X | X |
| Self-Refresh Entry | REFS | H | L | L | L | L | H | X | X | X |
| Self-Refresh Exit | REFSX | L | H | H | LX | X | X | X | X | X |
| | | L | H | L | H | H | H | X | X | X |
| Burst Terminate | TERM | H | X | L | H | H | L | X | X | X |
| Mode Register Set | MRS | H | X | L | L | L | L | L | L | V*1 |

H =High Level, L = Low Level, V = Valid, X = Don't Care, n = CK cycle number

NOTE:
1.A7-9 = 0, A0-6 = Mode Address

# FUNCTION TRUTH TABLE

| Current State | /S | /RAS | /CAS | /WE | Address | Command | Action |
|---|---|---|---|---|---|---|---|
| IDLE | H | X | X | X | X | DESEL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | BA | TBST | ILLEGAL*2 |
| | L | H | L | X | BA,CA,A10 | READ/WRITE | ILLEGAL*2 |
| | L | L | H | H | BA,RA | ACT | Bank Active,Latch RA |
| | L | L | H | L | BA,A10 | PRE/PREA | NOP*4 |
| | L | L | L | H | X | REFA | Auto-Refresh*5 |
| | L | L | L | L | Op-Code, Mode-Add | MRS | Mode Register Set*5 |
| ROW ACTIVE | H | X | X | X | X | DESEL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | BA | TBST | NOP |
| | L | H | L | H | BA,CA,A10 | READ/READA | Begin Read,Latch CA, Determine Auto-Precharge |
| | L | H | L | L | BA,CA,A10 | WRITE/ WRITEA | Begin Write,Latch CA, Determine Auto-Precharge |
| | L | L | H | H | BA,RA | ACT | Bank Active/ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | Precharge/Precharge All |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| READ | H | X | X | X | X | DESEL | NOP(Continue Burst to END) |
| | L | H | H | H | X | NOP | NOP(Continue Burst to END) |
| | L | H | H | L | BA | TBST | Terminate Burst |
| | L | H | L | H | BA,CA,A10 | READ/READA | Terminate Burst,Latch CA, Begin New Read,Determine Auto-Precharge*3 |
| | L | H | L | L | BA,CA,A10 | WRITE/WRITEA | Terminate Burst,Latch CA, Begin Write,Determine Auto-Precharge*3 |
| | L | L | H | H | BA,RA | ACT | Bank Active/ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | Terminate Burst,Precharge |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |

## FUNCTION TRUTH TABLE(continued)

| Current State | /S | /RAS | /CAS | /WE | Address | Command | Action |
|---|---|---|---|---|---|---|---|
| WRITE | H | X | X | X | X | DESEL | NOP(Continue Burst to END) |
| | L | H | H | H | X | NOP | NOP(Continue Burst to END) |
| | L | H | H | L | BA | TBST | Terminate Burst |
| | L | H | L | H | BA,CA,A10 | READ/READA | Terminate Burst,Latch CA, Begin Read,Determine Auto-Precharge*3 |
| | L | H | L | L | BA,CA,A10 | WRITE/ WRITEA | Terminate Burst,Latch CA, Begin Write,Determine Auto-Precharge*3 |
| | L | L | H | H | BA,RA | ACT | Bank Active/ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | Terminate Burst,Precharge |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| READ with AUTO PRECHARGE | H | X | X | X | X | DESEL | NOP(Continue Burst to END) |
| | L | H | H | H | X | NOP | NOP(Continue Burst to END) |
| | L | H | H | L | BA | TBST | ILLEGAL |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL |
| | L | H | L | L | BA,CA,A10 | WRITE/ WRITEA | ILLEGAL |
| | L | L | H | H | BA,RA | ACT | Bank Active/ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL*2 |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| WRITE with AUTO PRECHARGE | H | X | X | X | X | DESEL | NOP(Continue Burst to END) |
| | L | H | H | H | X | NOP | NOP(Continue Burst to END) |
| | L | H | H | L | BA | TBST | ILLEGAL |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL |
| | L | H | L | L | BA,CA,A10 | WRITE/ WRITEA | ILLEGAL |
| | L | L | H | H | BA,RA | ACT | Bank Active/ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL*2 |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |

## FUNCTION TRUTH TABLE(continued)

| Current State | /S | /RAS | /CAS | /WE | Address | Command | Action |
|---|---|---|---|---|---|---|---|
| PRE - CHARGING | H | X | X | X | X | DESEL | NOP(Idle after tRP) |
| | L | H | H | H | X | NOP | NOP(Idle after tRP) |
| | L | H | H | L | BA | TBST | ILLEGAL*2 |
| | L | H | L | X | BA,CA,A10 | READ/WRITE | ILLEGAL*2 |
| | L | L | H | H | BA,RA | ACT | ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | NOP*4(Idle after tRP) |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| ROW ACTIVATING | H | X | X | X | X | DESEL | NOP(Row Active after tRCD |
| | L | H | H | H | X | NOP | NOP(Row Active after tRCD |
| | L | H | H | L | BA | TBST | ILLEGAL*2 |
| | L | H | L | X | BA,CA,A10 | READ/WRITE | ILLEGAL*2 |
| | L | L | H | H | BA,RA | ACT | ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL*2 |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| WRITE RE-COVERING | H | X | X | X | X | DESEL | NOP |
| | L | H | H | H | X | NOP | NOP |
| | L | H | H | L | BA | TBST | ILLEGAL*2 |
| | L | H | L | X | BA,CA,A10 | READ/WRITE | ILLEGAL*2 |
| | L | L | H | H | BA,RA | ACT | ILLEGAL*2 |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL*2 |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |

## FUNCTION TRUTH TABLE(continued)

| Current State | /S | /RAS | /CAS | /WE | Address | Command | Action |
|---|---|---|---|---|---|---|---|
| RE- | H | X | X | X | X | DESEL | NOP(Idle after tRC) |
| FRESHING | L | H | H | H | X | NOP | NOP(Idle after tRC) |
| | L | H | H | L | BA | TBST | ILLEGAL |
| | L | H | L | X | BA,CA,A10 | READ/WRITE | ILLEGAL |
| | L | L | H | H | BA,RA | ACT | ILLEGAL |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| MODE | H | X | X | X | X | DESEL | NOP(Idle after tRSC) |
| REGISTER | L | H | H | H | X | NOP | NOP(Idle after tRSC) |
| SETTING | L | H | H | L | BA | TBST | ILLEGAL |
| | L | H | L | X | BA,CA,A10 | READ/WRITE | ILLEGAL |
| | L | L | H | H | BA,RA | ACT | ILLEGAL |
| | L | L | H | L | BA,A10 | PRE/PREA | ILLEGAL |
| | L | L | L | H | X | REFA | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |

ABBREVIATIONS:
H = Hige Level, L = Low Level, X = Don't Care
BA = Bank Address, RA = Row Address, CA = Column Address, NOP = No Operation

NOTES:
1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state.May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and / or date-integrity are not guaranteed.

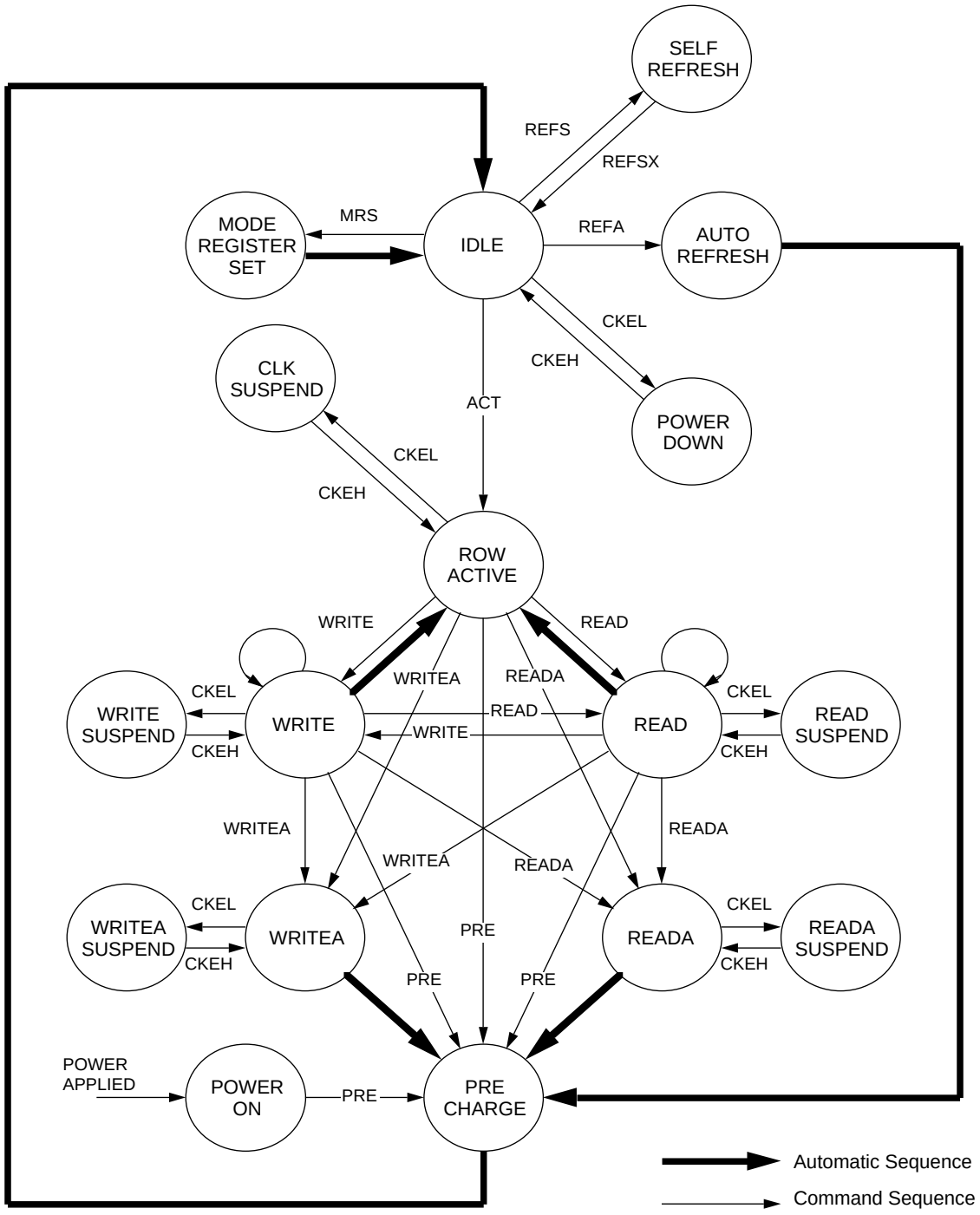
# FUNCTION TRUTH TABLE FOR CKE

| Current State | CK n-1 | CK n | /S | /RAS | /CAS | /WE | Add | Action |
|---|---|---|---|---|---|---|---|---|
| SELF - REFRESH*1 | H | X | X | X | X | X | X | INVALID |
| | L | H | H | X | X | X | X | Exit Self-Refresh(Idle after tRC) |
| | L | H | L | H | H | H | X | Exit Self-Refresh(Idle after tRC) |
| | L | H | L | H | H | L | X | ILLEGAL |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP(Maintain Self-Refresh) |
| POWER DOWN | H | X | X | X | X | X | X | INVALID |
| | L | H | X | X | X | X | X | Exit Power Down to Idle |
| | L | L | X | X | X | X | X | NOP(Maintain Self-Refresh) |
| ALL BANKS IDLE*2 | H | H | X | X | X | X | X | Refer to Function Truth Table |
| | H | L | L | L | L | H | X | Enter Self-Refresh |
| | H | L | H | X | X | X | X | Enter Power Down |
| | H | L | L | H | H | H | X | Enter Power Down |
| | H | L | L | H | H | L | X | ILLEGAL |
| | H | L | L | H | L | X | X | ILLEGAL |
| | H | L | L | L | X | X | X | ILLEGAL |
| | L | X | X | X | X | X | X | Refer to Current State = Power Down |
| ANY STATE other than listed above | H | H | X | X | X | X | X | Refer to Function Truth Table |
| | H | L | X | X | X | X | X | Begin CK0 Suspend at Next Cycle*3 |
| | L | H | X | X | X | X | X | Exit CK0 Suspend at Next Cycle*3 |
| | L | L | X | X | X | X | X | Maintain CK0 Suspend |

ABBREVIATIONS:
H = High Level, L = Low Level, X = Don't Care

NOTES:
1. CKE Low to High transition will re-enable CK and other inputs **asynchronously**.
   A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only form the All banks idle State.
3. Must be legal command.

## SIMPLIFIED STATE DIAGRAM



## POWER ON SEQUENCE

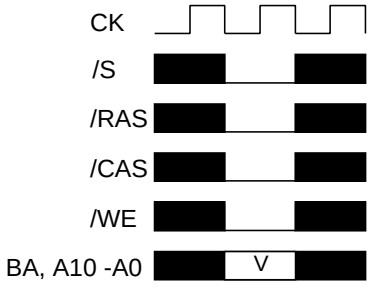
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high, DQMB0-7 high and NOP condition at the inputs.
2. Maintain stable power, stable cock, and NOP input conditions for a minimum of 500É s.
3. Issue precharge commands for all banks. (PRE or PREA)
4. After all banks become idle state (after tRP), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

After these sequence, the SDRAM is idle state and ready for normal operation.

## MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register(MRS). The mode register stores these date until the next MRS command, which may be issue when both banks are in idle state. After tRSC from a MRS command, the SDRAM is ready for new command.



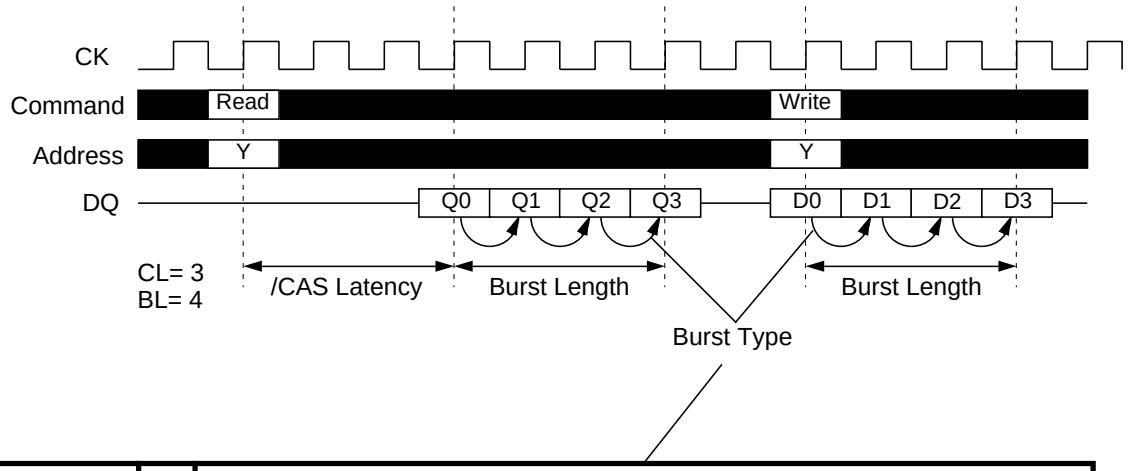

| BA | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | LTMODE | | | BT | BL | | |

| | CL | /CAS LATENCY |
|---|---|---|
| LATENCY MODE | 0 0 0 | R |
| | 0 0 1 | 1 |
| | 0 1 0 | 2 |
| | 0 1 1 | 3 |
| | 1 0 0 | R |
| | 1 0 1 | R |
| | 1 1 0 | R |
| | 1 1 1 | R |

| | BL | BT= 0 | BT= 1 |
|---|---|---|---|
| BURST LENGTH | 0 0 0 | 1 | 1 |
| | 0 0 1 | 2 | 2 |
| | 0 1 0 | 4 | 4 |
| | 0 1 1 | 8 | 8 |
| | 1 0 0 | R | R |
| | 1 0 1 | R | R |
| | 1 1 0 | R | R |
| | 1 1 1 | R | R |

| | | |
|---|---|---|
| BURST TYPE | 0 | SEQUENTIAL |
| | 1 | INTERLEAVED |

R:Reserved for Future Use




| Initial Address | | | BL | Column Addressing | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A2 | A1 | A0 | | Sequential | | | | | | | | Interleaved | | | | | | | |
| 0 | 0 | 0 | 8 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 0 | 1 | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 0 | 3 | 2 | 5 | 4 | 7 | 6 |
| 0 | 1 | 0 | | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 0 | 1 | 6 | 7 | 4 | 5 |
| 0 | 1 | 1 | | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 |
| 1 | 0 | 0 | | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 |
| 1 | 0 | 1 | | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 4 | 7 | 6 | 1 | 0 | 3 | 2 |
| 1 | 1 | 0 | | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 4 | 5 | 2 | 3 | 0 | 1 |
| 1 | 1 | 1 | | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | 0 | 0 | 4 | 0 | 1 | 2 | 3 | | | | | 0 | 1 | 2 | 3 | | | | |
| - | 0 | 1 | | 1 | 2 | 3 | 0 | | | | | 1 | 0 | 3 | 2 | | | | |
| - | 1 | 0 | | 2 | 3 | 0 | 1 | | | | | 2 | 3 | 0 | 1 | | | | |
| - | 1 | 1 | | 3 | 0 | 1 | 2 | | | | | 3 | 2 | 1 | 0 | | | | |
| - | - | 0 | 2 | 0 | 1 | | | | | | | 0 | 1 | | | | | | |
| - | - | 1 | | 1 | 0 | | | | | | | 1 | 0 | | | | | | |

## OPERATION DESCRIPTION

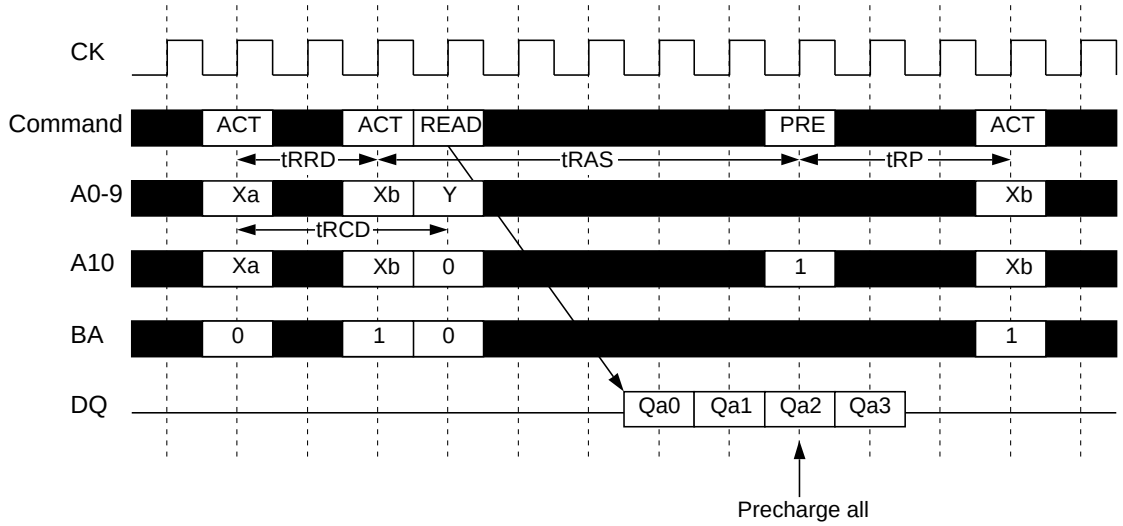
### BANK ACTIVATE

The SDRAM has two independent banks. Each bank is activated by the ACT command with the bank address(BA). A row is indicated by the row address A10-0. The minimum activation interval between one bank and the other bank is tRRD.

### PRECHARGE

The PRE command deactivates indicated by BA. When both banks are active, the precharge all command(PREA,PRE + A10=H) is available to deactivate them at the same time. After tRP from the precharge, an ACT command can be issued.

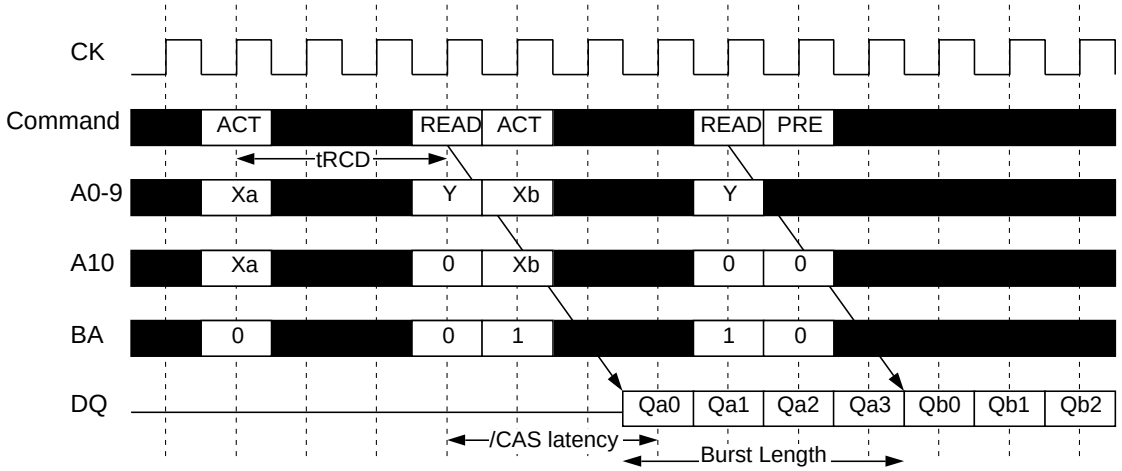
**Bank Activation and Precharge All (BL=4, CL=3)**



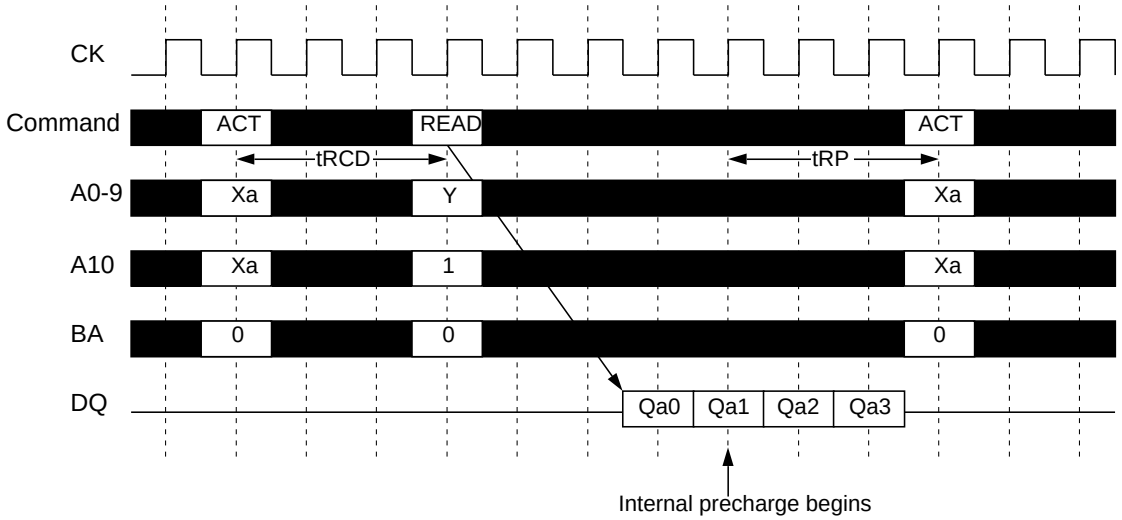

### READ

After tRCD from the bank activation, a READ command can be issued. 1st output date is available after the /CAS Latency from the READ, followed by (BL-1) consecutive date when the Burst Length is BL. The start address is specified by A7-0, and the address sequence of burst data is defined by the Burst Type. A READ command may be applied to any active bank, so the row precharge time(tRP) can be hidden behind continuous output data(in case of BL=8) by interleaving the dual banks. When A10 is high at a READ command, the auto-precharge(READA) is performed. Any command (READ, WRITE, PRE, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge start timing depends on /CAD Latency. The next ACT command can be issued after tRP from the internal precharge timing.

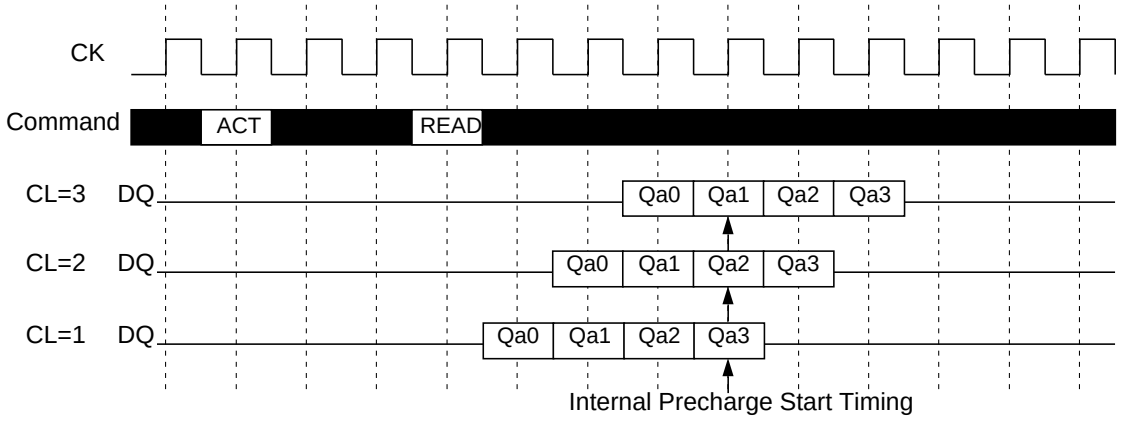
## Dual Bank Interleaving READ (BL=4, CL=3)




## READ with Auto-Precharge (BL=4, CL=3)



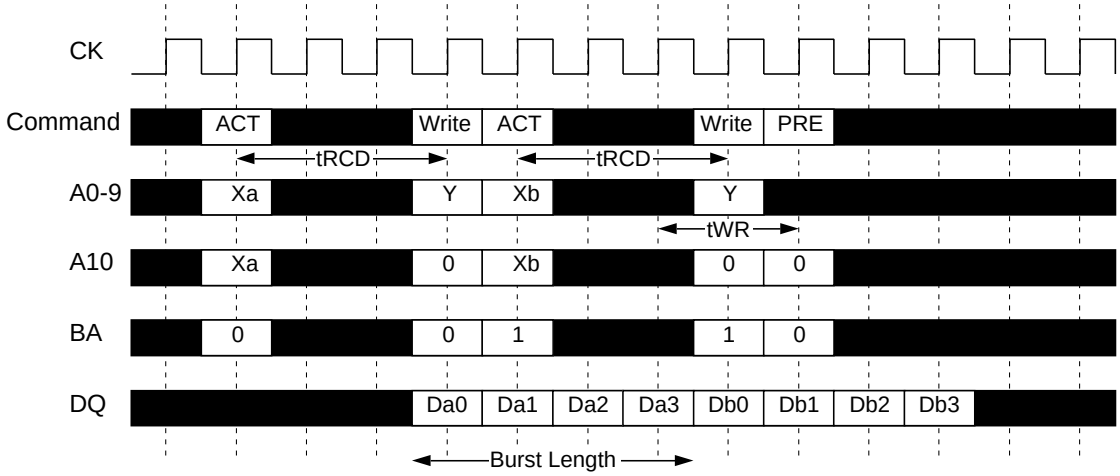

## READ Auto-Precharge Timing (BL=4)



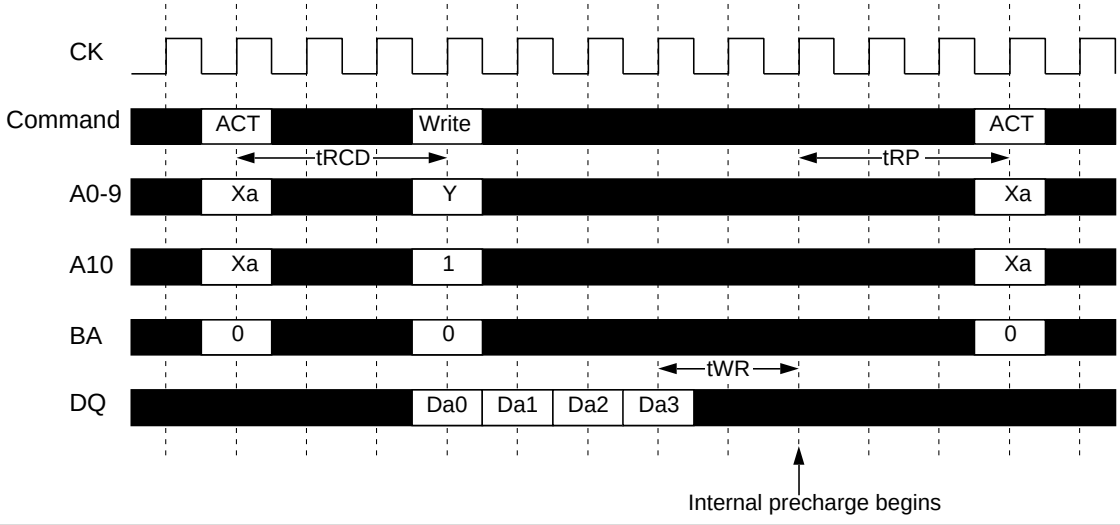
**WRITE**

After tRCD from the bank activation, a WRITE command can be issued. 1st input data is set at the same cycle as the WRITE. Following(BL-1) data are written into the RAM, when the Burst Length is BL. The start address is specified by A7-0, and the address sequence of burst data is defined by the Burst Type. A WRITE command may be applied to any active bank, so the row precharge time(tRP) can be hidden behind continuous input data (in case of BL=4) by interleaving the dual banks. From the last input data to the PRE command, the write recovery time (tWR) is required. When A10 is high at a WRITE command, the auto-precharge(WRITEA) is performed. Any command(READ, WRITE, PRE, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge begins at tWR after the last input data cycle. The next ACT command can be issued after tRP from the internal precharge timing.

**Dual Bank Interleaving WRITE (BL=4)**




**WRITE with Auto-Precharge (BL=4)**

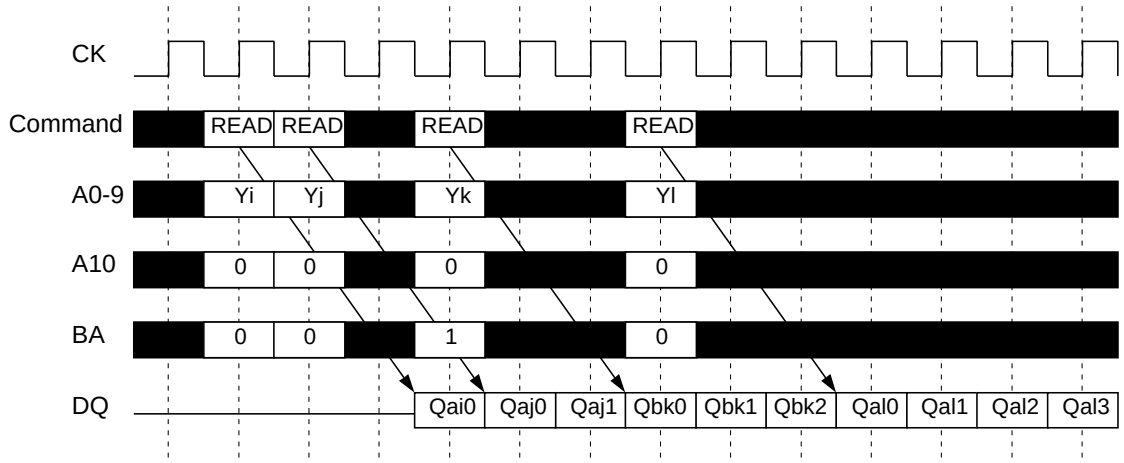


**BURST INTERRUPTION**

**[ Read Interrupted by Read ]**

Burst read option can be interrupted by new read of the same or the other bank. MH4S64CTJ allows random column access. READ to READ interval is minimum 1 CK

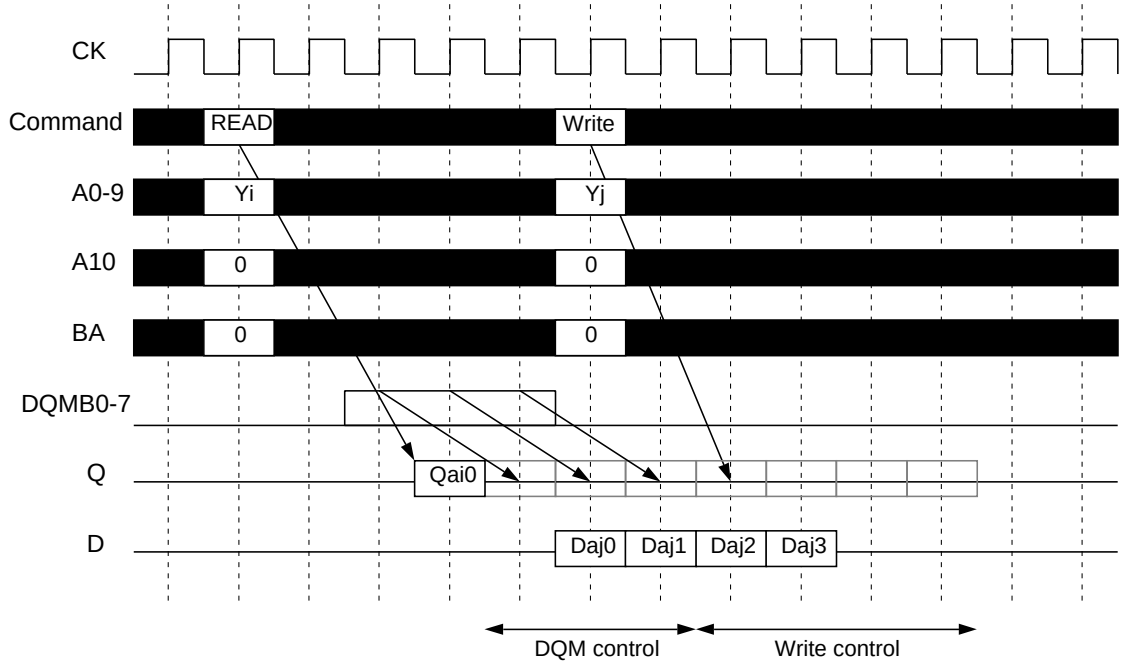
**Read Interrupted by Read (BL=4, CL=3)**




**[ Read Interrupted by Write ]**

Burst read operation can be interrupted by write of the same or the other bank. Random column access is allowed. In this case, the DQ should be controlled adequately by using the DQMB0-7 to prevent the bus contention. The output is disabled automatically 2 cycle after WRITE assertion.

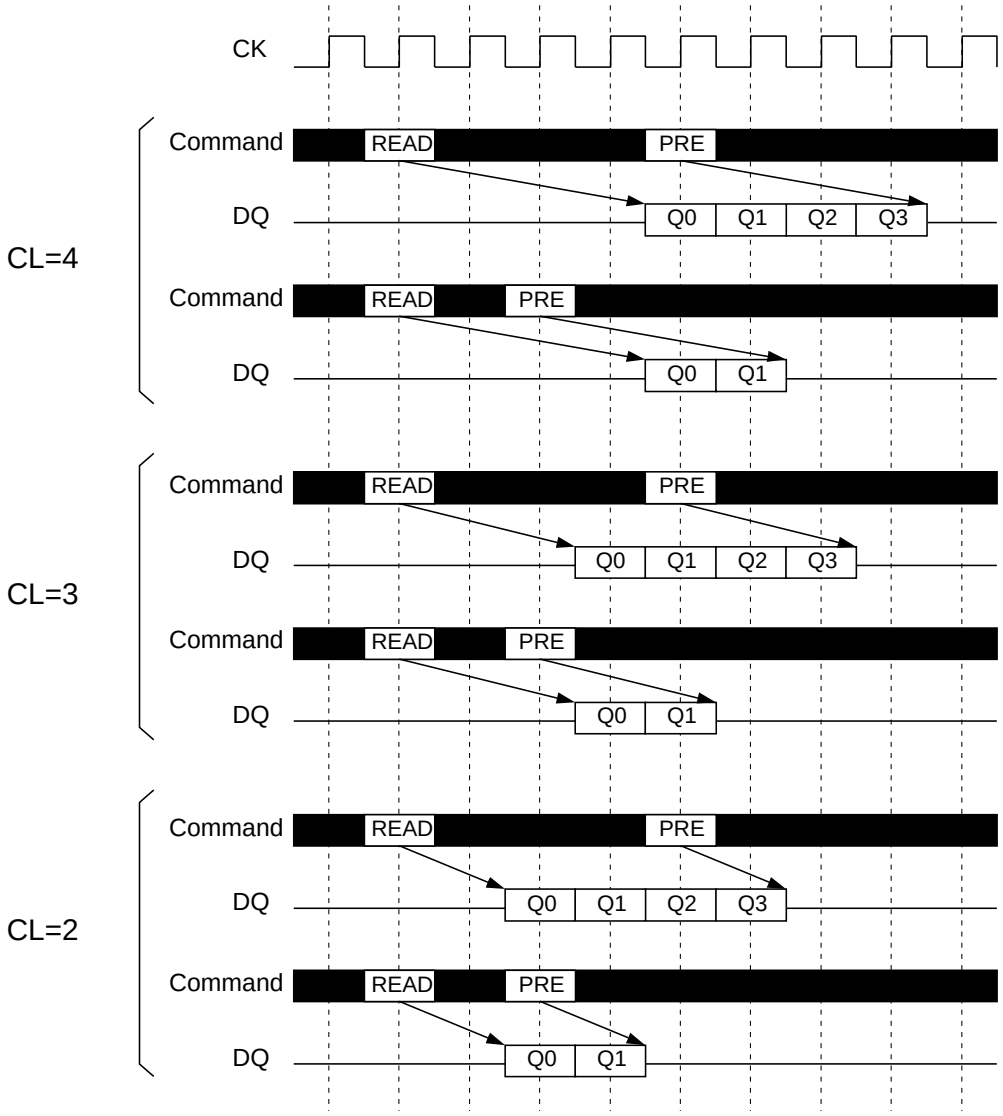
**Read Interrupted by Write (BL=4, CL=3)**



**[ Read Interrupted by Precharge ]**

Burst read operation can be interrupted by precharge of the same or the other bank. Read to PRE interval is minimum 1 CK. A PRE command disables the data output, depending on the /CAS Latency. The figure below shows examples, when the dataout is terminated.

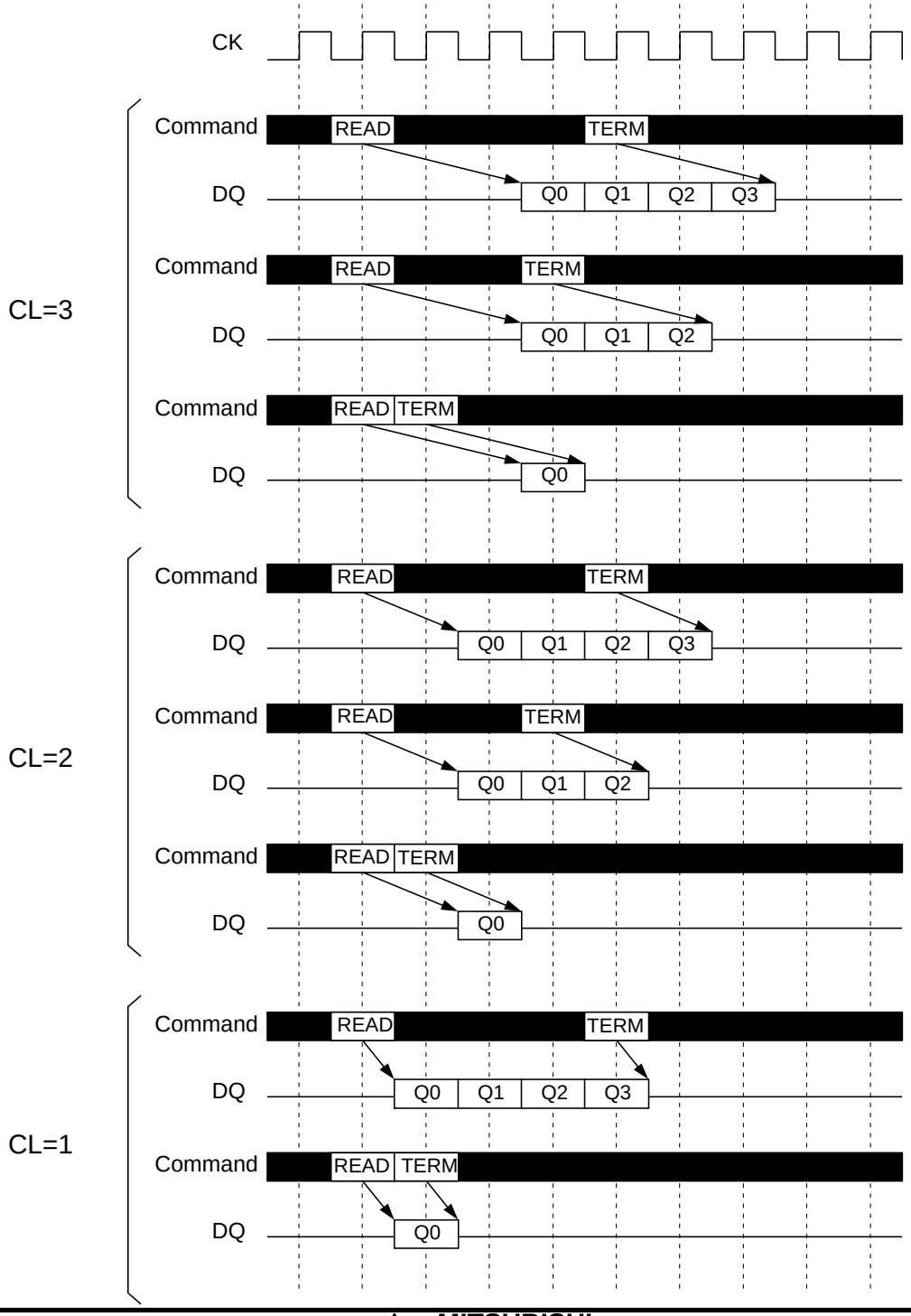
**Read Interrupted by Precharge (BL=4)**



**[ Read Interrupted by Burst Terminate ]**

Similarly to the precharge, burst terminate command can interrupt burst read operation and disable the data output. READ to TERM interval is minimum 1 CK. The figure below shows examples, when the dataout is terminated.

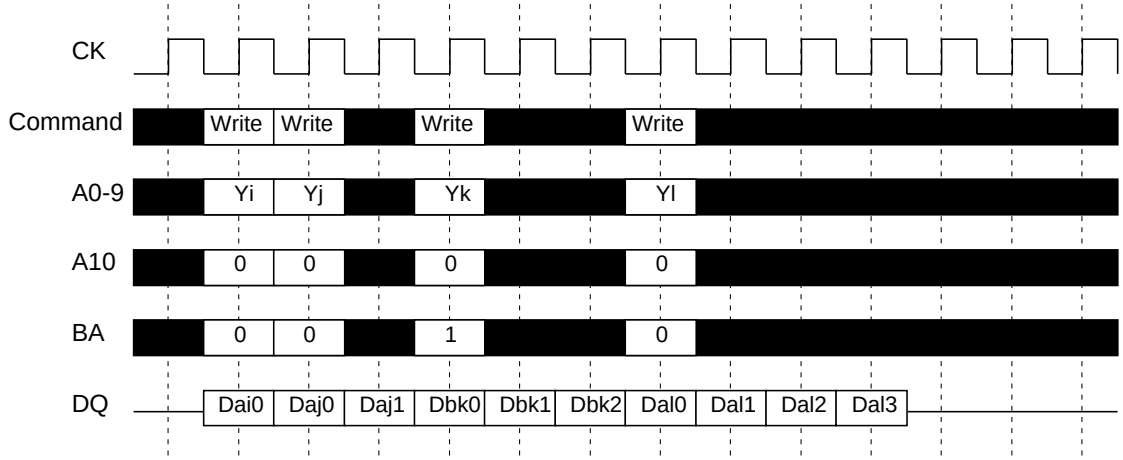
**Read Interrupted by Burst Terminate (BL=4)**



**[ Write Interrupted by Write ]**

Burst write operation can be interrupted by new write of the same or the other bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CK.

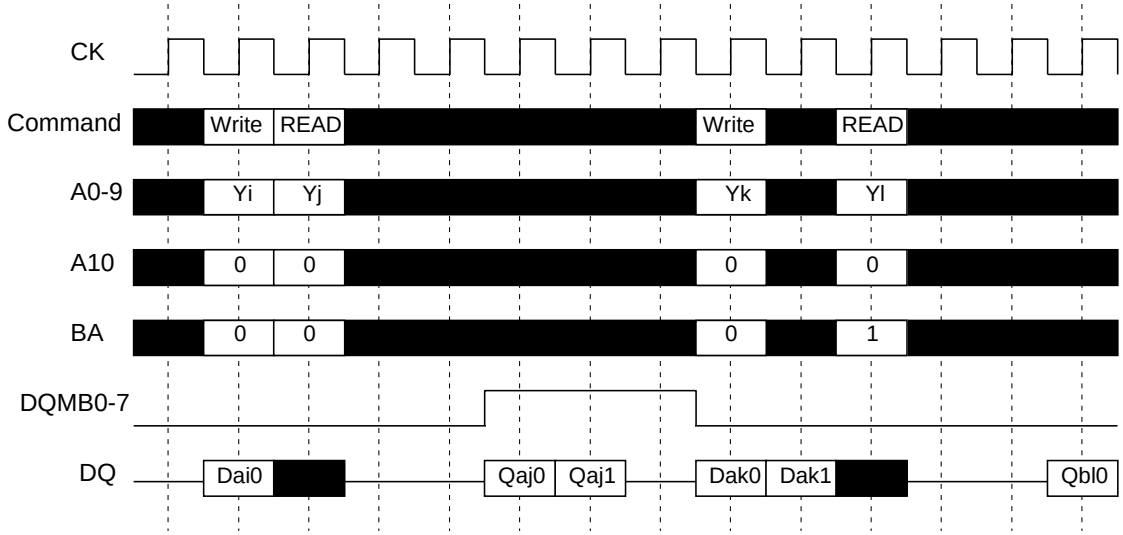
**Write Interrupted by Write (BL=4)**




**[ Write Interrupted by Read ]**

Burst write operation can be interrupted by read of the same or the other bank. Random column access is allowed. WRITE to READ interval is minimum 1 CK. The input data on DQ at the interrupting READ cycle is "don't care".

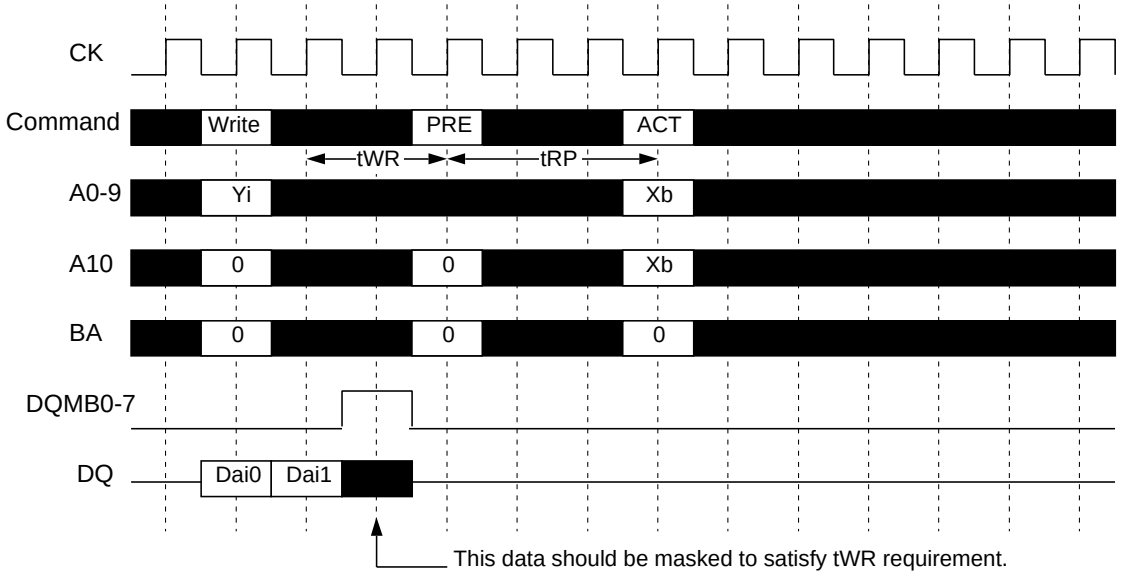
**Write Interrupted by Read (BL=4, CL=3)**



**[ Write Interrupted by Precharge ]**

Burst write operation can be interrupted by precharge of the same bank. Random column access is allowed. Because the write recovery time(tWR) is required between the last input data and the next PRE, 3rd data should be masked with DQMB0-7 shown as below.

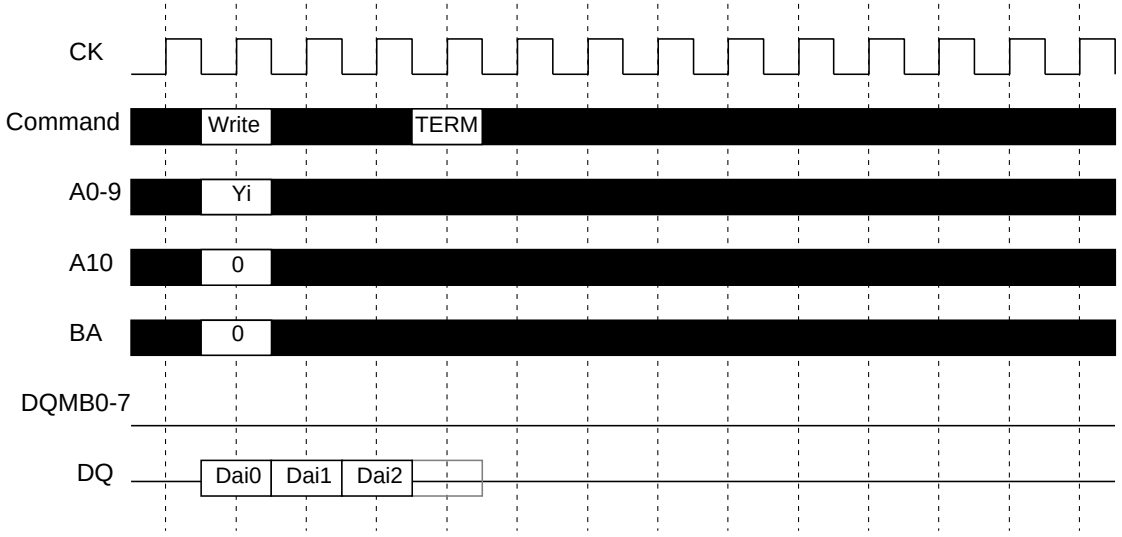
**Write Interrupted by Precharge (BL=4)**




**[ Write Interrupted by Burst Terminate ]**

Burst terminate command can terminate burst write operation. In this case, the write recovery time is not required and the bank remains active. The figure below shows the case 3 words of data are written. Random column access is allowed. WRITE to TERM interval is minimum 1 CK.

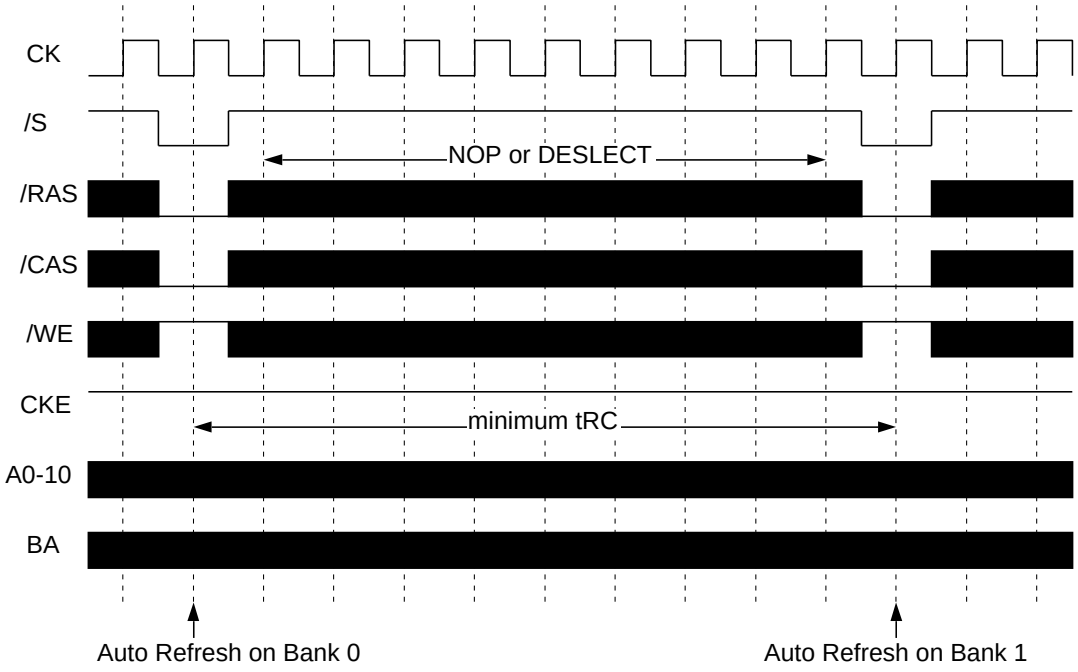
**Write Interrupted by Burst Terminate (BL=4)**



**AUTO REFRESH**

Single cycle of auto-refresh is initiated with a REFA(/CS=/RAS=/CAS=L, /WE=/CKE=H) command. The refresh address is generated internally. 4096 REFA cycle within 64ms refresh 16Mbit memory cells. The auto-refresh is performed on each bank alternately(ping-pong refresh). Before performing an auto-refresh, both banks must be in the idle state. Additional commands must not be supplied to the device before tRC from the REFA command.

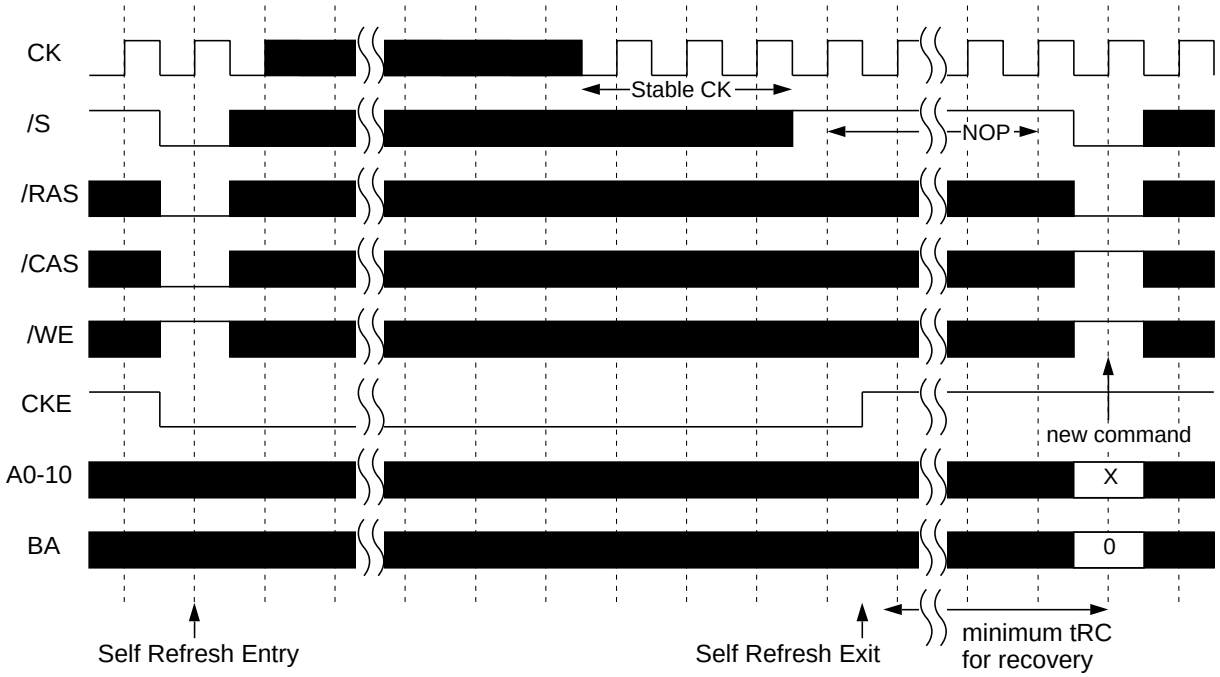
**Auto-Refresh**



**SELF REFRESH**

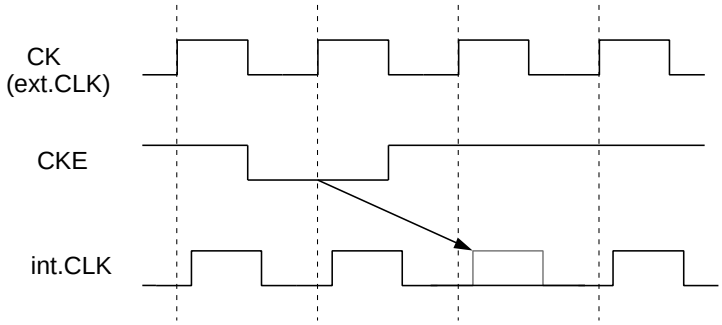
Self-refresh mode is entered by issuing a REFS command (/CS=/RAS=/CAS=L, /WE=H, CKE=L). Once the self-refresh is initiated, it is maintained as log as CKE is kept low.During the self-refresh mode, CKE is asynchronous and the only enabled input (but asynchronous), all other inputs including CK0 are disabled and ignored, and power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CK0 inputs, asserting DESEL or NOP command and then asserting CKE(REFSX). After tRC from REFSX both banks are in the idle state and a new command can be issued after tRC, but DESEL or NOP commands must be asserted till then.

**Self-Refresh**

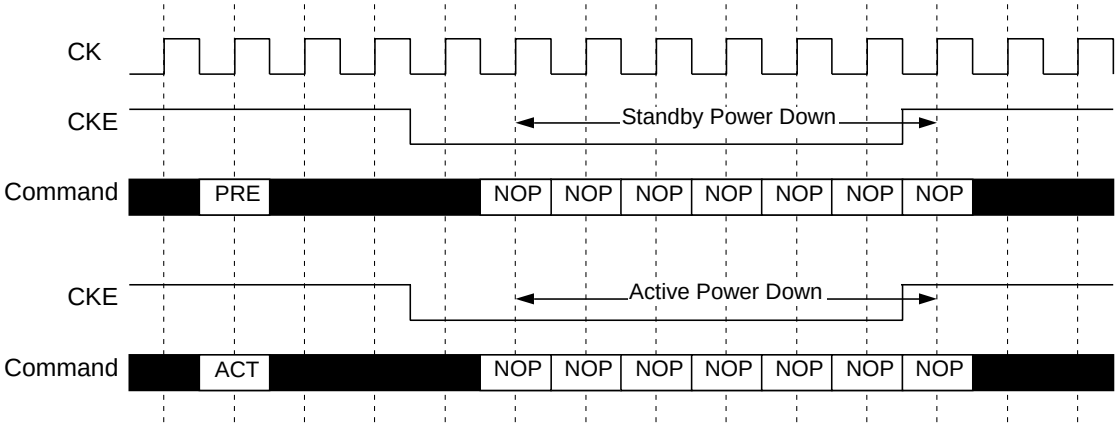


**CLK SUSPEND**

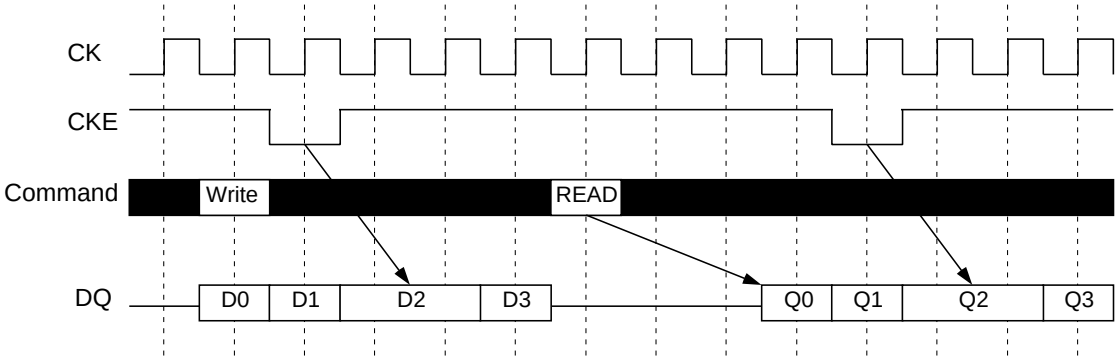
CKE controls the internal CLK at the following cycle. Figure below shows how CKE works. By negating CKE, the next internal CLK is suspended. The purpose of CLK suspend is power down, output suspend or input suspend. CKE is a synchronous input except during the self-refresh mode. CLK suspend can be performed either when the banks are active or idle, but a command at the following cycle is ignored.




**Power Down by CKE**



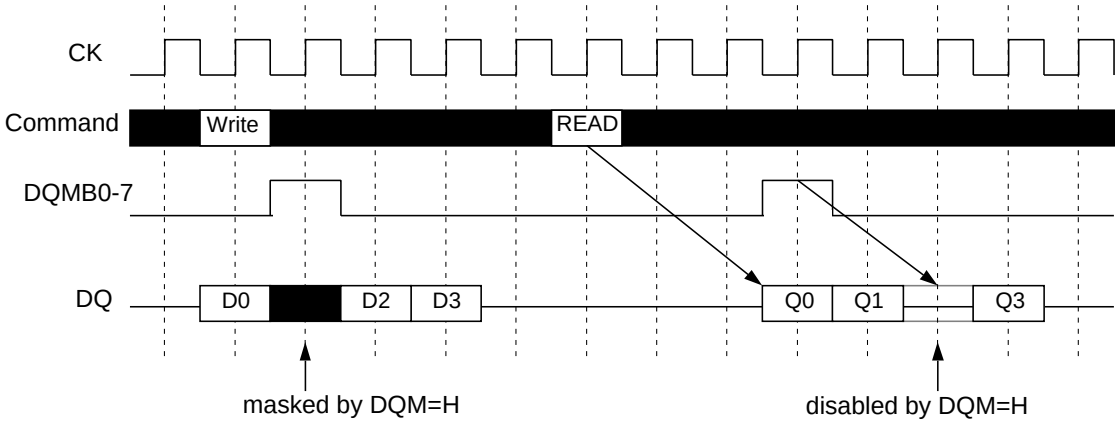

**DQ Suspend by CKE**



**DQM CONTROL**

DQMB0-7 is a dual function signal defined as the data mask for writes and the output disable for reads. During writes, DQMB0-7 masks input data word by word. DQMB0-7 to write mask latency is 0.
During reads, DQMB0-7 forces output to Hi-Z word by word. DQMB0-7 to output Hi-Z latency is 2.

**DQM Function**



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Condition | Ratings | Unit |
|---|---|---|---|---|
| Vdd | Supply Voltage | with respect to Vss | -0.5 ~ 4.6 | V |
| VI | Input Voltage | with respect to Vss | -0.5 ~ 4.6 | V |
| VO | Output Voltage | with respect to Vss | -0.5 ~ 4.6 | V |
| IO | Output Current | | 50 | mA |
| Pd | Power Dissipation | Ta=25°C | 4 | W |
| Topr | Operating Temperature | | 0 ~ 70 | °C |
| Tstg | Storage Temperature | | -40 ~ 100 | °C |

## RECOMMENDED OPERATING CONDITION

(Ta=0 ~ 70°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Vdd | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| Vss | Supply Voltage | 0 | 0 | 0 | V |
| VIH | High-Level Input Voltage all inputs | 2.0 | | Vdd+0.3 | V |
| VIL | Low-Level Input Voltage all inputs | -0.3 | | 0.8 | V |

## CAPACITANCE

(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

| Symbol | Parameter | Test Condition | Limits(max.) | Unit |
|---|---|---|---|---|
| CI(A) | Input Capacitance, address pin | VI = Vss<br>f=1MHz<br>Vi=25mVrms | 30 | pF |
| CI(C) | Input Capacitance, control pin | | 30 | pF |
| CI(K) | Input Capacitance, CK pin | | 15 | pF |
| CI/O | Input Capacitance, I/O pin | | 12 | pF |

## AVERAGE SUPPLY CURRENT from Vdd

(Ta=0 ~70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

| Symbol | Parameter | Test Condition | Limits(max) | | | Unit |
|---|---|---|---|---|---|---|
| | | | -12 | -15 | -1539 | |
| Icc1s | operating current, single bank | tRC=min.tCLK=min, BL=1, CL=3 | 360 | 360 | 300 | mA |
| Icc1d | operating current, dual bank | tRC=min.tCLK=min, BL=1, CL=3 | 520 | 520 | 440 | mA |
| Icc2h | standby current, CKE=H | both banks idle, tCLK=min, CKE=H | 72 | 72 | 64 | mA |
| Icc2l | standby current, CKE=L | both banks idle, tCLK=min, CKE=L | 8 | 8 | 8 | mA |
| Icc3 | active standby current | both banks active, tCLK=min, CKE=H | 140 | 140 | 120 | mA |
| Icc4 | burst current | tCLK=min, BL=4, CL=3, 1 bank idle(discerte) | 480 | 480 | 400 | mA |
| Icc5 | auto-refresh current | tRC=min, tCLK=min | 240 | 240 | 200 | mA |
| Icc6 | self-refresh current | CKE <0.2V | 4 | 4 | 4 | mA |

## AC OPERATING CONDITIONS AND CHARACTERISTICS

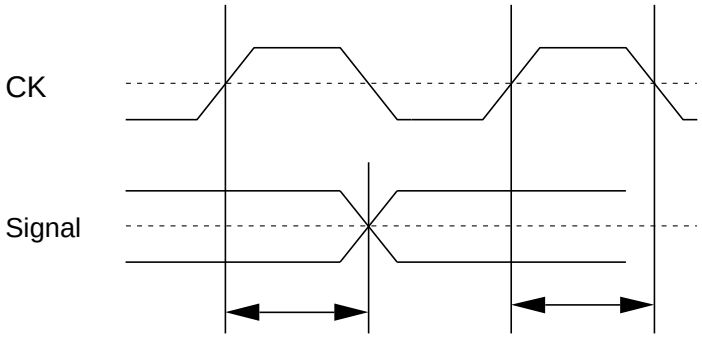
(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

| Symbol | Parameter | Test Condition | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| VOH(DC) | High-Level Output Voltage(DC) | IOH=-2mA | 2.4 | | V |
| VOL(DC) | Low-Level Output Voltage(DC) | IOL=2mA | | 0.4 | V |
| IOZ | Off-stare Output Current | Q floating VO=0 ~ Vdd | -10 | 10 | uA |
| Ii | Input Current | VIH=0 ~ Vdd+0.3V | -40 | 40 | uA |

## AC TIMING REQUIREMENTS

(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)
Input Pulse Levels: 0.8V to 2.0V
Input Timing Measurement Level: 1.4V

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -12 | | -15 | | -1539 | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| tCLK | CK cycle time | CL=1 | 30 | | 30 | | 30 | | ns |
| | | CL=2 | 15 | | 15 | | 20 | | ns |
| | | CL=3 | 12 | | 12 | | 15 | | ns |
| tCH | CK High pulse width | | 4 | | 4 | | 4 | | ns |
| tCL | CK Low pilse width | | 4 | | 4 | | 4 | | ns |
| tT | Transition time of CK | | 1 | 10 | 1 | 10 | 1 | 10 | ns |
| tIS | Input Setup time(all inputs) | | 3 | | 3 | | 3 | | ns |
| tIH | Input Hold time(all inputs) | | 1 | | 1 | | 1.5 | | ns |
| tRC | Row cycle time | | 100 | | 100 | | 120 | | ns |
| tRCD | Row to Column Delay | | 30 | | 30 | | 30 | | ns |
| tRAS | Row Active time | | 70 | 10000 | 70 | 10000 | 80 | 10000 | ns |
| tRP | Row Precharge time | | 30 | | 30 | | 40 | | ns |
| tWR | Write Recovery time | | 12 | | 12 | | 15 | | ns |
| tRRD | Act to Act Deley time | | 24 | | 24 | | 30 | | ns |
| tRSC | Mode Register Set Cycle time | | 24 | | 24 | | 30 | | ns |
| tPDE | Power Down Exit time | | 12 | | 12 | | 15 | | ns |
| tREF | Refresh Interval time | | | 65.6 | | 65.6 | | 65.6 | ms |



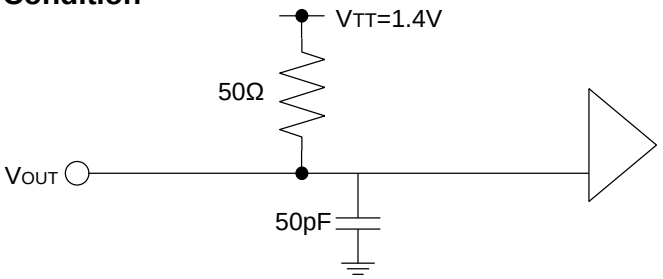

Any AC timing is referenced to the input signal crossing through 1.4V.

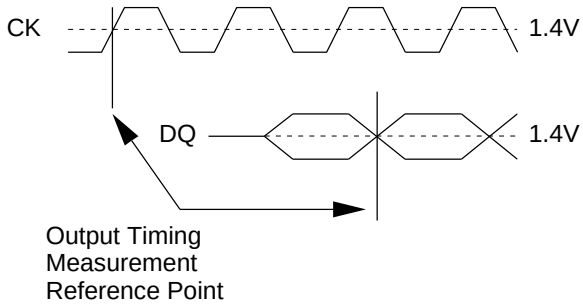
## SWITCHING CHARACTERISTICS

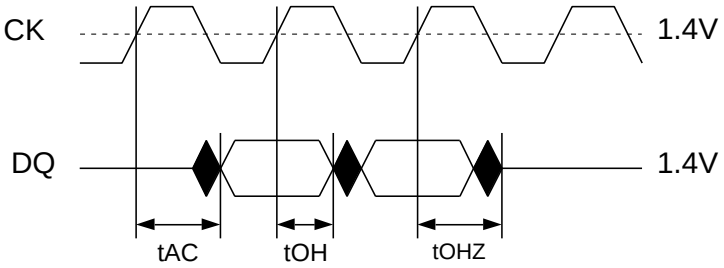
(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -12 | | -15 | | -1539 | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| tAC | Access time from CK | CL=1 | | 27 | | 27 | | 30 | ns |
| | | CL=2 | | 9.5 | | 9.5 | | 12 | ns |
| | | CL=3 | | 8 | | 8 | | 9 | ns |
| tCAC | Column Access Time | | | 24.5 | | 24.5 | | 30 | ns |
| tRAC | Row Access Time | | | 54.5 | | 54.5 | | 60 | ns |
| tOH | Output Hold time from CK | | 3 | | 3 | | 3 | | ns |
| tOLZ | Delay time, output low impedance from CK | | 0 | | 0 | | 0 | | ns |
| tOHZ | Delay time, output high impedance from CK | | 3 | 8 | 3 | 8 | 3 | 10 | ns |

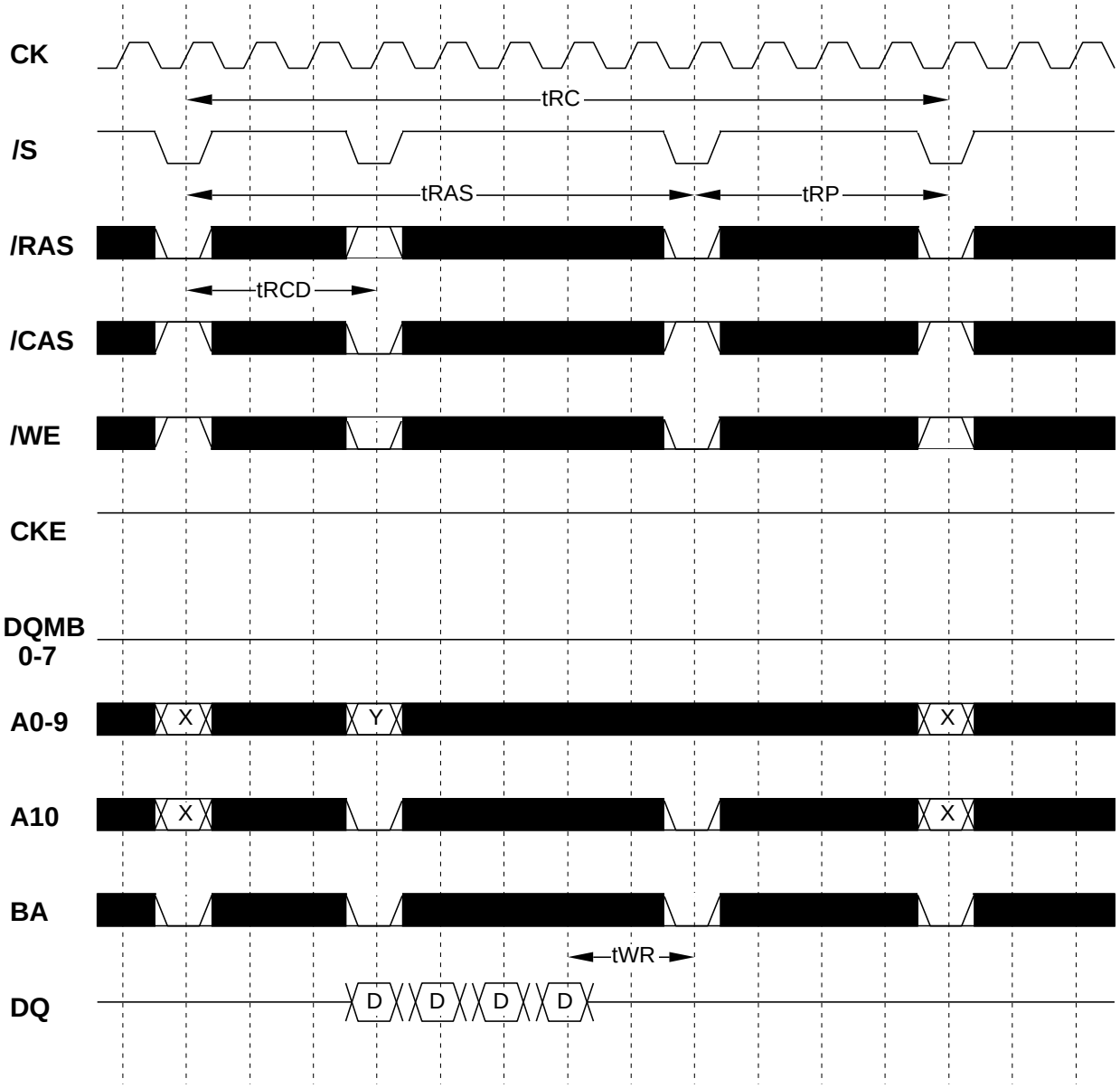
**Output Load Condition**



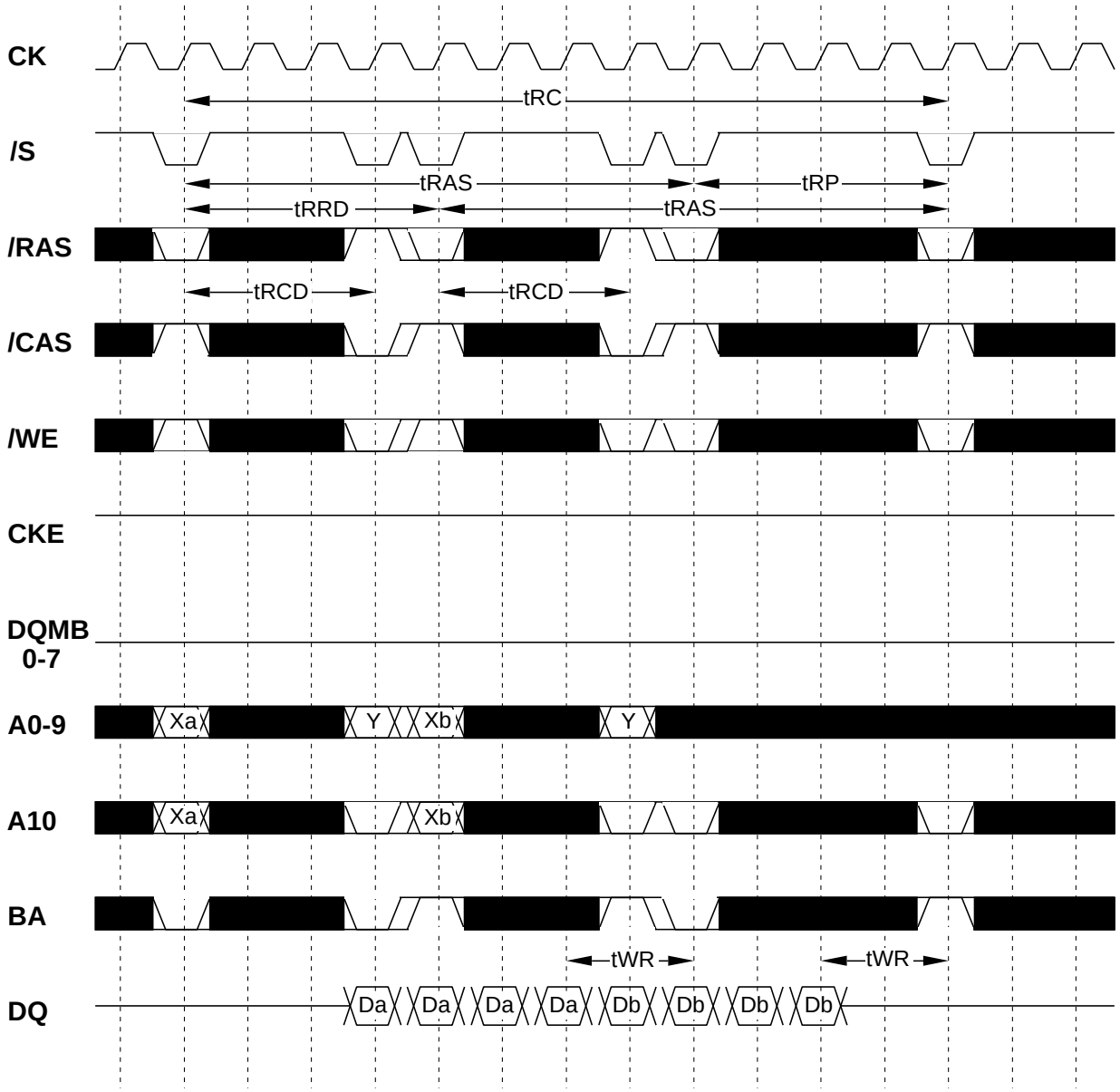



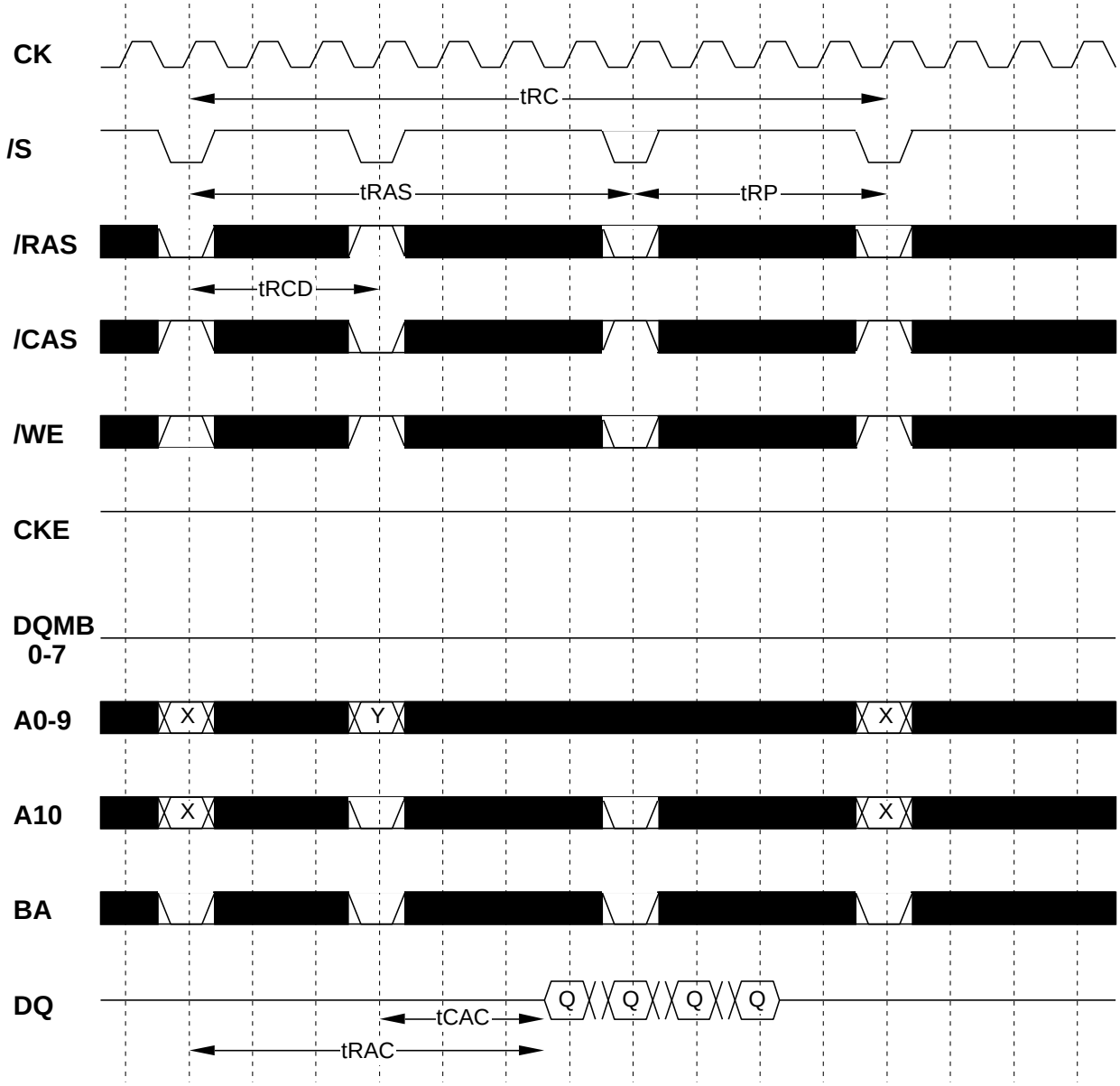
**WRITE CYCLE (single bank)** BL=4



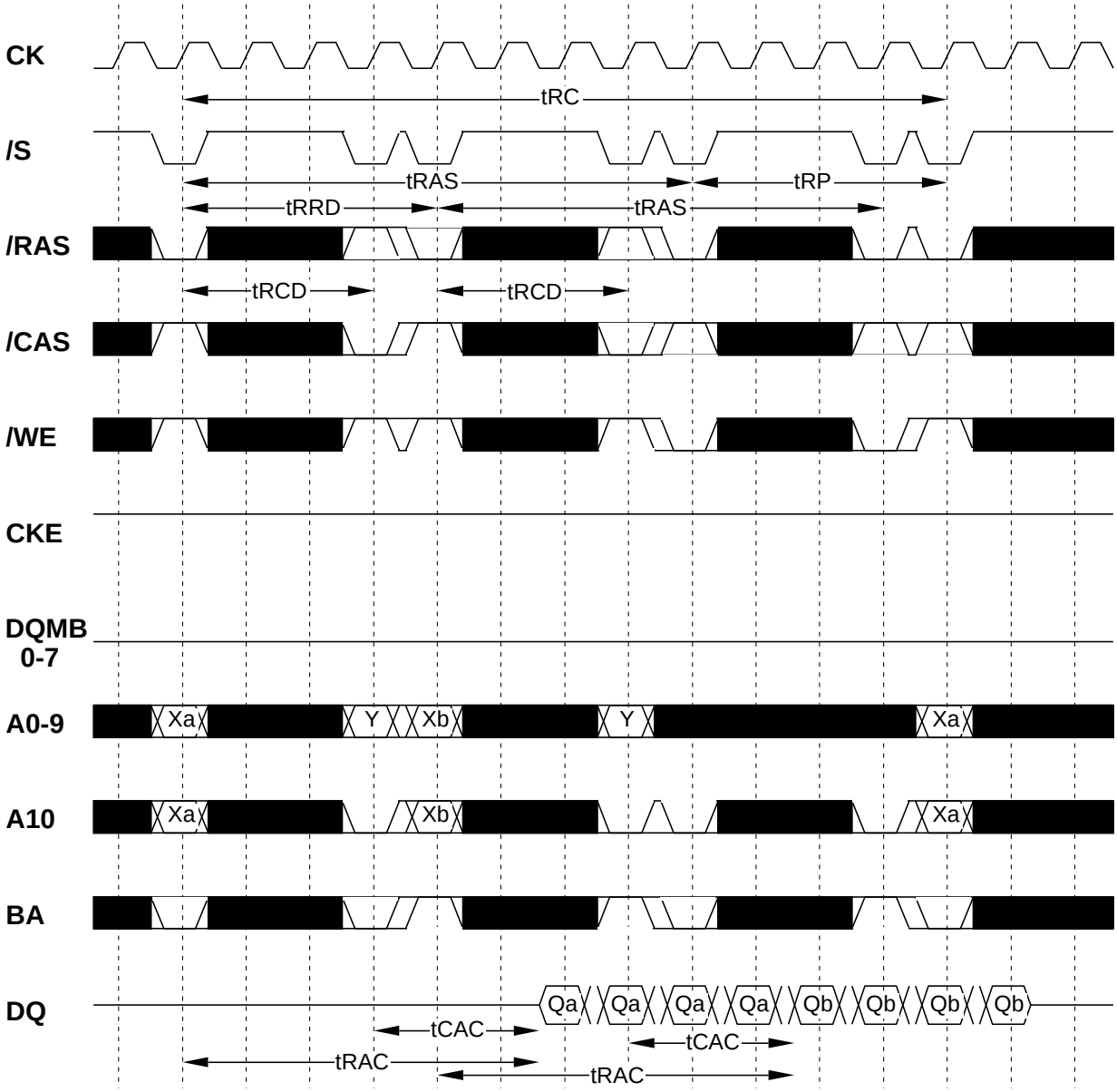
**WRITE CYCLE (dual bank)** BL=4



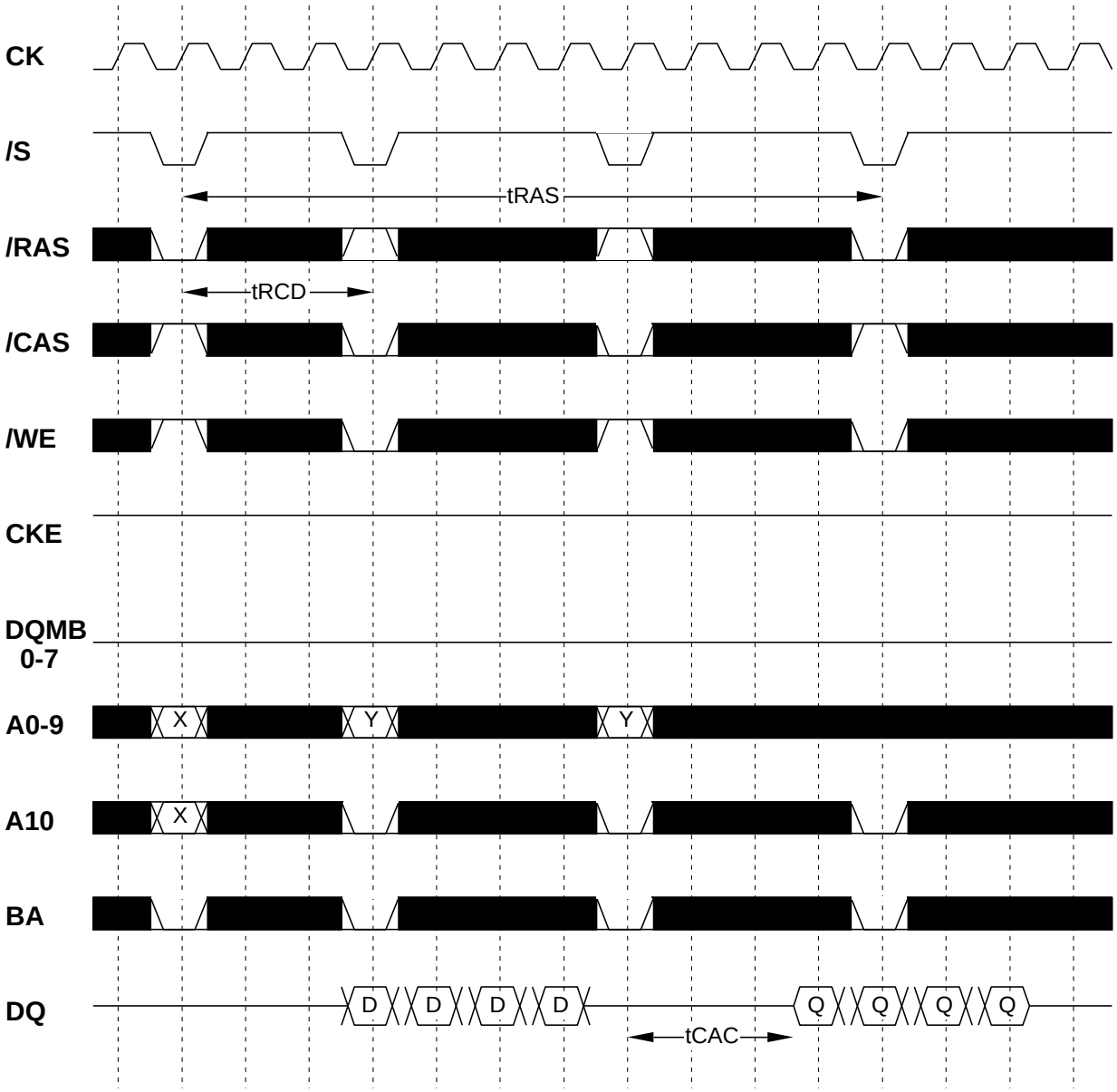
**READ CYCLE (single bank)** BL=4, CL=3



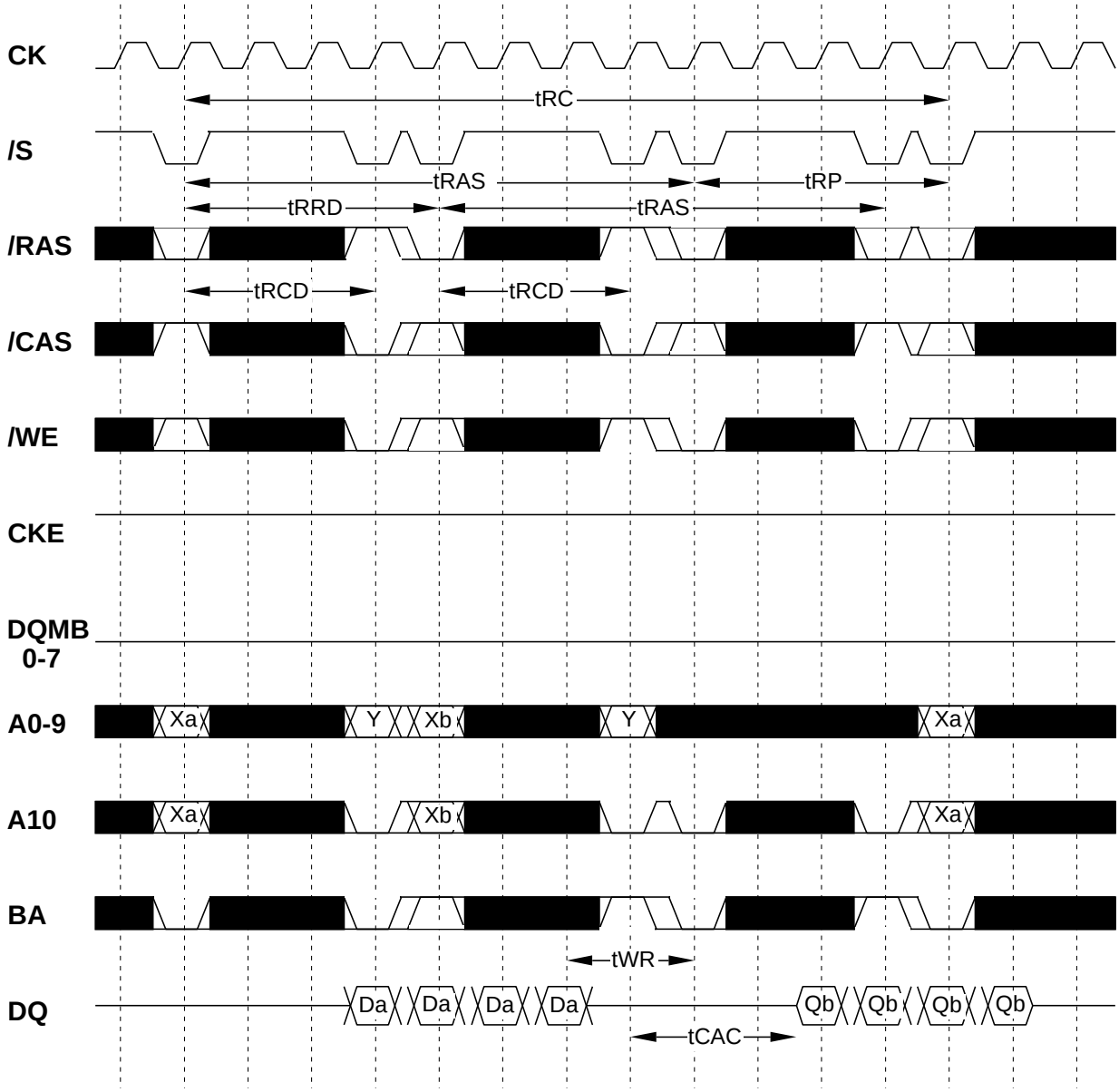
**READ CYCLE (dual bank)** BL=4, CL=3



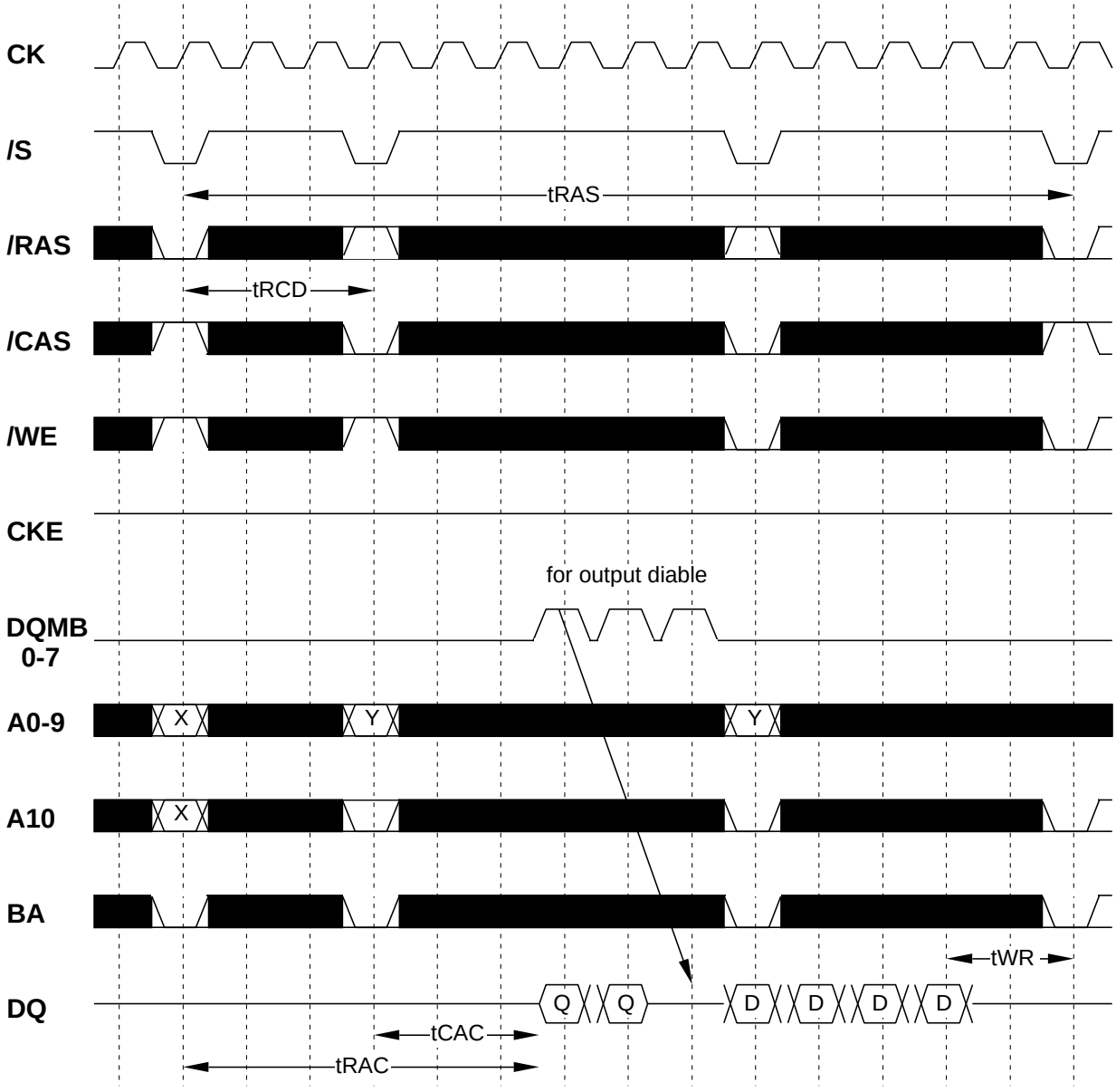
**WRITE to READ (single bank)** BL=4, CL=3



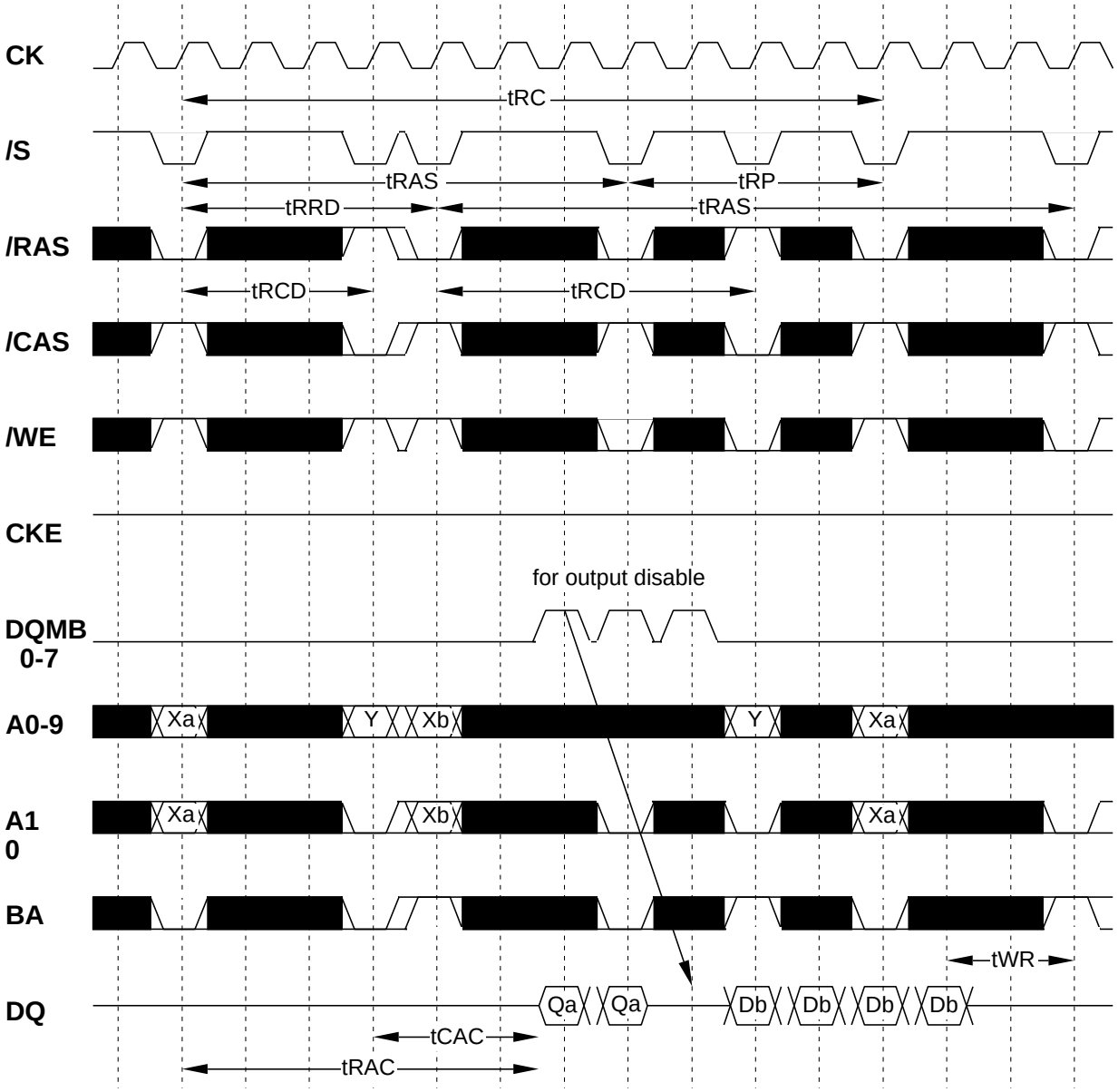
**WRITE to READ (dual bank)** BL=4, CL=3



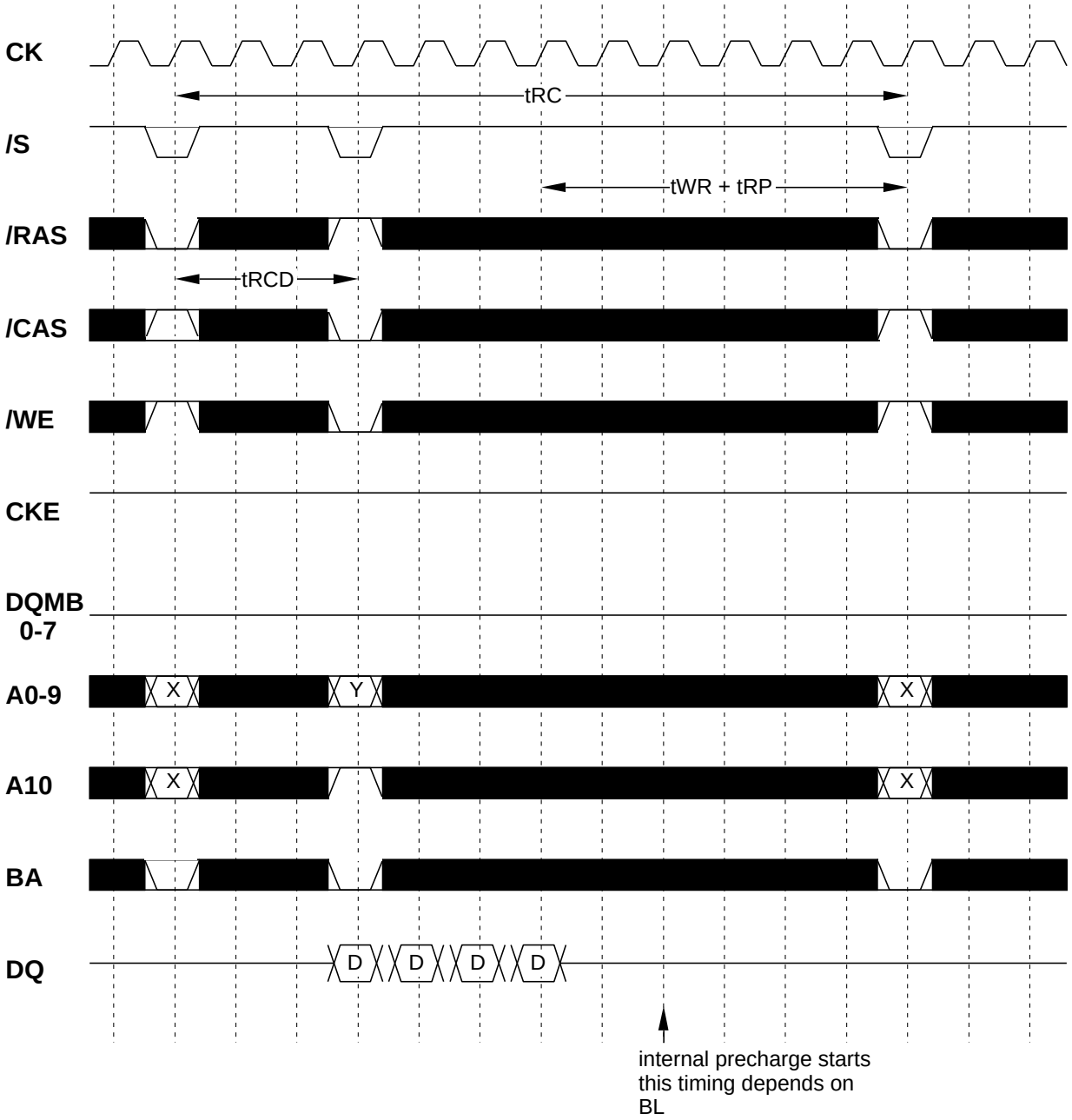
**READ to WRITE (single bank)** BL=4, CL=3



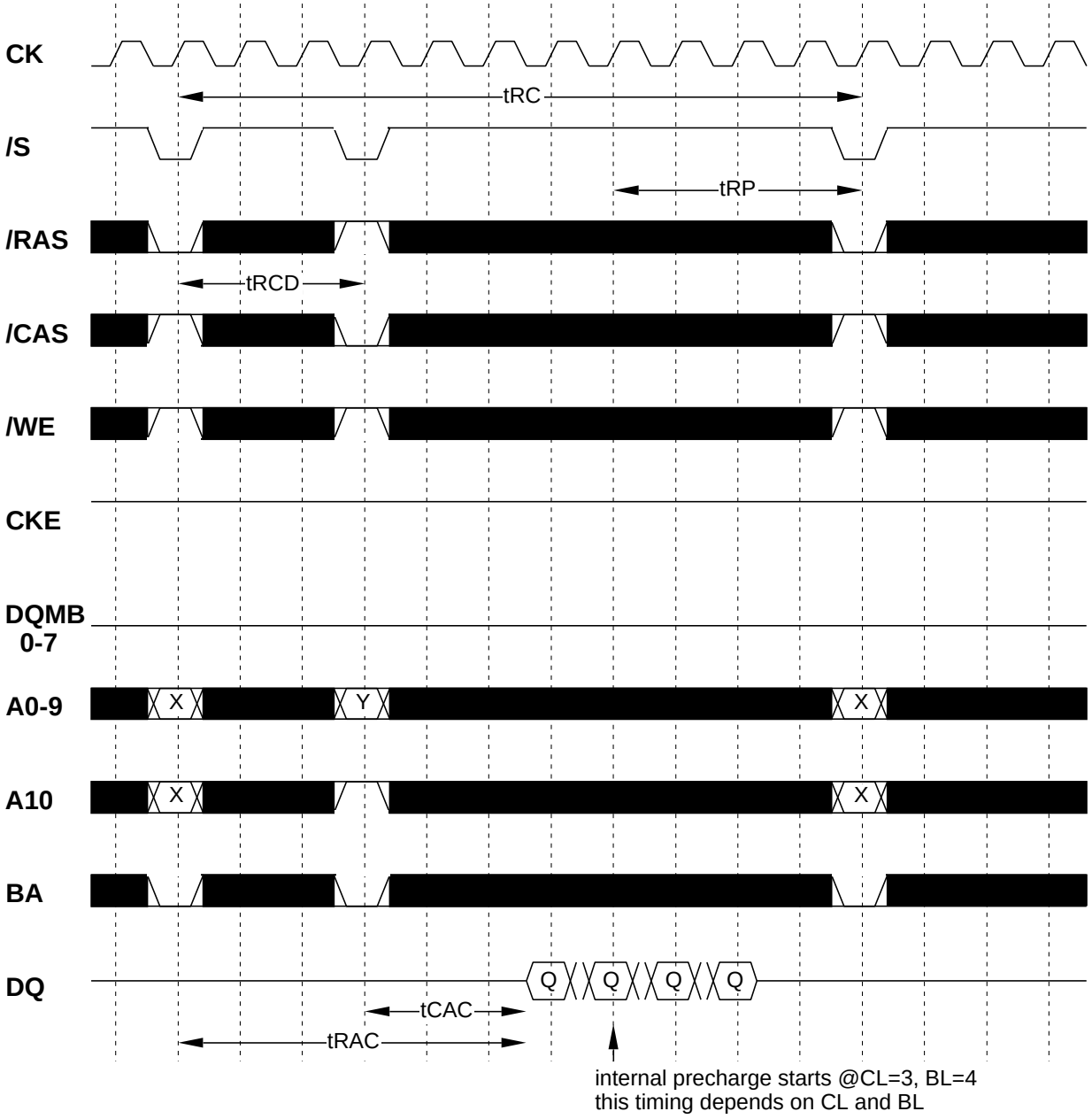
**READ to WRITE (dual bank)** BL=4, CL=3



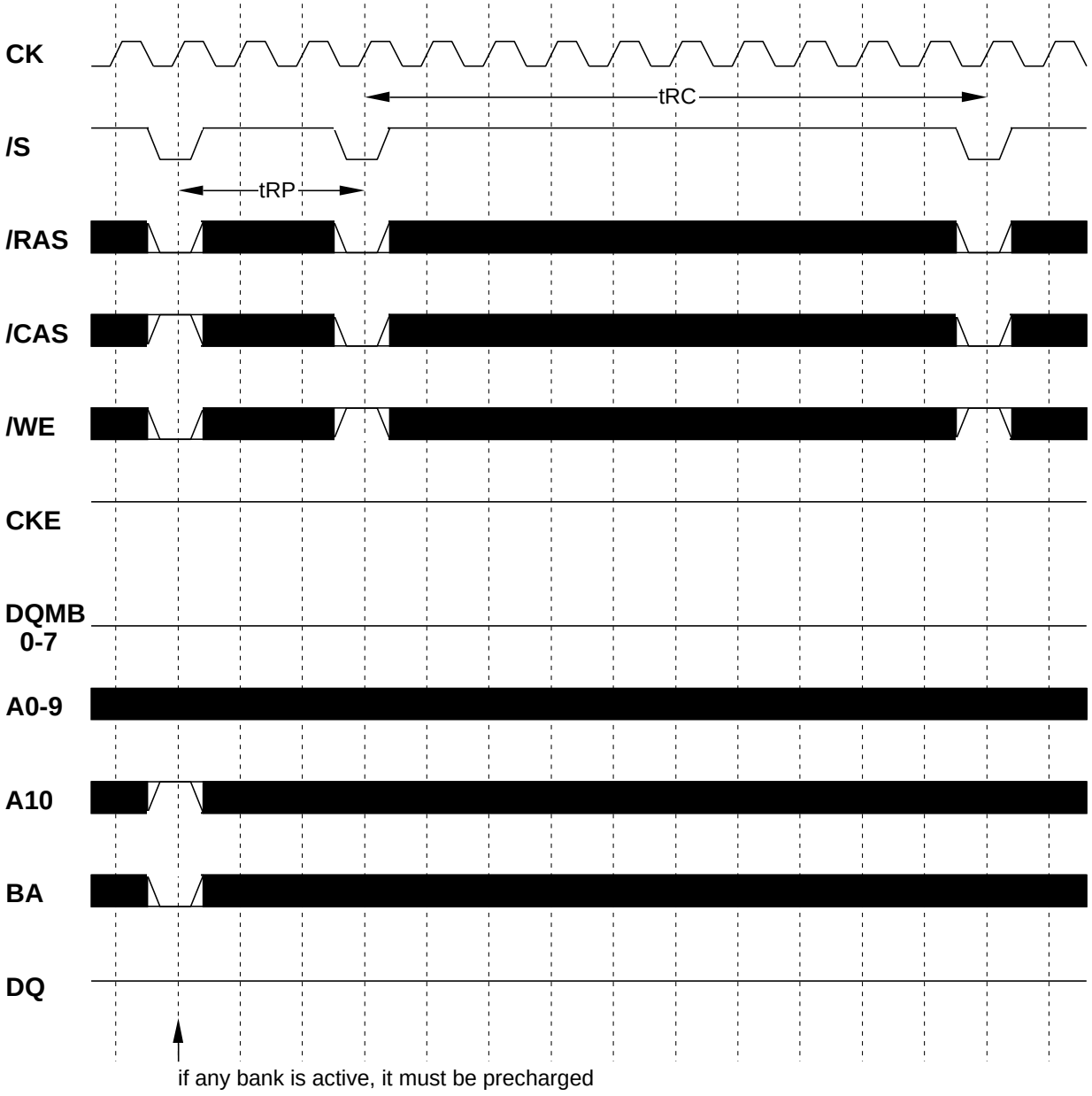
**WRITE with AUTO-PRECHARGE** BL=4



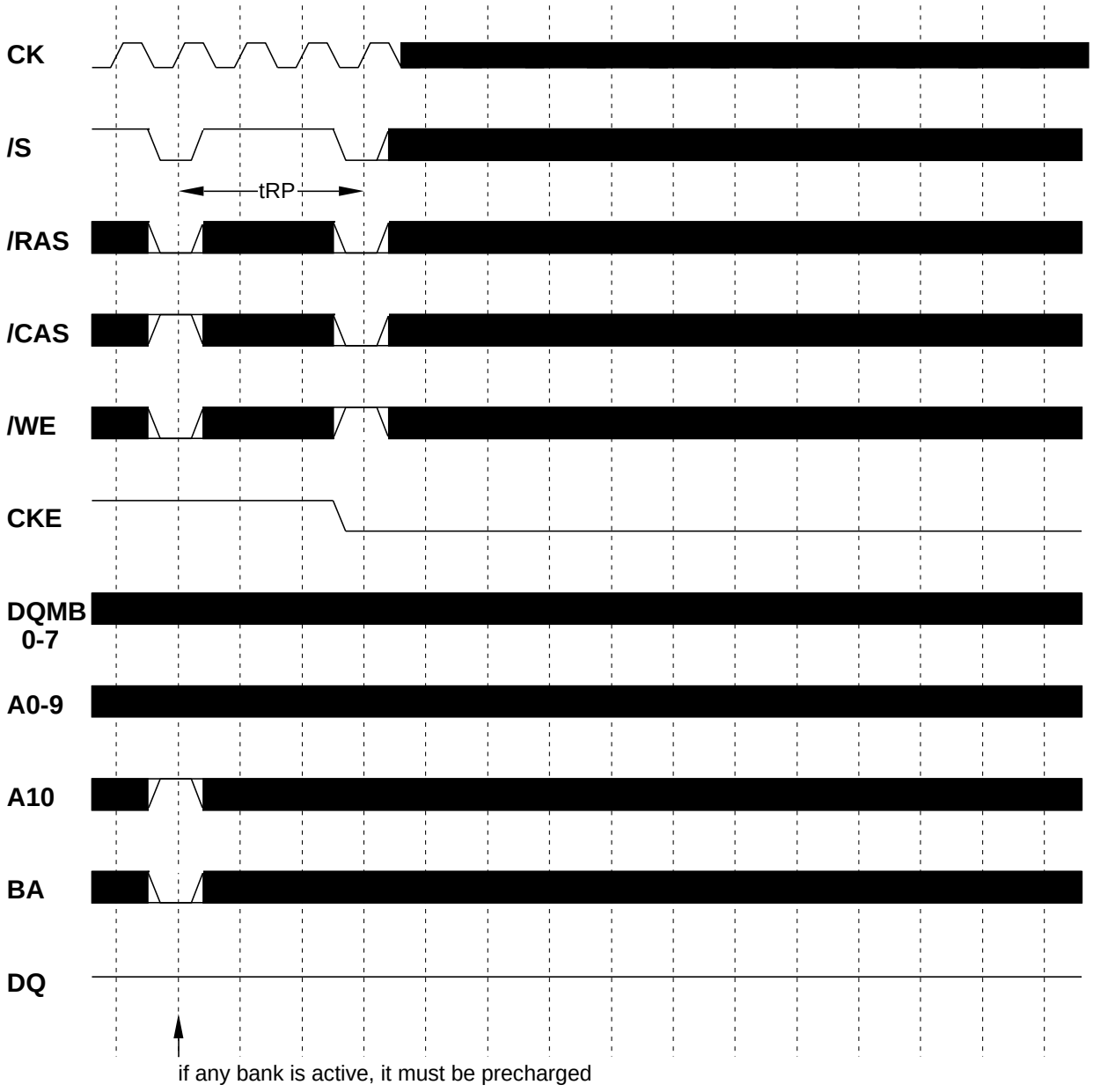
**READ with AUTO-PRECHARGE** BL=4, CL=3



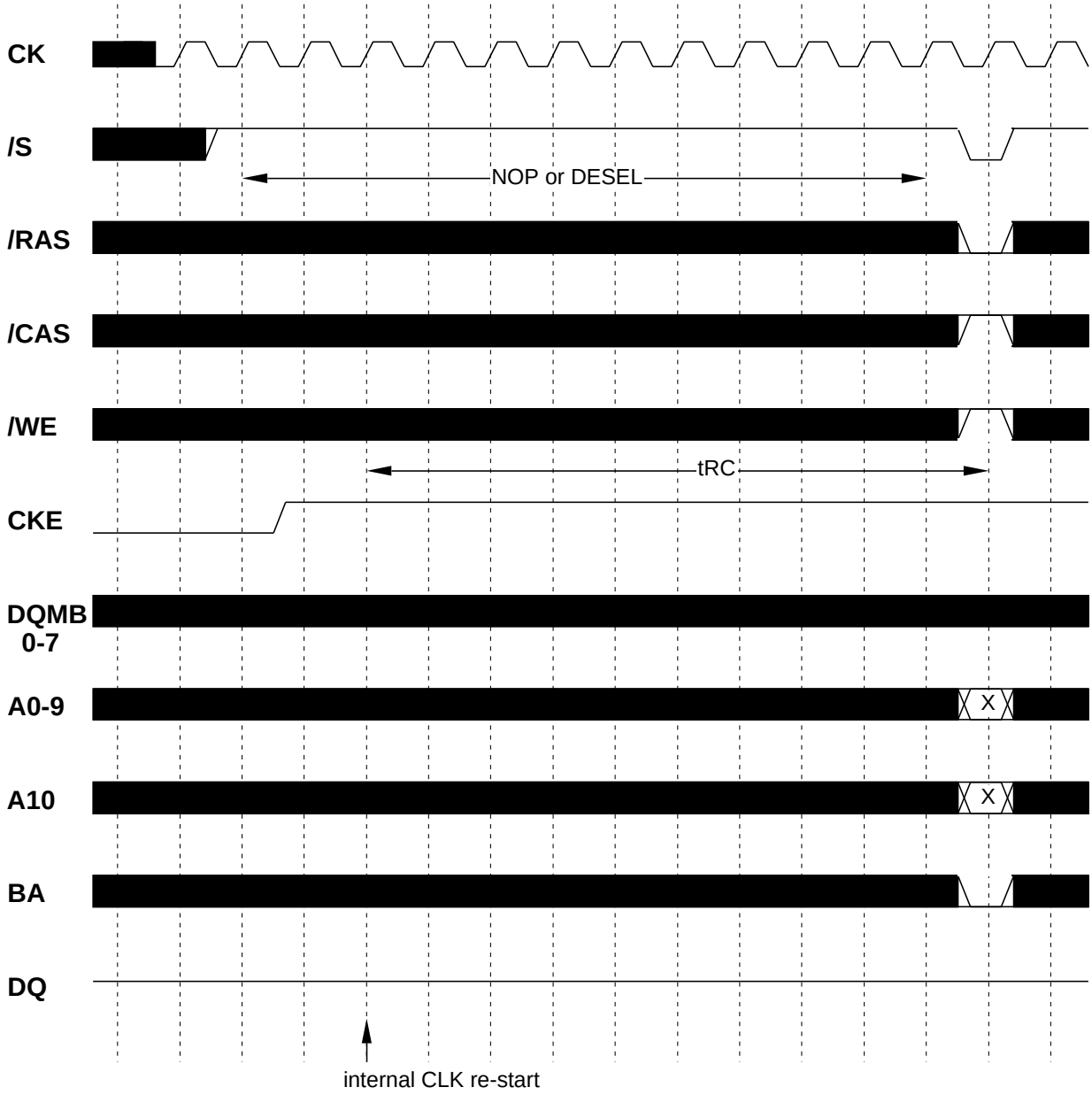
**AUTO-REFRESH**



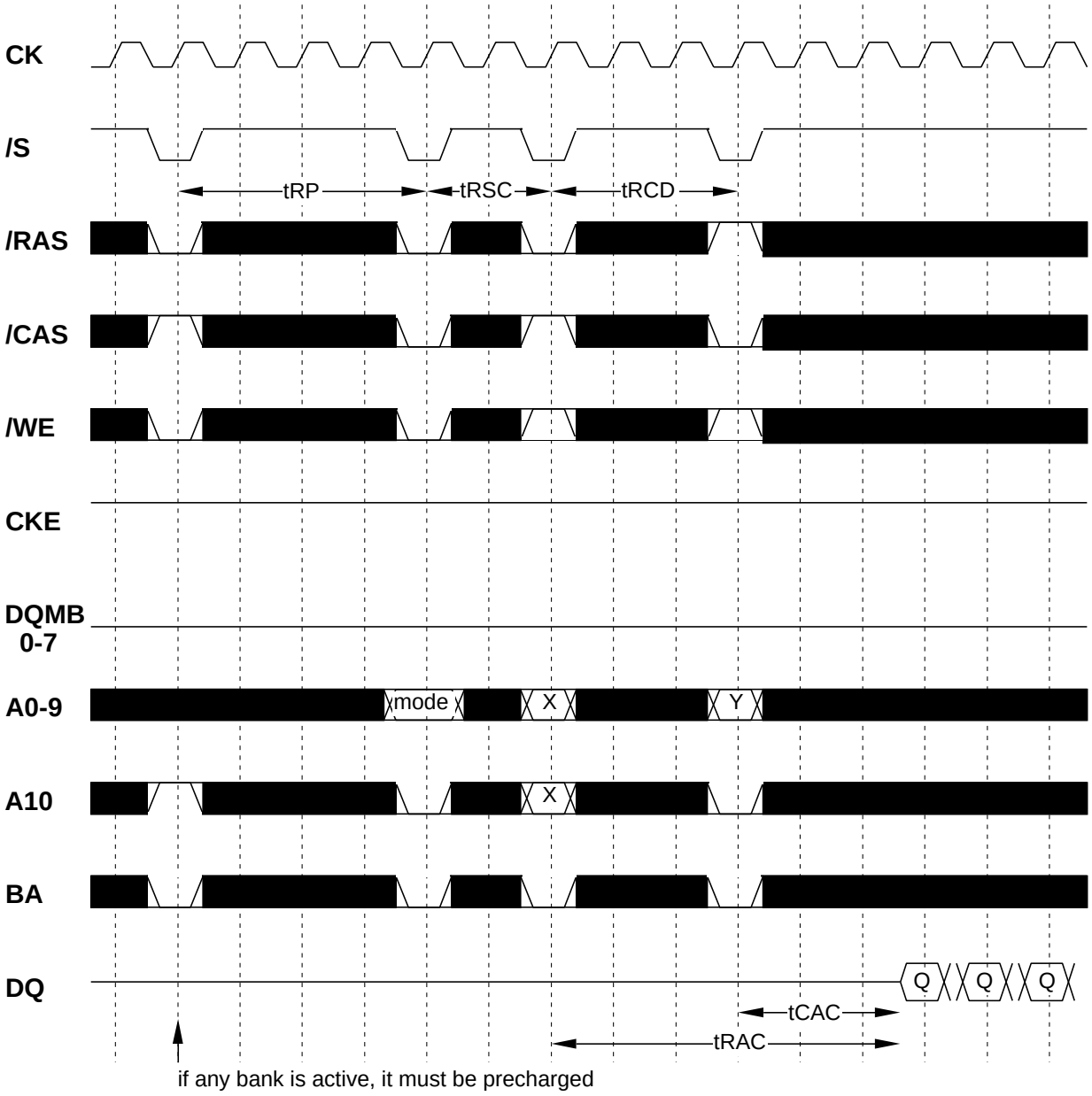
**SELF-REFRESH ENTRY**



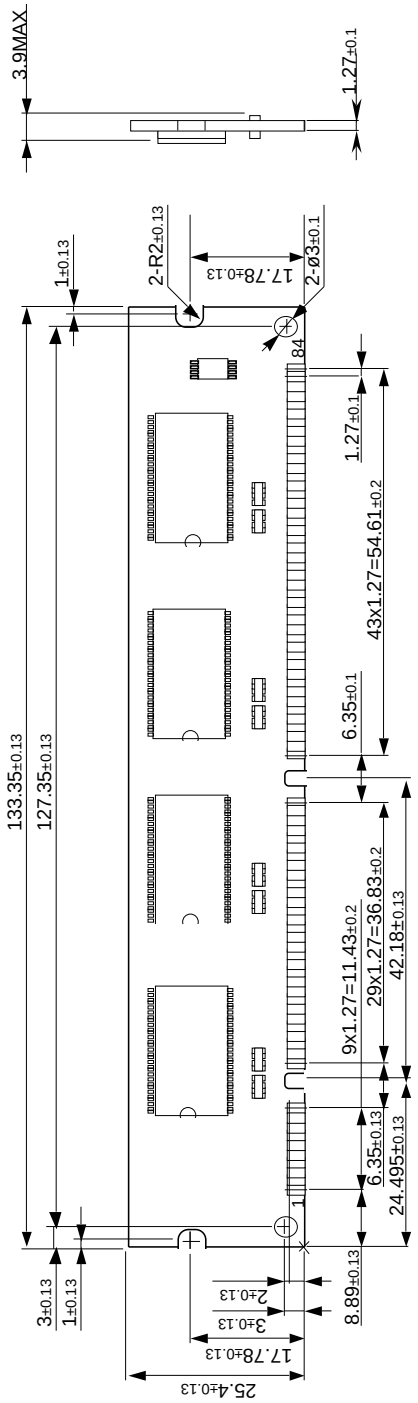
**SELF-REFRESH EXIT**



**MODE REGISTER SET** BL=4, CL=3



# Outline


3.9MAX
1.27±0.1
2-R2±0.13
17.78±0.13
2-ø3±0.1
1±0.13
84
1.27±0.1
43x1.27=54.61±0.2
6.35±0.1
133.35±0.13
127.35±0.13
9x1.27=11.43±0.2
29x1.27=36.83±0.2
42.18±0.13
6.35±0.13
24.495±0.13
1
3±0.13
1±0.13
2±0.13
3±0.13
8.89±0.13
17.78±0.13
25.4±0.13