

MH4M36CJD-5,-6,-7

FAST PAGE MODE (4194304-WORD BY 36-BIT) DYNAMIC RAM

DESCRIPTION

The MH4M36CJD is an 4M word by 36-bit dynamic RAM module and consists of 8 industry standard 4M X 4 dynamic RAMs in TSOP and 4 industry standard 4M X 1 dynamic RAMs in TSOP.

The ICs are mounted on both sides of small ceracom PC boards and form a convenient 64-pin WDIP package.

FEATURES

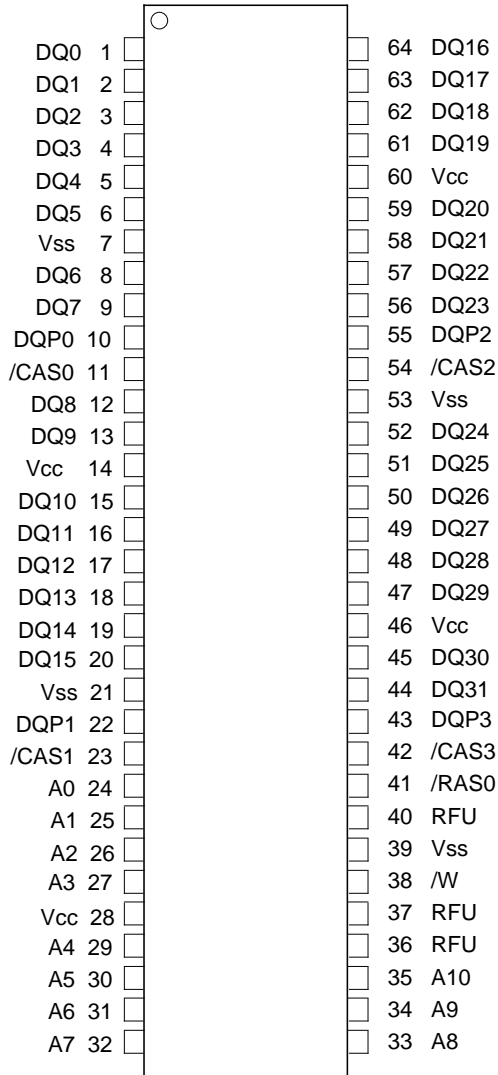
Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
MH4M36CJD-5	50	13	25	13	90	7240
MH4M36CJD-6	60	15	30	15	110	5920
MH4M36CJD-7	70	20	35	20	130	5200

- Utilizes industry standard 4M X 4 DRAMs in TSOP package and 4M X 1 DRAMs in TSOP package
- Single 5V ± 10% supply
- Low stand-by power dissipation
66mW (Max) CMOS Input level
- Low operating power dissipation
MH4M36CJD - 5 9.15W (Max)
MH4M36CJD - 6 7.48W (Max)
MH4M36CJD - 7 6.51W (Max)
- All inputs, output TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A₀ ~ A₁₀)
- Includes 12 0.22uF decoupling capacitors

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



MH4M36CJD-5,-6,-7

FAST PAGE MODE (4194304-WORD BY 36-BIT) DYNAMIC RAM

FUNCTION

The MH4M36CJD provide, in addition to normal read and write a number of other functions,

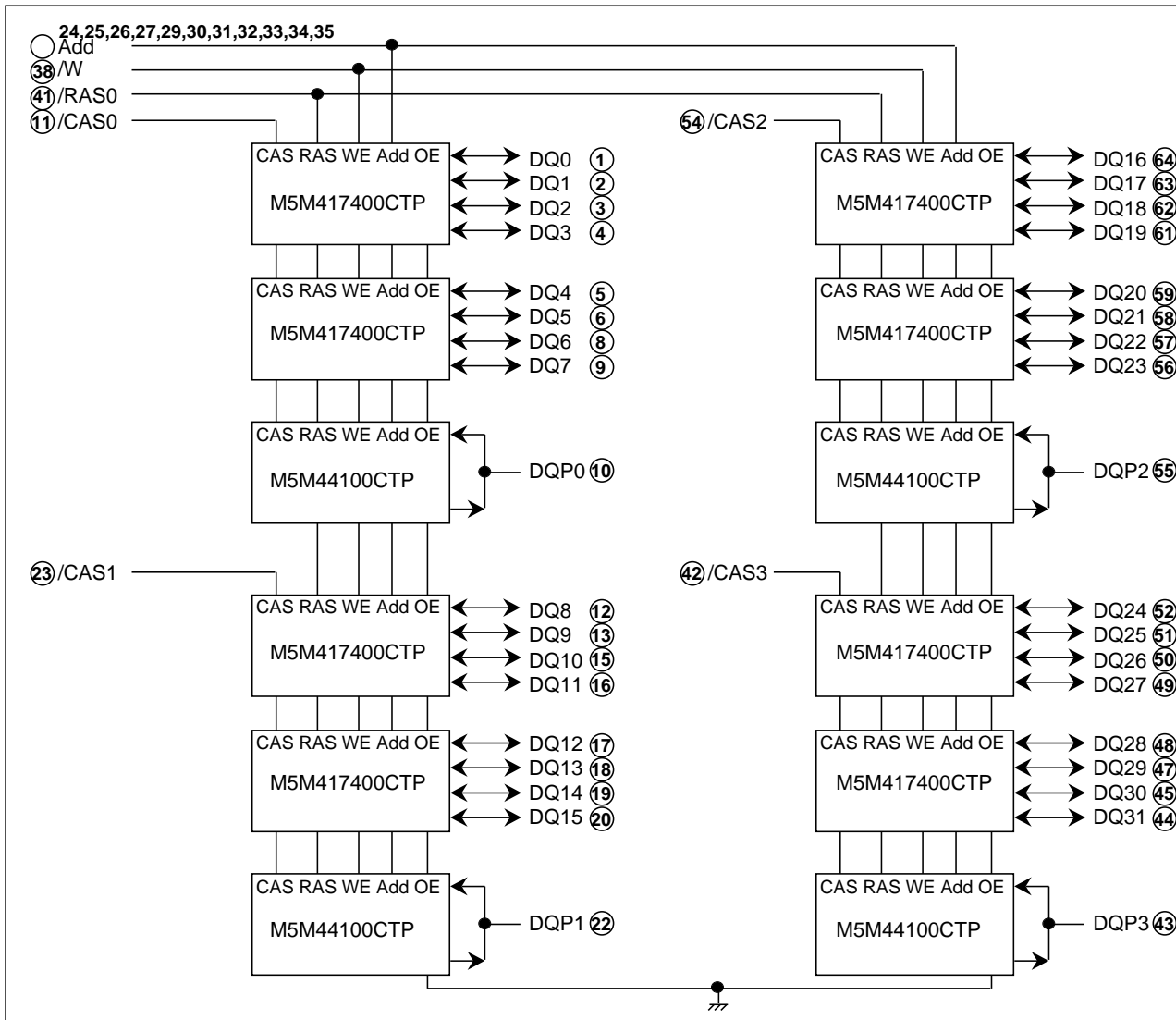
e.g., fast page mode, $\overline{\text{RAS}}$ -only refresh.
The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	APD	OPN	YES	
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



MH4M36CJD-5,-6,-7

FAST PAGE MODE (4194304-WORD BY 36-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1 ~ 7	V
VI	Input voltage		-1 ~ 7	V
VO	Output voltage		-1 ~ 7	V
IO	Output current		50	mA
Pd	Power dissipation	Ta=25°C	12	W
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-40 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0 ~ 70 °C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5	5.5	V
Vss	Supply voltage	0	0	0	V
VIH	High-level input voltage, all inputs	2.4		6.0	V
VIL	Low-level input voltage, all inputs	-1.0		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
VOH	High-level output voltage	IOH=-5mA	2.4		Vcc	V
VOL	Low-level output voltage	IOL=4.2mA	0		0.4	V
IOZ	Off-state output current	Q floating 0V Vout 5.5V	-10		10	uA
II	Input current	0V VIH 6.0V, Other inputs pins=0V	-120		120	uA
Icc1 (AV)	Average supply current from Vcc operating (Note 3,4)	MH4M36CJD-5	RAS, CAS cycling trc=twc=min. output open		1660	mA
		MH4M36CJD-6			1360	
		MH4M36CJD-7			1180	
Icc2	Supply current from Vcc, stand-by	RAS= CAS =VIH, output open			24	mA
		RAS= CAS Vcc-0.5			12	
Icc3 (AV)	Average supply current from Vcc refreshing (Note 3)	MH4M36CJD-5	RAS cycling, CAS= VIH trc=min. output open		1660	mA
		MH4M36CJD-6			1360	
		MH4M36CJD-7			1180	
Icc4(AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4)	MH4M36CJD-5	RAS=VIL, CAS cycling trc=min. output open		1060	mA
		MH4M36CJD-6			900	
		MH4M36CJD-7			780	
Icc6(AV)	Average supply current from Vcc CAS before RAS refresh mode (Note 3)	MH4M36CJD-5	CAS before RAS refresh cycling trc=min. output open		1580	mA
		MH4M36CJD-6			1300	
		MH4M36CJD-7			1140	

Note 2: Current flowing into an IC is positive, out is negative.

3: Icc1 (AV), Icc3 (AV), Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0 ~ 70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CI(A)	Input capacitance, address inputs	VI=Vss f=1MHz VI=25mVrms			90	pF
CI(W)	Input capacitance, write control input				130	pF
CI(RAS)	Input capacitance, RAS input				130	pF
CI(CAS)	Input capacitance, CAS input				35	pF
CI/O	Input/Output capacitance, data ports				20	pF

MH4M36CJD-5,-6,-7

FAST PAGE MODE (4194304-WORD BY 36-BIT) DYNAMIC RAM

SWITCHING CHARACTERISTICS (Ta=0 ~ 70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted , see notes 5,12,13)

Symbol	Parameter	Limits						Unit
		MH4M36CJD-5		MH4M36CJD-6		MH4M36CJD-7		
		Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{\text{CAS}}$ (Note 6,7)		13		15		20	ns
tRAC	Access time from $\overline{\text{RAS}}$ (Note 6,8)		50		60		70	ns
tAA	Column address access time (Note 6,9)		25		30		35	ns
tCPA	Access time from $\overline{\text{CAS}}$ precharge (Note 6,10)		30		35		40	ns
tCLZ	Output low impedance time from $\overline{\text{CAS}}$ low (Note 6)	5		5		5		ns
tOFF	Output disable time after $\overline{\text{CAS}}$ high (Note 11)	0	13	0	15	0	15	ns

- Note 5: An initial pause of 500us is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh).
 Note the $\overline{\text{RAS}}$ may be cycled during the initial pause . And any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles are required after prolonged periods (greater than 32 ms) of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.
- 6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
- 7: Assumes that tRCD = tRCD(max) and tASC = tASC(max).
- 8: Assumes that tRCD = tRCD(max) and tRAD = tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.
- 9: Assumes that tRAD = tRAD(max) and tASC = tASC(max).
- 10: Assumes that tCP = tCP(max) and tASC = tASC(max).
- 11: tOFF(max) and tOEZ (max) defines the time at which the output achieves the high impedance state (| IOUT | 10 uA) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Write,Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~ 70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted See notes 12,13)

Symbol	Parameter	Limits						Unit
		MH4M36CJD-5		MH4M36CJD-6		MH4M36CJD-7		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		32		32		32	ms
tRP	$\overline{\text{RAS}}$ high pulse width	30		40		50		ns
tRCD	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (Note14)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	10		10		10		ns
tRPC	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low	0		0		0		ns
tCPN	$\overline{\text{CAS}}$ high pulse width	10		10		10		ns
tRAD	Column address delay time from $\overline{\text{RAS}}$ low (Note15)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{\text{RAS}}$ low	0		0		0		ns
tASC	Column address setup time before $\overline{\text{CAS}}$ low (Note16)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{\text{RAS}}$ low	8		10		10		ns
tCAH	Column address hold time after $\overline{\text{CAS}}$ low	13		15		15		ns
tdZC	Delay time, data to $\overline{\text{CAS}}$ low (Note17)	0		0		0		ns
tCDD	Delay time, $\overline{\text{CAS}}$ high to data (Note18)	13		15		15		ns
tT	Transition time (Note19)	1	50	1	50	1	50	ns

- Note 12: The timing requirements are assumed tT =5ns.
- 13: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
- 14: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) =tRAH(min) +2tH+tASC(min).
- 15: tRAD(max) is specified as a reference point only. If tRAD = tRAD(max) and tASC = tASC(max), access time is controlled exclusively by tAA.
- 16: tASC(max) is specified as a reference point only. If tRCD = tRCD(max) and tASC = tASC(max), access time is controlled exclusively by tCAC.
- 17: Either tDZC or tDZO must be satisfied.
- 18: Either tCDD or tODD must be satisfied.
- 19: tT is measured between VIH(min) and VIL(max).

MH4M36CJD-5,-6,-7

FAST PAGE MODE (4194304-WORD BY 36-BIT) DYNAMIC RAM

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		MH4M36CJD-5		MH4M36CJD-6		MH4M36CJD-7		
		Min	Max	Min	Max	Min	Max	
trc	Read cycle time	90		110		130		ns
trAS	RAS iow pulse width	50	10000	60	10000	70	10000	ns
tcAS	CAS iow pulse width	13	10000	15	10000	20	10000	ns
tCSH	CAS hold time after RAS iow	50		60		70		ns
trSH	RAS hold time after CAS iow	13		15		20		ns
trCS	Read Setup time after CAS high	0		0		0		ns
trCH	Read hold time after CAS iow (Note 20)	0		0		0		ns
trRH	Read hold time after RAS iow (Note 20)	10		10		10		ns
trAL	Column address to RAS hold time	25		30		35		ns

Note 20: Either trCH or trRH must be satisfied for a read cycle.

Write Cycle

Symbol	Parameter	Limits						Unit
		MH4M36CJD-5		MH4M36CJD-6		MH4M36CJD-7		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
trAS	RAS iow pulse width	50	10000	60	10000	70	10000	ns
tcAS	CAS iow pulse width	13	10000	15	10000	20	10000	ns
tCSH	CAS hold time after RAS iow	50		60		70		ns
trSH	RAS hold time after CAS iow	13		15		20		ns
twCS	Write setup time before CAS iow	0		0		0		ns
twCH	Write hold time after CAS iow	8		10		15		ns
tcWL	CAS hold time after W iow	13		15		20		ns
trWL	RAS hold time after W iow	13		15		20		ns
tWP	Write pulse width	8		10		15		ns
tDS	Data setup time before CAS iow or W iow	0		0		0		ns
tDH	Data hold time after CAS iow or W iow	8		10		15		ns

MH4M36CJD-5,-6,-7

FAST PAGE MODE (4194304-WORD BY 36-BIT) DYNAMIC RAM

Fast-Page Mode Cycle (Read, Early Write Cycle) (Note 21)

Symbol	Parameter	Limits						Unit
		MH4M36CJD-5		MH4M36CJD-6		MH4M36CJD-7		
		Min	Max	Min	Max	Min	Max	
t _{PC}	Fast page mode read/write cycle time	40		45		50		ns
t _{RAS}	RAS low pulse width for read write cycle (Note22)	95	125000	110	125000	125	125000	ns
t _{CP}	CAS high pulse width (Note23)	8	12	10	15	10	15	ns
t _{CPRH}	RAS hold time after CAS precharge	35		40		45		ns
t _{CPWD}	Delay time, CAS precharge to W low	53		60		65		ns

Note 21: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

22: t_{RAS(min)} is specified as two cycles of CAS input are performed.

23: t_{CP(max)} is specified as a reference point only.

CAS before RAS Refresh Cycle (Note 24)

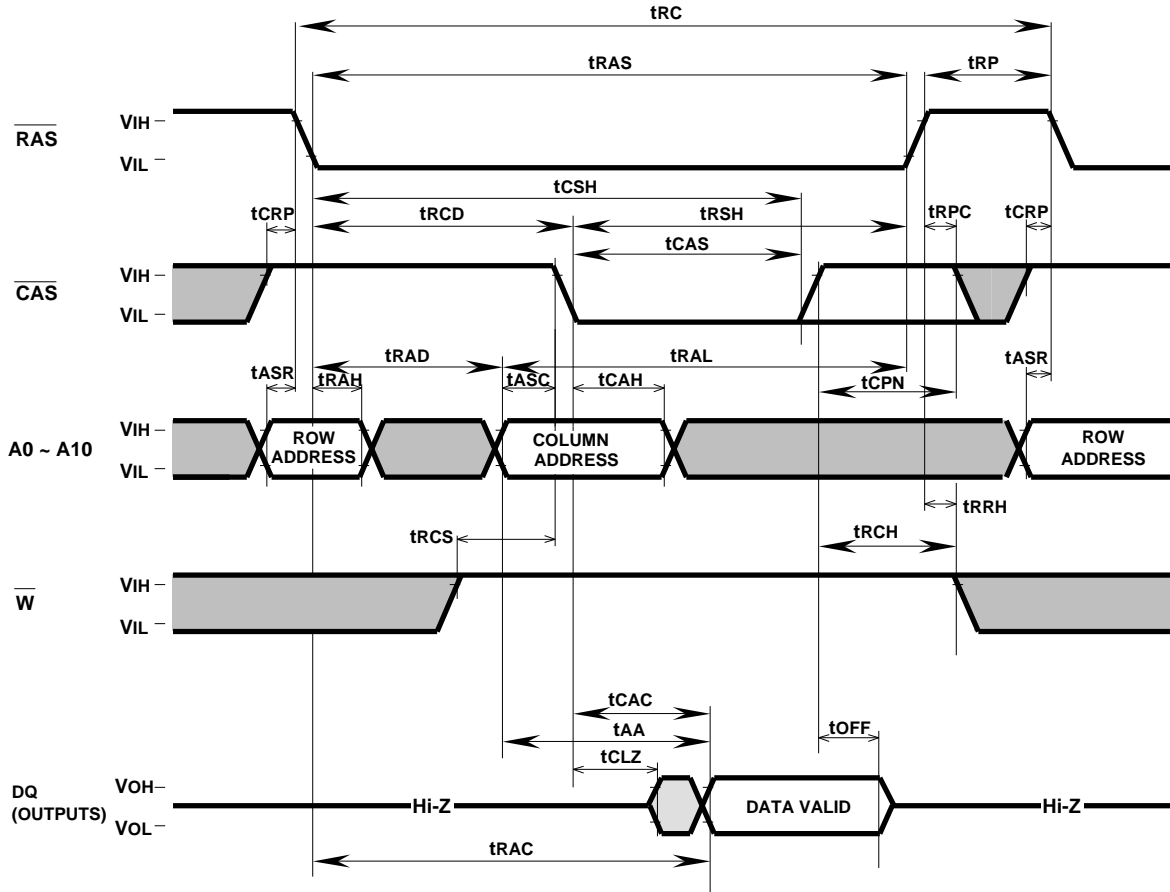
Symbol	Parameter	Limits						Unit
		MH4M36CJD-5		MH4M36CJD-6		MH4M36CJD-7		
		Min	Max	Min	Max	Min	Max	
t _{CSR}	CAS setup time before RAS low	10		10		10		ns
t _{CHR}	CAS hold time after RAS low	10		10		15		ns
t _{RSR}	Read setup time before RAS low	10		10		10		ns
t _{RHR}	Read hold time after RAS low	10		10		15		ns

Note 24: Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

MH4M36CJD-5,-6,-7

FAST PAGE MODE (4194304-WORD BY 36-BIT) DYNAMIC RAM

Timing Diagrams (Note 25) Read Cycle



Note 25

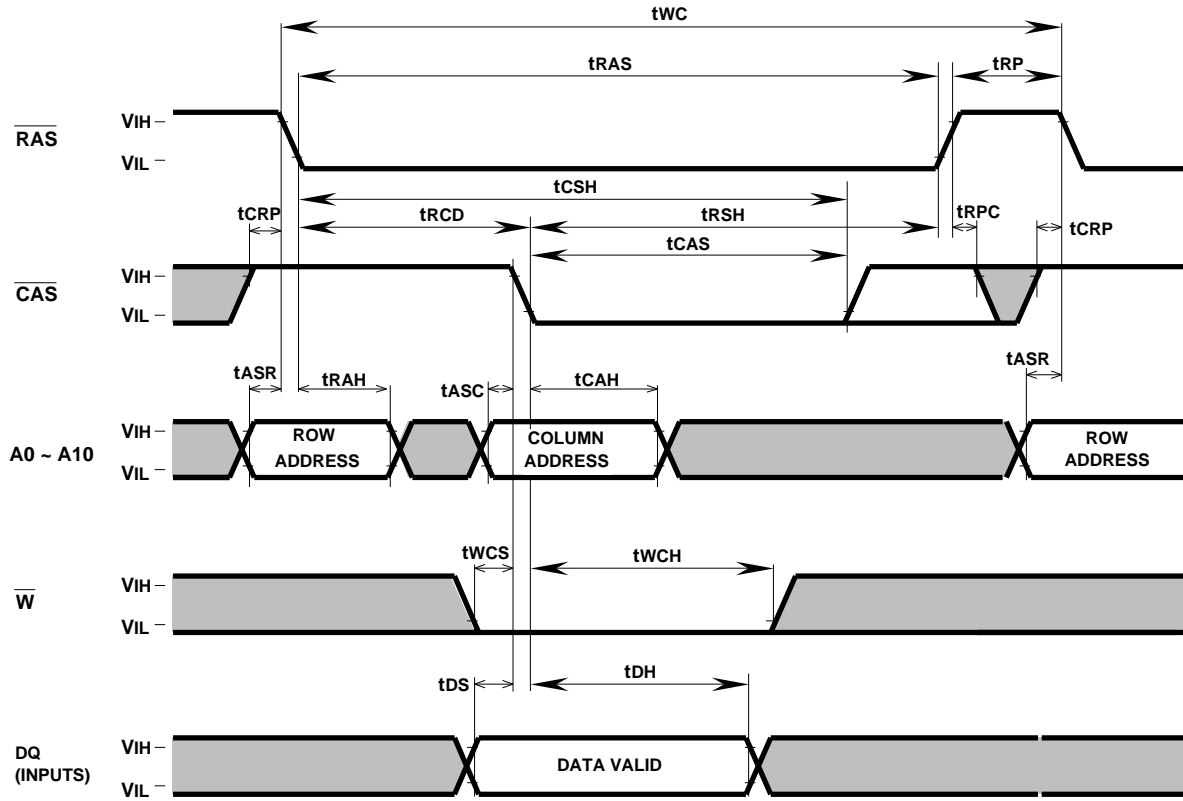
Indicates the don't care input.
 $V_{IH}(\min)$ V_{IN} $V_{IH}(\max)$ or $V_{IL}(\min)$ V_{IN} $V_{IL}(\max)$

Indicates the invalid output.

MH4M36CJD-5,-6,-7

FAST PAGE MODE (4194304-WORD BY 36-BIT) DYNAMIC RAM

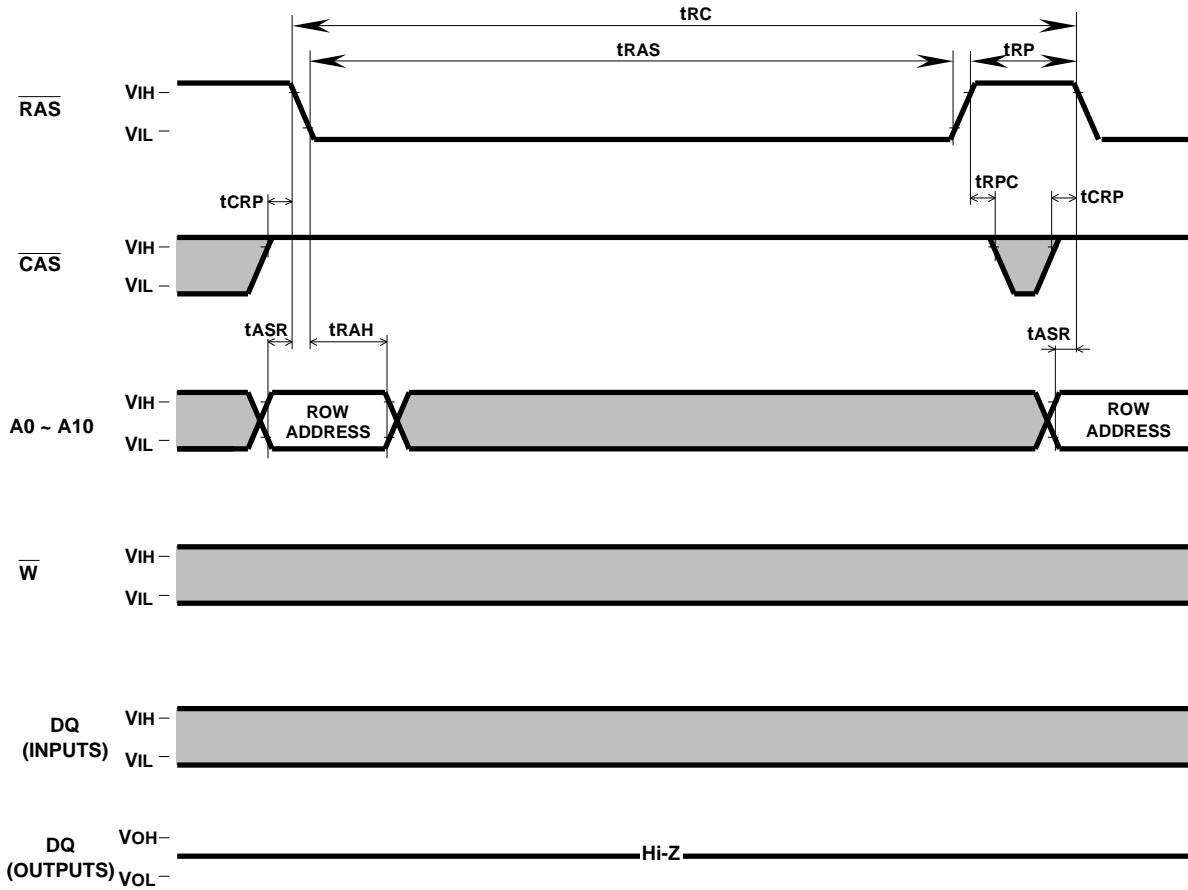
Write Cycle (Early write)



MH4M36CJD-5,-6,-7

FAST PAGE MODE (4194304-WORD BY 36-BIT) DYNAMIC RAM

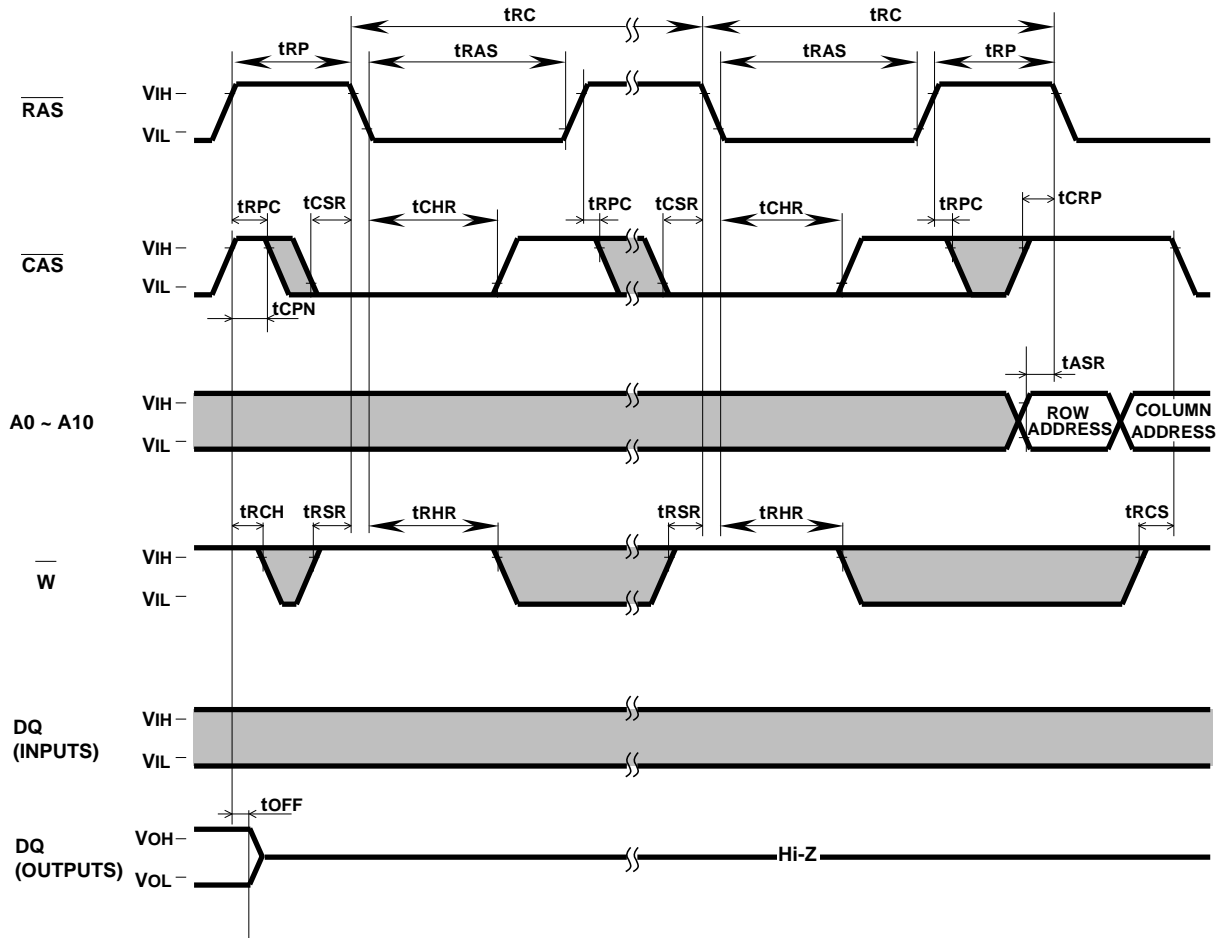
RAS-only Refresh Cycle



MH4M36CJD-5,-6,-7

FAST PAGE MODE (4194304-WORD BY 36-BIT) DYNAMIC RAM

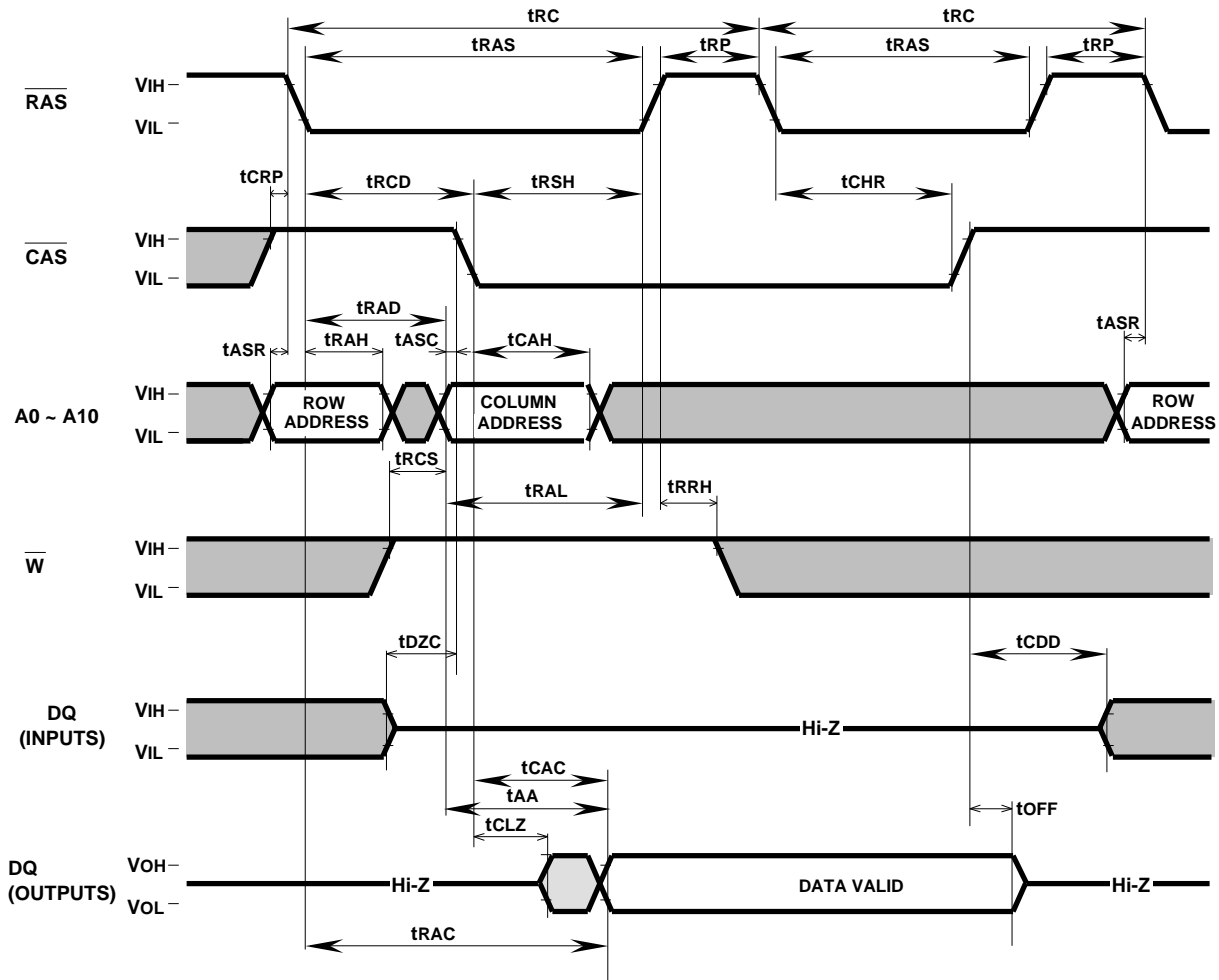
CAS before RAS Refresh Cycle



MH4M36CJD-5,-6,-7

FAST PAGE MODE (4194304-WORD BY 36-BIT) DYNAMIC RAM

Hidden Refresh Cycle (Read) (Note 26)

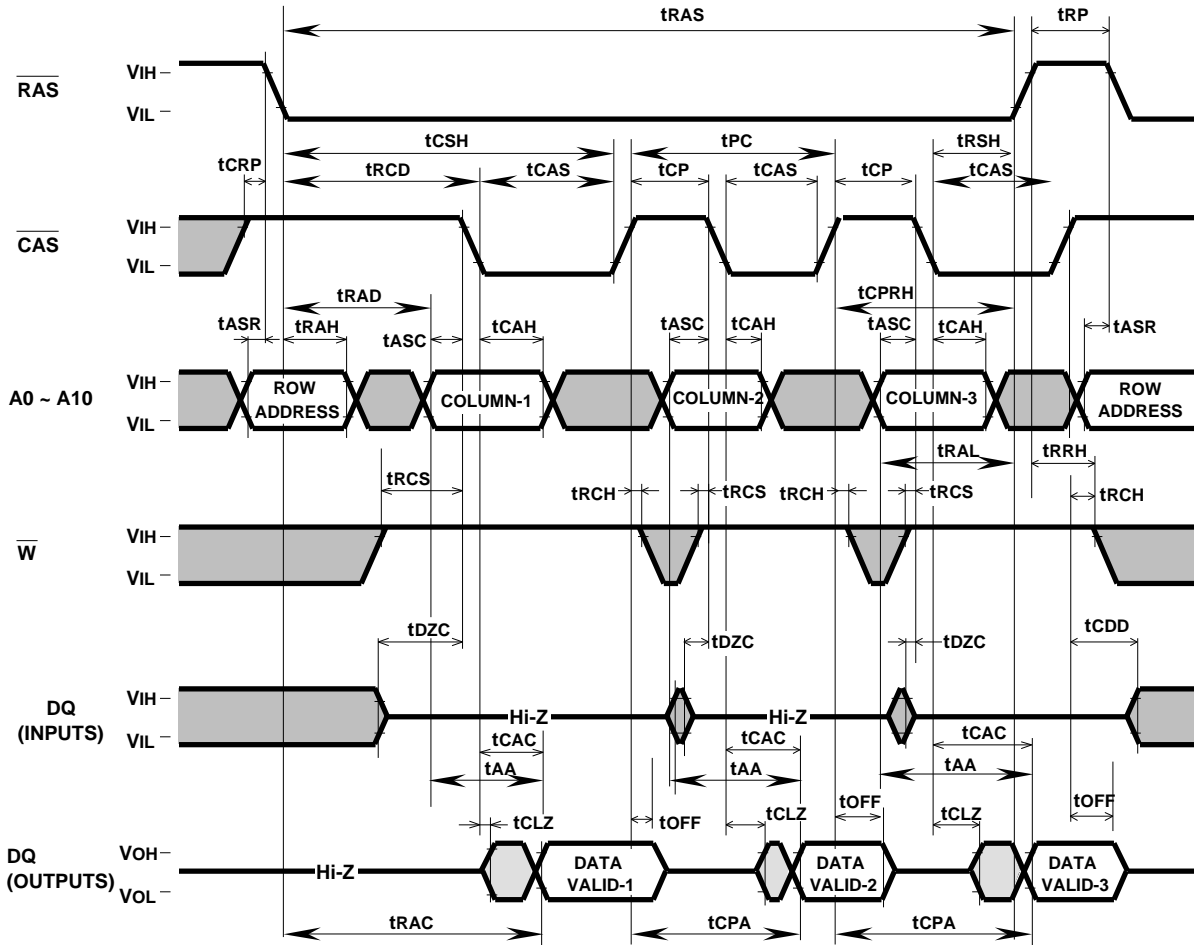


Note 26: Early write cycle is applicable instead of read cycle.
 Timing requirements and output state are the same as that of each cycle shown above.

MH4M36CJD-5,-6,-7

FAST PAGE MODE (4194304-WORD BY 36-BIT) DYNAMIC RAM

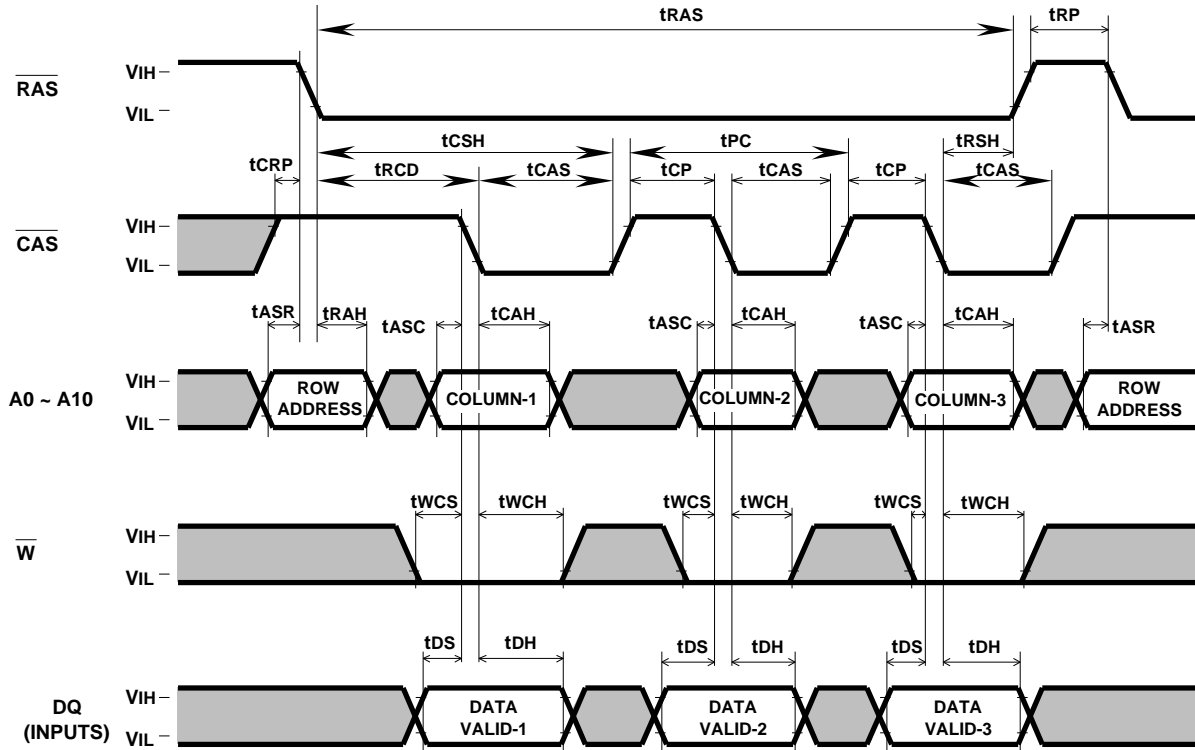
Fast Page Mode Read Cycle



MH4M36CJD-5,-6,-7

FAST PAGE MODE (4194304-WORD BY 36-BIT) DYNAMIC RAM

Fast Page Mode Write Cycle (Early Write)



MH4M36CJD-5,-6,-7

FAST PAGE MODE (4194304-WORD BY 36-BIT) DYNAMIC RAM

