2001.July   Rev.0.2
Advanced Information
Notice: This is not final specification.
Some parametric limits are subject to change.

MITSUBISHI LSIs
M5M5T5636UG – 25,22,20
18874368-BIT(524288-WORD BY 36-BIT) NETWORK SRAM

DESCRIPTION

The M5M5T5636UG is a family of 18M bit synchronous SRAMs organized as 524288-words by 36-bit. It is designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Mitsubishi's SRAMs are fabricated with high performance, low power CMOS technology, providing greater reliability. M5M5T5636UG operates on 2.5V power/ 1.8V I/O supply or a single 2.5V power supply and are 2.5V CMOS compatible.

FEATURES

• **Fully registered inputs and outputs for pipelined operation**
• **Fast clock speed: 250, 225, and 200 MHz**
• **Fast access time: 2.6, 2.8, 3.2 ns**
• **Single 2.5V -5% and +5% power supply V_{DD}**
• **Separate V_{DDQ} for 2.5V or 1.8V I/O**
• **Individual byte write (BWa# - BWd#) controls may be tied LOW**
• **Single Read/Write control pin (W#)**
• **CKE# pin to enable clock and suspend operations**
• **Internally self-timed, registers outputs eliminate the need to control G#**
• **Snooze mode (ZZ) for power down**
• **Linear or Interleaved Burst Modes**
• **Three chip enables for simple depth expansion**
• **JTAG boundary scan support**

Package

    165(11x15) bump BGA
    Body Size (13mm x 15mm)
    Bump Pitch 1.0mm

PART NAME TABLE

Part Name	Frequency	Access	Cycle	Active Current (max.)	Standby Current (max.)
M5M5T5636UG - 25	250MHz	2.6ns	4.0ns	400mA	20mA
M5M5T5636UG - 22	225MHz	2.8ns	4.4ns	380mA	20mA
M5M5T5636UG - 20	200MHz	3.2ns	5.0ns	360mA	20mA

APPLICATION

High-end networking products that require high bandwidth, such as switches and routers.

FUNCTION

   Synchronous circuitry allows for precise cycle control triggered by a positive edge clock transition.
   Synchronous signals include : all Addresses, all Data Inputs, all Chip Enables (E1#, E2, E3#), Address Advance/Load (ADV), Clock Enable (CKE#), Byte Write Enables (BWa#, BWb#, BWc#, BWd#) and Read/Write (W#). Write operations are controlled by the four Byte Write Enables (BWa# - BWd#) and Read/Write(W#) inputs. All writes are conducted with on-chip synchronous self-timed write circuitry.
   Asynchronous inputs include Output Enable (G#), Clock (CLK) and Snooze Enable (ZZ). The HIGH input of ZZ pin puts the SRAM in the power-down state.The Linear Burst order (LBO#) is DC operated pin. LBO# pin will allow the choice of either an interleaved burst, or a linear burst.
   All read, write and deselect cycles are initiated by the ADV LOW input. Subsequent burst address can be internally generated as controlled by the ADV HIGH input.

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BUMP LAYOUT(TOP VIEW)

165bump-BGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A_7	E1#	BWc#	BWb#	E3#	CKE#	ADV	A_{17}	A_8	NC
B	NC	A_6	E2	BWd#	BWa#	CLK	W#	G#	A_{18}	A_9	NC
C	DQPc	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQPb
D	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
H	MCH	MCH	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
N	DQPd	NC	V_{DDQ}	V_{SS}	NC	NC	MCH	V_{SS}	V_{DDQ}	NC	DQPa
P	NC	NC	A_5	A_3	TDI	A_1	TDO	A_{15}	A_{13}	A_{11}	NC
R	LBO#	NC	A_4	A_2	TMS	A_0	TCK	A_{16}	A_{14}	A_{12}	A_{10}

Note1. MCH means "Must Connect High". MCH should be connected to HIGH.

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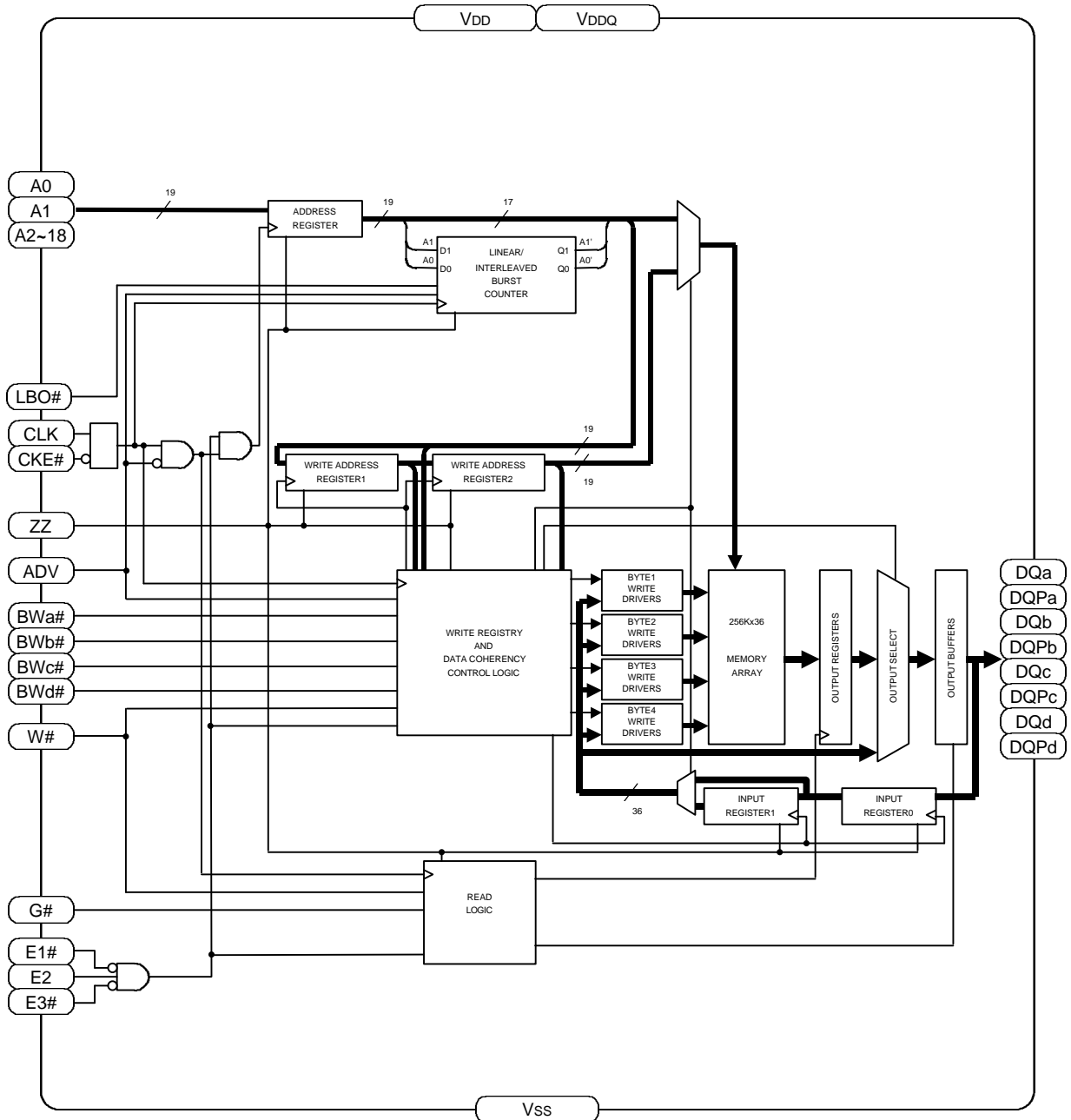
BLOCK DIAGRAM

Note2. The BLOCK DIAGRAM does not include the Boundary Scan logic. See Boundary Scan chapter.
Note3. The BLOCK DIAGRAM illustrates simplified device operation. See TRUTH TABLE, PIN FUNCTION
and timing diagrams for detailed information.

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PIN FUNCTION

Pin	Name	Function
A0~A18	Synchronous Address Inputs	These inputs are registered and must meet the setup and hold times around the rising edge of CLK. A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.
BWa#, BWb#, BWc#, BWd#	Synchronous Byte Write Enables	These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITEs need to be asserted on the same cycle as the address. BWs are associated with addresses and apply to subsequent data. BWa# controls DQa, DQPa pins; BWb# controls DQb, DQPb pins; BWc# controls DQc, DQPc pins; BWd# controls DQd, DQPd pins.
CLK	Clock Input	This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
E1#	Synchronous Chip Enable	This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV is LOW).
E2	Synchronous Chip Enable	This active High input is used to enable the device and is sampled only when a new external address is loaded (ADV is LOW). This input can be used for memory depth expansion.
E3#	Synchronous Chip Enable	This active Low input is used to enable the device and is sampled only when a new external address is loaded (ADV is LOW). This input can be used for memory depth expansion.
G#	Output Enable	This active LOW asynchronous input enable the data I/O output drivers.
ADV	Synchronous Address Advance/Load	When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When HIGH, W# is ignored. A LOW on this pin permits a new address to be loaded at CLK rising edge.
CKE#	Synchronous Clock Enable	This active LOW input permits CLK to propagate throughout the device. When HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK.
ZZ	Snooze Enable	This active HIGH asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When active, all other inputs are ignored. When this pin is LOW or NC, the SRAM normally operates.
W#	Synchronous Read/Write	This active input determines the cycle type when ADV is LOW. This is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on the pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus width WRITEs occur if all byte write enables are LOW.
DQa,DQPa,DQb,DQPb DQc,DQPc,DQd,DQPd	Synchronous Data I/O	Byte "a" is DQa , DQPa pins; Byte "b" is DQb, DQPb pins; Byte "c" is DQc, DQPc pins; Byte "d" is DQd,DQPd pins. Input data must meet setup and hold times around CLK rising edge.
LBO#	Burst Mode Control	This DC operated pin allows the choice of either an interleaved burst or a linear burst. If this pin is HIGH or NC, an interleaved burst occurs. When this pin is LOW, a linear burst occurs, and input leak current to this pin.
V$_{DD}$	V$_{DD}$	Core Power Supply
Vss	Vss	Ground
V$_{DDQ}$	V$_{DDQ}$	I/O buffer Power supply
TDI	Test Data Input	These pins are used for Boundary Scan Test.
TDO	Test Data Output	
TCK	Test Clock	
TMS	Test Mode Select	
MCH	Must Connect High	These pins should be connected to HIGH
NC	No Connect	These pins are not internally connected and may be connected to ground.

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DC OPERATED TRUTH TABLE

Name	Input Status	Operation
LBO#	HIGH or NC	Interleaved Burst Sequence
	LOW	Linear Burst Sequence

Note4. LBO# is DC operated pin.
Note5. NC means No Connection.
Note6. See BURST SEQUENCE TABLE about interleaved and Linear Burst Sequence.

BURST SEQUENCE TABLE

Interleaved Burst Sequence (when LBO# = HIGH or NC)

Operation	A18~A2	A1,A0			
First access, latch external address	A18~A2	0 , 0	0 , 1	1 , 0	1 , 1
Second access(first burst address)	latched A18~A2	0 , 1	0 , 0	1 , 1	1 , 0
Third access(second burst address)	latched A18~A2	1 , 0	1 , 1	0 , 0	0 , 1
Fourth access(third burst address)	latched A18~A2	1 , 1	1 , 0	0 , 1	0 , 0

Linear Burst Sequence (when LBO# = LOW)

Operation	A18~A2	A1,A0			
First access, latch external address	A18~A2	0 , 0	0 , 1	1 , 0	1 , 1
Second access(first burst address)	latched A18~A2	0 , 1	1 , 0	1 , 1	0 , 0
Third access(second burst address)	latched A18~A2	1 , 0	1 , 1	0 , 0	0 , 1
Fourth access(third burst address)	latched A18~A2	1 , 1	0 , 0	0 , 1	1 , 0

Note7. The burst sequence wraps around to its initial state upon completion.

TRUTH TABLE

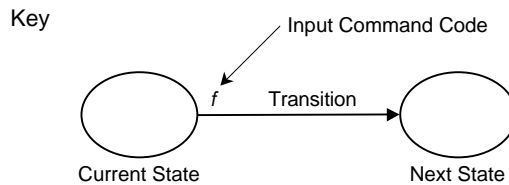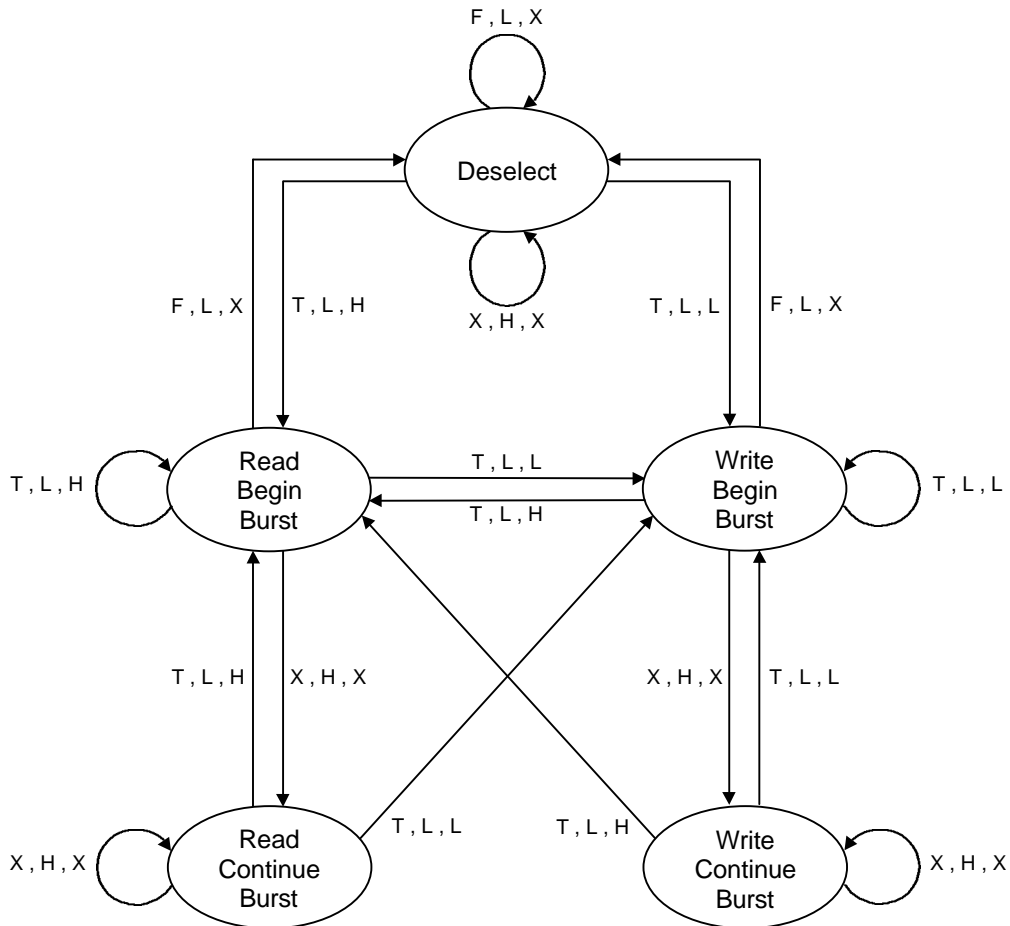| E1#	E2	E3#	ZZ	ADV	W#	BWx#	G#	CKE#	CLK	DQ	Address used	Operation
H	X	X	L	L	X	X	X	L	L->H	High-Z	None	Deselect Cycle
X	**L**	X	L	L	X	X	X	L	L->H	High-Z	None	Deselect Cycle
X	X	**H**	L	L	X	X	X	L	L->H	High-Z	None	Deselect Cycle
X	X	X	L	**H**	X	X	X	L	L->H	High-Z	None	Continue Deselect Cycle
L	**H**	**L**	L	L	**H**	X	**L**	L	L->H	Q	External	Read Cycle, Begin Burst
X	X	X	L	**H**	X	X	L	L	L->H	Q	Next	Read Cycle, Continue Burst
L	**H**	**L**	L	L	**H**	X	**H**	L	L->H	High-Z	External	NOP/Dummy Read, Begin Burst
X	X	X	L	**H**	X	X	**H**	L	L->H	High-Z	Next	Dummy Read, Continue Burst
L	**H**	**L**	L	L	**L**	L	X	L	L->H	D	External	Write Cycle, Begin Burst
X	X	X	L	**H**	X	L	X	L	L->H	D	Next	Write Cycle, Continue Burst
L	**H**	**L**	L	L	**L**	**H**	X	L	L->H	High-Z	None	NOP/Write Abort, Begin Burst
X	X	X	L	**H**	X	**H**	X	L	L->H	High-Z	Next	Write Abort, Continue Burst
X	X	X	L	X	X	X	X	H	L->H	-	Current	Ignore Clock edge, Stall
X	X	X	**H**	X	X	X	X	X	X	High-Z	None	Snooze Mode

Note8. X means "don't care". H means logic HIGH. L means logic LOW.
Note9. BWx#=H means all Synchronous Byte Write Enables (BWa#,BWb#,BWc#,BWd#) are HIGH. BWx#=L means one or more Synchronous Byte Write Enables are LOW.
Note10. All inputs except G# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.

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STATE DIAGRAM

F , L , X

Deselect

X , H , X

F , L , X   T , L , H   T , L , L   F , L , X

T , L , H Read Begin Burst   T , L , L → Write Begin Burst   T , L , L
                               T , L , H ←

T , L , H   X , H , X   X , H , X   T , L , L

X , H , X Read Continue Burst   T , L , L   T , L , H   Write Continue Burst   X , H , X

Key

Input Command Code

Current State   *f*   Transition →   Next State

Note11. The notation "x , x , x" controlling the state transitions above indicate the state of inputs E, ADV and W# respectively.
Note12. If (E1# = L and E2 = H and E3# = L) then E="T" else E="F".
Note13. "H" = input "high"; "L" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".

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WRITE TRUTH TABLE

W#	BWa#	BWb#	BWc#	BWd#	Function
H	X	X	X	X	Read
L	L	H	H	H	Write Byte a
L	H	L	H	H	Write Byte b
L	H	H	L	H	Write Byte c
L	H	H	H	L	Write Byte d
L	L	L	L	L	Write All Bytes
L	H	H	H	H	Write Abort/NOP

Note14.X means "don't care". H means logic HIGH. L means logic LOW.
Note15. All inputs except G# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Power Supply Voltage		-1.0*~3.6	V
V_{DDQ}	I/O Buffer Power Supply Voltage		-1.0*~3.6	V
V_I	Input Voltage	With respect to V_{SS}	-1.0~V_{DDQ}+1.0**	V
V_O	Output Voltage		-1.0~V_{DDQ}+1.0**	V
PD	Maximum Power Dissipation (V_{DD})		1050	mW
T_{OPR}	Operating Temperature		0~70	℃
$T_{STG(bias)}$	Storage Temperature(bias)		-10~85	℃
T_{STG}	Storage Temperature		-65~150	℃

Note16.* This is –1.0V when pulse width≤2ns, and –0.5V in case of DC.
   ** This is –1.0V~V_{DDQ}+1.0V when pulse width≤2ns, and –0.5V~V_{DDQ}+0.5V in case of DC.

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DC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{DD}=2.375~2.625V, unless otherwise noted)

Symbol	Parameter	Condition		Limits		Unit
				Min	Max	
V_{DD}	Power Supply Voltage			2.375	2.625	V
V_{DDQ}	I/O Buffer Power Supply Voltage	V_{DDQ} = 2.5V		2.375	2.625	V
		V_{DDQ} = 1.8V		1.7	1.95	
V_{IH}	High-level Input Voltage	V_{DDQ} = 2.375~2.625V		0.65*V_{DDQ}	V_{DDQ}+0.3*	V
		V_{DDQ} = 1.7~1.95V				
V_{IL}	Low-level Input Voltage	V_{DDQ} = 2.375~2.625V		-0.3*	0.35*V_{DDQ}	V
		V_{DDQ} = 1.7~1.95V				
V_{OH}	High-level Output Voltage	I_{OH} = -2.0mA		V_{DDQ}-0.4		V
V_{OL}	Low-level Output Voltage	I_{OL} = 2.0mA			0.4	V
I_{LI}	Input Current except ZZ and LBO#	V_I = 0V ~ V_{DDQ}			10	µA
	Input Current of LBO#	V_I = 0V ~ V_{DDQ}			10	
	Input Current of ZZ	V_I = 0V ~ V_{DDQ}			10	
I_{LO}	Off-state Output Current	V_I (G#) ≥ V_{IH}, V_O = 0V ~ V_{DDQ}			10	µA
I_{CC1}	Power Supply Current : Operating	Device selected; Output Open V_I≤V_{IL} or V_I≥V_{IH} ZZ≤V_{IL}	4.0ns cycle(250MHz)		400	mA
			4.4ns cycle(225MHz)		380	
			5.0ns cycle(200MHz)		360	
I_{CC2}	Power Supply Current : Deselected	Device deselected V_I≤V_{IL} or V_I≥V_{IH} ZZ≤V_{IL}	4.0ns cycle(250MHz)		140	mA
			4.4ns cycle(225MHz)		110	
			5.0ns cycle(200MHz)		100	
I_{CC3}	CMOS Standby Current (CLK stopped standby mode)	Device deselected; Output Open V_I≤V_{SS}+0.2V or V_I≥V_{DDQ}-0.2V CLK frequency=0Hz, All inputs static			20	mA
I_{CC4}	Snooze Mode Standby Current	Snooze mode ZZ≥V_{DDQ}-0.2V, LBO#≥V_{DD}-0.2V			20	mA
I_{CC5}	Stall Current	Device selected; Output Open CKE#≥V_{IH} V_I≤V_{SS}+0.2V or V_I≥V_{DDQ}-0.2V	4.0ns cycle(250MHz)		70	mA
			4.4ns cycle(225MHz)		60	
			5.0ns cycle(200MHz)		50	

Note17.*$V_{IL min}$ is −1.0V and $V_{IH max}$ is V_{DDQ}+1.0V in case of AC(Pulse width≤2ns).
Note18."Device Deselected" means device is in power-down mode as defined in the truth table.

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CAPACITANCE

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input Capacitance	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Input / Output(DQ) Capacitance	V_O=GND, V_O=25mVrms, f=1MHz			8	pF

Note19.This parameter is sampled.

THERMAL RESISTANCE

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
θ_{JA}	Thermal Resistance Junction Ambient	TBD		TBD		°C/W
θ_{JC}	Thermal Resistance Junction to Case	TBD		TBD		°C/W

Note20.This parameter is sampled.

AC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{DD}=2.375~2.625V, unless otherwise noted)
(1)MEASUREMENT CONDITION
Input pulse levels ·· V_{IH}=V_{DDQ}, V_{IL}=0V
Input rise and fall times ····························· faster than or equal to 1V/ns
Input timing reference levels ····················· V_{IH}=V_{IL}=0.5*V_{DDQ}
Output reference levels ······························V_{IH}=V_{IL}=0.5*V_{DDQ}
Output load ·· Fig.1
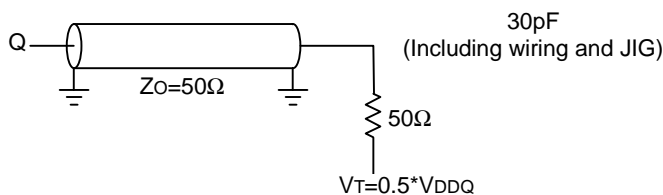
Fig.1 Output load
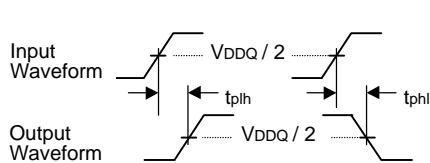
Fig.2 Tdly measurement
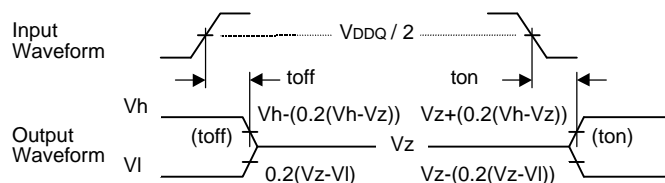
Fig.3 Tri-State measurement

Note21.Valid Delay Measurement is made from the V_{DDQ}/2 on the input waveform to the V_{DDQ}/2 on the output waveform.
Input waveform should have a slew rate of faster than or equal to 1V/ns.
Note22.Tri-state toff measurement is made from the V_{DDQ}/2 on the input waveform to the output waveform moving 20%
from its initial to final Value V_{DDQ}/2.
Note:the initial value is not V_{OL} or V_{OH} as specified in DC ELECTRICAL CHARACTERISTICS table.
Note23. Tri-state ton measurement is made from the V_{DDQ}/2 on the input waveform to the output waveform moving 20%
from its initial Value V_{DDQ}/2 to its final Value.
Note:the final value is not V_{OL} or V_{OH} as specified in DC ELECTRICAL CHARACTERISTICS table.
Note24.Clocks,Data,Address and control signals will be tested with a minimum input slew rate of faster than or equal to 1V/ns.

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(2)TIMING CHARACTERISTICS

Symbol	Parameter	250MHz -25 Min	250MHz -25 Max	225MHz -22 Min	225MHz -22 Max	200MHz -20 Min	200MHz -20 Max	Unit
Clock								
tKHKH	Clock cycle time	4.0		4.4		5.0		ns
tKHKL	Clock HIGH time	1.5		1.6		1.8		ns
tKLKH	Clock LOW time	1.5		1.6		1.8		ns
Output times								
tKHQV	Clock HIGH to output valid		2.6		2.8		3.2	ns
tKHQX	Clock HIGH to output invalid	0.5		0.6		0.7		ns
tKHQX1	Clock HIGH to output in LOW-Z	0.5		0.6		0.7		ns
tKHQZ	Clock HIGH to output in High-Z	0.5	2.6	0.6	2.8	0.7	3.2	ns
tGLQV	G# to output valid		2.6		2.8		3.2	ns
tGLQX1	G# to output in Low-Z	0.0		0.0		0.0		ns
tGHQZ	G# to output in High-Z		2.6		2.8		3.2	ns
Setup Times								
tAVKH	Address valid to clock HIGH	0.8		1.0		1.2		ns
tckeVKH	CKE# valid to clock HIGH	0.8		1.0		1.2		ns
tadvVKH	ADV valid to clock HIGH	0.8		1.0		1.2		ns
tWVKH	Write valid to clock HIGH	0.8		1.0		1.2		ns
tBVKH	Byte write valid to clock HIGH (BWa#~BWd#)	0.8		1.0		1.2		ns
tEVKH	Enable valid to clock HIGH (E1#,E2,E3#)	0.8		1.0		1.2		ns
tDVKH	Data In valid clock HIGH	0.8		1.0		1.2		ns
Hold Times								
tKHAX	Clock HIGH to Address don't care	0.5		0.5		0.5		ns
tKHckeX	Clock HIGH to CKE# don't care	0.5		0.5		0.5		ns
tKHadvX	Clock HIGH to ADV don't care	0.5		0.5		0.5		ns
tKHWX	Clock HIGH to Write don't care	0.5		0.5		0.5		ns
tKHBX	Clock HIGH to Byte Write don't care (BWa#~BWb#)	0.5		0.5		0.5		ns
tKHEX	Clock HIGH to Enable don't care (E1#,E2,E3#)	0.5		0.5		0.5		ns
tKHDX	Clock HIGH to Data In don't care	0.5		0.5		0.5		ns
ZZ								
tZZS	ZZ standby		2*tKHKH		2*tKHKH		2*tKHKH	ns
tZZREC	ZZ recovery		2*tKHKH		2*tKHKH		2*tKHKH	ns

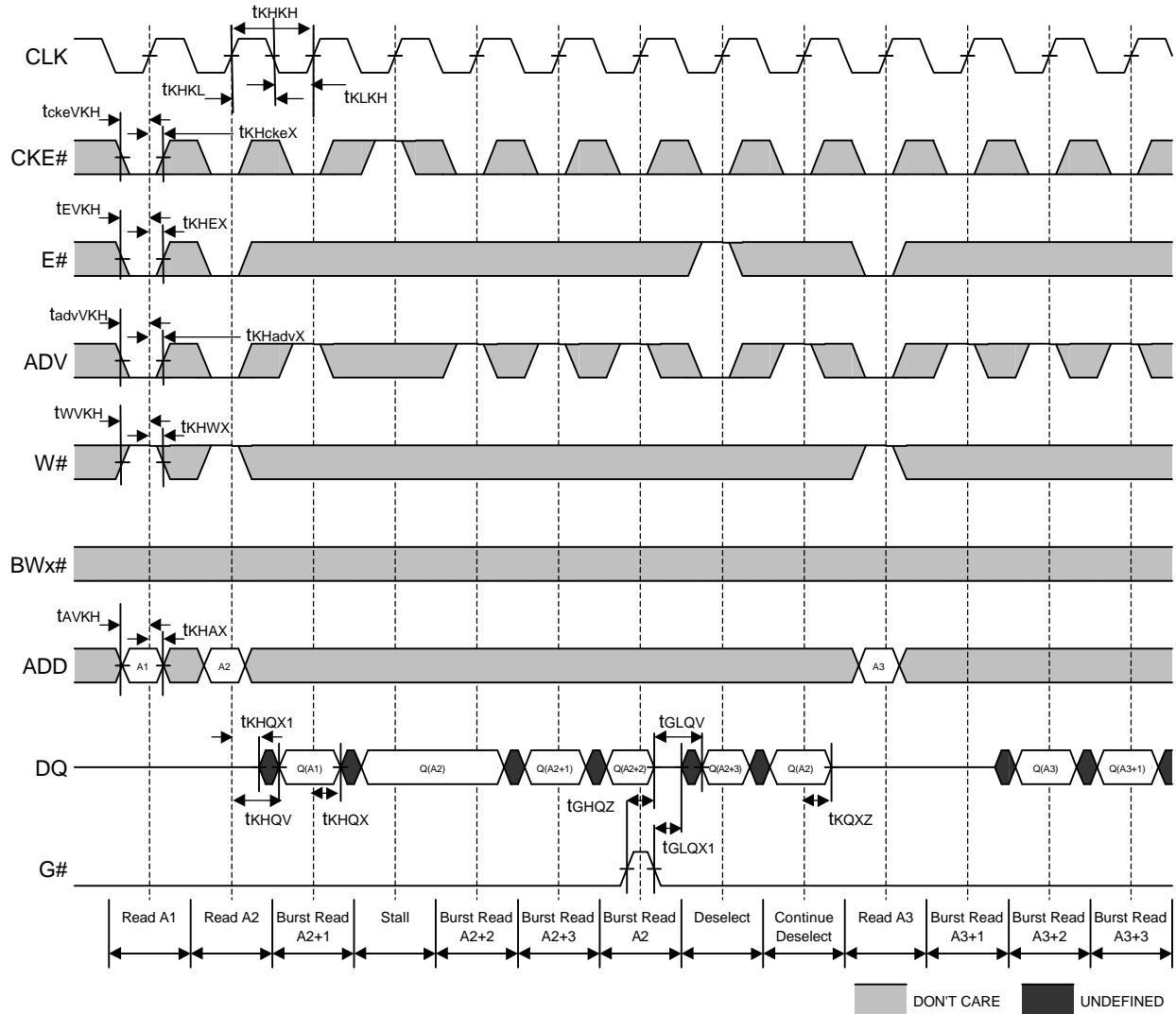Note25.All parameter except tZZS, tZZREC in this table are measured on condition that ZZ=LOW fix.
Note26.Test conditions is specified with the output loading shown in Fig.1 unless otherwise noted.
Note27. tKHQX1, tKHQZ, tGLQX1, tGHQZ are sampled.
Note28.LBO# is static and must not change during normal operation.
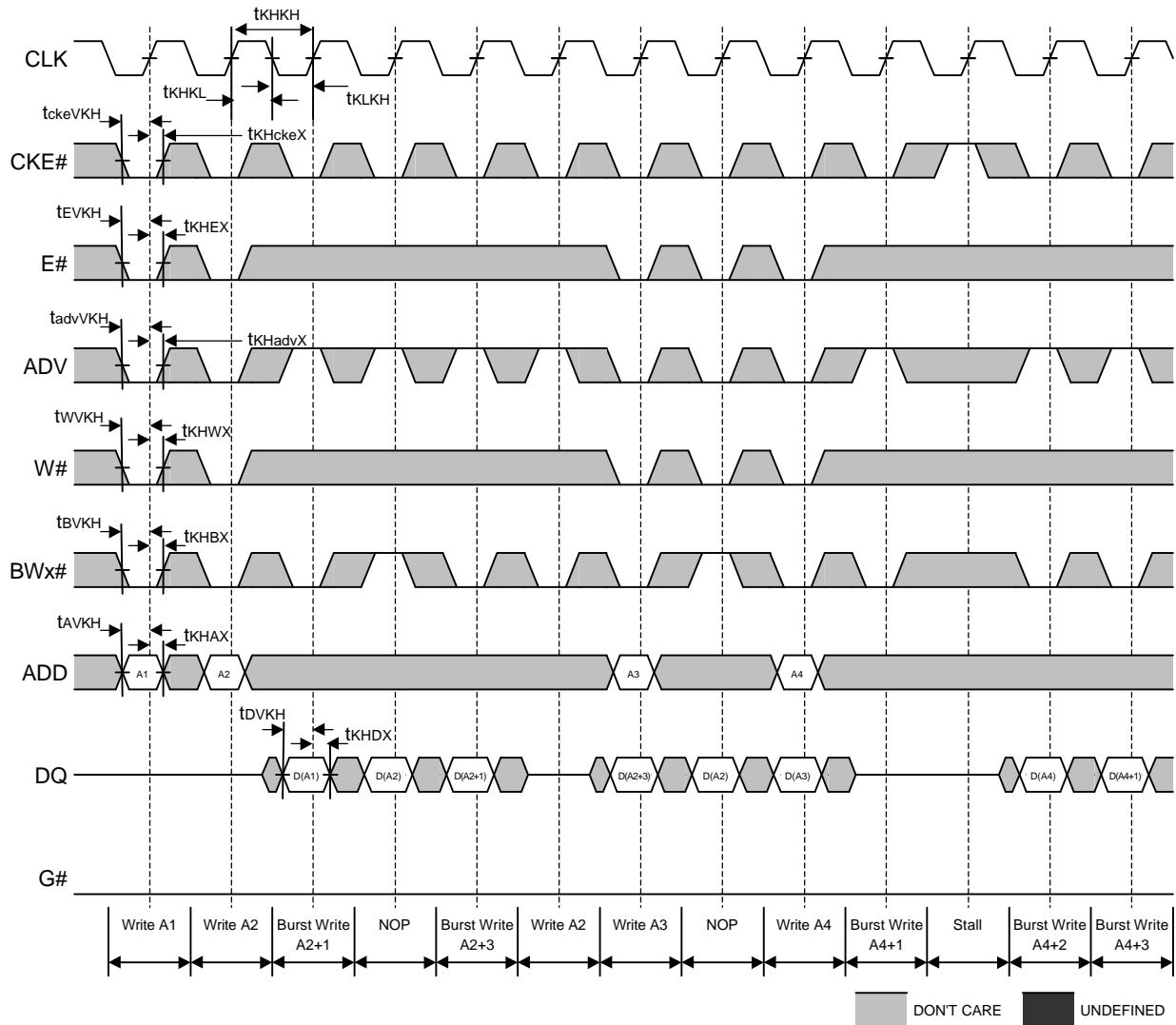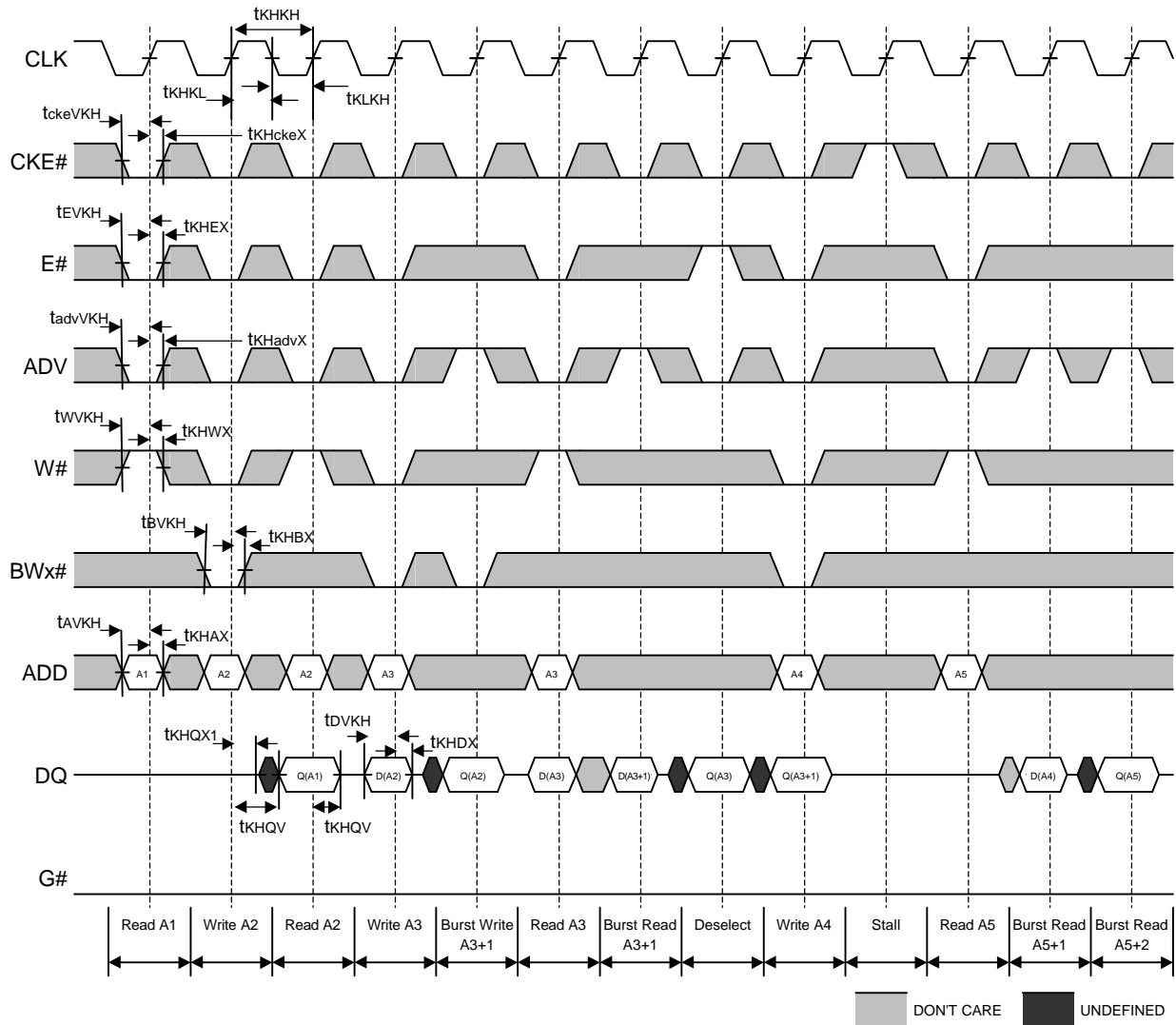
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(3)READ TIMING

Note29.Q(An) refers to output from address An. Q(An+1) refers to output from the next internal burst address following An.
Note30. E# represents three signals. When E# is LOW, it represents E1# is LOW, E2 is HIGH and E3# is LOW.
Note31.ZZ is fixed LOW.

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(4)WRITE TIMING

Note32.Q(An) refers to output from address An. Q(An+1) refers to output from the next internal burst address following An.
Note33. E# represents three signals. When E# is LOW, it represents E1# is LOW, E2 is HIGH and E3# is LOW.
Note34.ZZ is fixed LOW.

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Advanced Information
M5M5T5636UG REV.0.2

(5)READ/WRITE TIMING

Note35.Q(An) refers to output from address An. Q(An+1) refers to output from the next internal burst address following An.
Note36. E# represents three signals. When E# is LOW, it represents E1# is LOW, E2 is HIGH and E3# is LOW.
Note37.ZZ is fixed LOW.

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(6)SNOOZE MODE TIMING
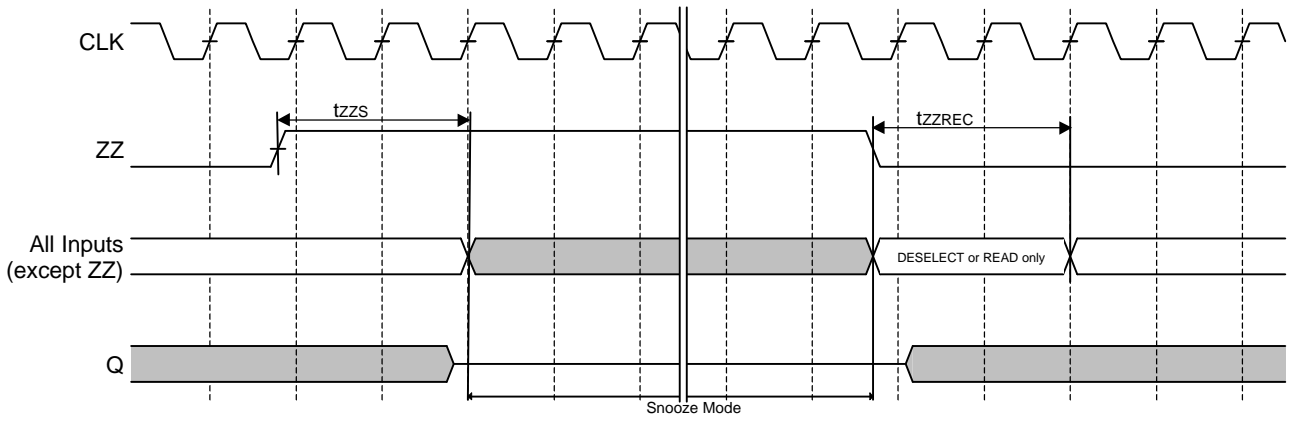
JTAG PORT OPERATION

Overview
The JTAG Port on this SRAM operates in a manner consistent with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG), but dose not implement all of the function required for 1149.1 compliance. The JTAG Port interfaces with conventional CMOS logic level signaling.

Disabling the JTAG port
It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. To assure normal operation of the SRAM with the JTAG Port unused, the TCK, TDI and TMS pins may be left floating or tied to High. The TDO pin should be left unconnected.

JTAG Pin Description

Test Clock (TCK)
The TCK input is clock for all TAP events. All inputs are captured on the rising edge of TCK and the Test Data Out (TDO) propagates from the falling edge of TCK.

Test Mode Select (TMS)
The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP Controller state machine. An undriven TMS input will produce the same result as a logic one input level.

Test Data In (TDI)
The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between the TDI and TDO pins. the register placed between the TDI and TDO pins is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Resister (refer to the TAP Controller State Diagram). An undriven TDI Input will produce the same result as a logic one input level.

Test Data Out (TDO)
The TDO output is active depending on the state of the TAP Controller state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between the TDI and TDO pins.

Note:
This device dose not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automatically at power-up.

JTAG Port Registers

Overview
The various JTAG registers, referred to as Test Access Port or TAP Registers, are selected (one at a time) via the sequence of 1s and 0s applied to TMS as TCK is strobed. Each of TAP Registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register
The Instruction Register holds the instructions that are executed by the TAP Controller when it is moved into the Run-Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Resister can be loaded when it is placed between the TDI and TDO pins. The Instruction Resister is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

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Bypass Register

The Bypass resister is a single-bit register that can be placed between the TDI and TDO pins. It allows serial test data to be passed through the SRAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the SRAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pins. The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the SRAM's I/O ring when the controller is in the Capture-RD state and then is placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instruction can be used to activate the Boundary Scan Register.

Identification (ID) Register

The ID register is a 32-bit register that is loaded with a device and vender specific 32-bit code when the controllers put in the Capture-DR state with the IDCODE Instruction loaded in the Instruction Register. The code is loaded from 32-bit on-chip ROM. It describes various attributes of the SRAM (see page 20). The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach the TDO pin when shifting begins.

TAP Controller Instruction Set

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; standard (Public) instructions, and device specific (Private) instructions. Some public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP Controller in this device is not fully 1194.1-compliant because some of the mandatory 1149.1 instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads. This device will not perform INTEST or PRELOAD portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in the Shift-IR state, the Instruction Register is placed between the TDI and TDO pins. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at the TDO output). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to the Update-IR state. The TAP Instruction Set for this device is listed in the following table.

Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register, the Bypass Register is placed between the TDI and TDO pins. This occurs when the TAP Controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard1149.1 mandatory public instruction. When the SAMPLE/PRELOAD instruction is loaded in the Instruction Register, moving the TAP Controller into the Capture-DR state loads the data in the SRAM's input and I/O buffers into the Boundary Scan Register. Because the SRAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. SRAM input signals must be stabilized for long enough to meet the TAP's input data capture set-up plus hold time (tTS plus tTH). The SRAM's clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to the Shift-DR state then places the Boundary Scan Register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the Update-DR state with the SAMPLE/PRELOAD instruction loaded in the Instruction Register has the same effect as the Pause-DR command. This functionality is not Standard 1149.1 compliant.

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EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the Instruction Register is loaded with all logic 0s. EXTEST is not implemented in the TAP Controller, and therefore this device is not compliant to the 1149.1 Standard. When the EXTEST instruction is loaded into the Instruction Register, the device responds as if the SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST place the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction cause the ID ROM to be loaded into the ID register when the controller is in the Capture-DR state and places the ID Register between the TDI and TDO pins in the Shift-DR state. The IDCODE instruction is the default instruction loaded in at power-up and any time the controller is placed in the Test-Logic-Reset state.
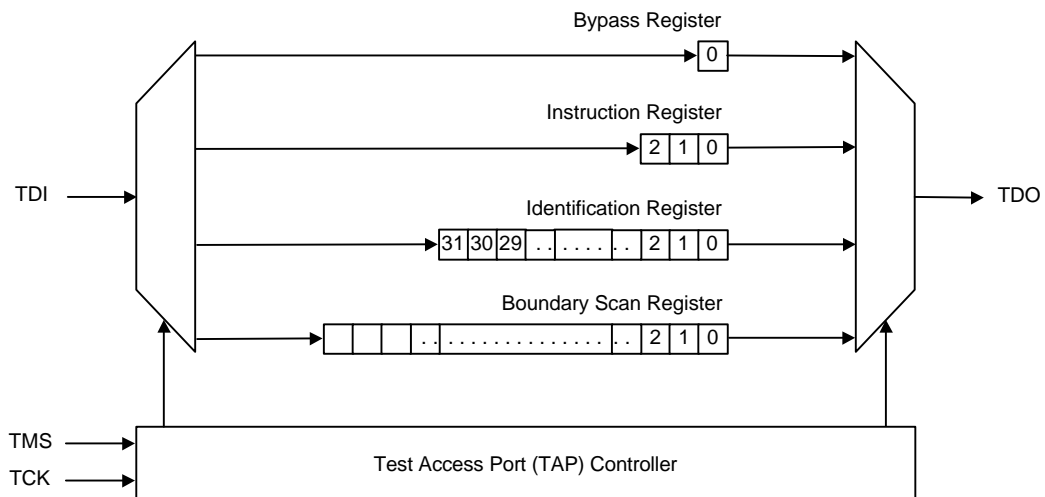
SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the Instruction Register, all SRAM outputs are forced to an inactive drive state (High-Z) and the Boundary Scan Register is placed between the TDI and TDO pins when the TAP Controller is moved to the Shift-DR state.

RFU

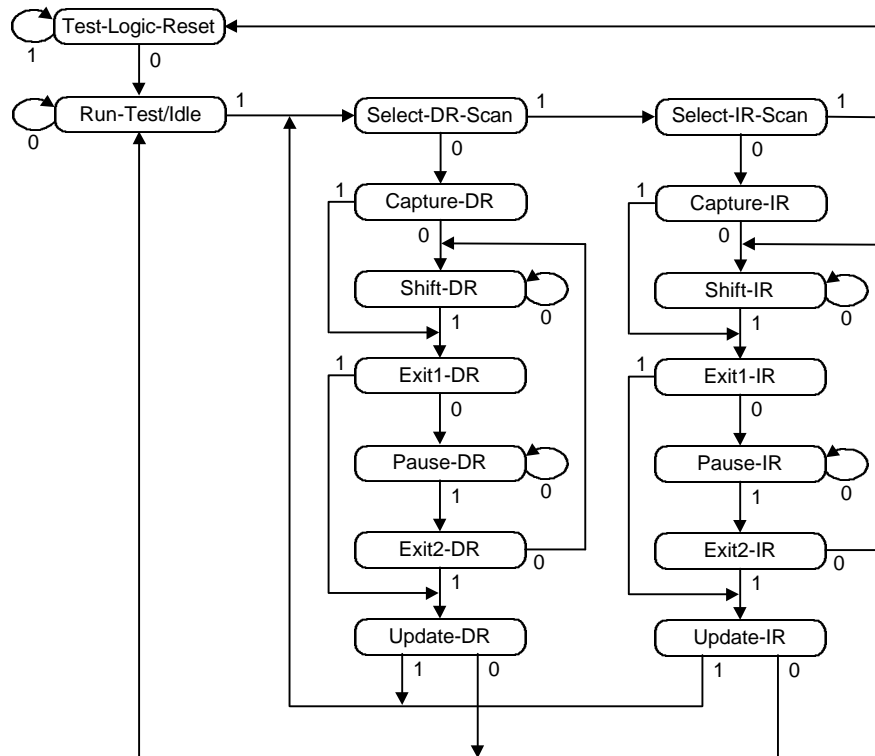These instructions are reserved for future use. Do not use these instructions.

JTAG TAP BLOCK DIAGRAM

BOUNDARY SCAN ORDER

TBD

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JTAG TAP CONTROLLER STATE DIAGRAM

TAP CONTROLLER DC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{DD}=2.375~2.625V, unless otherwise noted)

Symbol	Parameter	Condition	Limits		Unit
			Min	Max	
V_{IHT}	Test Port Input High Voltage		0.65*V_{DDQ}	V_{DDQ}+0.3 **	V
V_{ILT}	Test Port Input Low Voltage		-0.3 **	0.35*V_{DDQ}	V
V_{OHT}	Test Port Output High Voltage	I_{OH}=-100µA	V_{DDQ}-0.1	-	V
V_{OLT}	Test Port Output Low Voltage	I_{OL}=+100µA	-	0.1	V
I_{INT}	TMS, TCK and TDI Input Leakage Current		-10	10	µA
I_{OLT}	TDO Output Leakage Current	Output Disable, V_{OUT}=0V~V_{DDQ}	-10	10	µA

Note38. **Input Undershoot/Overshoot voltage must be -1V<Vi<V_{DDQ}+1V with a pulse width not to exceed 20% tTCK.

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TAP CONTROLLER AC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, VDD=2.375~2.625V, unless otherwise noted)

(1)MEASUREMENT CONDITION

Input pulse levels ·· V_{IH}=V_{DDQ}, V_{IL}=0V
Input rise and fall times ···························· faster than or equal to 1V/ns
Input timing reference levels ···················· V_{IH}=V_{IL}=0.5*V_{DDQ}
Output reference levels ···························· V_{IH}=V_{IL}=0.5*V_{DDQ}
Output load ··· Fig.4

Q — Z$_O$=50Ω

30pF
(Including wiring and JIG)

50Ω

V_T=0.5*V_{DDQ}
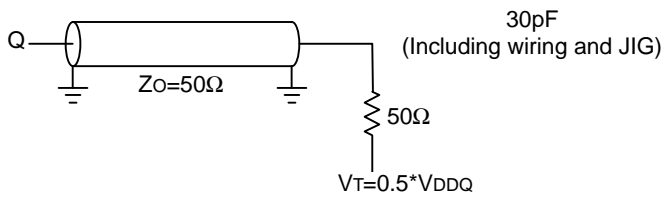
Fig.4 Output load

(2)TIMING CHARACTERISTICS

Symbol	Parameter	Limits		Unit
		Min	Max	
tTF	TCK Frequency		20	MHz
tTKC	TCK Cycle Time	50		ns
tTKH	TCK High Pulse Width	20		ns
tTKL	TCK Low Pulse Width	20		ns
tTS	TDI, TMS setup time	10		ns
tTH	TDI, TMS hold time	10		ns
tTKQ	TCK Low to TDO valid		20	ns

(3) TIMING

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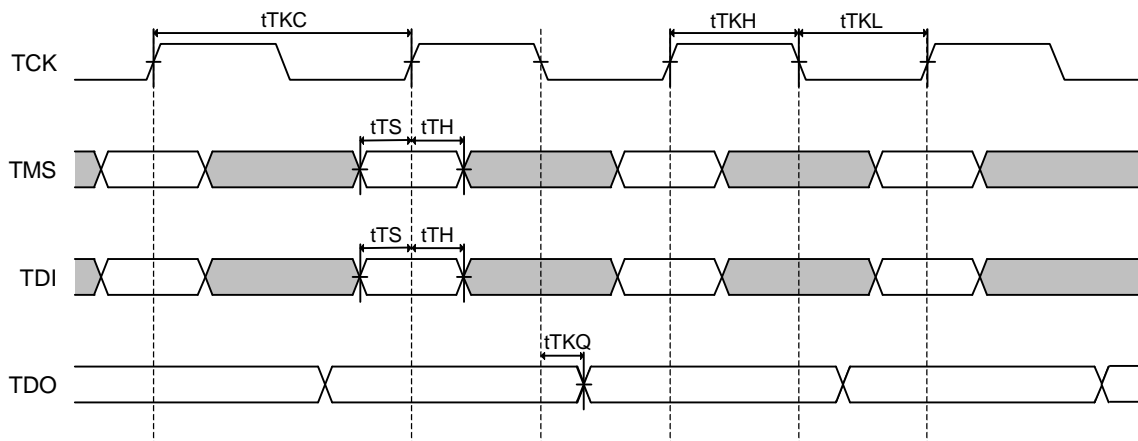
JTAG TAP INSTRUCTION SET SUMMARY

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Preloads ID Register and places it between TDI and TDO
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all Data output drivers to High-Z
RFU	011	Do not use this instruction; Reserved for Future Use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. This instruction dose not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RFU	101	Do not use this instruction; Reserved for Future Use.
RFU	110	Do not use this instruction; Reserved for Future Use.
BYPASS	111	Places the BYPASS Register between TDI and TDO.

STRUCTURE OF IDENTIFICATION REGISTER

	Revision				Device Information															JEDEC Vendor Code of MITSUBISHI												
					VDD			Capacity				Function				Width			Gen.													
Bit No.	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M5M5T5636	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	1

MSB   LSB

Note39. Bit of Device Information "Gen.(Generation)" means

Bit No.	13	12
1st Generation	0	0
2nd Generation	0	1
3rd Generation	1	0

Note40. Bit of Device Information "Width" means

Bit No.	16	15	14
X16	0	0	0
X18	0	0	1
X32	0	1	0
X36	0	1	1
X64	1	0	0
X72	1	0	1

Note41. Bit of Device Information "Function" means

Bit No.	20	19	18	17
Network SRAM	0	1	0	0
PB	0	0	0	1

Note42. Bit of Device Information "Capacity" means

Bit No.	24	23	22	21
1M or 1.15M	0	0	0	1
2M or 2.3M	0	0	1	0
4M or 4.5M	0	0	1	1
8M or 9M	0	1	0	0
16M or 18M	0	1	0	1
32M or 36M	0	1	1	0

Note43. Bit of Device Information "VDD" means

Bit No.	27	26	25
3.3V	0	0	0
2.5V	0	0	1
1.8V	0	1	0
1.5V	0	1	1

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PACKAGE OUTLINE

165(11x15) bump Ball Grid Array(BGA) Pin Pitch 1.00mm

Refer to JEDEC Standard MO-216, Variation CAB-1,

which can be seen at:

http://www.jedec.org/download/search/MO-216c.pdf

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REVISION HISTORY

- Mar/16/2001   REV.0.0   First revision

- Mar/30/2001   REV.0.1   Changed V_{DD} to V_{DDQ} about specification associated with V_I/V_O in electrical characteristics

- Jul/16/2001   REV.0.2   Fixed WRITE TRUTH TABLE and ABSOLUTE MAXIMUM RATINGS

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