

# MITSUBISHI LSIs M5M5V4R04J-12,-15

1997.11.20 Rev.F

## 4194304-BIT (1048576-WORD BY 4-BIT) CMOS STATIC RAM

### DESCRIPTION

The M5M5V4R04J is a family of 1048576-word by 4-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high speed application.

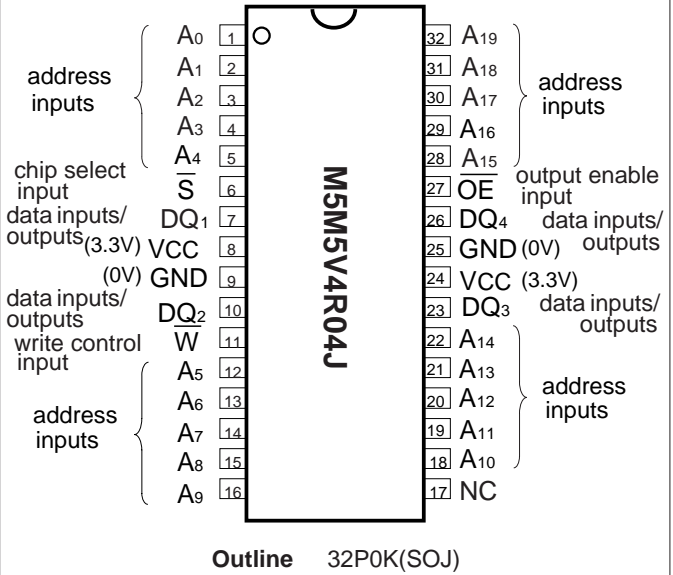
The M5M5V4R04J is offered in a 32-pin plastic small outline J-lead package(SOJ).

These device operate on a single 3.3V supply, and are directly TTL compatible. They include a power down feature as well.

### FEATURES

- Fast access time M5M5V4R04J-12 •••• 12ns(max)  
M5M5V4R04J-15 •••• 15ns(max)
- Low power dissipation Active •••••••• 297mW(typ)  
Stand by •••••••• 3.3mW(typ)
- Single +3.3V power supply
- Fully static operation : No clocks, No refresh
- Common data I/O
- Easy memory expansion by  $\bar{S}$
- Three-state outputs : OR-tie capability
- $\bar{OE}$  prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs

### PIN CONFIGURATION (TOP VIEW)



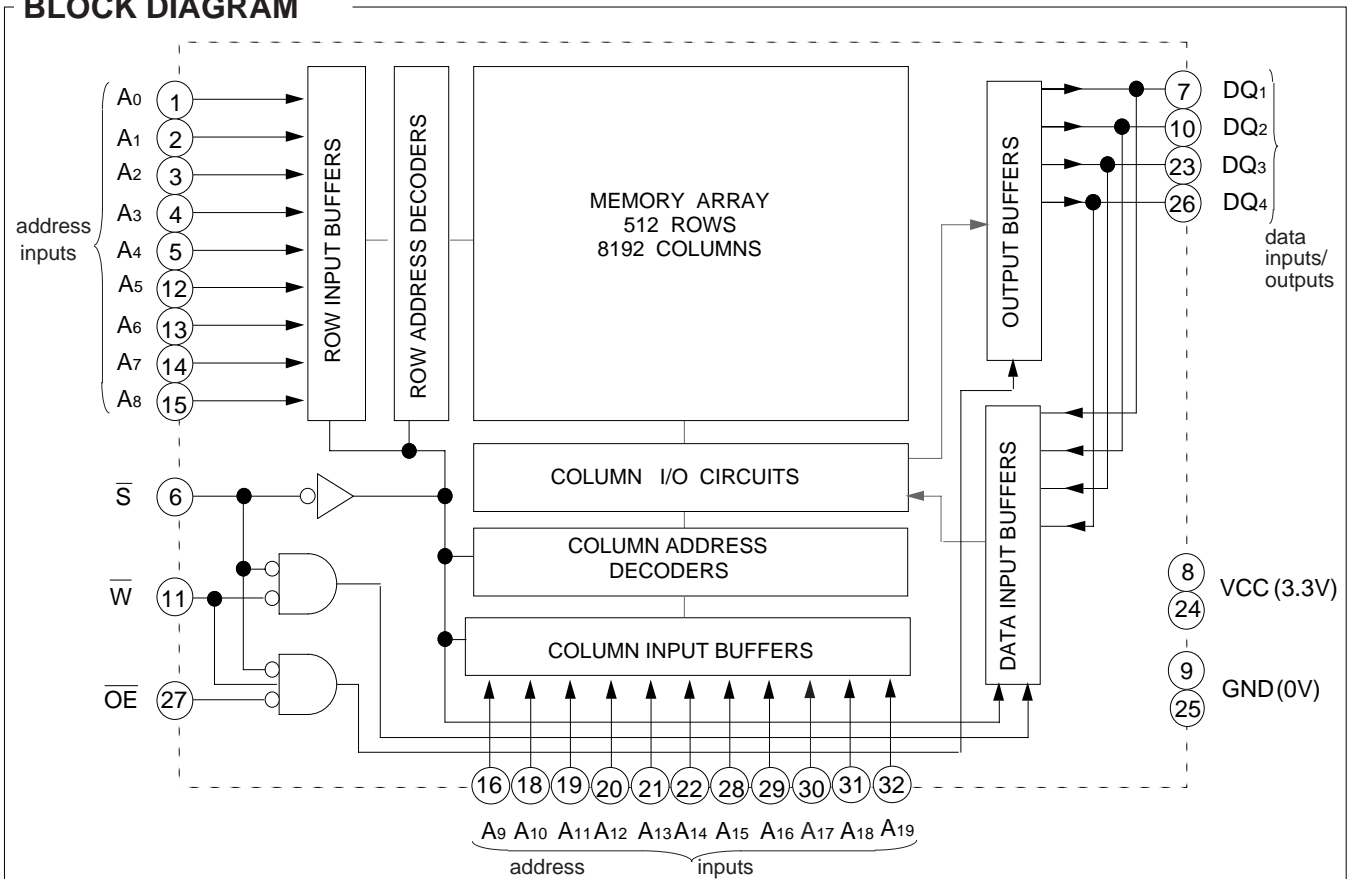
### APPLICATION

High-speed memory units

### PACKAGE

32pin 400mil SOJ

### BLOCK DIAGRAM



## FUNCTION

The operation mode of the M5M5V4R04J is determined by a combination of the device control inputs  $\overline{S}$ ,  $\overline{W}$  and  $\overline{OE}$ . Each mode is summarized in the function table.

A write cycle is executed whenever the low level  $\overline{W}$  overlaps with the low level  $\overline{S}$ . The address must be set-up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of  $\overline{W}$  or  $\overline{S}$ , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input  $\overline{OE}$  directly controls the output stage. Setting the  $\overline{OE}$  at a high level, the output stage is in a high impedance state, and the data bus

contention problem in the write cycle is eliminated.

A read cycle is executed by setting  $\overline{W}$  at a high level and  $\overline{OE}$  at a low level while  $\overline{S}$  are in an active state ( $\overline{S}=\text{L}$ ).

When setting  $\overline{S}$  at high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by  $\overline{S}$ .

Signal  $\overline{S}$  controls the power-down feature. When  $\overline{S}$  goes high, power dissipation is reduced extremely. The access time from  $\overline{S}$  is equivalent to the address access time.

## FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	I <sub>cc</sub>
H	X	X	Non selection	High-impedance	Stand by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>cc</sub>	Supply voltage	With respect to GND	-2.0* ~ 4.6	V
V <sub>I</sub>	Input voltage		-2.0* ~ V <sub>CC</sub> +0.5	V
V <sub>O</sub>	Output voltage		-2.0* ~ V <sub>CC</sub> +0.5	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =25 °C	1000	mW
T <sub>opr</sub>	Operating temperature		0 ~ 70	°C
T <sub>stg(bias)</sub>	Storage temperature (bias)		-10 ~ 85	°C
T <sub>stg</sub>	Storage temperature		-65 ~ 150	°C

\*Pulse width ≤ 20ns, In case of DC:-0.5V

## DC ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=0 ~ 70 °C, V<sub>cc</sub>=3.3V <sup>+10%</sup>/<sub>-5%</sub> unless otherwise noted)

Symbol	Parameter	Condition	Limits			Unit	
			Min	Typ	Max		
V <sub>IH</sub>	High-level input voltage		2.0		V <sub>cc</sub> +0.3	V	
V <sub>IL</sub>	Low-level input voltage		-0.3		0.8	V	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -4mA	2.4			V	
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 8mA			0.4	V	
I <sub>I</sub>	Input current	V <sub>I</sub> = 0~V <sub>cc</sub>			2	μA	
I <sub>OZ</sub>	Output current in off-state	V <sub>I</sub> ( $\overline{S}$ ) = V <sub>IH</sub> V <sub>O</sub> = 0~V <sub>cc</sub>			10	μA	
I <sub>CC1</sub>	Active supply current (TTL level)	V <sub>I</sub> ( $\overline{S}$ ) = V <sub>IL</sub> other inputs V <sub>IH</sub> or V <sub>IL</sub> Output-open(duty 100%)	AC	12ns cycle		160	mA
			DC			90	
I <sub>CC2</sub>	Stand by current (TTL level)	V <sub>I</sub> ( $\overline{S}$ ) = V <sub>IH</sub>	AC	12ns cycle		75	mA
			DC				
I <sub>CC3</sub>	Stand by current	V <sub>I</sub> ( $\overline{S}$ ) = V <sub>cc</sub> ≥ 0.2V other inputs V <sub>I</sub> ≤ 0.2V or V <sub>I</sub> ≥ V <sub>cc</sub> - 0.2V		1	10	mA	

**CAPACITANCE** ( $T_a=0 \sim 70 \text{ }^\circ\text{C}$ ,  $V_{cc}=3.3\text{V}$   $\begin{smallmatrix} +10\% \\ -5\% \end{smallmatrix}$  unless otherwise noted)

Symbol	Parameter	Test Condition	Limit			Unit
			Min	Typ	Max	
C <sub>I</sub>	Input capacitance	$V_I = \text{GND}, V_I = 25\text{mVrms}, f=1\text{MHz}$			7	pF
C <sub>O</sub>	Output capacitance	$V_O = \text{GND}, V_O = 25\text{mVrms}, f=1\text{MHz}$			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).  
 2: Typical value is  $V_{cc}=5\text{V}, T_a=25 \text{ }^\circ\text{C}$   
 3: C<sub>I</sub>, C<sub>O</sub> are periodically sampled and are not 100% tested.

**AC ELECTRICAL CHARACTERISTICS** ( $T_a=0 \sim 70 \text{ }^\circ\text{C}$ ,  $V_{cc}=3.3\text{V}$   $\begin{smallmatrix} +10\% \\ -5\% \end{smallmatrix}$  unless otherwise noted)

**(1) MEASUREMENT CONDITION**

- Input pulse levels .....  $V_{IH}=3.0\text{V}, V_{IL}=0.0\text{V}$
- Input rise and fall time ..... 3ns
- Input timing reference levels .....  $V_{IH}=1.5\text{V}, V_{IL}=1.5\text{V}$
- Output timing reference levels .....  $V_{OH}=1.5\text{V}, V_{OL}=1.5\text{V}$
- Output loads ..... Fig1, Fig2

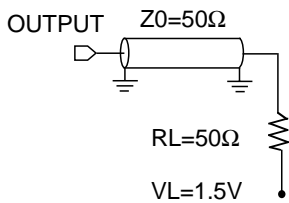


Fig.1 Output load

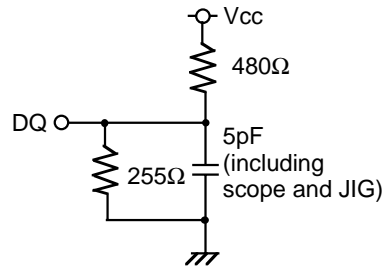


Fig.2 Output load for  $t_{en}, t_{dis}$

## (2)READ CYCLE

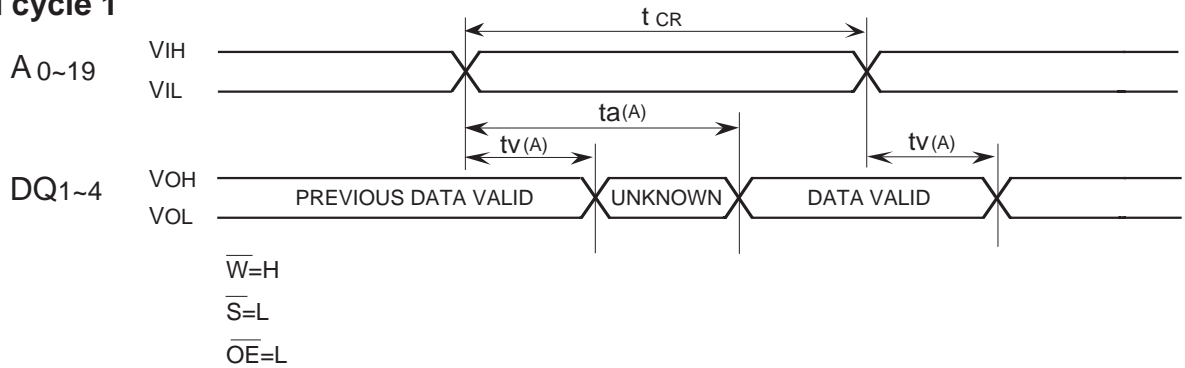
Symbol	Parameter	Limits				Unit
		M5M5V4R04J -12		M5M5V4R04J -15		
		Min	Max	Min	Max	
t <sub>CR</sub>	Read cycle time	12		15		ns
t <sub>a(A)</sub>	Address access time		12		15	ns
t <sub>a(S)</sub>	Chip select access time		12		15	ns
t <sub>a(OE)</sub>	Output enable access time		6		8	ns
t <sub>dis(S)</sub>	Output disable time after $\bar{S}$ high	0	6	0	7	ns
t <sub>dis(OE)</sub>	Output disable time after $\bar{OE}$ high	0	6	0	7	ns
t <sub>en(S)</sub>	Output enable time after $\bar{S}$ low	0		0		ns
t <sub>en(OE)</sub>	Output enable time after $\bar{OE}$ low	0		0		ns
t <sub>v(A)</sub>	Data valid time after address change	3		3		ns
t <sub>PU</sub>	Power-up time after chip selection	0		0		ns
t <sub>PD</sub>	Power-down time after chip selection		12		15	ns

## (3)WRITE CYCLE

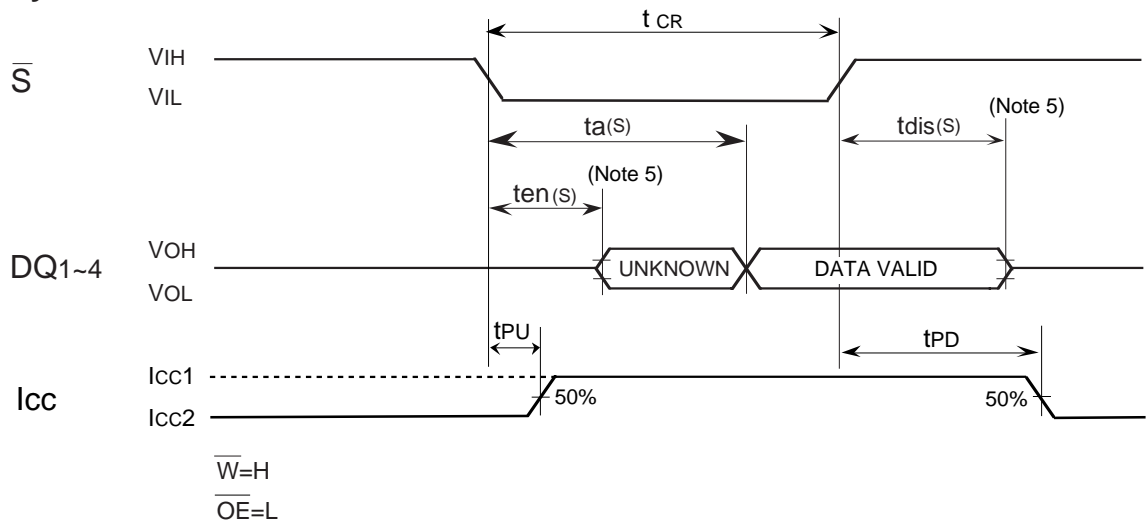
Symbol	Parameter	Limits				Unit
		M5M5V4R04J -12		M5M5V4R04J -15		
		Min	Max	Min	Max	
t <sub>cw</sub>	Write cycle time	12		15		ns
t <sub>w(W)</sub>	Write pulse width	10		12		ns
t <sub>su(A)1</sub>	Address setup time( $\bar{W}$ )	0		0		ns
t <sub>su(A)2</sub>	Address setup time( $\bar{S}$ )	0		0		ns
t <sub>su(S)</sub>	Chip select setup time	10		12		ns
t <sub>su(D)</sub>	Data setup time	6		7		ns
t <sub>h(D)</sub>	Data hold time	0		0		ns
t <sub>rec(W)</sub>	Write recovery time	1		1		ns
t <sub>dis(W)</sub>	Output disable time after $\bar{W}$ low	0	6	0	7	ns
t <sub>dis(OE)</sub>	Output disable time after $\bar{OE}$ high	0	6	0	7	ns
t <sub>en(W)</sub>	Output enable time after $\bar{W}$ high	0		0		ns
t <sub>en(OE)</sub>	Output enable time after $\bar{OE}$ low	0		0		ns
t <sub>su(A-WH)</sub>	Address to $\bar{W}$ High	10		12		ns

(4)TIMING DIAGRAMS

Read cycle 1



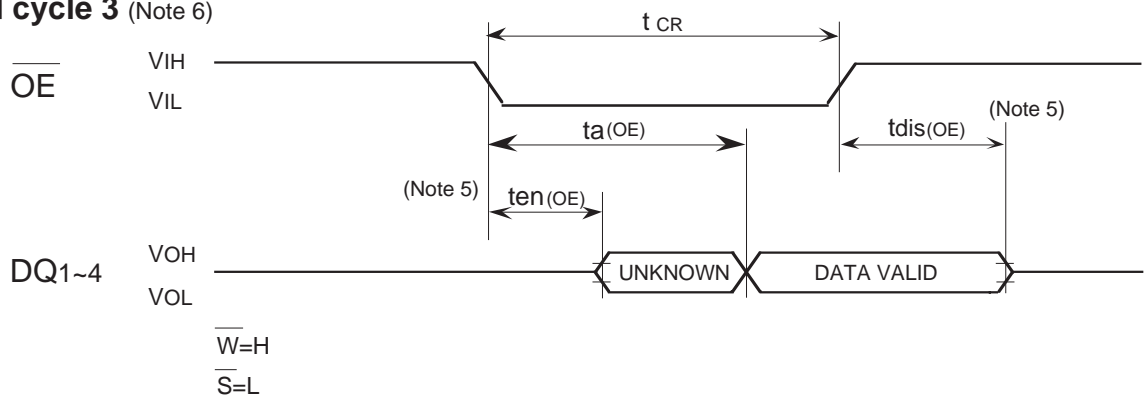
Read cycle 2 (Note 4)



Note 4. Addresses valid prior to or coincident with S transition low.

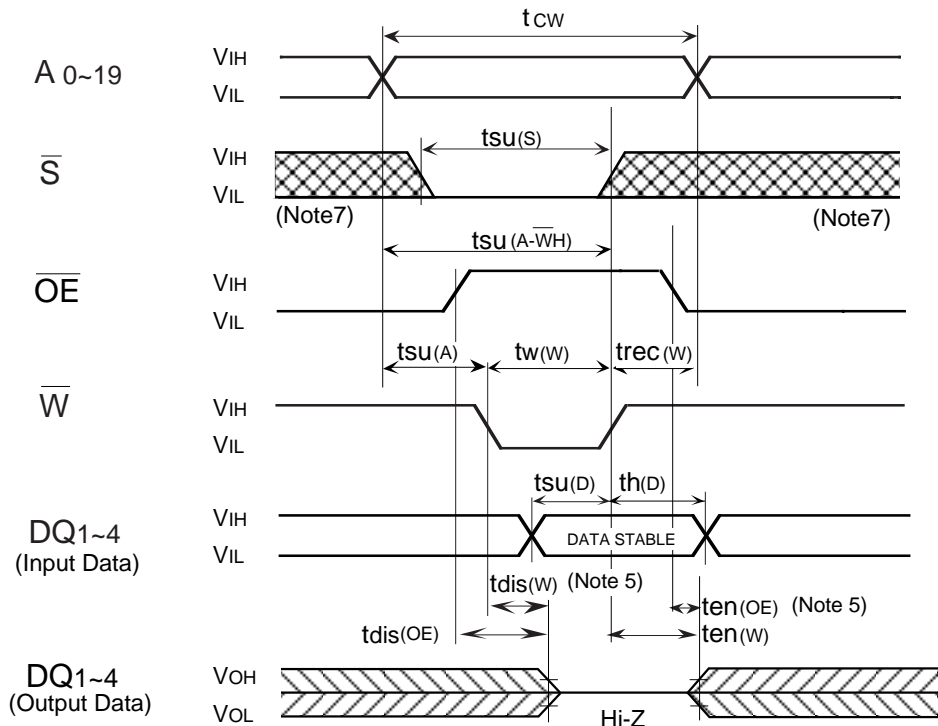
5. Transition is measured  $\pm 500\text{mV}$  from steady state voltage with specified loading in Figure 2.

Read cycle 3 (Note 6)

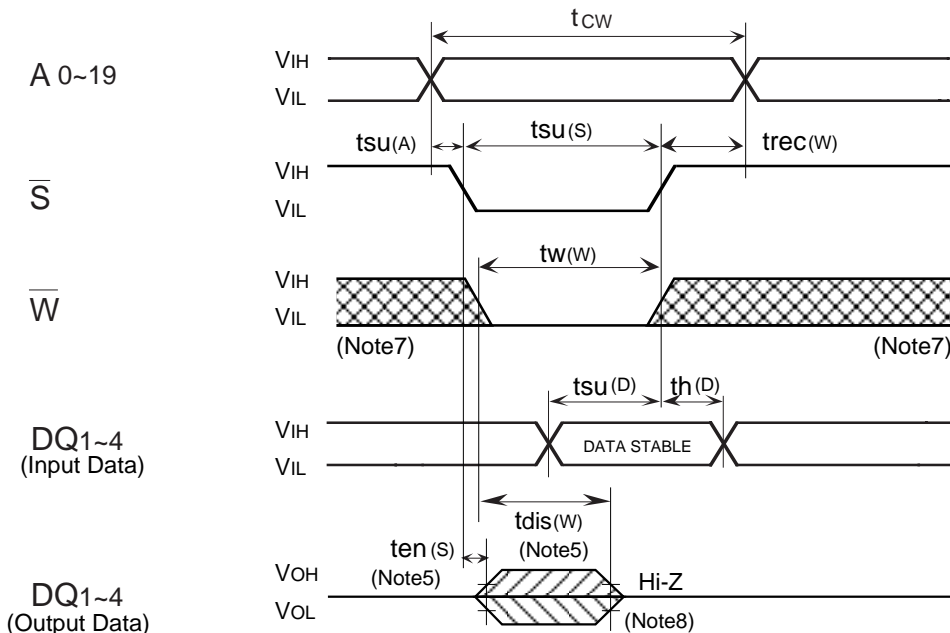


Note 6. Addresses and  $\bar{S}$  valid prior to  $\bar{OE}$  transition low by  $(t_{a(A)}-t_{a(OE)})$ ,  $(t_{a(S)}-t_{a(OE)})$

Write cycle ( $\overline{W}$  control mode)



Write cycle ( $\overline{S}$  control mode)



Note 7: Hatching indicates the state is don't care.

8: When the falling edge of  $\overline{W}$  is simultaneous or prior to the falling edge of  $\overline{S}$ , the output is maintained in the high impedance.

9:  $t_{en}$ ,  $t_{dis}$  are periodically sampled and are not 100% tested.