PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M66273FP

Ver.3.1 Dec,1999

LCD CONTROLLER with VRAM

DESCRIPTION

The M66273 is a graphic display-only controller for dot matrix type STN-LCD which is used widely for OA equipment, PDA, amusement equipment, etc.
The M66273 is an advanced product from the M66272 at the point of MPU interface and timing specifications. This LCD display functions are the same with the M66272.
It is capable of displaying six types of LCD by combining the panel configuration(single or dual scan), LCD display function(binary or gray scale), LCD display data bus width(4 or 8 bit).

Panel configuration	Binary/ gray scale	LCD display data	Displayable LCD size
Single scan	Binary	4bit	Equivalent to 640 x 240
		8bit	
	Gray scale	4bit	Equivalent to 320 x 240
		8bit	
Dual scan	Binary	4bit	Equivalent to 320 x 240 x 2 screens
	Gray scale	4bit	Equivalent to 320 x 120 x 2 screens

The M66273 can support the reflective color type LCD (ECB : Electrically Controlled Birefringence).
The IC has a built-in 19200-byte VRAM as a display data memory. All of the VRAM addresses are externally opened. Direct addressing of display data can be performed from MPU, thus display data processing such as drawing can be efficiently carried out.
The built-in arbiter circuit(cycle steal system) which gives priority to display access allows timing-free access from MPU to VRAM, preventing display screen distortion.
The IC provides has a function for LCD module built-in system by lessening connect pins between the MPU and the IC.

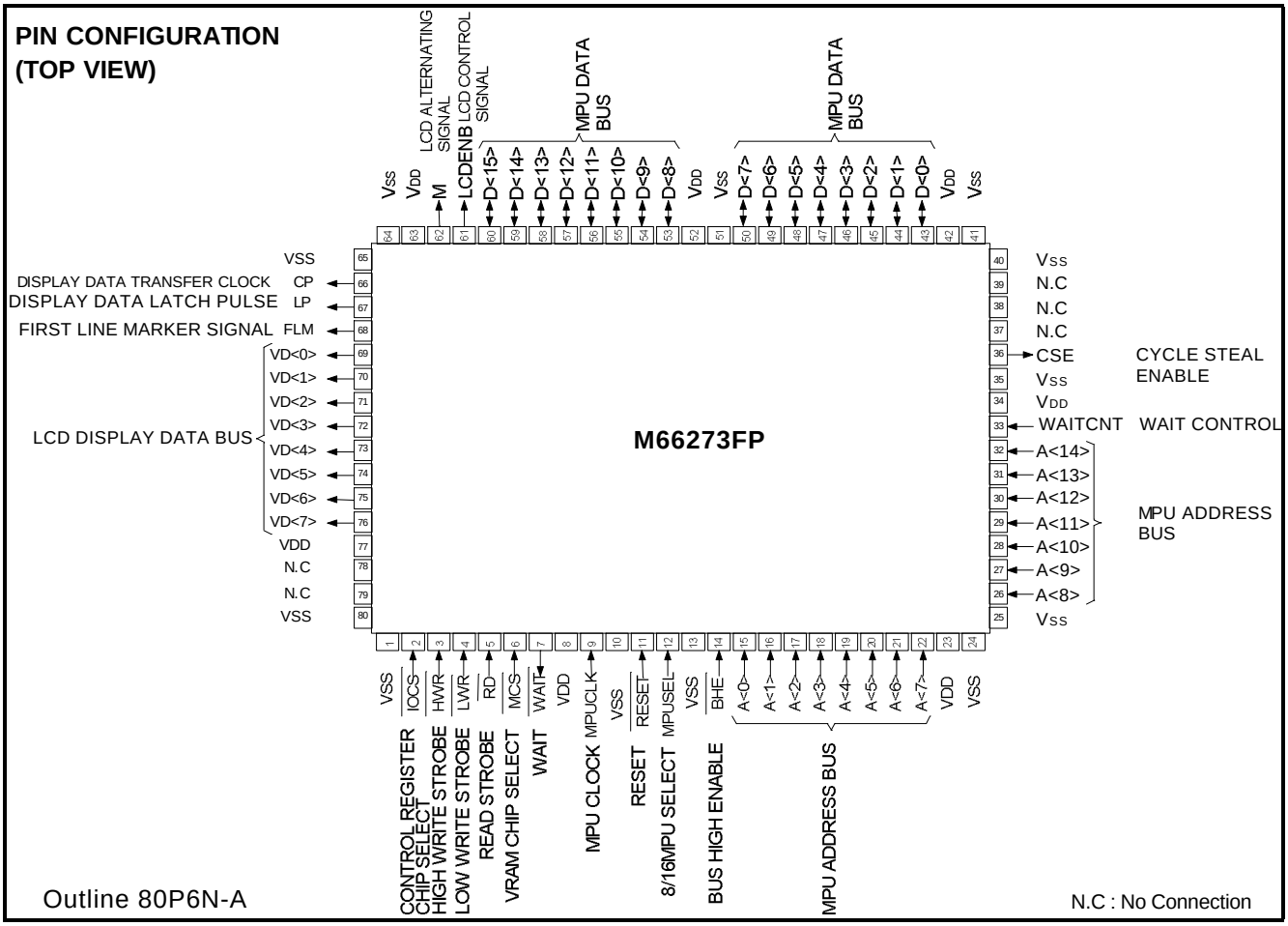
FEATURES

- Display memory
  - Built-in 19200-byte(153.6-Kbit) VRAM(Equivalent to 640 x 240 dots x 1 screen, 320 x 240 dots x 2 screens)
  - All addresses of built-in VRAM are externally opened.
- Displayable LCD
  - Binary display
    Monochrome STN-LCD of up to 153600 dots(equivalent to 1/2 VGA)
  - 4 gray scale display
    Monochrome STN-LCD of up to 76800 dots(equivalent to 1/4 VGA)
    Reflective color STN-LCD of up to 76800 dots (equivalent to 1/4 VGA)
- Interface with MPU
  - Capability of switching the interface with two-way 8/16-bit MPU
  - Provides WAIT output pin(WAIT output when access from MPU to VRAM is gained)
  - Capability of controlling $\overline{BHE}$ or $\overline{LWR}$/$\overline{HWR}$ at the interface with a 16-bit MPU
- Interface with LCD
  - LCD display data bus is a 4-bit or 8-bit parallel output.
  - 4 kinds of control signals: CP, LP, FLM and M
- Display functions
  - Graphic display only
  - Binary or 4 gray scale display(gray scale palette is used to set pseudo medium 2 gray scale.)
  - Reflective color(ECB) uses a gray scale function.
  - Vertical scrolling is allowed within memory range.
- Additional function for LCD module built-in system
  - Capability of interfacing with two-way 8/16-bit MPU(16-bit MPU byte access is not allowed.)
  - Access from MPU to VRAM is gained via the I/O register.
- 5V or 3V single power supply

APPLICATION

PPC/FAX operation panel, display/operation panel of other OA equipment, multifunction/public telephone
- PDA/electronic notebook/information terminal, portable terminal
- Game, Amusements, Kids computer, etc.

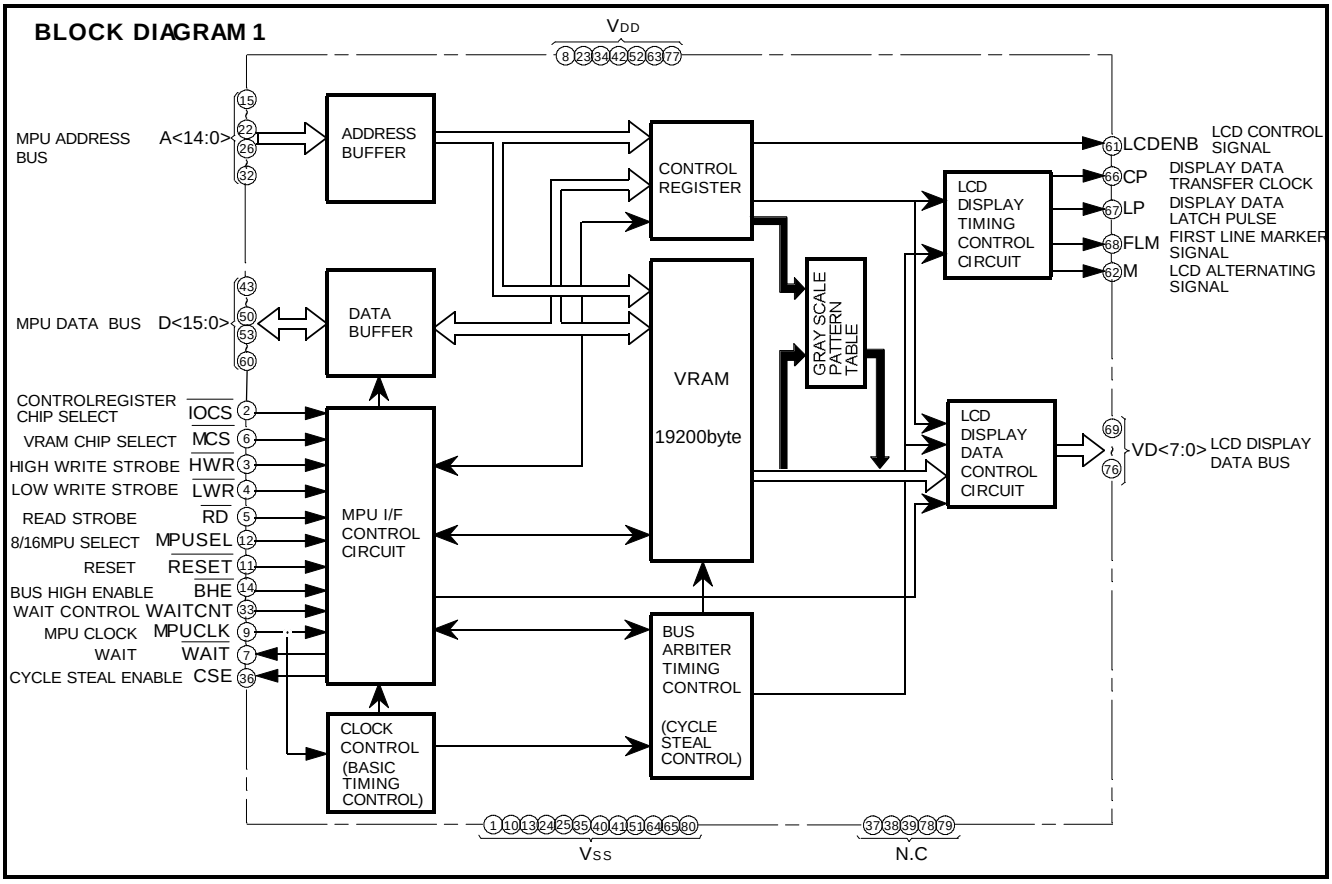
PIN CONFIGURATION (TOP VIEW)



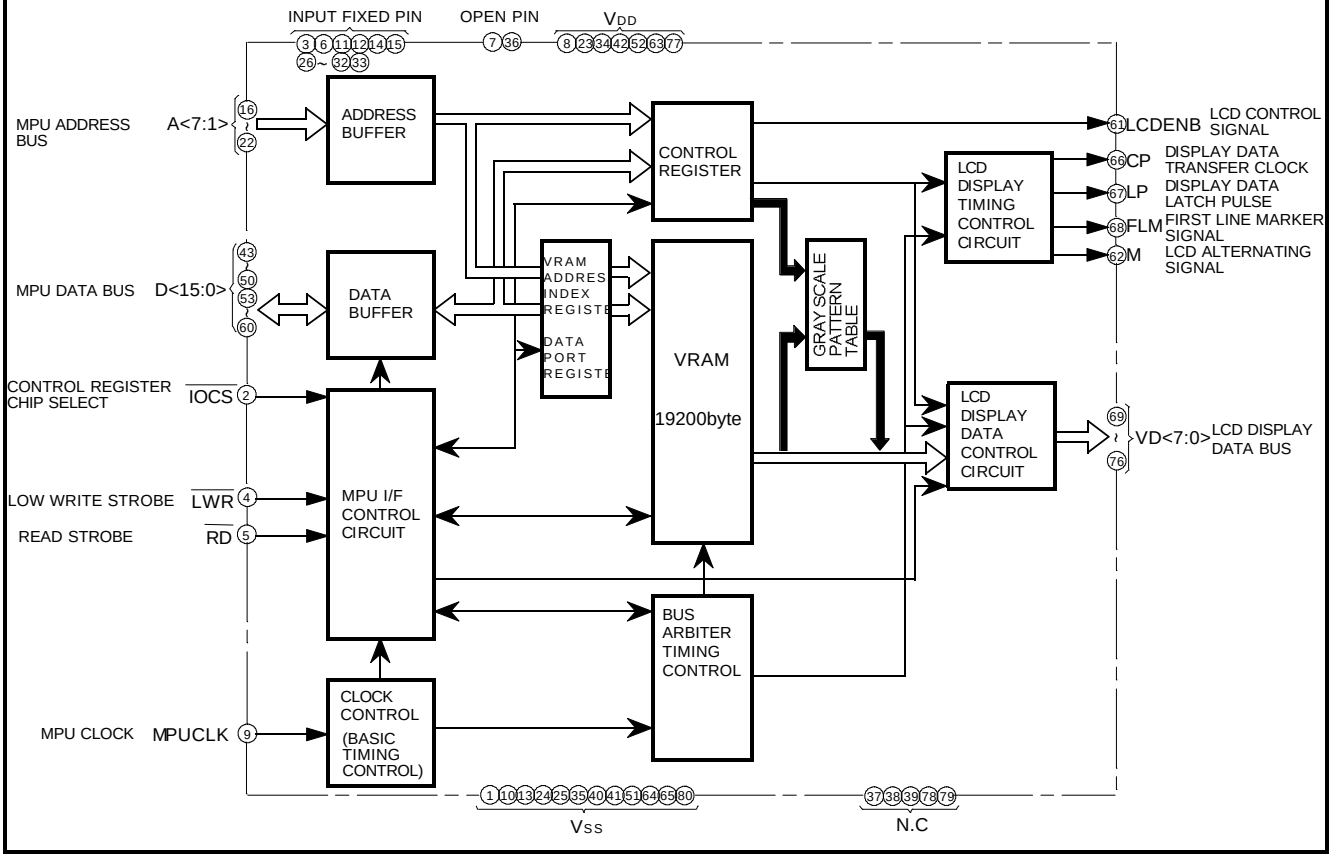
Outline 80P6N-A

N.C : No Connection

BLOCK DIAGRAM 1



BLOCK DIAGRAM 2 (When interfacing with the LCD module built-in system and having the maximum number of pins connected with MPU)



PIN DESCRIPTIONS

Item	Pin name	Input/ Output	Function	Number of pins
MPU interface	D<15:0>	Input/ Output	MPU data bus When selecting 8 bit MPU by MPUSEL input, connect D<15:8> to "V_{DD}" or "V_{SS}".	16
	A<14:0>	Input	MPU address bus When selecting 8-bit MPU, use A<14:0>. When selecting 16-bit MPU, use A<14:1> as a address bus. By combining A<0> and $\overline{BHE}$, access to internal VRAM can be gained. When driving two screens (dual scan mode), notice that the allowable setup range of VRAM address is restricted. When $\overline{IOCS}$ control use A <7:0>, and $\overline{MCS}$ control use A <14:0> for selecting address of control register.	15
	$\overline{IOCS}$	Input	Chip select input of control register When this pin is "L", select the internal control register. Assign to I/O space of MPU.	1
	$\overline{MCS}$	Input	Chip select input of VRAM / control register When this pin is "L", select the internal VRAM. Assign to memory space of MPU. And this pin can for chip select of control register. In detail, refer to "COMBINATIONS OF CONTROL INPUT PINS ON THE MPU INTERFACE" and "CONTROL REGISTER".	1
	$\overline{HWR}$	Input	High-Write strobe input When this pin is "L", write data to the internal VRAM. $\overline{HWR}$ is valid only in using 16-bit MPU controlled byte access by $\overline{LWR}$ and $\overline{HWR}$.	1
	$\overline{LWR}$	Input	Low-Write strobe input When this pin is "L", write data to the internal control register or VRAM.	1
	$\overline{RD}$	Input	Read strobe input When this pin is "L", read data from the internal control register or VRAM.	1
	MPUSEL	Input	8/16-bit MPU select input According to MPU, set "V_{SS}" for 8-bit MPU and set "V_{DD}" for 16-bit MPU.	1
	$\overline{RESET}$	Input	Reset input Use reset signal of MPU. When this pin is "L", initialize (reset) all internal control registers and counters.	1
	MPUCLK	Input	MPU clock Input system clock output from MPU.	1
	$\overline{BHE}$	Input	Bus-High-Enable input This pin is valid when using 16-bit MPU controlling byte access with A<0> and $\overline{BHE}$. Connect to "V_{DD}" to select 8-bit MPU.	1
	WAITCNT	Input	Wait control input This pin is used for controlling $\overline{WAIT}$ output timing when requested access from MPU to VRAM. Use this pin, when it is necessary to output $\overline{WAIT}$ earlier than the timing of falling edge of overlapping with $\overline{MCS}$ and $\overline{RD}$ or $\overline{LWR}$ and $\overline{HWR}$. And then connect AS, ALE or etc of MPU. Connect WAITCNT to "VDD" or "VSS", when it is necessary to output $\overline{WAIT}$ at the timing of falling edge of overlapping with $\overline{MCS}$ and $\overline{RD}$ or $\overline{LWR}$ and $\overline{HWR}$.	1
	$\overline{WAIT}$	Output	$\overline{WAIT}$ output for MPU This signal makes $\overline{WAIT}$ for MPU. In case of fixed WAITCNT input("V_{SS}" or "V_{DD}")change $\overline{WAIT}$ to "L" at the timing of falling edge of overlapping with $\overline{MCS}$ and $\overline{RD}$ or $\overline{LWR}$ and $\overline{HWR}$. And in case of using WAITCNT input, change $\overline{WAIT}$ to "L" at timing of falling edge of WAITCNT on $\overline{MCS}$ = "L". And $\overline{WAIT}$ output return to "H" at synchronization with the rising edge of MPUCLK after internal processing. (Output $\overline{WAIT}$ only when requested access from MPU to VRAM is gained during cycle steal access.)	1
	CSE	Output	Cycle Steal Enable output State output of internal cycle steal access.	1

PIN DESCRIPTIONS

Item	Pin name	Input/ Output	Function	Number of pins
LCD interface	VD<7:0>	Output	Display data bus for LCD Transfer the LCD display data in synchronization with a rising edge of CP by putting 4-bit or 8-bit in parallel. The VD<n:0> output pin in use differs depending on the number of driven screens and the display mode.	8
	CP	Output	Display data transfer clock Shift clock for the transfer of display data to LCD. Take the display data of VD<n:0> to LCD at falling edge of CP.	1
	LP	Output	Display data latch pulse This clock use both as the latch pulse of display data for LCD and the transfer of scanning signal. LP is output when it finishes transferring display data of a line. Latch of display data and the transfer of scanning signal at falling edge of LP.	1
	FLM	Output	First Line Marker signal output Output the start pulse of scanning line. This signal is "H" active, the IC for driving scanning line catches FLM at falling edge of LP.	1
	M	Output	LCD alternating signal output Signal for driving LCD by alternating current.	1
	LCDENB	Output	LCD (ON/OFF) control signal output Output data which is set at bit "0" of mode register (R1) in the control register. This signal can be used for controlling the LCD power supply, because LCDENB is set to "L" by RESET.	1
Others	V_{DD}	——	Power supply pin	7
	V_{SS}	——	Ground	7
	N.C	——	No connection	10

DIFFERENCE BETWEEN M66273FP AND M66272FP

The M66273FP is an advanced product from the M66272FP at the point of MPU interface and timing specifications.
LCD display functions are the same with the M66272FP.
The following shows difference between the M66273FP and the M66272FP without timing specifications.
Refer to the later item about timing specifications and detail specifications.

Specification	M66273FP	M66272FP
Pin function	WAITCNT input ($\overline{WAIT}$ control input)	SWAP input (Bus swap input)
$\overline{WAIT}$ output control	It is capable of selecting $\overline{WAIT}$ output trigger input. In case of fixed WAITCNT input, change $\overline{WAIT}$ to "L" at the timing of the falling edge of overlapping with $\overline{MCS}$ and $\overline{RD}$ or $\overline{LWR}$/$\overline{HWR}$, and in case of using WAITCNT input, change $\overline{WAIT}$ to "L" at the timing of the falling edge of WAITCNT on $\overline{MCS}$="L".	$\overline{WAIT}$ output change to "L" at the timing of the falling edge of overlapping with $\overline{MCS}$ and $\overline{RD}$ or $\overline{LWR}$/$\overline{HWR}$.
Access to control register	Use $\overline{IOCS}$ or $\overline{MCS}$ pins for chip select of control register. (capable of controlling VRAM and control register by $\overline{MCS}$ pin.)	Use $\overline{IOCS}$ pin for chip select of control register.
Bus swap function	Set by SWAP register.	Set by SWAP pin.

OUTLINE

The M66273 is a graphic display only controller for displaying a dot matrix type STN-LCD.

· LCD display mode
It is capable of displaying six types of LCD by combining the panel configuration, binary/gray scale, LCD display data bus width.

Display mode	Panel configuration	Binary/ gray scale	LCD display data	Displayable LCD size
①	Single scan	Binary	4bit	Equivalent to 640 x 240
②			8bit	
③		Gray scale	4bit	Equivalent to 320 x 240
④			8bit	
⑤	Dual scan	Binary	4bit	Equivalent to 320 x 240 x 2 screens
⑥		Gray scale	4bit	Equivalent to 320 x 120 x 2 screens

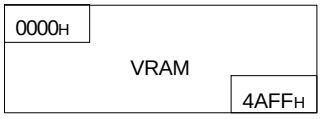
· Control register
When accessing the control register from MPU, use pins IOCS, LWR, RD, A<7:0> and D<7:0>, or MCS, LWR, RD,A<14:0> and D<7:0> (However, use D<15:0> only when 16-bit MPU controls the LCD module built-in support function.)
Refer to Table-1, setting of control input.

The IC contains the following registers as control registers.

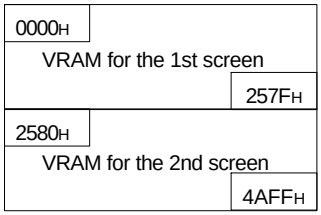
Operation control	R1 to R11
Supporting LCD module built-in type	R12 to 14 or R15 to 16
Gray scale pattern table	R17 to R80

· VRAM
This IC has a built-in 19200-byte VRAM which is equivalent to two screens of 320 x 240 dots LCD.
When accessing VRAM from MPU, use pins MCS, HWR, LWR, RD, BHE, A<14:0> and D<15:0>.
Use of MPUSEL input can support both 8/16 bit MPU.
Refer to table-2 to 6, VRAM specifications for 8/16 bit MPU and input setting in access.
The VRAM address settable range is restricted depending on the panel configuration, as follows.

VRAM address settable range
· When single scan mode
·A<14:0>=0000 to 4AFF$_H$ --- 19200 byte



· When dual scan mode
·For the 1st screen --- A<14:0>=0000 to 257F$_H$ --- 9600 byte
·For the 2nd screen --- A<14:0>=2580 to 4AFF$_H$ --- 9600 byte



· Cycle steal system
Cycle steal system is interact method of transforming display data for LCD from VRAM and accessing VRAM from MPU on the basic cycle (MAINCLK) of internal operation.
Basic timing is two clocks of MAINCLK, and assign first clock to the access from MPU to VRAM and second clock to the transfer of display data from VRAM to LCD.

In accessing VRAM from MPU, output WAIT. In case of fixed WAITCNT input, change WAIT to "L" at the timing of the falling edge of overlapping with MCS and RD or LWR / HWR,and in case of using WAITCNT input, change WAIT to "L" at the timing of the falling edge of WAITCNT on MCS="L", And return to "H" at synchronizing with rising edge of MPUCLK after internal processing.
For the cycle steal system, this IC provides a cycle steal control function to improve data transfer efficiency in a line. This func-tion gains access with the cycle steal system by taking WAIT for MPU during the display term with necessity for the display data transfer from built-in VRAM to LCD. On the other side, it does not output WAIT for keeping throughput of MPU during horizontal synchronous term (idle running term) with no necessity for the display data transfer from VRAM to LCD side.
In detail,refer to "Description of cycle steal".

· Output to LCD side
LCD display data VD<7:0> is output in parallel per 4 bits or 8 bits in synchronization with the rising edge of CP.
Pin VD<n:0> differs depending on the display mode.

Single scan		Dual scan
4-bit transfer	8-bit transfer	4-bit transfer
		VD<7:4>
VD<3:0>	VD<7:0>	VD<3:0>

Display mode ①③ ②④ ⑤⑥

When display data for a line has been sent, LP outputs data in synchronization with the falling edge of MAINCLK.
The IC enables adjustment to an optimum value of the frame frequency as requested from the LCD PANEL side by adjusting pulse width of LP with the LPW register value.
FLM is output when the display data for the first line has been sent.
M output is an LCD alternating signal for driving LCD with alternating current.
M output cycles can be set in lines with the M output cycle variable register and is available to prevent LCD from deterioration.

· Gray scale display function
Gray scale display can assign 2-bit VRAM data to a picture element of LCD display to show the display density at four levels.
Gray scale display pattern tables 0 and 1 (4 x 4 matrix x 16 patterns x 2 medium gray scale), consisting of SRAM of 64 bytes in total, can set any gray scale display pattern.
In detail,refer to "Description of gray scale function".

· Application to reflective color type LCD
The above gradation display function is available to control about four display colors on the reflective color type LCD with ECB (Electrically Controlled Birefringence).

COMBINATIONS OF CONTROL INPUT PINS ON THE MPU INTERFACE

Tables 1 to 6 show input setting conditions for access to the control register and VRAM from the MPU side.

(1) Access to the control register

For data, D<7:0> is used.

(Only when 16bit MPU is used to control the LCD module built-in system, D<15:0> is used for data.)

Table-1

$\overline{IOCS}$	$\overline{MCS}$	$\overline{LWR}$	$\overline{RD}$	A<14:0>	Operation	
L	H	L	H	0000H to 009EH	$\overline{IOCS}$ control	Writes to control register
L	H	H	L	0000H to 009EH		Reads from control register
H	L	L	H	5000H to 509EH	$\overline{MCS}$ control	Writes to control register
H	L	H	L	5000H to 509EH		Reads from control register
H	H	X	X	——	Invalid	

(2) Write to VRAM

(2-1) For use of 8bit MPU (Set as follow: MPUSEL="L", $\overline{BHE}$=$\overline{HWR}$="H")

Table-2

MPU SEL	$\overline{MCS}$	$\overline{BHE}$	A<0>	$\overline{HWR}$	$\overline{LWR}$	Odd address	Even address	Valid data bus width for MPU
L	L	H	L	H	L	Invalid	Write	8bit
			H			Write	Invalid	
			X		H	Invalid	Invalid	
	H		X		X			

(2-2) For use of 16bit MPU - 1 (For MPU controlling byte access with A<0> and $\overline{BHE}$, set as follow: MPUSEL=$\overline{HWR}$="H")

Table-3

MPU SEL	$\overline{MCS}$	$\overline{BHE}$	A<0>	$\overline{HWR}$	$\overline{LWR}$	Upper byte	Lower byte	Valid data bus width for MPU
H	L	L	L	H	L	Write	Write	16bit
					H	Invalid	Invalid	
			H		L	Write	Invalid	Upper 8bit
					H	Invalid	Invalid	
		H	L		L	Invalid	Write	Lower 8bit
					H	Invalid	Invalid	
			H		L			
					H			
	H	X	X		X			

(2-3) For use of 16bit MPU - 2 (For MPU controlling byte access with $\overline{LWR}$ and $\overline{HWR}$, set as follow: MPUSEL=$\overline{BHE}$="H", A<0>="L")

Table-4

MPU SEL	$\overline{MCS}$	$\overline{BHE}$	A<0>	$\overline{HWR}$	$\overline{LWR}$	Upper byte	Lower byte	Valid data bus width for MPU
H	L	H	L	L	L	Write	Write	16bit
					H	Write	Invalid	Upper 8bit
				H	L	Invalid	Write	Lower 8bit
					H	Invalid	Invalid	
	H			X	X			

(3) Read from VRAM

(3-1) For use of 8bit MPU (Set as follows: MPUSEL="L", $\overline{BHE}$="H")

Table-5

MPU SEL	$\overline{MCS}$	$\overline{BHE}$	A<0>	$\overline{RD}$	Odd address	Even address	Valid data bus width for MPU
L	L	H	L	L	Invalid	Read	8bit
			H		Read	Invalid	
			X	H	Invalid	Invalid	
	H			X			

(3-2) For use of 16bit MPU (Set as follow: MPUSEL="H")

Table-6

MPU SEL	$\overline{MCS}$	$\overline{BHE}$	A<0>	$\overline{RD}$	Upper byte	Lower byte	Valid data bus width for MPU
H	L	X	X	L	Read	Read	16bit
				H	Invalid	Invalid	
	H			X			

Notes : Combinations except for the above cause malfunction. Be sure to make settings according to the above combinations.
: X=either "L" or "H"

CONTROL REGISTER

M66273 is equipped with 80 types of built-in control registers.

For operation control	R1 to R11
Only for LCD module built-in system	R12 to R14, or R15 to R17
For gradation pattern table	R17 to R80

$\overline{IOCS}$, $\overline{LWR}$, $\overline{RD}$, A<7:0> and D<7:0>, or $\overline{MCS}$, $\overline{LWR}$, $\overline{RD}$, A<14:0> and D<7:0> are used for setting from the MPU to control register. And for address in $\overline{IOCS}$ control,use A<7:0>=00H to 9EH,and in $\overline{MCS}$ control, use A<14:0>=5000H to 509EH.
(However, D<15:0> is to be used only when registers R15 and R16 only for LCD module built-in system are used.)

(1) Types of control registers

· List of registers for operation control

No.	Name	Address ($\overline{IOCS}$ control) A<7:0>	Address ($\overline{MCS}$ control) A<14:0>	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Reset
R1	Basic operation mode	00H	5000H	RESET	IDXON	←	DIV	→	DISP	REV	LCDE	R/W	00H
R2	LCD output mode	02H	5002H			WAITC	SWAP		DUAL	GRAY	4/8	R/W	00H
R3	Number of horizontal display characters	04H	5004H	←			CR				→	W	28H
R4	Horizontal synchronous pulse width	06H	5006H	←			LPW				→	W	04H
R5	Cycle steal enable width	08H	5008H	←			CSW				→	W	02H
R6	Number of vertical lines	0AH	500AH	←			SLT				→	W	78H
R7	1st screen display start address	0CH	500CH	←			SA1L				D0 0	R/W	00H
R8		0EH	500EH		←		SA1H				→		00H
R9	2nd screen display start address	10H	5010H	←			SA2L				D0 0	R/W	80H
R10		12H	5012H		←		SA2H				→		25H
R11	M output frequency variable	14H	5014H	←			MT				→	W	00H

· List of registers only for LCD module built-in type support function
(For 8bit MPU only)

R12	VRAM address index	16H	5016H	←			IDX8L				→	R/W	00H
R13		18H	5018H		←		IDX8H				→		00H
R14	Data port	1AH	501AH	←			DP8				→	R/W	Undetermined

(For 16bit MPU only)

No.	Name	Address ($\overline{IOCS}$ control) A<7:0>	Address ($\overline{IOCS}$ control) A<14:0>	D15							D0	R/W	Reset
R15	VRAM address index	1CH	501CH		D14	←	IDX16			D1	D0 0	R/W	0000H
R16	Data port	1EH	501EH	D15	←		DP16				D0 →	R/W	Undetermined

· List of registers for gray scale pattern table

No.	Name	Address ($\overline{IOCS}$ control) A<7:0>	Address ($\overline{IOCS}$ control) A<14:0>	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Reset
R17	Gray scale pattern 0-1	20H	5020H	←		FRC0-1-2		→	←		FRC0-1-1	→	
R18	Gray scale pattern 0-2	22H	5022H	←		FRC0-1-4		→	←		FRC0-1-3	→	
to	to	to	to			to				to		R/W	Undetermined
R47	Gray scale pattern 0-31	5CH	505CH	←		FRC0-16-2		→	←		FRC0-16-1	→	
R48	Gray scale pattern 0-32	5EH	505EH	←		FRC0-16-4		→	←		FRC0-16-3	→	
R49	Gray scale pattern 1-1	60H	5060H	←		FRC1-1-2		→	←		FRC1-1-1	→	
R50	Gray scale pattern 1-2	62H	5062H	←		FRC1-1-4		→	←		FRC1-1-3	→	
to	to	to	to			to				to		R/W	Undetermined
R79	Gray scale pattern 1-31	9CH	509CH	←		FRC1-16-2		→	←		FRC1-16-1	→	
R80	Gray scale pattern 1-32	9EH	509EH	←		FRC1-16-4		→	←		FRC1-16-3	→	

(2) Description of registers

Address is listed for $\overline{ICOS}$ control. Incase of $\overline{MCS}$ control,set to address adding 50H to upper 7 bit (50**H).

[R1] Basic operation mode

Set the Basic operation mode

Address	R/W	Function	Restriction	Reset
00H	R/W	D7 RESET: 0 Reset OFF; 1 Reset ON ·Software reset.	·Surely return to reset off after reset on. And then, can't set another bits (D6 to D0) at the same time.	0
		D6 IDXON: 0 Index mode OFF; 1 Index mode ON ·Set to decide whether or not the function only for LCD module built-in system is used. ·Set Index mode OFF for reset.		0
		DIV D5 D4 D3 / Division of MPUCLK input: 0 0 0 1; 0 0 1 1/2 division; 0 1 0 1/4 division; 0 1 1 1/8 division; 1 0 0 1/16 division ·Set the division of MPUCLK input to set the reference clock cycle (MAINCLK) for internal operation. ·Resetting does not divide MPUCLK.	·Don't set except for the settings in the table at left.	000
		D2 DISP: 0 Display OFF; 1 Display ON ·Control display ON/OFF of LCD. ·In the reverse mode with REV (D1) set to "1", "1" is output to display data VD<n:0> with DISP="0". ·Reset sets display OFF.		0
		D1 REV: 0 Normal display; 1 Reverse display ·Controls normal/reverse of LCD display. ·Resetting sets normal display.		0
		D0 LCDE: 0 LCDENB="0"output; 1 LCDENB="1"output ·Sets the data output from the LCDENB output pin. ·Resetting outputs "0" (Vss potential) to the LCDENB output pin. ·This function is prepared for controlling the apply voltage to LCD. When the power supply is turned ON after registers have been completely set, set this LCDE to "1" to apply the LCD voltage. Conversely for turning OFF the power supply to the system, set the LCDE to "0" to turn OFF the LCD voltage. This prevents abnormal DC voltage from being applied to the LCD. This function depends on the LCD functions. Use the function, if necessary.		0

[R2] MPUI/LCD mode

Set the display data output mode on the LCD side.

Address	R/W	Function	Restriction	Reset
02H	R/W	D7 , D6 are not used. ·To read R2, "0" is output to D7 , D6.		0
		D5 = 0: $\overline{MCS}$ and $\overline{RD}$ or $\overline{H}/\overline{LWR}$ control; D5 = 1: WAITCNT control ·Set to select trigger signal of $\overline{WAIT}$ output. ·When setting WAITC to "0", change $\overline{WAIT}$ to "L" at timing of falling edge of overlapping with $\overline{MCS}$ and $\overline{RD}$ or $\overline{LWR}$ and HWR. And return to "H" at synchronization with the rising edge of MPUCLK offer internal processing. ·When setting WAITC to "T", change $\overline{WAIT}$ to "L" at timing of falling edge of WAITCNT on $\overline{MCS}$="L".And return to "H" at synchronization with rising edge of MPUCLK after internal processing. ·Output $\overline{WAIT}$ only when requested access from MPU to VRAM is gained during cycle steal access. ·Resetting set WAITC ="0".	·set when register is initialized. ·When setting to "0",connect WAITCNT input to V_{SS} or V_{DD}.	0
		D4: 0 = Order of upper/lower byte; 1 = Order of lower/upper byte ·When selecting 16 bit MPU, set SWAP to "0" to transfer VD<n:0> in order of Upper/Lower byte of MPU data bus,reversally set to "1" in order of Lower/Upper byte. ·When selecting 8 bit MPU, set to "0" ·Even if setting to "1", use D<7:0> to access to register of 8 bit width. ·Resetting set SWAP="0".	·set when register is initialized.	0
		D3 is not used. ·To read R2, "0" is output to D3.		0
		D2: 0 = 1 screen driving panel; 1 = 2 screen driving panel ·Set the LCD panel configuration. ·Resetting sets the 1 screen driving panel.	·set when register is initialized.	0
		D1: 0 = Binary display mode; 1 = Gray scale display mode ·Set the LCD display mode (binary or gray scale). ·Resetting sets the binary display mode.	·set when register is initialized.	0
		D0: 0 = 4bit transfer; 1 = 8bit transfer ·Set the transfer path width of the LCD display data path VD<n:0>. ·Resetting sets 4bit transfer.	·set when register is initialized.	0

[R3] Number of horizontal display characters

Address	R/W	Function	Restriction	Reset
04H	W	CR D7 to D0 / Number of characters / Number of LCD display dots: Binary display / Gray scale display 00H — — — 01H 1 8 4 02H 2 16 8 ↓ ↓ ↓ ↓ FFH 255 2040 1020 ·Sets the number of hori-zontal display characters per line. ·Resetting sets "28H" (=40 characters).	·For CR, maximum of 255 characters can be set. ·In display modes ② ③,④and⑥, the number of even cha-racters can be set.	28H

(Note) Definition of the number of characters
The number of display characters means data corresponding to 1byte of VRAM.
One character : In the case of binary, one character means 8dots of LCD display.
In the case of gray scale display, one character means 4dots of LCD display (because 2bits of VRAM corresponds to 1dot of LCD display).

[R4] Horizontal synchronous pulse width

Address	R/W	Function	Restriction	Reset
06H	W	LPW D7 to D0 / Number of characters 00H — 01H — 02H 2 ↓ ↓ FFH 255 ·In the unit of characters, set the width of horizontal synchronous pulse generated per line. Horizontal synchronous pulse is output from the LP pin and is used for serial/parallel conversion of displayed data. Adjustment of LPW can set the frame frequency to an optimum value. The LP output pulse actually generated takes the value(LPW setup value - 2CP), taking into account the CP output timing. Only in the case of display mode ④ however, the LP output pulse takes the value (LPW set value - 1CP). ·Resetting sets "04H" (= 4 characters).	·In display modes ② ,③, ④ and ⑥, only the number of even characters can be set. ·In display modes ①and ⑤ , set LPW to 02H or more. ·In display modes ② ,③, ④and⑥, set LPW to 04H or more.	04H

[R5] Cycle steal enable width

Address	R/W	Function	Restriction	Reset
08H	W	CSW D7 to D0 / Number of characters 00H — 01H 1 02H 2 ↓ ↓ FFH 255 ·In unit of characters, set the period of access by the cycle steal system near the end of the horizontal synchronous portion set with LPW. ·With CSW=LPW, gain access by the permanent cycle steal system. ·Resetting sets "02H" (=2 characters).	·Set CSW to the LPW set value or less. ·In display modes ② ③, ④ and ⑥ , only the number of even characters can be set. ·In display modes ①and ⑤ ,set CSW to 01H or more. ·In display modes ②, ③, ④ and⑥ , set CSW to 02H or more.	02H

[R6] Number of vertical lines

Address	R/W	Function	Restriction	Reset
0AH	W	SLT D7 to D0 / Number of vertical lines 00H — 01H 2 02H 4 ↓ ↓ FFH 510 ·Sets the number of lines displayed in the direction of LCD vertical line. ·SLT also sets the LCD display driving duty. ·In dual scan mode, the actual number of displayed lines is given by SLT x 2 screens. ·Resetting sets "78H" (=240 lines).	·Be sure to set SLT ac-cording to the number of LCD display lines. ·For SLT, a maximum of 510 even lines can be set.	78H

[R7, R8] 1st screen display start address

Address	R/W	Function	Restriction	Reset
0CH (SA1L) 0EH (SA1H)	R/W	SA1H D7 / SA1H D6 to D0 / SA1L D7 to D0 / 1st screen display start address 00H / 00H / 0000H 00H / 02H / 0002H 00H / 04H / 0004H ↓ / ↓ / ↓ 4AH / FEH / 4AFEH ·Sets the 1st screen display start address. ·The display start address is determined by writing data into SA1H. ·Reading SA1H outputs "0" to D7. ·Resetting sets "0000H".	·At the display start add-ress, even addresses can only be set. · For single scan; 0000H to 4AFEH · For dual scan; Sets 0000H to 257EH. Settings except for the above must not be made. ·To modify the display start address, be sure to respecify in order of SA1L-SA1H even when only SA1L is modified.	00H 00H

[R9, R10] 2nd screen display start address

Address	R/W	Function	Restriction	Reset
10H (SA2L) 12H (SA2H)	R/W	SA2H D7 / SA2H D6 to D0 / SA2L D7 to D0 / 2nd screen display start address 25H / 80H / 2580H 25H / 82H / 2582H 25H / 84H / 2584H ↓ / ↓ / ↓ 4AH / FEH / 4AFEH ·Used for dual scan mode only to set the 2nd screen display start address. ·The display start address is determined by writing data into SA2H. ·Reading SA2H outputs "0" to D7. ·Resetting sets "2580H".	·At the display start add-ress, only even addre-sses can be set, and; ·Can set 2580H to 4AFEH. Settings except for the above must not be made. ·To modify the display start address, be sure to respecify in order of SA2L - SA2H even when only SA2L is modified.	80H 25H

[R11] M output cycle variable

Address	R/W	Function	Restriction	Reset
14H	W	MT D7 to D0 / Output cycle of M signal 00H / Makes toggle change every frame. 01H / Makes toggle change every line (=1LP). 02H / Makes toggle change every 2 lines. ↓ / ↓ FFH / Makes toggle change every 255 lines. ·Sets the output cycle of M signal output from the M terminal. With MT=01H, for example, M signal repeatedly reverses (toggles) every line. ·Resetting sets "00H". ·It is recommended to set this register to an optimum value according to the LCD specification.		00H

[R12, R13] VRAM address index (8bit MPU only)

Address	R/W	Function	Restriction	Reset
16H (IDX8L) 18H (IDX8H)	R/W	IDX8H: D7 = 0, D6 to D0 = 00H; IDX8L: D7 to D0 = 00H; VRAM address to access = 0000H IDX8H: D7 = 0, D6 to D0 = 00H; IDX8L: D7 to D0 = 01H; VRAM address to access = 0001H IDX8H: D7 = 0, D6 to D0 = 00H; IDX8L: D7 to D0 = 02H; VRAM address to access = 0002H ↓ ↓ ↓ IDX8H: D7 = 0, D6 to D0 = 4AH; IDX8L: D7 to D0 = FFH; VRAM address to access = 4AFFH ·VRAM address index register only for LCD module built-in system. Sets the VRAM address to access. ·Since IDX8H and IDX8L are independent from each other, either one of the register values can also be set and modified. In addition, automatic increments are made for consecutive addresses. ·Reading IDX8H outputs "0" to D7. ·Resetting sets "0000H".	·VRAM addresses to access can be set to 0000H to 4AFFH. Settings except for the above must not be made.	00H 00H

[R14] Data port (8bit MPU only)

Address	R/W	Function	Restriction	Reset
1AH	R/W	DP8 / D7 to D0: Data port (8bit) ·Data port register only for LCD module built-in type support additional functions. Via this register, 8bit data is read/written between MPU and VRAM. ·Completion of access to DP8 increments the IDX8H and IDX8L values by +1. · Resetting outputs undetermined data.		XXH (Undetermined)

[R15] VRAM address index (16bit MPU only)

Address	R/W	Function	Restriction	Reset
1CH	R/W	IDX16: D15 = 0, D14 to D0 = 0000H; VRAM address to access = 0000H IDX16: D15 = 0, D14 to D0 = 0002H; VRAM address to access = 0002H IDX16: D15 = 0, D14 to D0 = 0004H; VRAM address to access = 0004H ↓ ↓ ↓ IDX16: D15 = 4AFEH; VRAM address to access = 4AFEH ·VRAM address index register only for LCD module built-in type support addi-tional functions. Sets the VRAM address to access. ·Automatically incremented for consecu-tive addresses. ·Reading IDX16 outputs "0" to D15. ·Resetting sets "0000H".	·VRAM address to ac-cess can be set to 0000H to 4AFEH. Settings except for the above must not be made. ·Set the VRAM address with D<14:1> and fix it to D<0>=0.	0000H

Note : With SWAP="1" set, set the byte-swapped data for the VRAM address to access.
(Set low order bytes of VRAM address to D<15:8> and set high order bytes of VRAM address to D<7:0>.)

[R16] Data port (16bit MPU only)

Address	R/W	Function	Restriction	Reset
1EH	R/W	DP16 / D15 to D0: Data port (16bit) ·Data port register only for LCD module built-in type support additional functions. Via this register, 16bit data is read/ written between MPU and VRAM. ·Completion of access to DP16 incre-ments the IDX16 value by +1. ·Resetting outputs undetermined data.		XXXXH (Undetermined)

Note : Registers R12 to R16 are used only for LCD module built-in system.
Register setting is not needed if these functions are not used.

[R17 to R80] Gradation patterns 0-1 to 32 and 1-1 to 32

<table>
<tr><th>Address</th><th>R/W</th><th>Function</th><th>Restriction</th><th>Reset</th></tr>
<tr><td>20H
to
5EH</td><td>R/W</td><td>
<table>
<tr><th colspan="2">Register</th><th>Address</th><th colspan="2">Data</th></tr>
<tr><th>No.</th><th>Name</th><th>A<7:0></th><th>D7 to D4</th><th>D3 to D0</th></tr>
<tr><td>R17</td><td>Gray scale pattern 0-1</td><td>20H</td><td>FRC0-1-2</td><td>FRC0-1-1</td></tr>
<tr><td>R18</td><td>Gray scale pattern 0-2</td><td>22H</td><td>FRC0-1-4</td><td>FRC0-1-3</td></tr>
<tr><td>to</td><td>to</td><td>to</td><td>to</td><td>to</td></tr>
<tr><td>R47</td><td>Gray scale pattern 0-31</td><td>5CH</td><td>FRC0-16-2</td><td>FRC0-16-1</td></tr>
<tr><td>R48</td><td>Gray scale pattern 0-32</td><td>5EH</td><td>FRC0-16-4</td><td>FRC0-16-3</td></tr>
</table>
·Sets data of gradation pattern 0.
Gradation pattern 0 provides 16 patterns of 4 x 4 matrix.
</td><td rowspan="2">·Set gradation patterns when the register is initialized.
·When access to R17 to R80, must be set DISP=OFF.
Can't access to R17 to R80 on DISP=ON.
·All registers R17 to R80 must be set.</td><td>XXH
(Undeter-
mined)</td></tr>
<tr><td>60H
to
9EH</td><td>R/W</td><td>
<table>
<tr><th colspan="2">Register</th><th>Address</th><th colspan="2">Data</th></tr>
<tr><th>No.</th><th>Name</th><th>A<7:0></th><th>D7 to D4</th><th>D3 to D0</th></tr>
<tr><td>R49</td><td>Gray scale pattern 1-1</td><td>60H</td><td>FRC1-1-2</td><td>FRC1-1-1</td></tr>
<tr><td>R50</td><td>Gray scale pattern 1-2</td><td>62H</td><td>FRC1-1-4</td><td>FRC1-1-3</td></tr>
<tr><td>to</td><td>to</td><td>to</td><td>to</td><td>to</td></tr>
<tr><td>R79</td><td>Gray scale pattern 1-31</td><td>9CH</td><td>FRC1-16-2</td><td>FRC1-16-1</td></tr>
<tr><td>R80</td><td>Gray scale pattern 1-32</td><td>9EH</td><td>FRC1-16-4</td><td>FRC1-16-3</td></tr>
</table>
·Sets data of gradation pattern 1.
Gradation pattern 1 provides 16 patterns of 4 x 4 matrix.
</td><td>XXH
(Undeter-
mined)</td></tr>
</table>

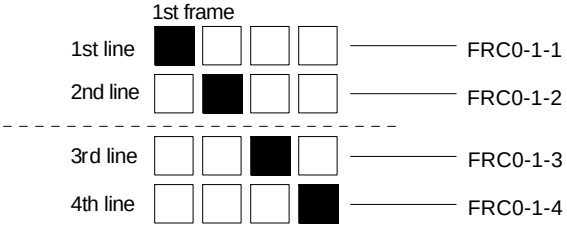
Gray scale pattern 0-1
- Gray scale pattern table 0 or 1
- Register running Nos. 1 to 32

FRC0-1-1
- Gray scale pattern table 0 or 1
- Number of patterns : 1 to 16
- Number of lines : 1 to 4

Gray scale pattern setting example

Gray scale pattern 0-1 = 48H

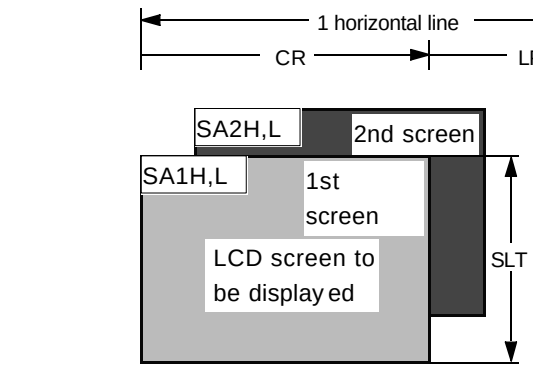
Gray scale pattern 0-2 = 12H



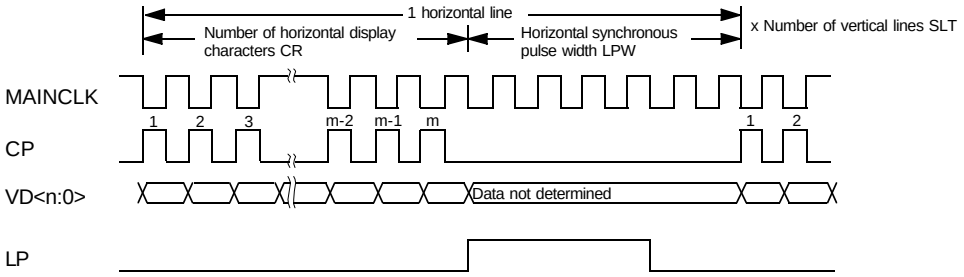
Note : Registers R17 to R80 are used to set grayscale patterns for grayscale display.
Register setting is not needed for binary display.

Description of LCD display

Relationships between control register setting and LCD display



Control register setting conditions
·1st screen drive
Binary --- (CR x 8) x SLT <=153600 dots
Gray scale --- <= 76800 dots
·2nd screen drive
Binary --- (CR x 8) x (SLT x 2) <=153600 dots
Gray scale --- <= 76800 dots



(1) Time required for processing 1 horizontal line (TH)

·Display modes ①and ⑤ $TH = \frac{2}{f_{MAINCLK}} \times (CR+LPW)$

·Display mode ②,③,④and ⑥ $TH = \frac{1}{f_{MAINCLK}} \times (CR+LPW)$

(2) Time required for processing 1 frame (TFR)

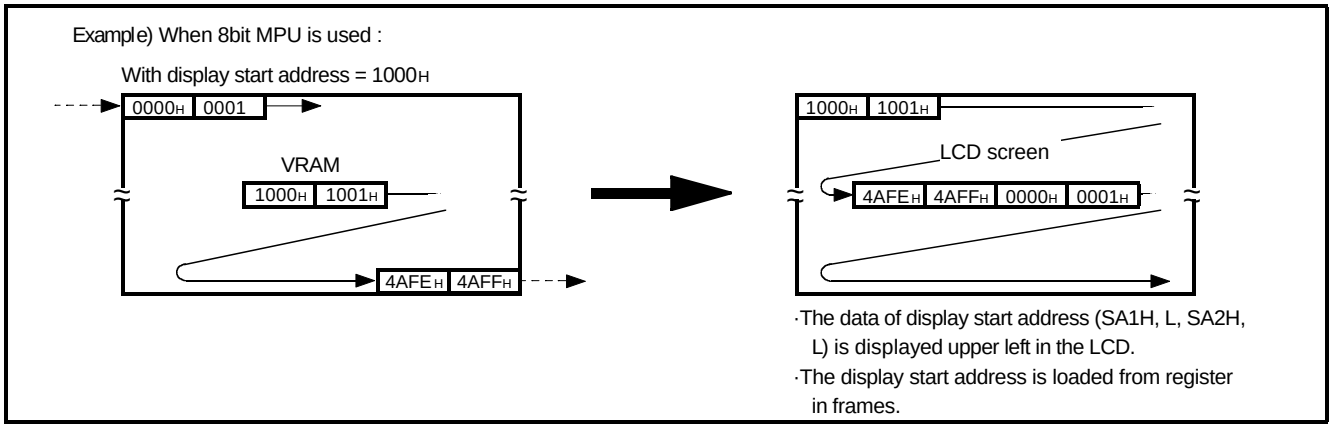
TFR = TH x SLT

CR,LPW,CSW : Unit of characters
SLT : Unit of even lines
$f_{MAINCLK}$: Frequency of MAINCLK for internal operation

Adjustment of LPW can set the number of frame frequencies requested on the LCD panel side to an optimum value.

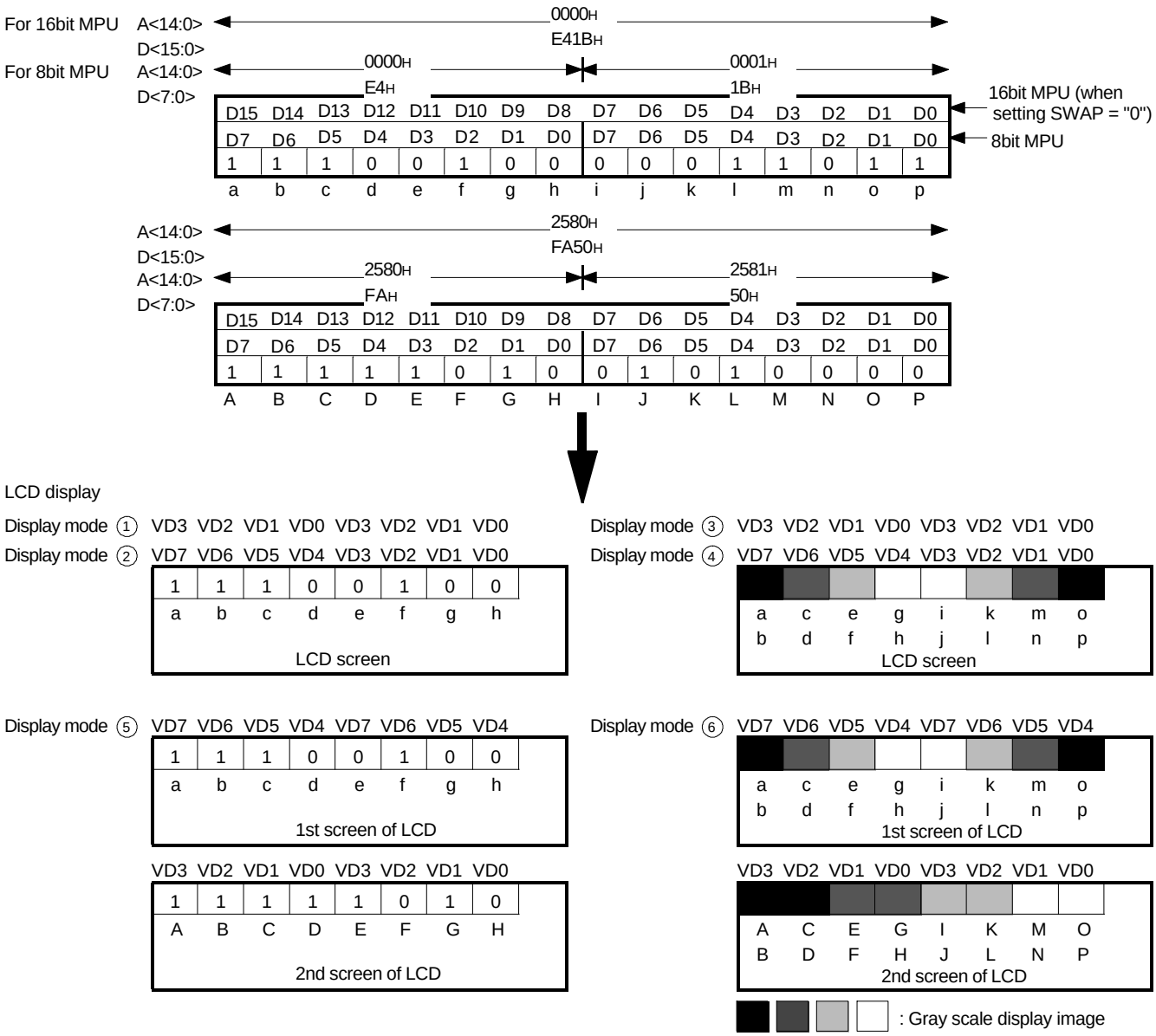
Relationships between control register setting and LCD display

Relationships between display start address and LCD display



Relationships between display start address and LCD display

Relationships between VRAM address, data and LCD display



Relationships between SWAP setting and LCD display

When 16bit MPU is in use, setting the SWAP register can modify the sending order of LCD display data in bytes.

SWAP setting	
0	For D<15:0>, sends VD<n:0> in order of upper / lower bytes.
1	For D<15:0>, sends VD<n:0> in order of lower / upper order bytes.

VRAM data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	0	1	0	0	0	0	0	1	1	0	1	1

High order byte = $E4_H$ Low order byte = $1B_H$

·Setting SWAP = "0"

D15 to D8D7 to D0

1	1	1	0	0	1	0	0	0	0	0	1	1	0	1	1

$E4_H$ $1B_H$

LCD screen

·Setting SWAP = "1"

D7 to D0D15 to D8

0	0	0	1	1	0	1	1	1	1	1	0	0	1	0	0

$1B_H$ $E4_H$

LCD screen

Relationships between LCD display mode and VD<n:0> pin

Single scan mode 4bit parallel Display mode ①, ③

VD3	VD2	VD1	VD0

LCD screen

Single scan mode 8bit parallel Display mode ②, ④

VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0

LCD screen

Dual scan mode 4bit parallel Display mode ⑤, ⑥

VD7	VD6	VD5	VD4

1st screen of LCD

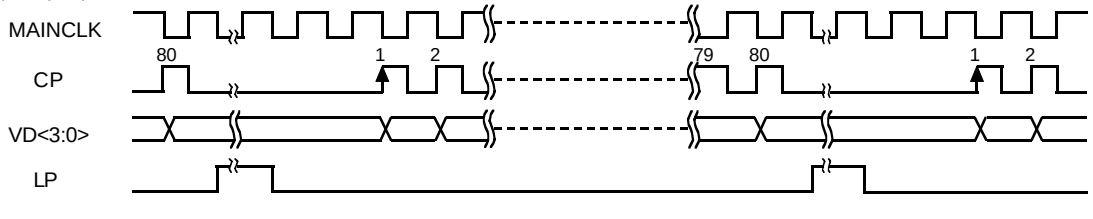
VD3	VD2	VD1	VD0

2nd screen of LCD

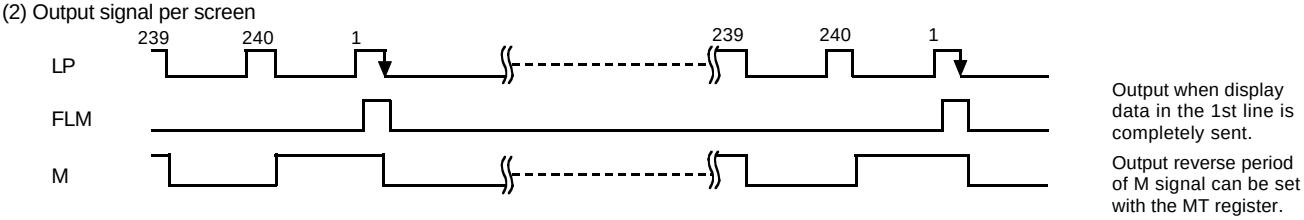
Output signal on the LCD side

Example) Assuming 320 x 240 dots LCD is used in display mode ①
(CR = 40 characters, LPW = 2 characters, SLT = 240 lines, DIV = division value 1, MT = 1)

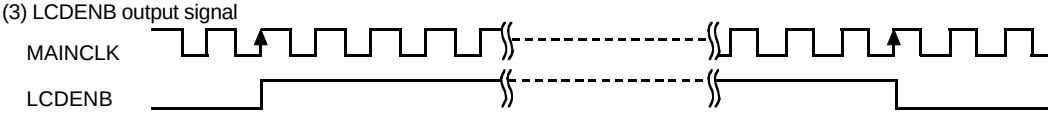
(1) Output per line



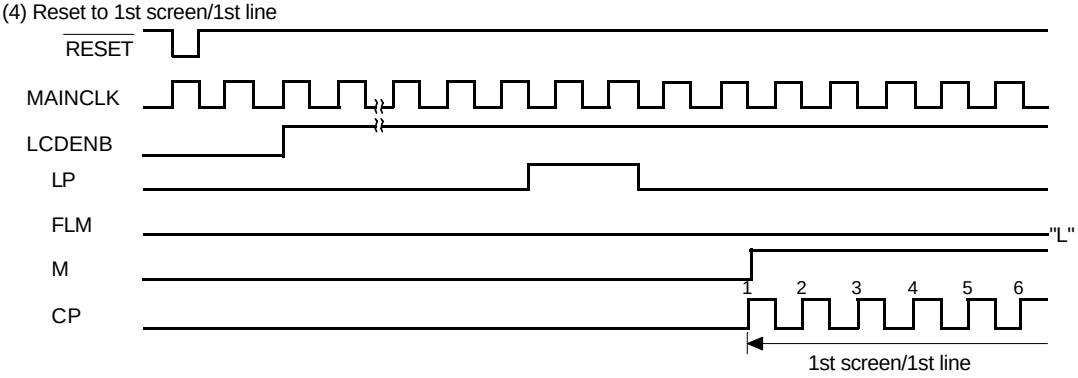
(2) Output signal per screen



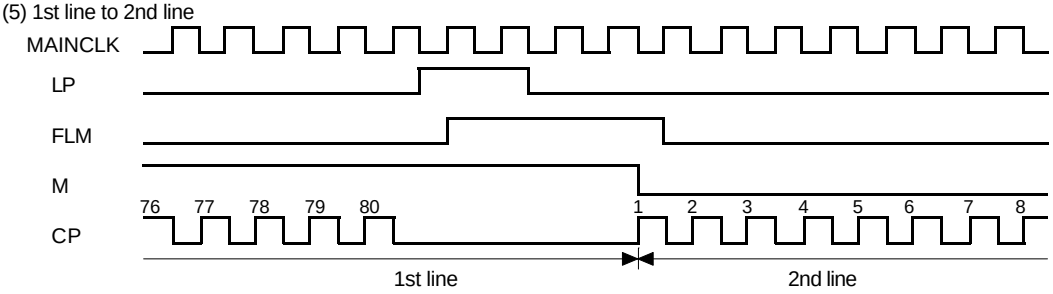
(3) LCDENB output signal



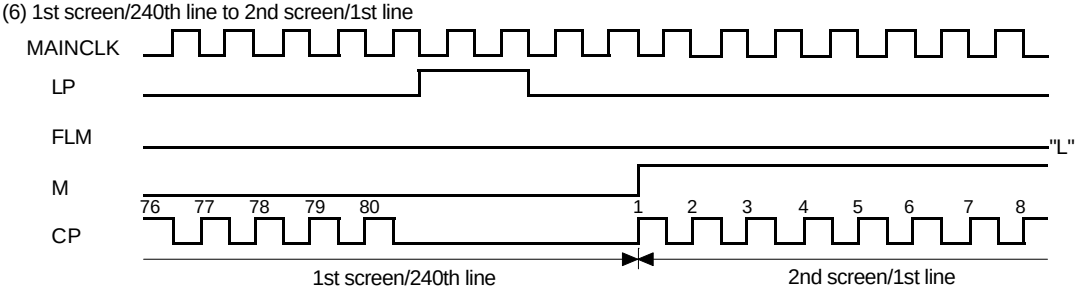
(4) Reset to 1st screen/1st line



(5) 1st line to 2nd line



(6) 1st screen/240th line to 2nd screen/1st line

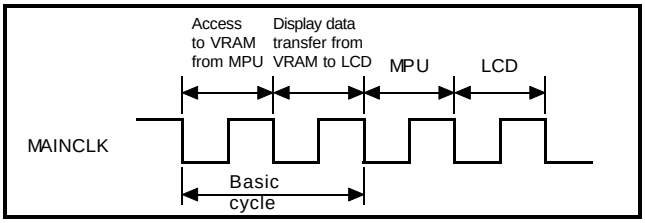


Description of cycle Steal

Basic timing

The basic timing for internal operation of the M66273 adopts 2 clocks of MAINCLK as a basic cycle to assign the 1st clock and 2nd clock to access from MPU to VRAM and transfer of display data from VRAM to the LCD side, respectively.

MAINCLK is reference clock for internal operation inputting division of MPUCLK and reference with rising edge of MPUCLK.

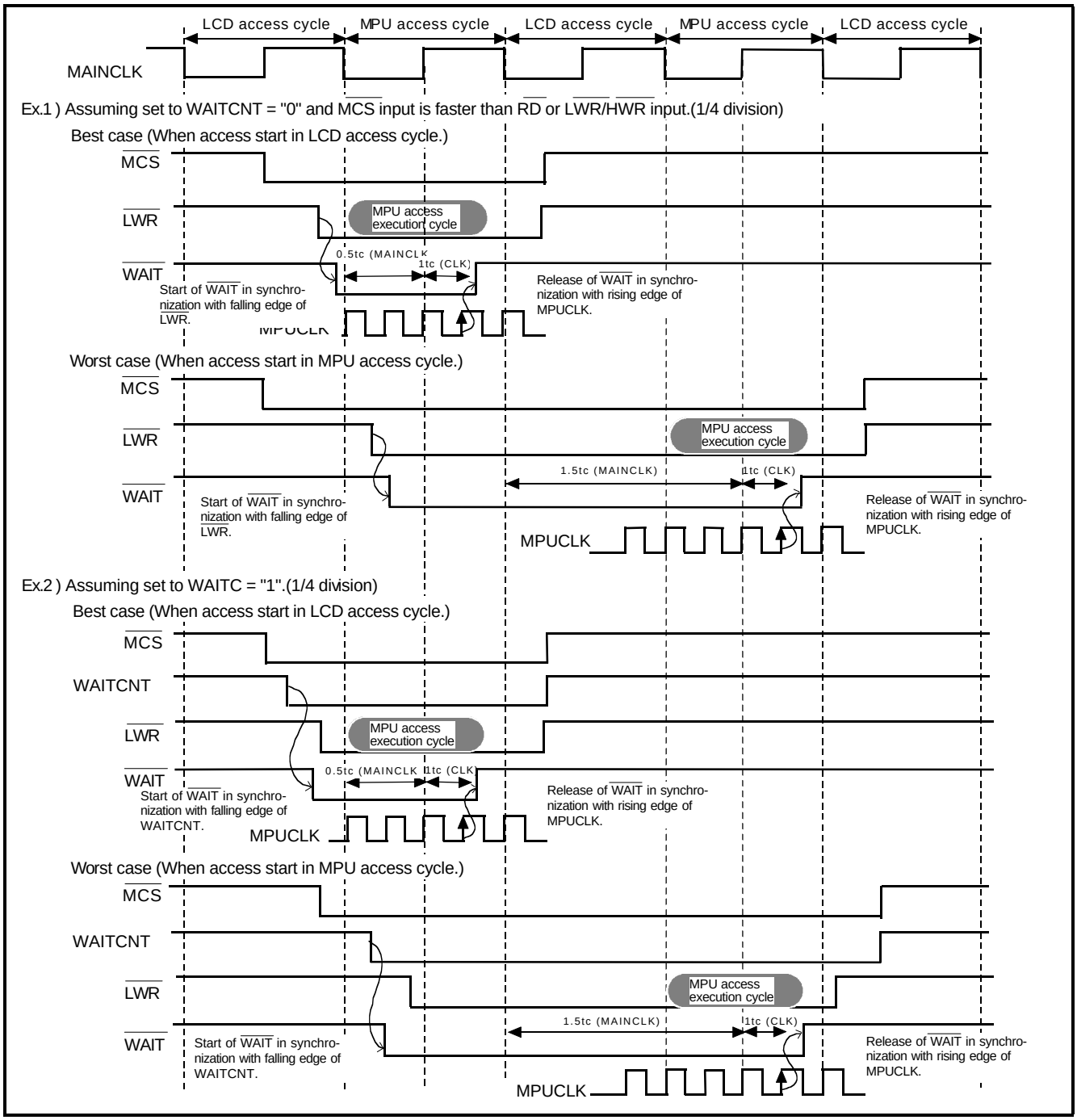


Basic timing

MPU access execution cycle (WAIT output period)

Writing/reading to/from VRAM in the display section takes,
Best case = 0.5tc(MAINCLK) + 1tc(CLK),
Worst case = 2.5tc(MAINCLK) + 1tc(CLK),
depending on the internal cycle steal status when access request from MPU starts.

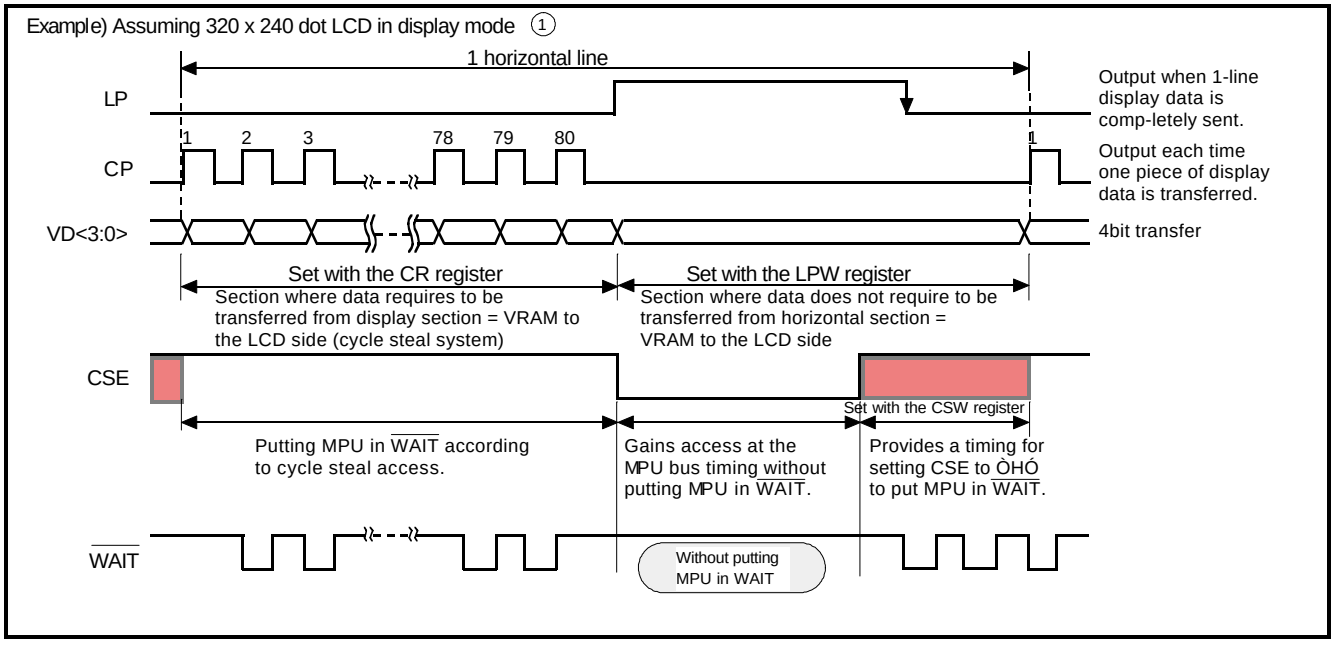
In this case, tc(CLK) = MPUCLK cycle time,
tc(MAINCLK) = MAINCLK cycle time.



MPU access execution cycle

Description of cycle steal control function

The M66273 provides the cycle steal control function to efficiently carry out one-line data processing.
In the display section where display data requires to be transferred from built-in VRAM to the LCD side, this function adopts a cycle steal system to gain access to the MPU while putting the MPU in $\overline{WAIT}$.
In a horizontal synchronous section where display data does not require to be transferred from VRAM to the LCD side, this function does not output $\overline{WAIT}$ in the section to avoid reducing the MPU throughput. However, since malfunction is restrained near the termination of horizontal synchronous section, the CSW register should be surely set to provide a period of access by the cycle steal system.
(It need to set at least 1 cycle of MPU bus timing.)



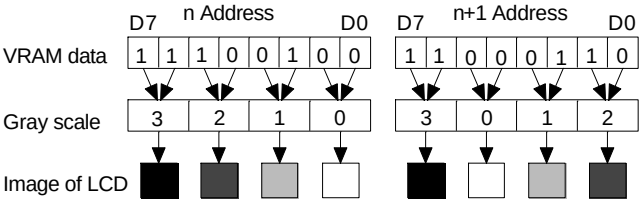
Description of gray scale function

Set gray scale mode by register (GRAY="1").
Gray scale assign 2bits of VRAM to 1dot of LCD and displaying 4density.

ex.) for 8bit-MPU 1 Address

VRAM data	D7	D6	D5	D4	D3	D2	D1	D0
Pack	C1	C0	C1	C0	C1	C0	C1	C0

C1	C0	Contents of display
0	0	Display OFF
0	1	Followed gray scale pattern table 0
1	0	Followed gray scale pattern table 1
1	1	Display ON



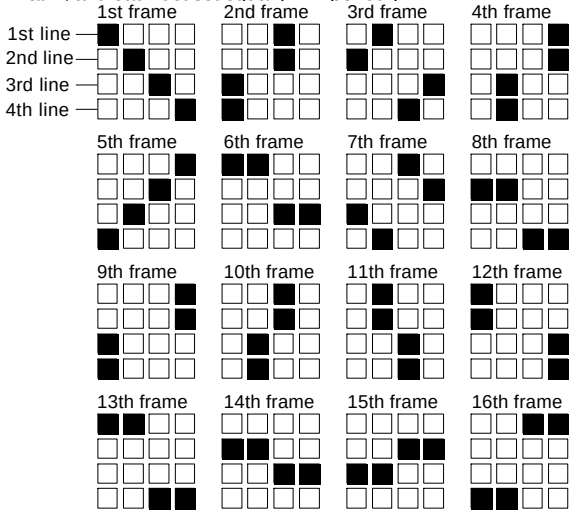
Upper figure are image of gray scale display of LCD and VRAM data, actually controlling pseudo medium gray scale.

Setting of gray scale pattern table

Gray scale pattern table 0, 1 a used for controlling display density. It set to control register R17-R80 (SRAM configuration).
Gray scale pattern set 16 patterns for 1 medium gray scale (1 pattern = 4dots x 4lines matrix).
It need to set 32 patterns (64 byte) because 2 medium gray scale.
Medium gray scale period is a maximum of 16 frames.

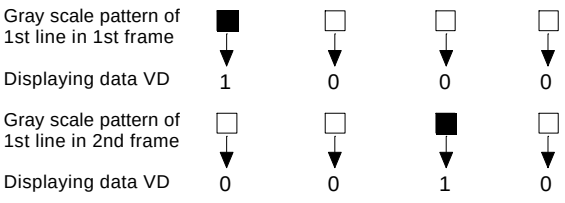
Example of gray scale pattern

The following are example of gray scale pattern. (Select 4dots from 1matrix, and each dot set equally in 1 period.)



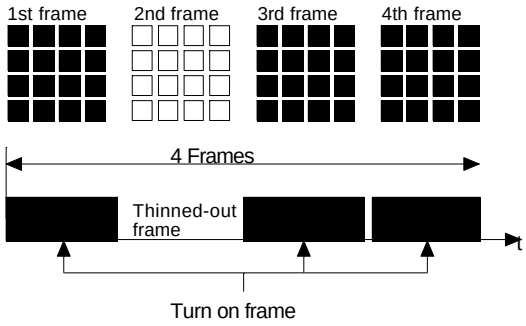
When VRAM data are following, VD output 1 for only ■ dot.

Pack	C1	C0	C1	C0	C1	C0	C1	C0
VRAM data	0	1	0	1	0	1	0	1



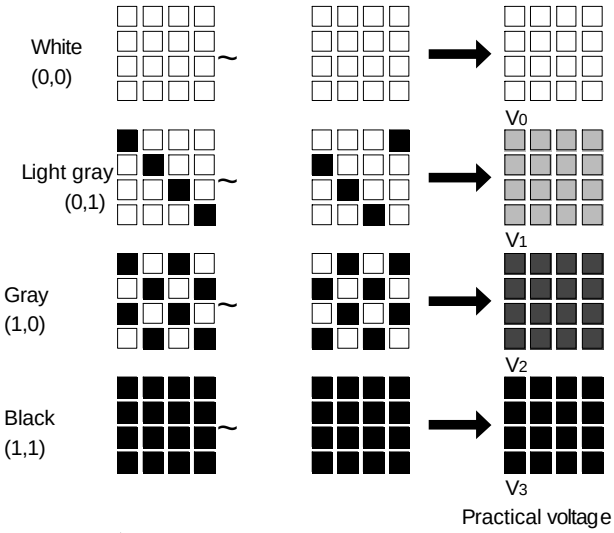
Set the same pattern for each 4 or 8 frames period in 16 frames.
So enable to decrease frame numbers of gray scale period.

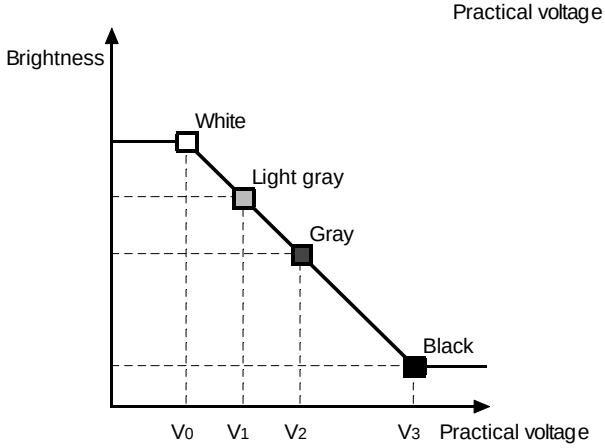
Still more, set the same gray scale pattern table in frame unit, so enable to display thinned-out frame method.
When thinned-out 1frame from continuous 4frames, the following are example of setting pattern table.



When use thinned-out frame, distribute thinned-out equally, and avoid thinned-out continuous frame together.

Gray scale function use the features of liquid crystal changed brightness by practical voltage.
The following are gray scale patterns for each frame, and the relation between brightness and practical voltage.





Additional function for LCD module built-in system

(When use this function,recommend using $\overline{ICOS}$ to control I/O registers.)

As all of the VRAM address in the M66273 are externally opened for addressing VRAM from MPU directly.

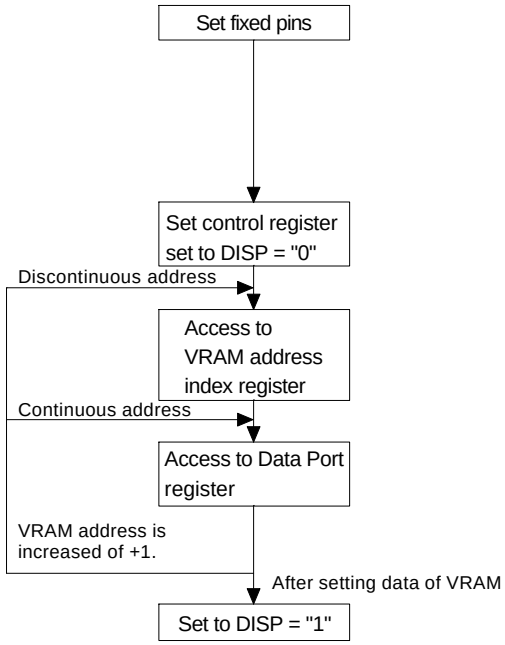
When consider the LCD module built-in system, connect pins are increased.
But the M66273 has an additional function for the LCD module built-in system by lessening connect pins.

Access the internal VRAM through the VRAM address index register in this function.
When use this function, need to set to IDXON = "0".
When use this function and access to VRAM, it need to set to DISP = "0".

· Interface pins with MPU and I/O register for access to VRAM.

	8bit MPU	16bit MPU
Interface pins	A<7:1> D<7:0> $\overline{IOCS}$ $\overline{LWR}$ $\overline{RD}$ MPUCLK (19 pins)	A<7:1> D<15:0> $\overline{IOCS}$ $\overline{LWR}$ $\overline{RD}$ MPUCLK (27 pins)
I/O register	IDX8H, IDX8L DP8	IDX16 DP16

· Method of accessing the internal VRAM
The following show the process of accessing VRAM.



· No use pins set the following.
·$\overline{HWR}$, $\overline{MCS}$ = "H",
·$\overline{BHE}$, A<0>, A<14:8> = "L" , D<15:8> = "L" (only for 8bit MPU),
·MPUSEL, WAITCNT = "L" or "H",
·$\overline{WAIT}$, CSE = open,
RESET = Power on reset or software reset.

· (In case of software reset $\overline{RESET}$ = "H" : set)

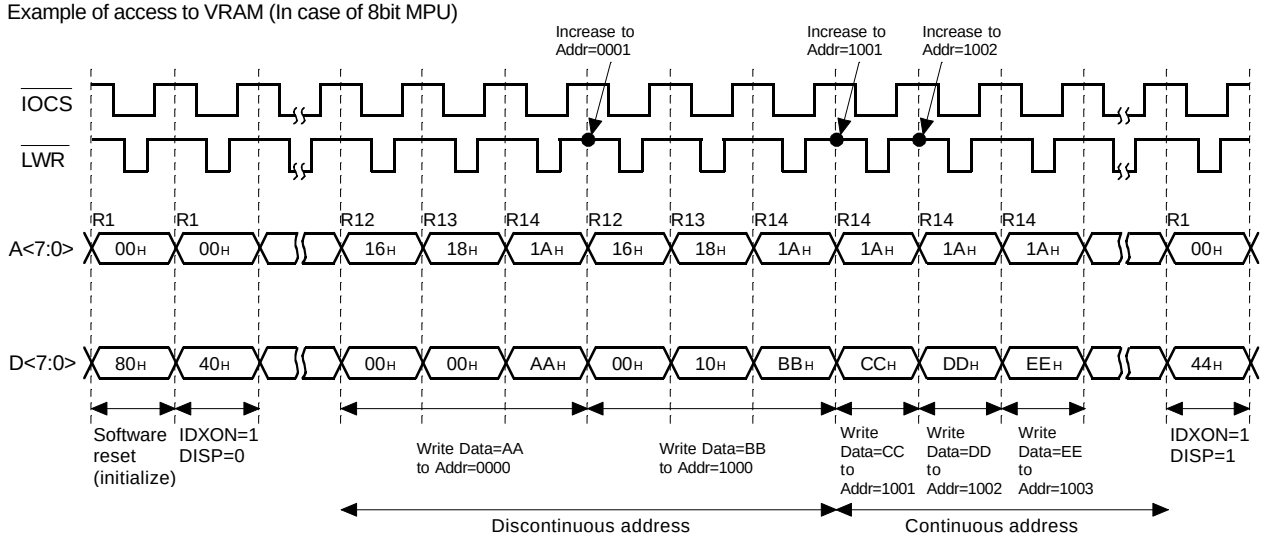
· Access the DP after writing the mode register DISP = "0".
Always enable to access, because the display signal fixed "H" or "L" in DISP = "0" and a term is no wait access.

· Select IDX8L, IDX8H (or IDX16), and write address (15bit) of VRAM as data.
Enable to change IDXL and IDXH, even if either.

· Select DP8 (or DP16), and read or write data to address of VRAM.
Access DP and IDX without WAIT function.
VRAM address is automatically increased of +1, when finished access to DP.
It doesn't need to set IDX, when access to continuous address.

· Set to DISP = "1", and displaying LCD.

· Example of access to VRAM (In case of 8bit MPU)



ABSOLUTE MAXIMUM RATINGS (Ta=-20 to +75℃ unless otherwise noted)

Symbol	Parameter	Condition	Ratings	Unit
V_{DD}	Supply voltage		-0.3 to +6.5	V
V_I	Input voltage		-0.3 to V_{DD}+0.3	V
V_O	Output voltage		-0.3 to V_{DD}+0.3	V
I_O	Output current		±20	mA
P_d	Power dissipation		600	mW
T_{stg}	Storage temperature		-55 to +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=-20 to +75℃ unless otherwise noted)

Symbol	Parameter	Condition		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{DD}	Supply voltage		5.0V support	4.5	5.0	5.5	V
			3.0V support	2.7	3.0	3.3	
V_{SS}	Supply voltage				0		V
V_I	Input voltage			0		V_{DD}	V
V_O	Output voltage			0		V_{DD}	V
T_{opr}	Operating temperature			-20	+25	+75	℃
t_r, t_f	Input rise, down time		Normal input			500	ns
			Schmidt trigger input			5	ms

ELECTRICAL CHARACTERISTICS (5V version support specifications, Ta=-20 to +75℃ unless otherwise noted)

Symbol	Parameter		Condition		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{IH}	"H" input voltage	Note 1	V_{DD} = 5.5V		3.85		5.5	V
V_{IL}	"L" input voltage		V_{DD} = 4.5V		0		1.35	
V_{T+}	Threshold voltage in positive direction	Note 2	V_{DD} = 5.0V		2.3		3.7	V
V_{T-}	Threshold voltage in negative direction				1.25		2.3	
V_{OH}	"H" output voltage		V_{DD} = 4.5V	I_{OH} = -4mA	4.1			V
V_{OL}	"L" output voltage			I_{OL} = 4mA			0.4	
I_{IH}	"H" input current		V_{DD} = 5.5V	V_I = V_{DD}			10	uA
I_{IL}	"L" input current			V_I = V_{SS}			-10	
I_{OZH}	"H" output current in off status	D<15:0>	V_{DD} = 5.5V	V_O = V_{DD}			10	uA
I_{OZL}	"L" output current in off status			V_O = V_{SS}			-10	
$I_{DD(A)}$	Average supply current in operation mode		V_{DD} = 5.5V, V_I = V_{DD} or V_{SS} $f_{MAINCLK}$ = 15MHz(MAX), Output =open	Display mode 1,2,3,4			60	mA
				Display mode 5,6			80	
$I_{DD(S)}$	Supply current in static mode		V_{DD} = 5.5V, $\overline{IOCS}$, $\overline{MCS}$ = V_{DD} Other V_I = V_{DD} or V_{SS} fixed				200	uA

Notes 1: Normal input terminal --- A<14:0>, D<15:0>
2: Schmidt trigger input terminal --- All input pins except for A<14:0>, D<15:0>

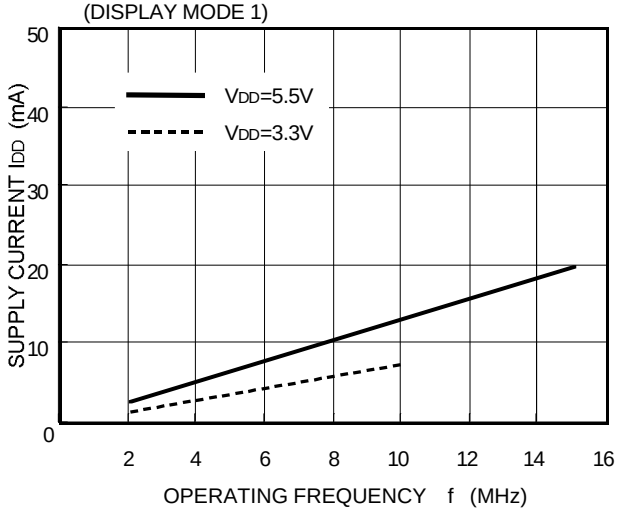
ELECTRICAL CHARACTERISTICS (3V version support specification, Ta=-20~+75℃ unless otherwise noted)

Symbol	Parameter		Condition		Limits			Unit
					Min.	Typ.	Max.	
V_{IH}	"H" input voltage	Note 1	V_{DD} = 3.3V		2.31		3.3	V
V_{IL}	"L" input voltage		V_{DD} = 2.7V		0		0.81	
V_{T+}	Threshold voltage in positive direction	Note 2	V_{DD} = 3.0V		1.27		2.18	V
V_{T-}	Threshold voltage in negative direction				0.45		1.5	
V_{OH}	"H" output voltage		V_{DD} = 2.7V	I_{OH} = -4mA	2.3			V
V_{OL}	"L" output voltage			I_{OL} = 4mA			0.4	
I_{IH}	"H" input current		V_{DD} = 3.3V	V_I = V_{DD}			10	uA
I_{IL}	"L" input current			V_I = V_{SS}			-10	
I_{OZH}	"H" output current in off status	D<15:0>	V_{DD} = 3.3V	V_O = V_{DD}			10	uA
I_{OZL}	"L" output current in off status			V_O = V_{SS}			-10	
$I_{DD(A)}$	Average supply current in operation mode		V_{DD} = 3.3V, V_I = V_{DD} or V_{SS} $f_{MAINCLK}$ = 10MHz(MAX), Output = open	Display mode 1 to 4			25	mA
				Display mode 5 and 6			35	
$I_{DD(S)}$	Supply current in static mode		V_{DD} = 3.3V, $\overline{IOCS}$, $\overline{MCS}$ = V_{DD} Other V_I = V_{DD} or V_{SS} fixed				200	uA

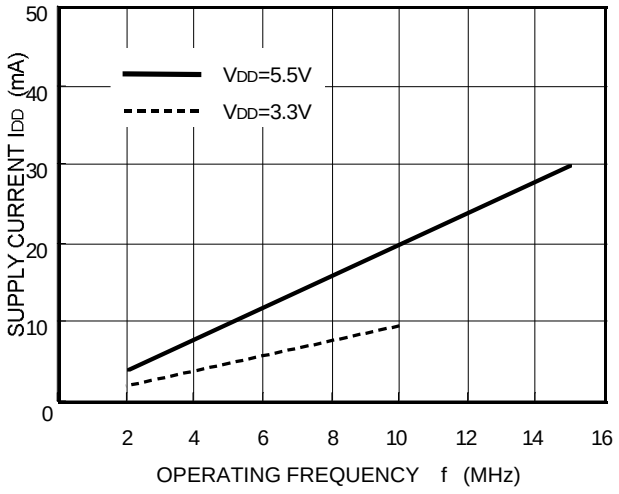
Notes 1: Normal input terminal --- A<14:0>, D<15:0>
2: Schmidt trigger input terminal --- All input pins except for A<14:0>, D<15:0>

STANDARD CHARACTERISTICS (Ta=25℃)

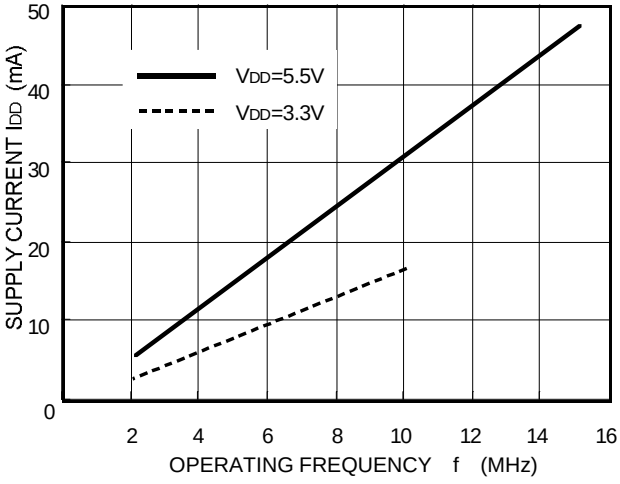
SUPPLY CURRENT VS OPERATING FREQUENCY
(DISPLAY MODE 1)



SUPPLY CURRENT VS OPERATING FREQUENCY
(DISPLAY MODE 3)



SUPPLY CURRENT VS OPERATING FREQUENCY
(DISPLAY MODE 6)



5V version support spcification

SWITCHING CHARACTERISTICS (V_{DD}=5V±10%, Ta=-20~+75℃)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
ta(IOCS-D) ta(MCS-D) ta(RD-D)	IOCS data access time MCS data access time RD data access time	CL=50pF			70	ns
tdis(IOCS-D) tdis(MCS-D) tdis(RD-D)	Output disable time after IOCS Output disable time after MCS Output disable time after RD				20	ns
tpHL(MCS-WAIT) tpHL(WR-WAIT) tpHL(RD-WAIT) tpHL(WC-WAIT)	WAIT output propagation time after MCS WAIT output propagation time after WR WAIT output propagation time after RD WAIT output propagation time after WAITCNT				15	ns
tpLH(CLK-WAIT)	WAIT output propagation time after MPUCLK				15	ns
tpd(CLK-CP)	CP output propagation time after MPUCLK				30	ns
tpLH(CLK-LP) tpHL(CLK-LP)	LP output propagation time after MPUCLK				30	ns
ta(VD)	VD access time				30	ns
tpLH(CLK-FLM) tpHL(CLK-FLM)	FLM output propagation time after MPUCLK				30	ns
tpd(CLK-M)	M output propagation time after MPUCLK				30	ns
tpLH(CLK-LE) tpHL(CLK-LE)	LCDENB output propagation time after MPUCLK				30	ns
tpLH(CLK-CSE) tpHL(CLK-CSE)	CSE output propagation time after MPUCLK				30	ns
tpd(D-WAIT)	Data definite time before cancelling WAIT		0			ns

TIMING REQUIREMENTS (V_{DD}=5V±10%, Ta=-20~+75℃)

(1) Accessing to control register

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{W(CS)}$ $t_{W(LWR)}$	IOCS/MCSpulse width LWR pulse width		35			ns
$t_{su(D-CS)}$ $t_{su(D-LWR)}$	Data set up time before rising edge of IOCS/MCS Data set up time before rising edge of LWR		20			ns
$t_{h(CS-D)}$ $t_{h(LWR-D)}$	Data hold time after rising edge of IOCS/MCS Data hold time after rising edge of LWR		2			ns
$t_{su(A-CS)}$ $t_{su(A-LWR)}$ $t_{su(A-RD)}$	Address set up time before falling edge of IOCS/MCS Address set up time before falling edge of LWR Address set up time before falling edge of RD		10			ns
$t_{h(CS-A)}$ $t_{h(LWR-A)}$ $t_{h(RD-A)}$	Address hold time after rising edge of IOCS/MCS Address hold time after rising edge of LWR Address hold time after rising edge of RD		0			ns

(2) Accessing to VRAM

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{W(MCS)}$ $t_{W(WR)}$	MCS pulse width WR pulse width		35			ns
$t_{su(D-MCS)}$ $t_{su(D-WR)}$	Data set up time before rising edge of MCS Data set up time before rising edge of WR		20			ns
$t_{h(MCS-D)}$ $t_{h(WR-D)}$	Data hold time after rising edge of MCS Data hold time after rising edge of WR		2			ns
$t_{su(A-MCS)}$ $t_{su(A-WR)}$ $t_{su(A-RD)}$	Address set up time before falling edge of MCS Address set up time before falling edge of WR Address set up time before falling edge of RD		10			ns
$t_{h(MCS-A)}$ $t_{h(WR-A)}$ $t_{h(RD-A)}$	Address hold time after rising edge of MCS Address hold time after rising edge of WR Address hold time after rising edge of RD		0			ns
$t_{su(D-CLKD)}$	Data set up time before rising edge of WAIT		$t_{su(CLK)}$+10			ns
$t_{su(MCS-WC)}$	MCS set up time before falling edge of WAITCNT		5			ns

* tc(CLK)=MPUCLK cycle time

(3) Clock and accessing to LCD display

Symbol	Parameter		Test condition	Limits			Unit
				Min.	Typ.	Max.	
$t_{C(CLK)}$	MPUCLK cycle time			50			ns
$t_{WH(CLK)}$	MPUCLK "H" pulse width				$\frac{t_{C(CLK)}}{2}$		ns
$t_{WL(CLK)}$	MPUCLK "L" pulse width						
$t_{C(CP)}$	CP syscle time	Display mode 1,2,3,5,6			$\frac{t_{C(CLK)}}{(1/n)}$		ns
		Display mode 4			$\frac{2 \cdot t_{C(CLK)}}{(1/n)}$		ns
$t_{WH(CP)}$	CP "H" pulse width	Display mode 1,2,3,5,6			$\frac{t_{C(CLK)}}{2 \cdot (1/n)}$		ns
$t_{WL(CP)}$	CP "L" pulse width						
$t_{WH(CP)}$	CP "H" pulse width	Display mode 4			$\frac{t_{C(CLK)}}{(1/n)}$		ns
$t_{WL(CP)}$	CP "L" pulse width						
$t_{W(FLM)}$	FLM pluse width	Display mode 1,2,3,5,6			$\frac{t_{C(CLK)} \cdot LPW}{(1/n)}$		ns
		Display mode 4			$\frac{2 \cdot t_{C(CLK)} \cdot LPW}{(1/n)}$		ns

Note : Clock frequency of MPUCLK input is less than fmax = 20MHz.
Limit of clock for the internal operation is fmax = 15MHz.
When MPUCLK is more than 15MHz from extemal input,set clock for the internal operation up to 15MHz by using division of DIV register.
Division is set with rising dege of MPUCLK input.

1/n =Division of MPUCLK
LPW =Setting value of LPW register

3V version support spcification

SWITCHING CHARACTERISTICS (V_{DD}=3V±10%, Ta=-20~+75℃)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
ta(IOCS-D) ta(MCS-D) ta(RD-D)	IOCS data access time MCS data access time RD data access time	CL=50pF			100	ns
tdis(IOCS-D) tdis(MCS-D) tdis(RD-D)	Output disable time after IOCS Output disable time after MCS Output disable time after RD				30	ns
tpHL(MCS-WAIT) tpHL(WR-WAIT) tpHL(RD-WAIT) tpHL(WC-WAIT)	WAIT output propagation time after MCS WAIT output propagation time after WR WAIT output propagation time after RD WAIT output propagation time after WAITCNT				25	ns
tpLH(CLK-WAIT)	WAIT output propagation time after MPUCLK				25	ns
tpd(CLK-CP)	CP output propagation time after MPUCLK				40	ns
tpLH(CLK-LP) tpHL(CLK-LP)	LP output propagation time after MPUCLK				40	ns
ta(VD)	VD access time				40	ns
tpLH(CLK-FLM) tpHL(CLK-FLM)	FLM output propagation time after MPUCLK				40	ns
tpd(CLK-M)	M output propagation time after MPUCLK				40	ns
tpLH(CLK-LE) tpHL(CLK-LE)	LCDENB output propagation time after MPUCLK				40	ns
tpLH(CLK-CSE) tpHL(CLK-CSE)	CSE output propagation time after MPUCLK				40	ns
tpd(D-WAIT)	Data definite time before cancelling WAIT		0			ns

TIMING REQUIREMENTS (V_{DD}=3V±10%, Ta=-20~+75℃)

(1) Accessing to control register

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{W(CS)}$ $t_{W(LWR)}$	IOCS/MCS pulse width LWR pulse width		50			ns
$t_{su(D-CS)}$ $t_{su(D-LWR)}$	Data set up time before rising edge of IOCS/MCS Data set up time before rising edge of LWR		30			ns
$t_{h(CS-D)}$ $t_{h(LWR-D)}$	Data hold time after rising edge of IOCS/MCS Data hold time after rising edge of LWR		2			ns
$t_{su(A-CS)}$ $t_{su(A-LWR)}$ $t_{su(A-RD)}$	Address set up time before falling edge of IOCS/MCS Address set up time before falling edge of LWR Address set up time before falling edge of RD		15			ns
$t_{h(CS-A)}$ $t_{h(LWR-A)}$ $t_{h(RD-A)}$	Address hold time after rising edge of IOCS/MCS Address hold time after rising edge of LWR Address hold time after rising edge of RD		0			ns

(2) Accessing to VRAM

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{W(MCS)}$ $t_{W(WR)}$	MCS pulse width WR pulse width		50			ns
$t_{su(D-MCS)}$ $t_{su(D-WR)}$	Data set up time before rising edge of MCS Data set up time before rising edge of WR		30			ns
$t_{h(MCS-D)}$ $t_{h(WR-D)}$	Data hold time after rising edge of MCS Data hold time after rising edge of WR		2			ns
$t_{su(A-MCS)}$ $t_{su(A-WR)}$ $t_{su(A-RD)}$	Address set up time before falling edge of MCS Address set up time before falling edge of WR Address set up time before falling edge of RD		15			ns
$t_{h(MCS-A)}$ $t_{h(WR-A)}$ $t_{h(RD-A)}$	Address hold time after rising edge of MCS Address hold time after rising edge of WR Address hold time after rising edge of RD		0			ns
$t_{su(D-CLK)}$	Data set up time before rising edge of WAIT		$t_{c(CLK)}$+15			ns
$t_{su(MCS-WC)}$	MCS set up time before falling edge of WAITCNT		7			ns

* tc(CLK)=MPUCLK cycle time

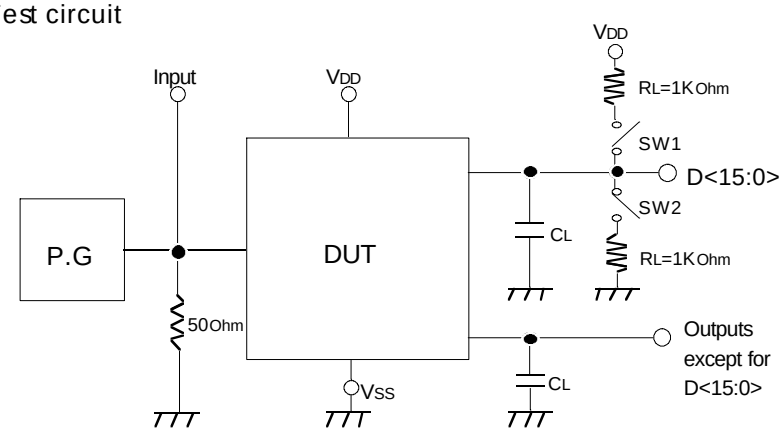
(3) Clock and accessing to LCD display

Symbol	Parameter		Test condition	Limits			Unit
				Min.	Typ.	Max.	
$t_{C(CLK)}$	MPUCLK cycle time			50			ns
$t_{WH(CLK)}$	MPUCLK "H" pulse width				$\frac{t_{C(CLK)}}{2}$		ns
$t_{WL(CLK)}$	MPUCLK "L" pulse width						
$t_{C(CP)}$	CP syscle time	Display mode 1,2,3,5,6			$\frac{t_{C(CLK)}}{(1/n)}$		ns
		Display mode 4			$\frac{2 \cdot t_{C(CLK)}}{(1/n)}$		ns
$t_{WH(CP)}$	CP "H" pulse width	Display mode 1,2,3,5,6			$\frac{t_{C(CLK)}}{2 \cdot (1/n)}$		ns
$t_{WL(CP)}$	CP "L" pulse width						
$t_{WH(CP)}$	CP "H" pulse width	Display mode 4			$\frac{t_{C(CLK)}}{(1/n)}$		ns
$t_{WL(CP)}$	CP "L" pulse width						
$t_{W(FLM)}$	FLM pluse width	Display mode 1,2,3,5,6			$\frac{t_{C(CLK)} \cdot LPW}{(1/n)}$		ns
		Display mode 4			$\frac{2 \cdot t_{C(CLK)} \cdot LPW}{(1/n)}$		ns

Note : Clock frequency of MPUCLK input is less than fmax = 20MHz.
Limit of clock for the internal operation is fmax = 10MHz.
When MPUCLK is more than 10MHz from extemal input,set clock for the internal operation up to 10MHz by using division of DIV register.
Division is set with rising dege of MPUCLK input.

1/n =Division of MPUCLK
LPW =Setting value of LPW register

Test circuit



Parameter	SW1	SW2
$t_{dis(LZ)}$	Closed	Open
$t_{dis(HZ)}$	Open	Closed
$t_{a(ZL)}$	Closed	Open
$t_{a(ZH)}$	Open	Closed

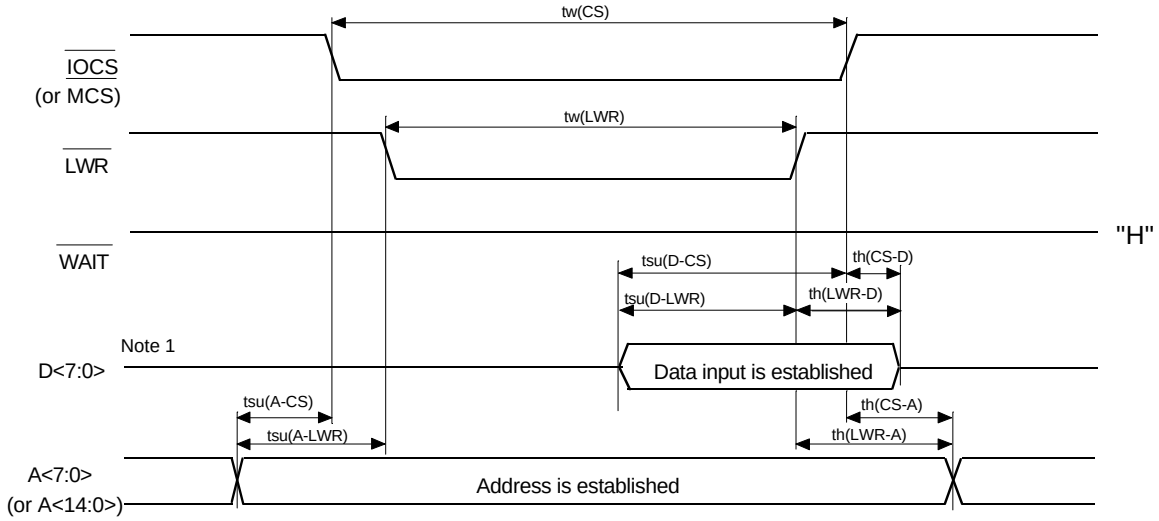
(1) Input pulse level: 0 to 3V
Input pulse rise/fall time: tr,tf=3ns
Input decision voltage: 1.5V
Output decision voltage: VDD/2
(However,tdis(LZ) is 10% of output amplitude and tdis(HZ) is 90% of that for dezision.)

(2) Load capacity C_L include float capacity of connection and input capacity of probe.

TIMING DIAGRAM

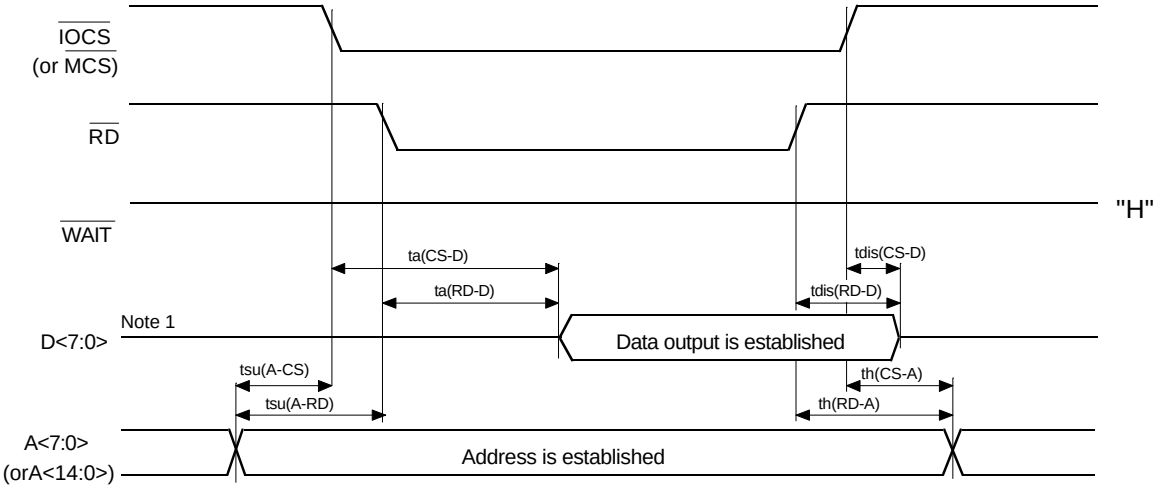
(1) Write to control register ($\overline{RD}$ = "H")

No WAIT



(2) Read from control register ($\overline{LWR}$= "H")

No WAIT

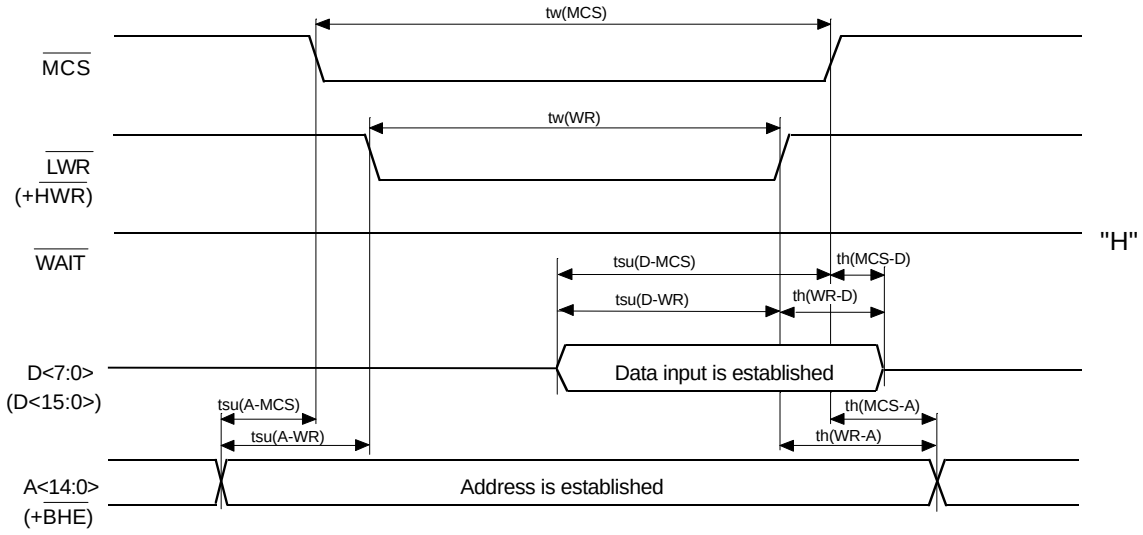


Note 1 : D<15:0> is used only when 16bit MPU controls the LCD module built-in type support function.

2 : Writing/reading operation for the control register is performed during "L" overlapping of $\overline{IOCS}$ or $\overline{MCS}$ and $\overline{LWR}$ or $\overline{RD}$ input signal. Limits of $\overline{IOCS}$,$\overline{MCS}$, $\overline{LWR}$ and $\overline{RD}$ are prescribed by the input signal of last change to "L" in starting access, and by the input signal of first change to "H" in ending access.

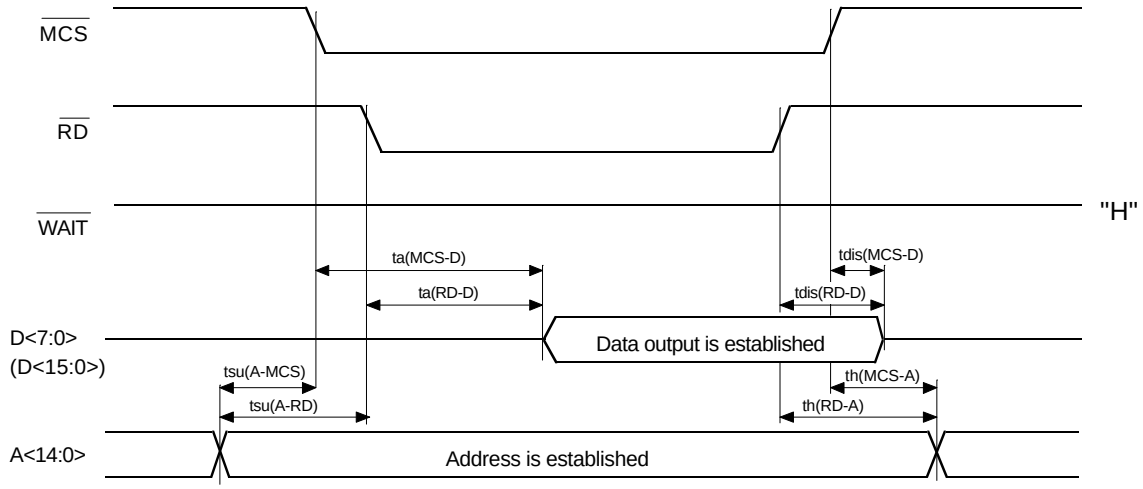
(3) Write to VRAM ($\overline{RD}$ = "H")

Term of non cycle steal access



(4) Read from VRAM ($\overline{LWR}$, $\overline{HWR}$ = "H")

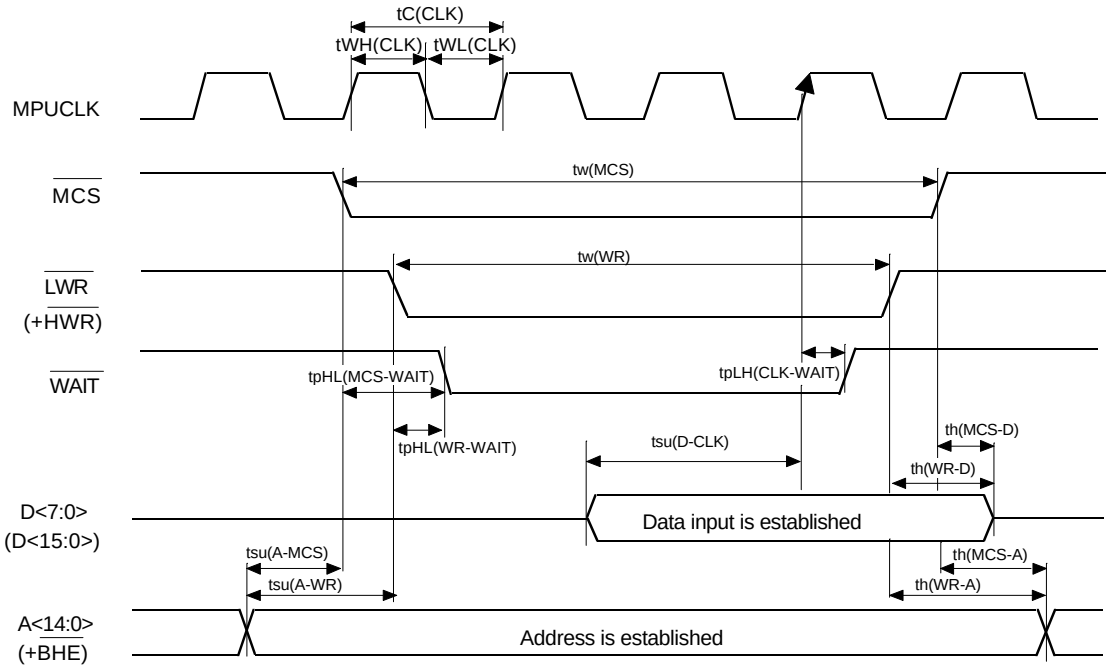
Term of non cycle steal access



Note 3 : Writing/reading operation for VRAM during non cycle steal access is performed during "L" overlapping of $\overline{MCS}$ and $\overline{LWR}$ (+$\overline{HWR}$) or $\overline{RD}$ input signal.
Limits of $\overline{MCS}$, $\overline{LWR}$ (+$\overline{HWR}$) and $\overline{RD}$ are prescribed by the input signal of last change to "L" in starting access, and by the input signal of first change to "H" in ending access.

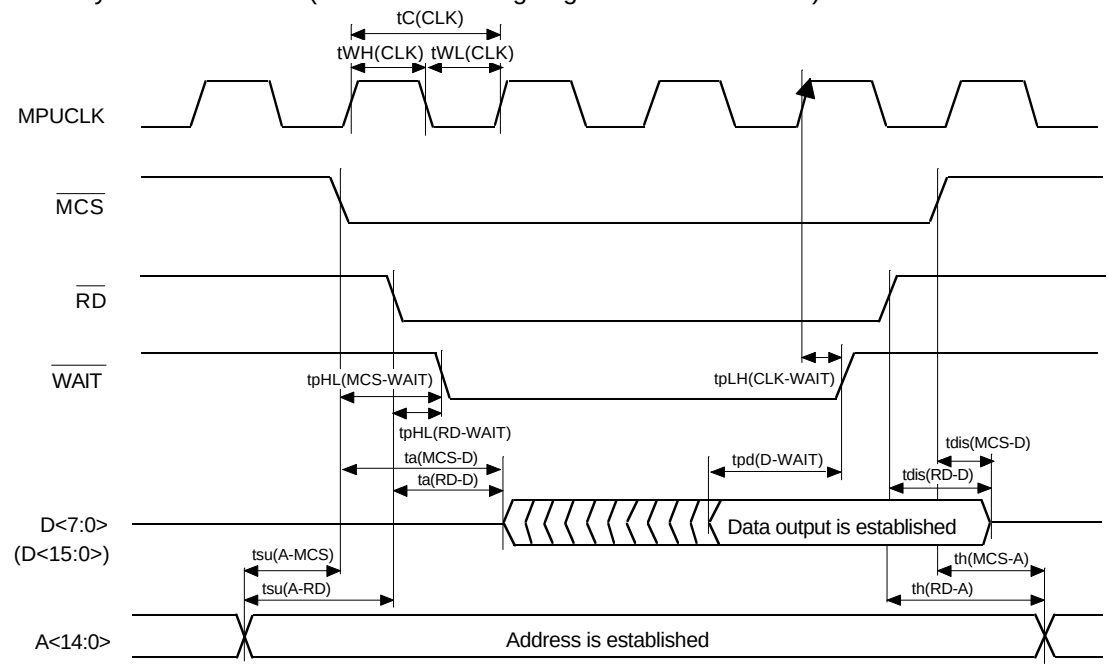
(5) Write to VRAM ($\overline{RD}$ = "H",WAITCNT= "L" or "H" fixed)

Term of cycle steal access (and When setting register WAITC to "0")



(6) Read from VRAM($\overline{LWR}$, $\overline{HWR}$ = "H",WAITCNT = "L" or "H" fiexed)

Term of cycle steal access (and when setting segester WAITC to "0")



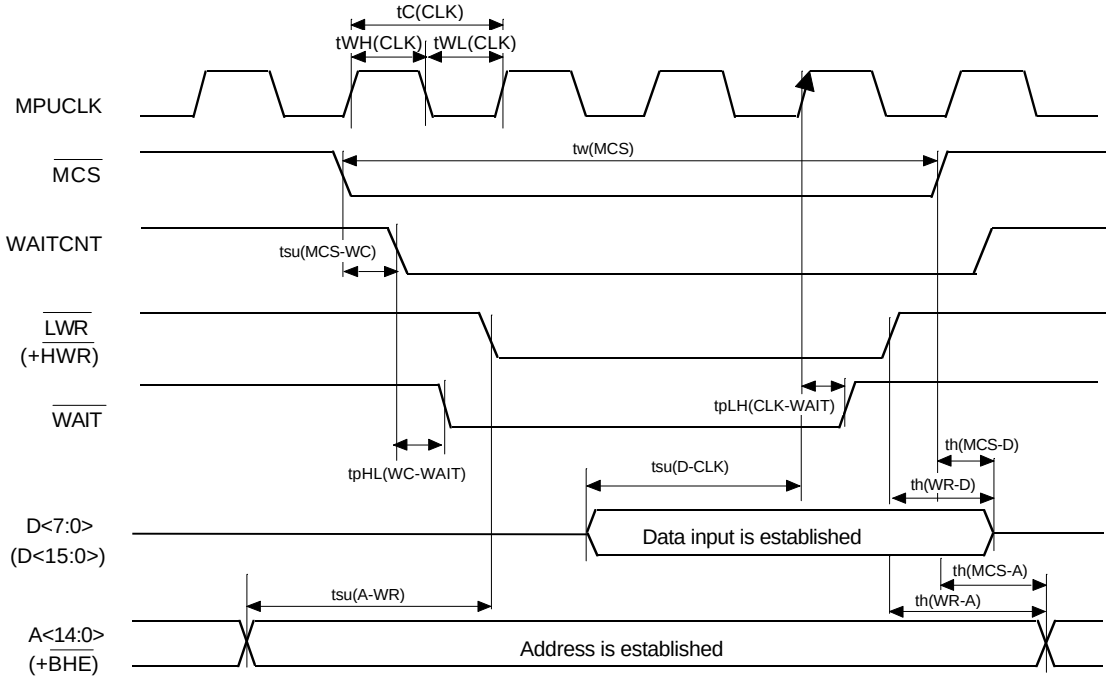
Note 4 :Writing/reading operation for VRAM during cycle steal access needs 0.5tc(MAINCLK) + 1tc(CLK) in best case or 2.5tc(MAINCLK)+1tc(CLK) in worst case, according to the condition of the internal cycle steal at starting access requested from MPU.
Data output D is established before changing $\overline{WAIT}$ output.
tc(MAINCLK) = Reference clock cycle time for internal operation after setting division of MPUCLK.

5 : Limits of $\overline{MCS}$, $\overline{LWR}$ (+$\overline{HWR}$) and $\overline{RD}$ are prescribed by the input signal of last change to "L" in starting access, and by the input signal of first change to "H" in ending access.

6 : Always once return $\overline{MCS}$, $\overline{LWR}$ (+$\overline{HWR}$) or $\overline{RD}$ to "H" after canceling $\overline{WAIT}$ output. In case of latching "L", as next $\overline{WAIT}$ does not output, this causes malfunction to occur.

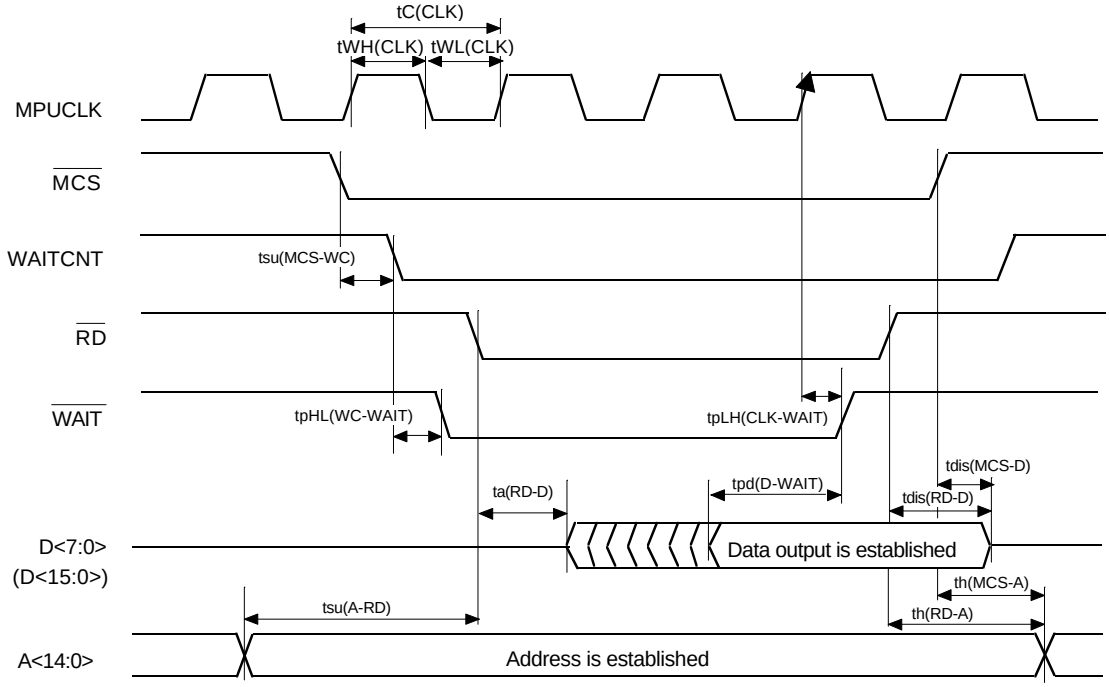
(7) Write to VRAM ($\overline{RD}$ = "H")

Term of cycle steal access (and When setting register WAITC to "1")



(8) Read from VRAM ($\overline{LWR}$, $\overline{HWR}$ = "H")

Term of cycle steal access (and when setting register WAITC to "1")



Note 7 : Writing/reading operation for VRAM during cycle steal access needs 0.5tc(MAINCLK) + 1tc(CLK) in best case or 2.5tc(MAINCLK)+1tc(CLK) in worst case, according to the condition of the internal cycle steal at starting access requested from MPU.
Data output D is established before changing $\overline{WAIT}$ output.
tc(MAINCLK) = Reference clock cycle time for internal operation after setting division of MPUCLK.

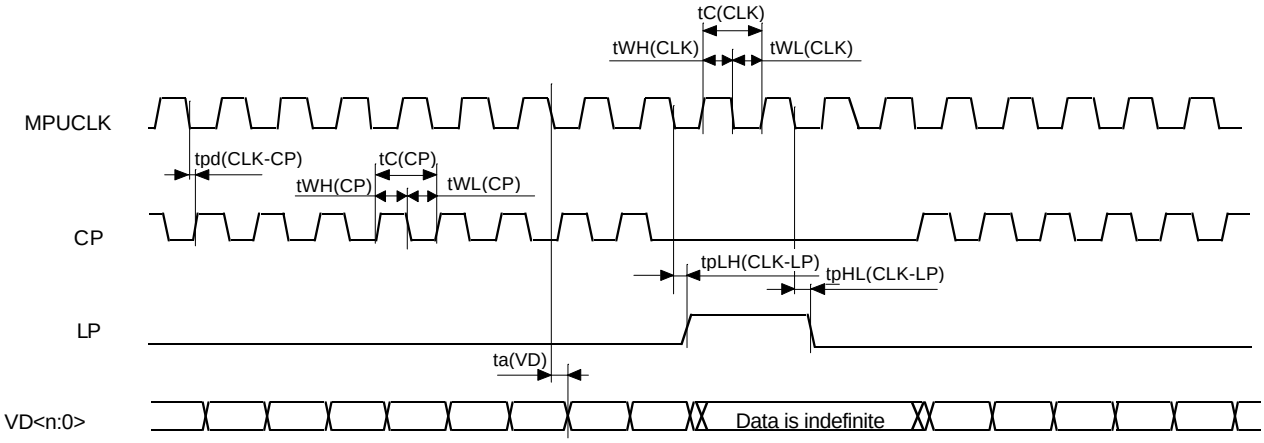
8 : When setting WAITC to "1" , $\overline{MCS}$ is necessary to change "L" earier than LWR (+HWR) ,RD.
Limits of $\overline{MCS}$, $\overline{LWR}$ (+$\overline{HWR}$) and $\overline{RD}$ are prescribed by the input signal of last change to "L" in starting access, and by the input signal of first change to "H" in ending access.

9 : Always once return $\overline{MCS}$, $\overline{LWR}$ (+$\overline{HWR}$) or $\overline{RD}$ to "H" after canceling $\overline{WAIT}$ output. In case of latching "L", as next $\overline{WAIT}$ does not output, this causes malfunction to occur.

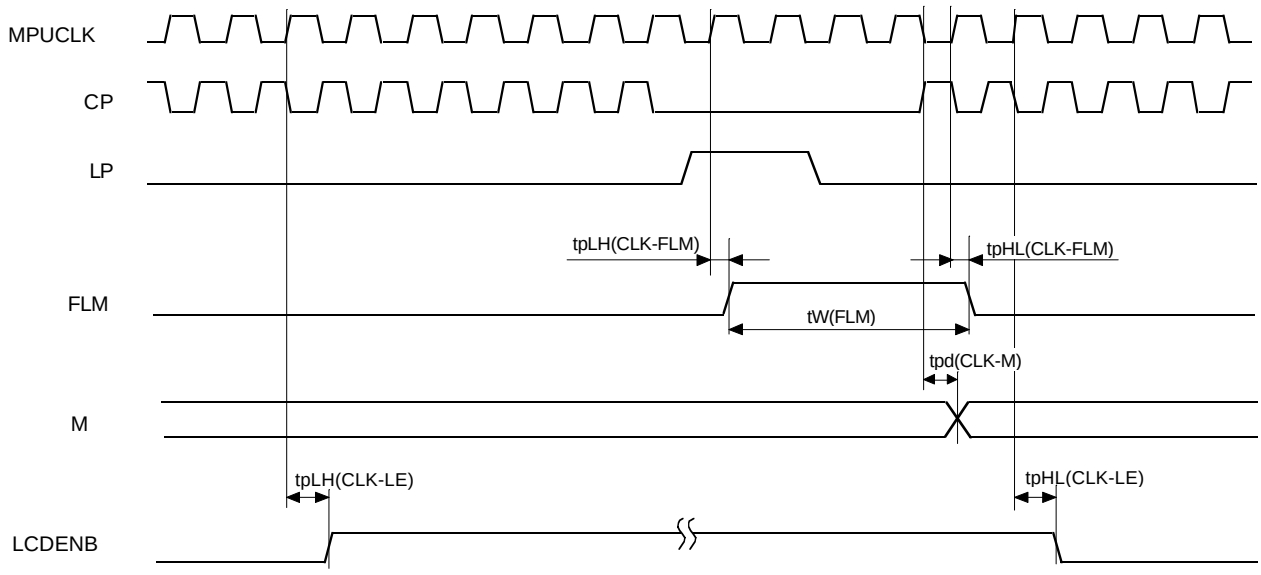
(9) Interface timing with LCD (DIV = 1 division : set)

(9-1) LCD display data transfer

* When DIV = 1 division, MAINCLK for internal operation = MPUCLK input.

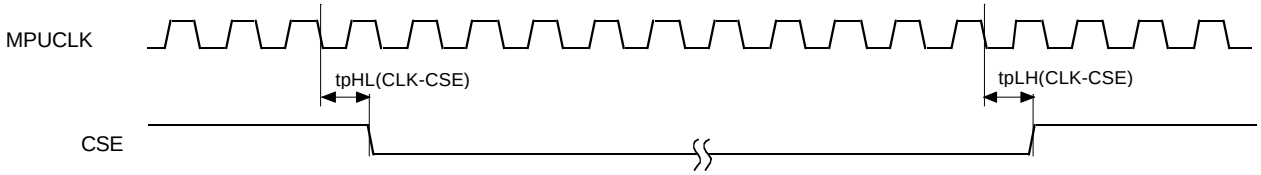


(9-2) Control signal



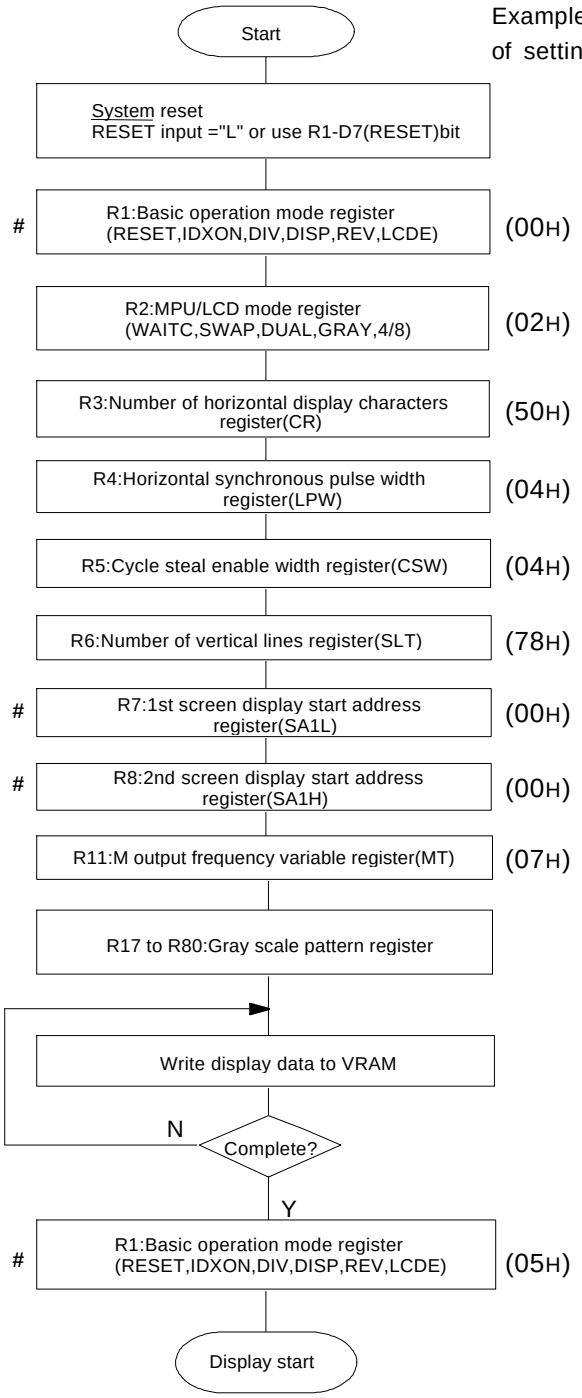
Note 10 : Output signal to LCD side is synchronized with MAINCLK (reference clock for internal operation).
When division is set to 1/2 to 1/16 by DIV register, switching characteristics is defined by rising edge of MPUCLK.

(10) CSE output timing (DIV=1 divison : set)



FLOWCHART

EXAMPLE OF INITIALIZE ON DISPLAY MODE 3 (STANDARD ACCESS)



Example of setting

Note) When use software reset, surely return to reset off after reset on.
And then, can't set another bits (D6 to D0) at the same time.

Set IDXON=OFF,DISP=OFF.
(Set RESET,IDXON,DIV when register is initialized.)

Set display mode, only when register is initialized.

Note) Set R1-D6(IDXON) and R2 register at the beginning of initializing register after system reset.

Set suitable value for LCD.
(Set these value only when register is initialized.)

Set lower address of 1st screen display start address.

Set upper address of 1st screen display start address.

Set suitable value for LCD.
(Set MT only when register is initialized.)

Set gray scale pattern.

Note) When access to R17 to R80, must be set DISP=OFF.
Can't access to R17 to R80 on DISP=ON.

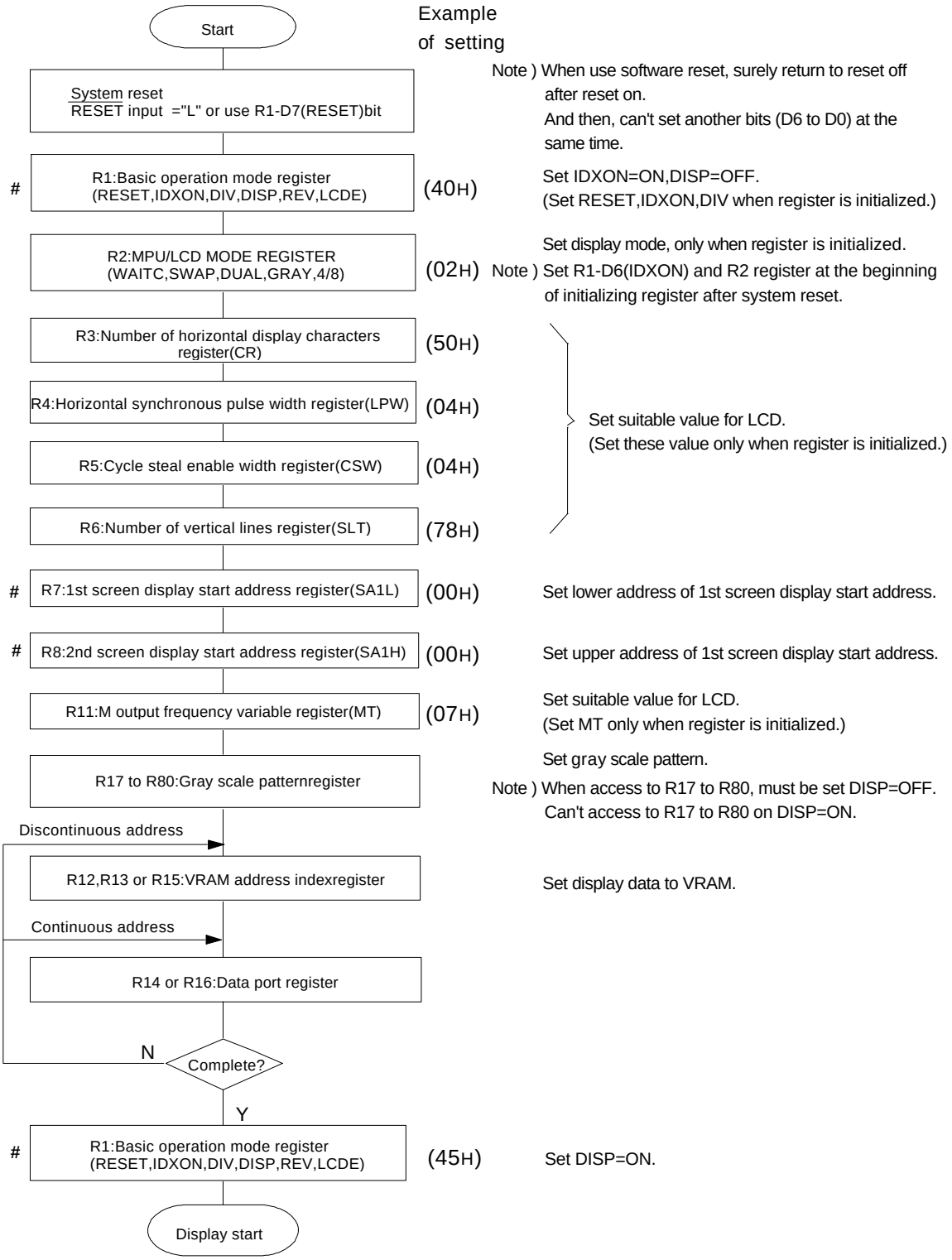
Set display data to VRAM.

Set DISP=ON.

Setting example suppose LCD size = 320x240dots and display mode 3 (Single scan,Gray scale, 4bit transfer).

Can change R1(DISP,REV,LCDE),R7(SA1L),R6(SA1h) registers value during display on.

EXAMPLE OF INITIALIZE ON DISPLAY MODE 3 (LCD MODULE BUILT-IN ACCESS)



Setting example suppose LCD size = 320x240dots and display mode 3 (Single scan,Gray scale, 4bit transfer).

Can change R1(DISP,REV,LCDE),R7(SA1L),R6(SA1h) registers value during display on.