# 32171 Group

SINGLE-CHIP 32-BIT CMOS MICROCOMPUTER

## Description

32171 Group is a 32-bit, single-chip RISC microcomputer with built-in flash memory, which was developed for use in general industrial and household equipment.

To make full use of microcomputer built-in mass volume flash memory, this microcomputer contains a variety of peripheral functions ranging from two independent blocks of 16-channel A-D converters to 37-channel multifunction timers, 10-channel DMAs, 3-channel serial I/Os, and 1-channel real time debugger. Also included 1-channel Full-CAN modules and JTAG (boundary scan facility).

With lower power consumption and low noise characteristics also considered, these microcomputers are ideal for embedded equipment applications.

## Features

M32R RISC CPU core

- Uses the M32R family RISC CPU core (Instruction set common to all microcomputers in the M32R family)
- Five-stage pipelined processing
- Sixteen 32-bit general-purpose registers
- 16-bit/32-bit instructions implemented
- DSP function instructions (sum-of-products calculation using 56-bit accumulator)
- Built-in flash memory
- Built-in flash programming boot program
- Built-in RAM
- PLL clock generating circuit ..... Built-in × 4 PLL circuit
- Maximum operating frequency of the CPU clock
  40MHz(when operating at -40 to +85°C)
  32MHz(when operating at -40 to +125°C)

**Table 1 Type Name List (32171 Group)**

| Type Name | RAM Size | ROM Size |
|---|---|---|
| M32171F4VFP | 16K bytes | 512K bytes |
| M32171F3VFP | 16K bytes | 384K bytes |
| M32171F2VFP | 16K bytes | 256K bytes |

### 37-channel multijunction timers (MJT)

Multifunction timers are incorporated that support various purposes of use.

- 16-bit output related timers ..... 35ch
- 16-bit input/output related timers ..... 10ch
- 16-bit input related timers ..... 8ch
- 32-bit input related timers ..... 8ch

- Flexible configuration is possible through interconnection of timers.
- The internal DMAC and A-D converter can be started by a timer.

## Real-time Debugger

- Includes dedicated clock-synchronized serial I/O that can read and write the contents of the internalRAM independently of the CPU.
- Can look up and update the data table in real time while the program is running.
- Can generate a dedicated interrupt based on RTD communication.

## Abundant internal peripheral functions

In addition to the timers and real-time debugger, the microcomputer contains the following peripheral functions.

- DMAC ..... 10 channels
- A-D converter ..... 10-bit converter × 16 channels
- Serial I/O ..... 3 channels
- Interrupt controller ..... 22 interrupt sources, 8 priority levels
- Wait controller
- Full CAN ..... 1 channel
- JTAG (Boundary scan function, Mitsubishi original)

## Designed to operate at high temperatures

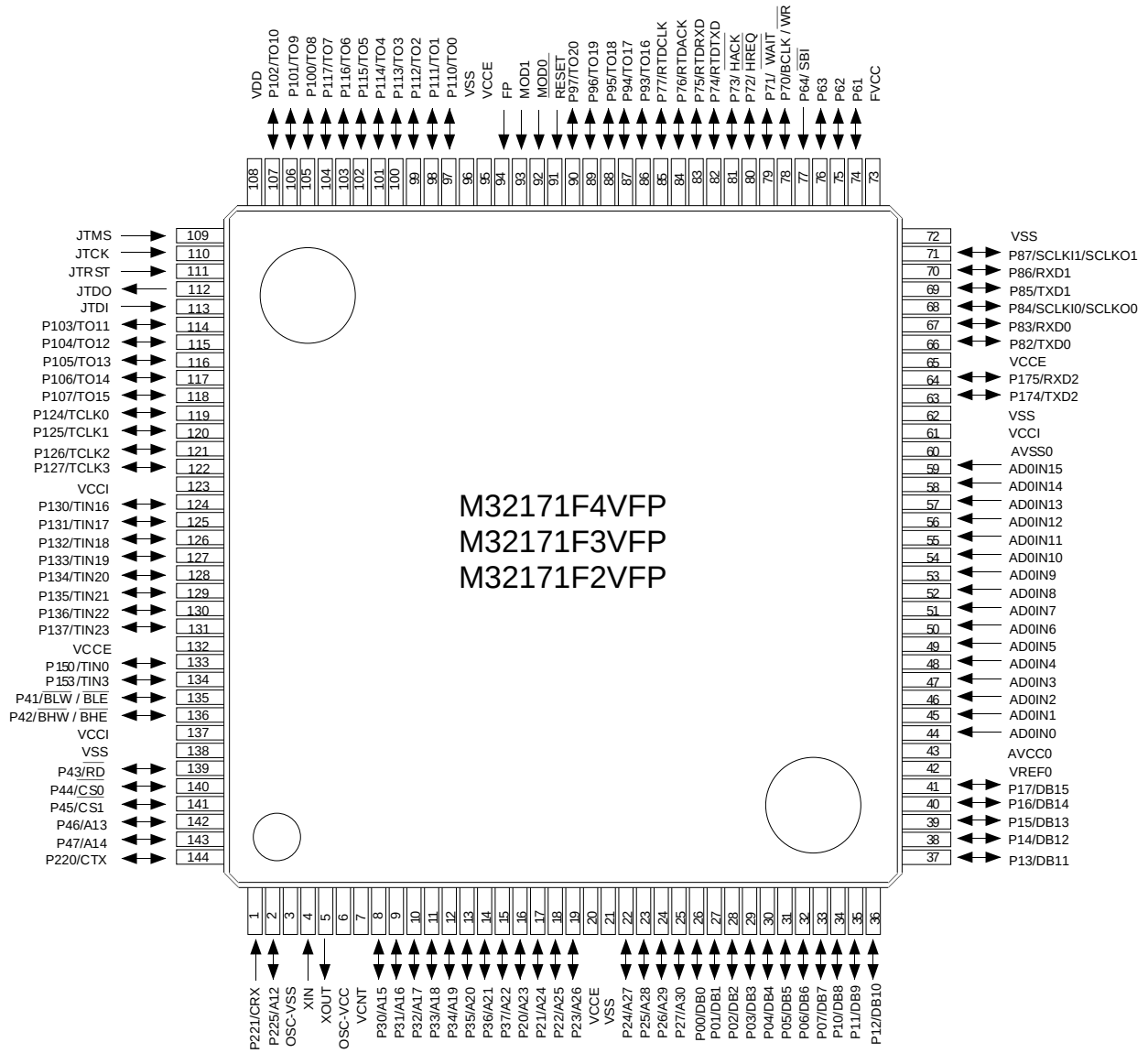
To meet the need for use at high temperatures, the microcomputer is designed to be able to operate in the temperature range of -40 to +125°C when CPU clock operating frequency = 32 MHz. When CPU clock operating frequency = 40 MHz, the microcomputer can be used in the temperature range of -40 to +85°C.

Note: This does not guarantee continuous operation at 125°C. If you are considering use of the microcomputer at 125°C, please consult Mitsubishi.

## Applications

Automobile equipment control (e.g., Engine, ABS, AT), industrial equipment system control, and high-function OA equipment (e.g., PPC)

Pin Assignment(top view)




Package 144P6Q-A

**Figure 1 Pin Layout Diagram of the M32171**

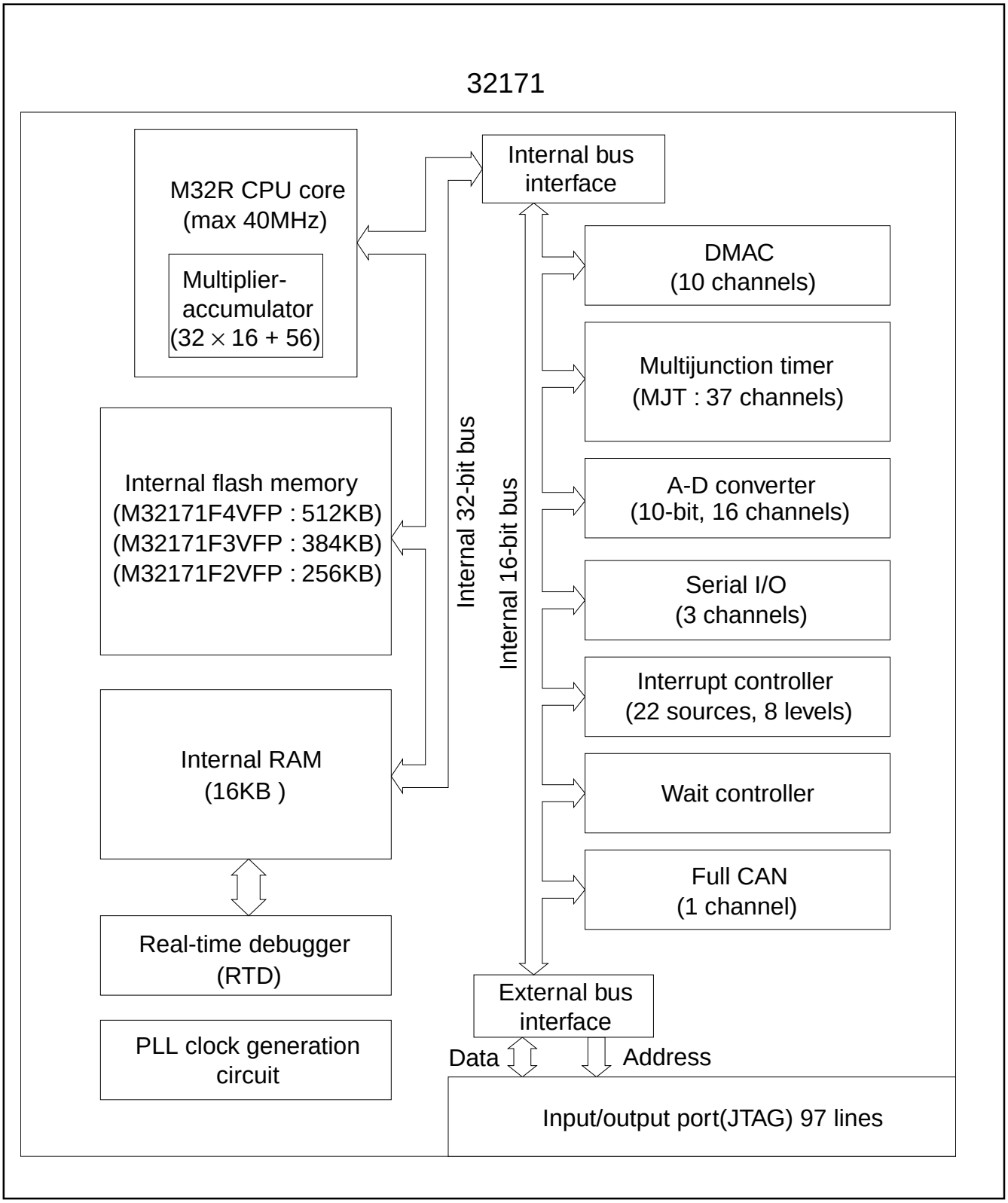



**Figure 2 Block diagram**

**Table 2 Outline Performance (1/2)**

| Functional Block | Features |
|---|---|
| M32R CPU core | M32R family CPU core, internally configured in 32 bits<br>Built-in multiplier-accumulator (32 × 16 + 56)<br>Basic bus cycle : 25 ns (CPU clock frequency at 40 MHz, Internal peripheral clock frequency at 20 MHz)<br>Logical address space : 4G bytes, linear<br>General-purpose register : 32-bit register × 16, Control register: 32-bit register × 5<br>accumulator : 56 bits |
| External data bus | 16 bits data bus |
| Instruction set | 16-bit/32-bit instruction formats<br>83 instructions/ 9 addressing modes |
| Internal flash memory | M32171F4VFP : 512K bytes<br>M32171F3VFP : 384K bytes<br>M32171F2VFP : 256K bytes<br>Rewrite durability : 100 times |
| Internal RAM | 16K bytes |
| DMAC | 10 channels (DMA transfers between internal peripheral I/Os, between internal peripheral I/O and internal RAM, and between internal RAMs)<br>Channels can be cascaded and can operate in combination with internal peripheral I/O |
| Multijunction timer | 37 channels of multijunction timers<br>• 16-bit output-related timers × 11 channels (single-shot, delayed single-shot)<br>• 16-bit input/output-related timers × 10 channels (event count mode, single-shot, PWM, measurement)<br>• 16-bit input-related timers × 8 channels (measurement, event count mode)<br>• 32-bit input-related timers × 8 channels (measurement)<br>Flexible timer configuration is possible through interconnection of channels using the event bus. |
| A-D converter | 10-bit multifunction A-D converters<br>• Input 16 channels<br>• Scan-based conversion can be switched with 4, 8, and 16<br>• Capable of interrupt conversion during scan<br>• 8-bit/10-bit readout function available |
| Serial I/O | 3 channels (The serial I/Os can be set for synchronous serial I/O or UART.<br>SIO2 is UART mode only) |
| Real-time debugger (RTD) | 1-channels dedicated clock-synchronized serial<br>• The entire internal RAM can be read or rewritten from the outside without CPU intervention |
| Interrupt controller | Controls interrupts from internal peripheral I/Os<br>(Priority can be set to one of 8 levels including interrupt disabled) |
| Wait controller | Controls wait when accessing external extended area<br>(1 to 4 wait cycles inserted + prolonged by external WAIT signal input) |
| CAN | 16-channels message slots |
| JTAG | Boundary-Scan function |

**Table 1 Outline Performance (2/2)**

| Function Block | Features |
|---|---|
| Clock | Maximum internal CPU memory clock : 40MHz (access to CPU, internal ROM, andinternal RAM)<br>Maximum internal peripheral clock : 20MHz (access to internal peripheral module)<br>Maximum external input clock : 10.0MHz, Built-in multiply-by-4 PLL circuit |
| Power Supply Voltage | External I/O : 5V (±0.5V) or 3.3V (±0.3V)<br>Internal logic : 3.3V (±0.3V) |
| Operating temperature rang | -40 to +125°C (CPU memory clock 32MHz , internal peripheral clock 16MHz)<br>-40 to +85°C (CPU memory clock 40MHz , internal peripheral clock 20MHz) |
| Package | 0.5mm pitches / 144-pin plastic LQFP |

### Outline of the CPU core

The M32171 Group uses the M32R RISC CPU core, and has an instruction set which is common to all microcomputers in the M32R family.

Instructions are processed in five pipelined stages consisting of instruction fetch, decode, execution, memory access, and write back. Thanks to its "out-of-order-completion" mechanism, the M32R CPU allows for clock cycle efficient, instruction execution control.

The M32R CPU internally has sixteen 32-bit general-purpose registers. The instruction set consists of 83 discrete instructions, which come in either a 16-bit instruction or a 32-bit instruction format. Use of the 16-bit instruction format helps to reduce the code size of a program. Also, the availability of 32-bit instructions facilitates programming and increases the performance at the same clock speed, as compared to architectures with segmented address spaces.

### Sum-of-products instructions comparable to DSP

The M32R CPU contains a multiplier/accumulator that can execute 32 bits $\times$ 16 bits in one cycle. Therefore, it executes a 32 bit $\times$ 32 bit integer multiplication instruction in three cycles.

Also, the M32R CPU supports the following four sum-of-products instructions (or multiplication instructions) for DSP function use.

(1) 16 high-order register bits $\times$ 16 high-order register bits
(2) 16 low-order register bits $\times$ 16 low-order register bits
(3) All 32 register bits $\times$ 16 high-order register bits
(4) All 32 register bits $\times$ 16 low-order register bits

Furthermore, the M32R CPU has instructions for rounding the value stored in the accumulator to 16 or 32 bits, and instructions for shifting the accumulator value to adjust digits before storing in a register. Because these instructions also can be executed in one cycle, DSP comparable data processing capability can be obtained by using them in combination with high-speed data transfer instructions such as Load & Address Update or Store & Address Update.

### Three operation modes

The M32170 and M32174 Group has three operation modes: single-chip mode, external extended mode, and processor mode. These operation modes are changed from one to another by setting the MOD0 and MOD1 pins.

### Address space

The M32171 Group's logical addresses are always handled in 32 bits, providing 4 Gbytes of linear address space. The M32171 Group's address space consists of the following.

### User space

A 2-Gbyte area from H'0000 0000 to H'7FFF FFFF is the user space. Located in this space are the user ROM area, external extended area, internal RAM area, and SFR (Special Function Register) area (internal peripheral I/O registers). Of these, the user ROM area and external extended area are located differently depending on mode settings.

### Boot program space

A 1-Gbyte area from H'8000 0000 to H'BFFF FFFF is the boot program area. This space contains the on-board programming program (boot program) used in blank state by the internal flash memory.

### System space

A 1-Gbyte area from H'C000 0000 to H'FFFF FFFF is the system area. This space is reserved for use by development tools such as an in-circuit emulator and debug monitor, and cannot be used by the user.

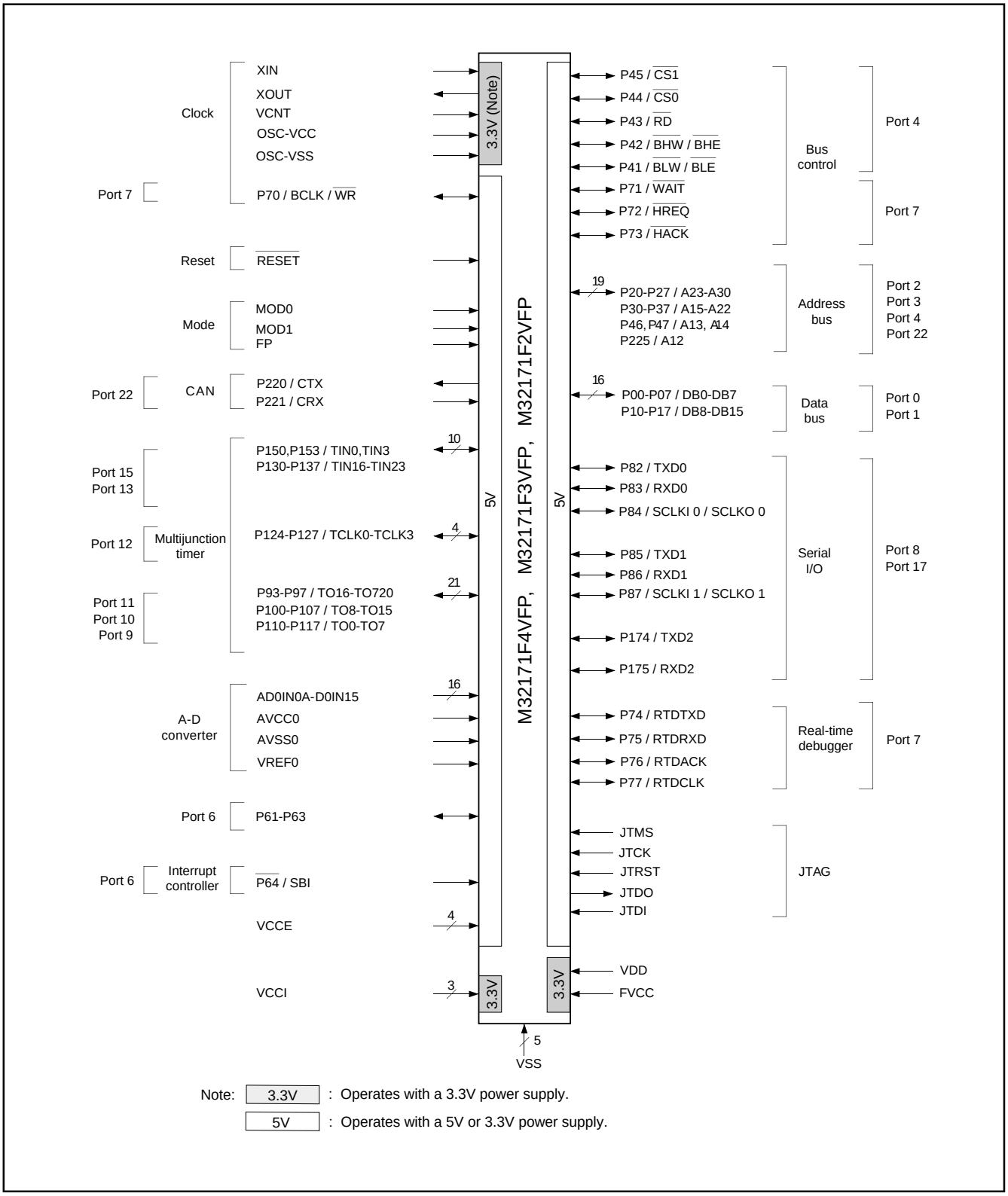



**Figure 3 Pin Function Diagram of 240QFP**

**Table 4 Description of Pin Function (1/4 )**

| Type | Pin Name | Description | Input/Output | Function |
|---|---|---|---|---|
| Power | VCCE | Power supply | — | Supplies power (5 V or 3.3V) to external I/O ports. |
| supply | VCCI | Power supply | — | Supplies power (3.3 V) to the internal logic. |
| | VDD | RAM power supply | — | nternal RAM backup power supply (3.3 V). |
| | FVCC | Flash power supply | — | Internal flash memory backup power supply (3.3 V). |
| | VSS | Ground | — | Connect all VSS pins to ground (GND). |
| Clock | XIN,<br>XOUT | Clock | Input<br>Output | Clock input/output pins. These pins contain a PLL-based frequency multiply-by-4, so input the clock whose frequency is quarter the operating frequency. (XIN input = 10 MHz when CPU clock operates at 40 MHz) |
| | BCLK /<br>$\overline{WR}$ | System clock | Output | When this signal is System Clock(BCLK), it outputs a clock whose is twice that of external inpout clock. (BCLK output = 20 MHz when CPU clock operates at 40 MHz). Use this clock when circuits are synchronized externally.<br>When this signal is Write($\overline{WR}$), during external write access it indicates the valid data on the data bus to transfer. |
| | OSC-VCC | Power supply | — | Power supply to the PLL circuit. Connect OSC-VCC to the power supply(3.3V) |
| | OSC-VSS | Ground | — | Connect OSC-VSS to ground. |
| | VCNT | PLL control | Input | This pin controls the PLL circuit. Connect a resistor and capacitor to this pin. |
| Reset | $\overline{RESET}$ | Reset | Input | This pin resets the internal circuits. |
| Mode | MOD0<br>MOD1 | Mode | Input | These pins set an operation mode.<br>MOD0 / MOD1 / Mode<br>0 / 0 / Single-chip mode<br>0 / 1 / Expanded external mode<br>1 / 0 / Processor mode (Boot mode) (Note)<br>1 / 1 / (Reserved) |
| Address bus | A12-A30 | Address bus | Output | 19 lines of address bus (A12-A30) are provided to accommodate two channels of 1 MB memory space (max.) connected external to the chip. A31 is not output.<br>In the write cycle, of the 16-bit data bus the valid byte positions to write are output as $\overline{BHW}$/ $\overline{BHE}$ and $\overline{BLW}$/ $\overline{BLE}$. In read cycle, data on the entire 16-bit data bus is read. However, only the data at the valid byte positions are transferred to the M32R's internal circuit. |
| Data bus | DB0-DB15 | Data bus | Input/output | This 16-bit data bus connects to external device. |

Note: FP pin should be "H" level in Boot Mode.

**Table 5 Description of Pin Function (2/4)**

| Type | Pin type | Description | Input/Output | Function |
|---|---|---|---|---|
| Bus control | $\overline{CS0}$, CS1 | Chip select | Output | Chip select signals for external devices. |
| | $\overline{RD}$ | Read | Output | This signal is output when reading external devices. |
| | $\overline{BHW}$/ $\overline{BHE}$ | Byte high write | Output | Indicates the byte positions to which valid are transferred when writing to external devices.$\overline{BHW}$/ $\overline{BHE}$ and $\overline{BLW}$/ $\overline{BLE}$ correspond to the upper address side(D0-D7 effective) and the lower address side(D8-D15 effective),respectivel. |
| | $\overline{BLW}$/ $\overline{BLE}$ | Byte low write | Output | |
| | $\overline{WAIT}$ | Wait | Input | If $\overline{WAIT}$ input is low when the M32R accesses external devices, the wait cycle extended. |
| | $\overline{HREQ}$ | Hold request | Input | This pin is used by an external device to request control of the external bus. The M32R goes to a hold state when $\overline{HREQ}$ input is pulled low. |
| | $\overline{HACK}$ | Hold acknowledge | Output | This signal indicates to the external device that the M32R has entered a hold state and relinquished control of the external bus. |
| Multijunction timer | TIN0, TIN3 TIN16-TIN23 | Timer input | Input | Input pins for multijunction timer. |
| | TO0 -TO20 | Timer output | Output | Output pins for multijunction timer. |
| | TCLK0 -TCLK3 | Timer clock | Input | Clock input pins for multijunction timer. |
| A-D converter | AVCC0, | Analog power upply | – | AVCC0 is the power supply for the A-D0 converters.Connect AVCC0 to the power supply (5V or 3.3V). |
| | AVSS0 | Analog ground | – | AVSS0 is the analog ground for the A-D0 converters. Connect AVCC0 to ground |
| | AD0IN0 -AD0IN15 | Analog input | Input | 16-channel analog input pin for A-D0 converter. |
| | VREF0 | Reference voltage input | Input | VREF0 is the reference voltage input pin (5V or 3.3V) for the A-D0 converters. |
| Interrupt controller | $\overline{SBI}$ | System break interrupt | Input | System break interrupt(SBI) input pin of the interrupt controller. |

**Table 6 Description of Pin Functions (3/4)**

| Type | Pin name | Description | Input/output | Function |
|---|---|---|---|---|
| Serial I/O | SCLKI0/ SCLKO0 | UART transmit/ receive clock output or CSIO transmit/receive clock input/output | Input/output | When channel 0 is in UART mode:<br>Clock output derived from BRG output by dividing it by 2<br>When channel 0 is in CSIO mode:<br>Transmit/receive clock input when external clock is selected<br>Transmit/receive clock output when internal clock is selected |
| | SCLKI1/ SCLKO1 | UART transmit/ receive clock output or CSIO transmit/receive clock input/output | Input/output | When channel 1 is in UART mode:<br>Clock output derived from BRG output by dividing it by 2<br>When channel 1 is in CSIO mode:<br>Transmit/receive clock input when external clock is selected<br>Transmit/receive clock output when internal clock is selected |
| | TXD0 | Transmit data | Output | Transmit data output pin for serial I/O channel 0 |
| | RXD0 | Receive data | Input | Receive data input pin for serial I/O channel 0 |
| | TXD1 | Transmit data | Output | Transmit data output pin for serial I/O channel 1 |
| | RXD1 | Receive data | Input | Receive data input pin for serial I/O channel 1 |
| | TXD2 | Transmit data | Output | Transmit data output pin for serial I/O channel 2 |
| | RXD2 | Receive data | Input | Receive data input pin for serial I/O channel 2 |
| Real-Time Debugger | RTDTXD | Transmit data | Output | Serial data output pin of the real-time debugger |
| | RTDRXD | Receive data | Input | Serial data input pin of the real-time debugger |
| | RTDCLK | Clock input | Input | Serial data transmit/receive clock input pin of the real-time debugger |
| | RTDACK | Acknowledge | Output | This pin outputs a low pulse synchronously with the real-time debugger's first clock of serial data output word. The low pulse width indicates the type of the command/data the realtime debugger has received. |
| Flash-only | FP | Flash protect | Input | This pin protects the flash memory against E/W in hardware. |
| CAN | CTX | Transmit data | Output | Data output pin from CAN module. |
| | CRX | Receive data | Input | Data input pin to CAN module. |
| JTAG | JTMS | Test mode | Input | Test select input for controlling the test circuit's state transition |
| | JTCK | Clock | Input | Clock input to the debugger module and test circuit. |
| | JTRST | Test reset | Input | Test reset input for initializing the test circuit asynchronously. |
| | JTDO | Serial output | Output | Serial output of test instruction code or test data. |
| | JTDI | Serial input | Input | Serial input of test instruction code or test data. |

**Table 7 Description of Pin Functions (4/4)**

| Type | Pin name | Description | Input/output | Function |
|---|---|---|---|---|
| Input/ output port (Note) | P00-P07 | Input/output port 0 | Input/output | Programmable input/output port. |
| | P10-P17 | Input/output port 1 | Input/output | Programmable input/output port. |
| | P20-P27 | Input/output port 2 | Input/output | Programmable input/output port. |
| | P30-P37 | Input/output port 3 | Input/output | Programmable input/output port. |
| | P41-P47 | Input/output port 4 | Input/output | Programmable input/output port. |
| | P61-P64 | Input/output port 6 | Input/output | Programmable input/output port. (However, P64 is an input-only port) |
| | P70-P77 | Input/output port 7 | Input/output | Programmable input/output port. |
| | P82-P87 | Input/output port 8 | Input/output | Programmable input/output port. |
| | P93-P97 | Input/output port 9 | Input/output | Programmable input/output port. |
| | P100 -P107 | Input/output port 10 | Input/output | Programmable input/output port. |
| | P110 -P117 | Input/output port 11 | Input/output | Programmable input/output port. |
| | P124 -P127 | Input/output port1 2 | Input/output | Programmable input/output port. |
| | P130 -P137 | Input/output port 13 | Input/output | Programmable input/output port. |
| | P150, P153 | Input/output port 15 | Input/output | Programmable input/output port. |
| | P174, P175 | Input/output port 17 | Input/output | Programmable input/output port. |
| | P220, P221, P225 | Input/output port 22 | Input/output | Programmable input/output port. (However, P221 is an input-only port) |

Note: Input/output port 5 is reserved for future use.

Input/output ports 14, 16, 18, 19, 20, and 21 do not exist.

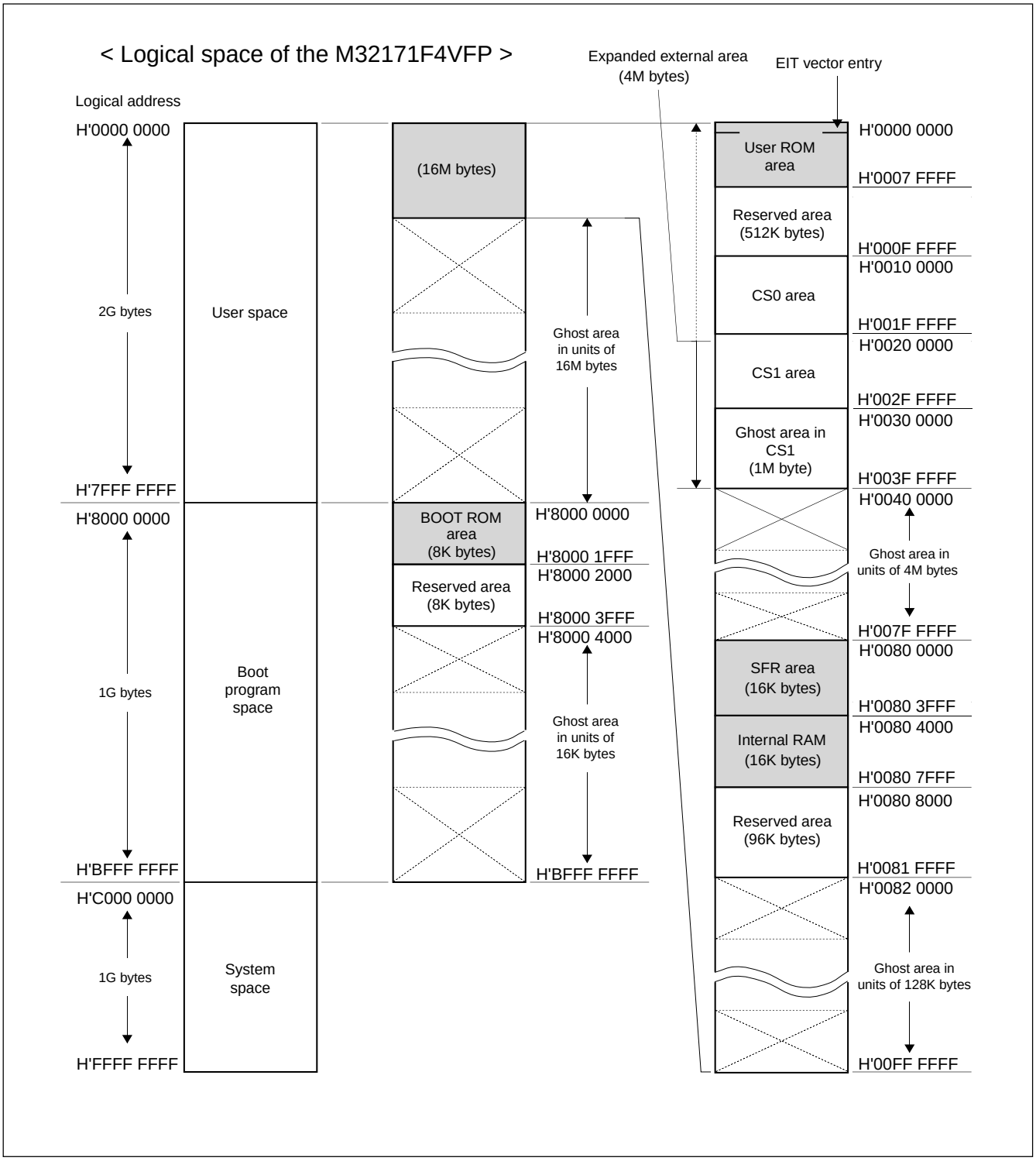



**Figure 4 Address Space of the M32171F4VFP**

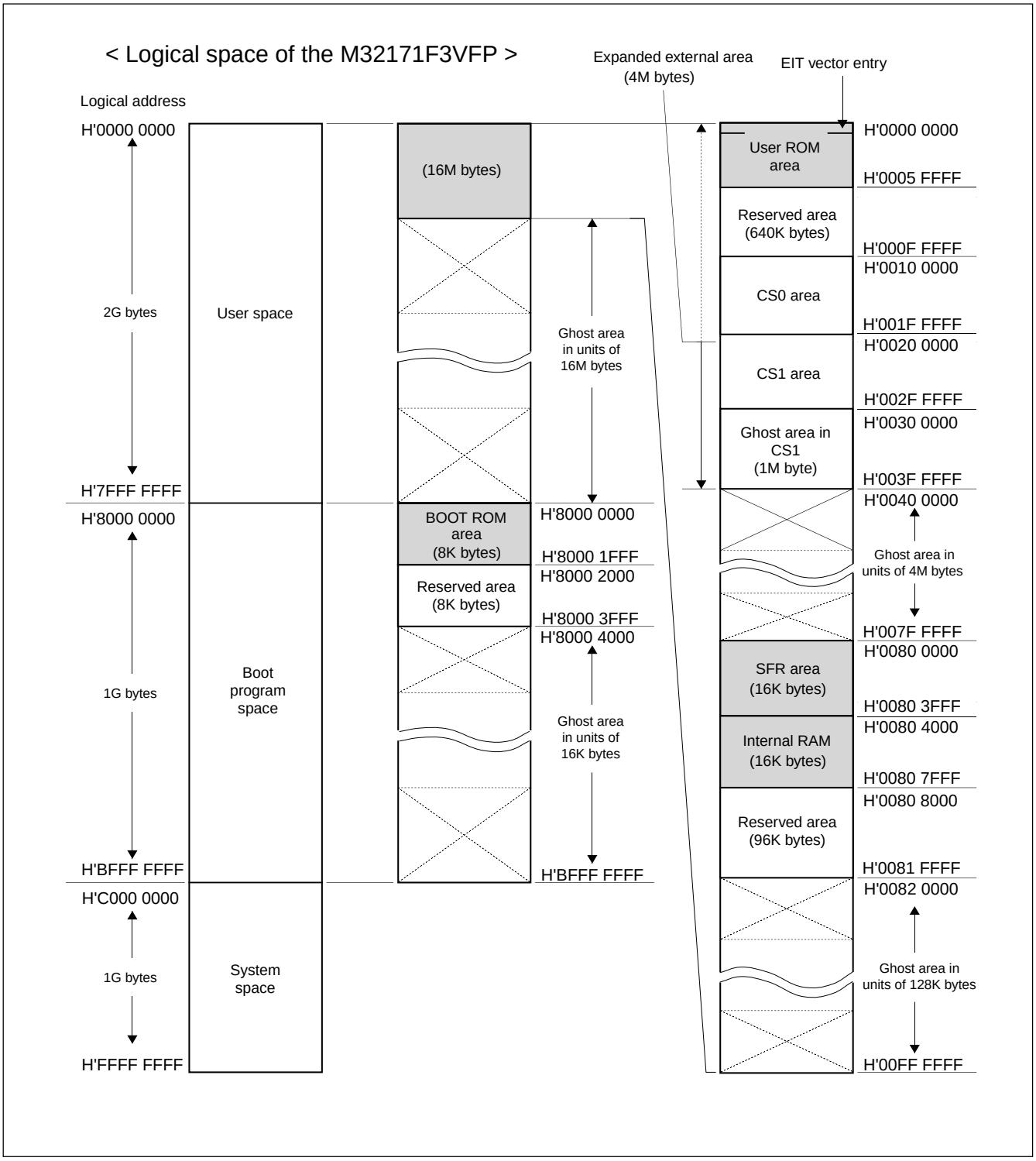



**Figure 5 Address Space of the M32171F3VFP**

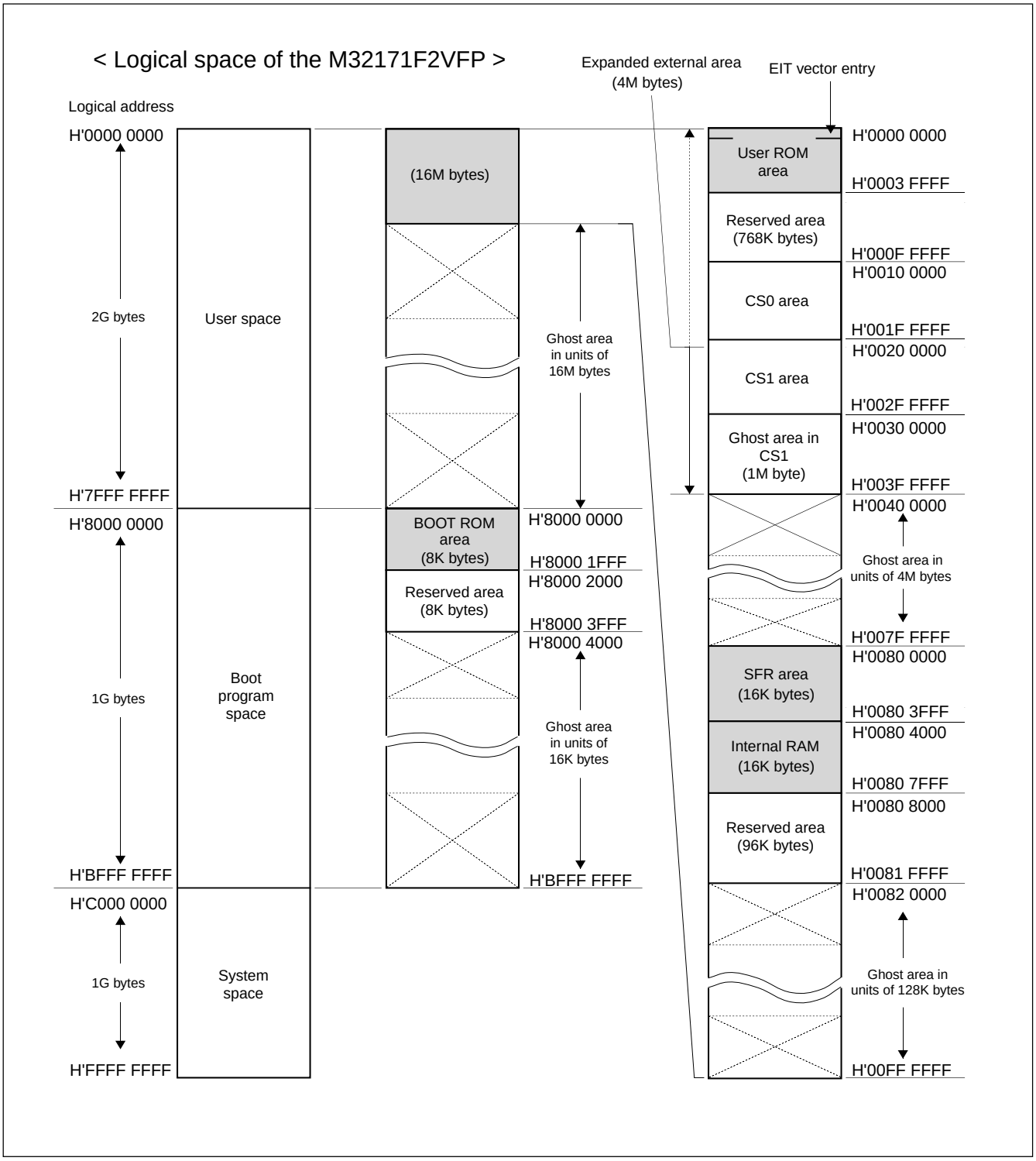
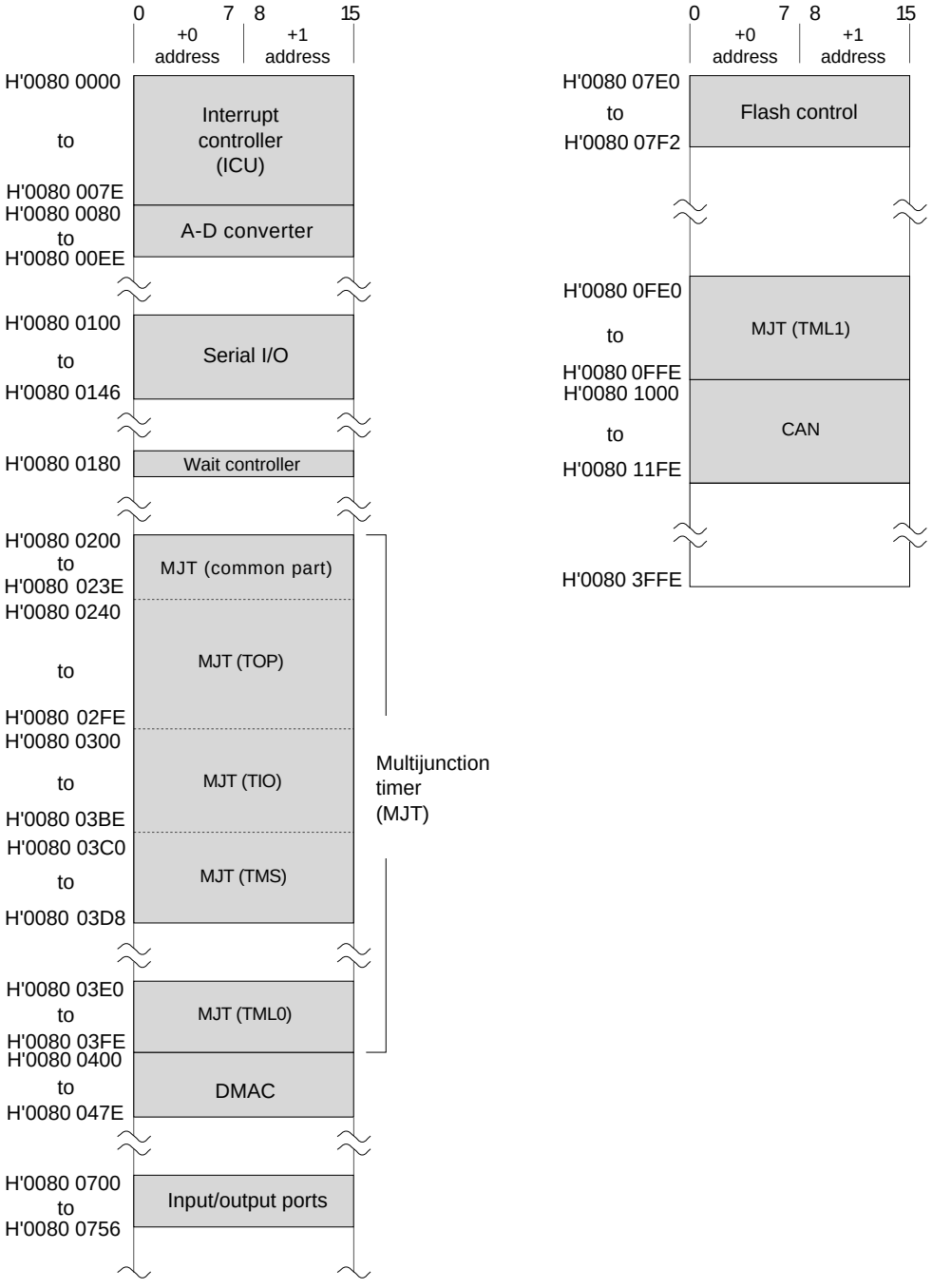



**Figure 6 Address Space of the M32171F2VFP**




Note: The Real-time debugger (RTD) is an independent module operated from external circuits, and is transparent to the CPU.

**Figure 7 SFR Area**

### Built-in Flash Memory and RAM

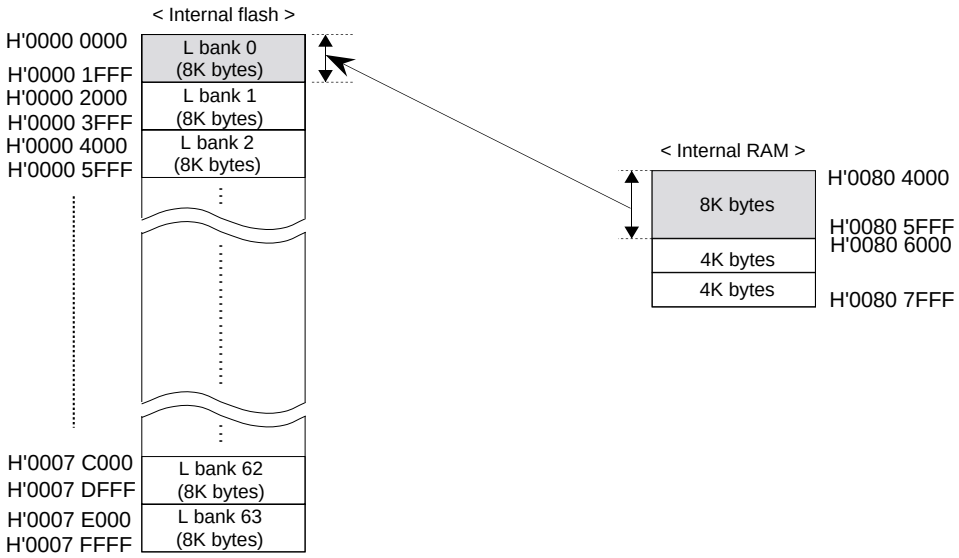
The M32171F4VFP contains 512-Kbyte flash memory and 16-Kbyte RAM. The M32171F3VFP contains 384-Kbyte flash memory and 16-Kbyte RAM. The M32171F2VFP contains 256-Kbyte flash memory and 16-Kbyte RAM.

The internal flash memory can be programmed on-board (i.e., while being mounted on the printed circuit board). This means that the same chip as will be used in mass-production can be used directly from the development stage on, allowing for system development without having to change the printed circuit board when proceeding from trial production to mass-production.

### Built-in Virtual-Flash Emulation Function

Internal flash memory, which is divided from the first address in units of 8 Kbyte (L banks), can be replaced in 8 -Kbyte blocks (H70080 4000-H'0080 5FFF) from the beginning of the internal RAM. And also the internal flash memory, which is divided from the first address in units of 4-Kbyte area (All S banks), can be replaced within two 4 Kbytes areas (H'0080 6000-H'0080 7FFF).

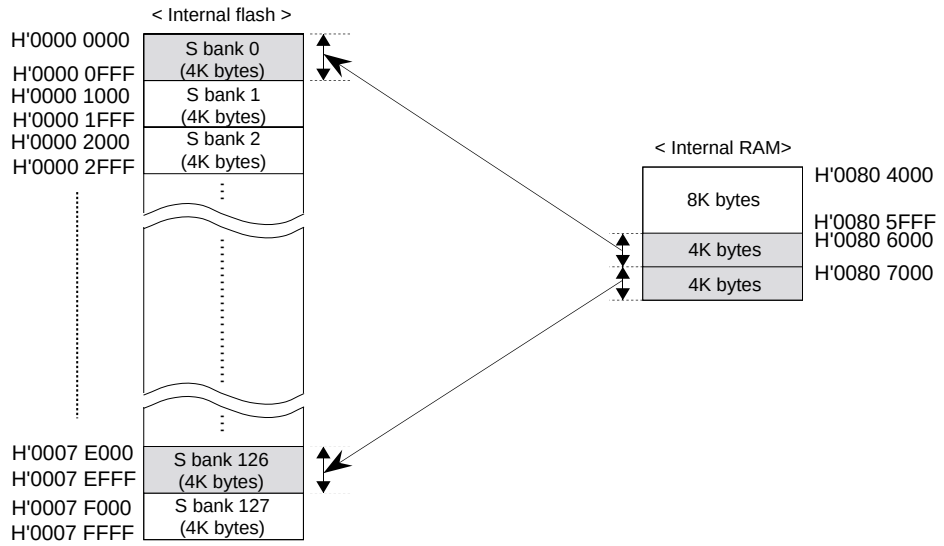
This function allows parts of the program which are frequently changed during development to be altered or evaluated without having to reset the microcomputer each time. What's more, when combined with the realtime debugger, this function helps to reduce the program evaluation period, because data in the RAM can be rewritten without requiring any CPU load.




Note 1: If the same bank area is set in multiple virtual-flash bank registers and the virtual-flash emulation enable bit is enabled, the corresponding internal RAM area is assigned to either bank register according to the priority FELBANK0 > FESBANK0 > FESBANK1.

Note 2: When access is made to the 8-Kbyte area (L bank) specified with pseudo-flash bank register 0, the internal RAM area is accessed. During pseudo-flash emulation mode, RAM data can read and written to and from both the internal RAM area and the virtual-flash setup area.

**Figure 8 Virtual-Flash Emulation Areas of the M32171F4VFP (Replaced in Units of 8 Kbytes)**




Note 1: If the same bank area is set in multiple virtual-flash bank registers and the virtual-flash emulation enable bit is enabled, the corresponding internal RAM area is assigned to either bank register according to the priority FELBANK0 > FESBANK0 > FESBANK1.

Note 2: When access is made to the 4-Kbyte area (S bank) specified with virtual-flash bank registers 0 and 1, the internal RAM area is accessed. During virtual-flash emulation mode, RAM data can read and written to and from both the internal RAM area and the virtual-flash setup area.

**Figure 9 Virtual-Flash Emulation Areas of the M32171F4VFP (Replaced in Units of 4 Kbytes)**

Virtual-Flash Emulation Areas of M32171F4VFP, M32171F3VFP, and M32171F2VFP are shown as follows.

**Table 8 Virtual-Flash Emulation Areas**

| Type Name | Virtual-Flash Emulation Areas |
|---|---|
| M32171F4VFP | H' 0000 0000 - H' 0007 FFFF |
| M32171F3VFP | H' 0000 0000 - H' 0005 FFFF |
| M32171F2VFP | H' 0000 0000 - H' 0003 FFFF |

### Input/output Ports

The microcomputer has a total of 97 input/output ports P0-P22. (However, P5 is reserved for future use, P14, P16, and P18-P21 do not exist.) The input/output ports can be used as input ports or output ports by setting uptheir direction registers.

Each input/output port is a dual-function pin shared with otherinternal peripheral I/O or external extended bus signal lines. These pin functions are selected by using the chip operation mode select or the input/output port operation mode registers. These input/output ports are interfaced using a dedicated power supply to allow for connections to the peripheral circuits operating with 5V or 3.3V.

**Table 9 Outline of Input/output Ports**

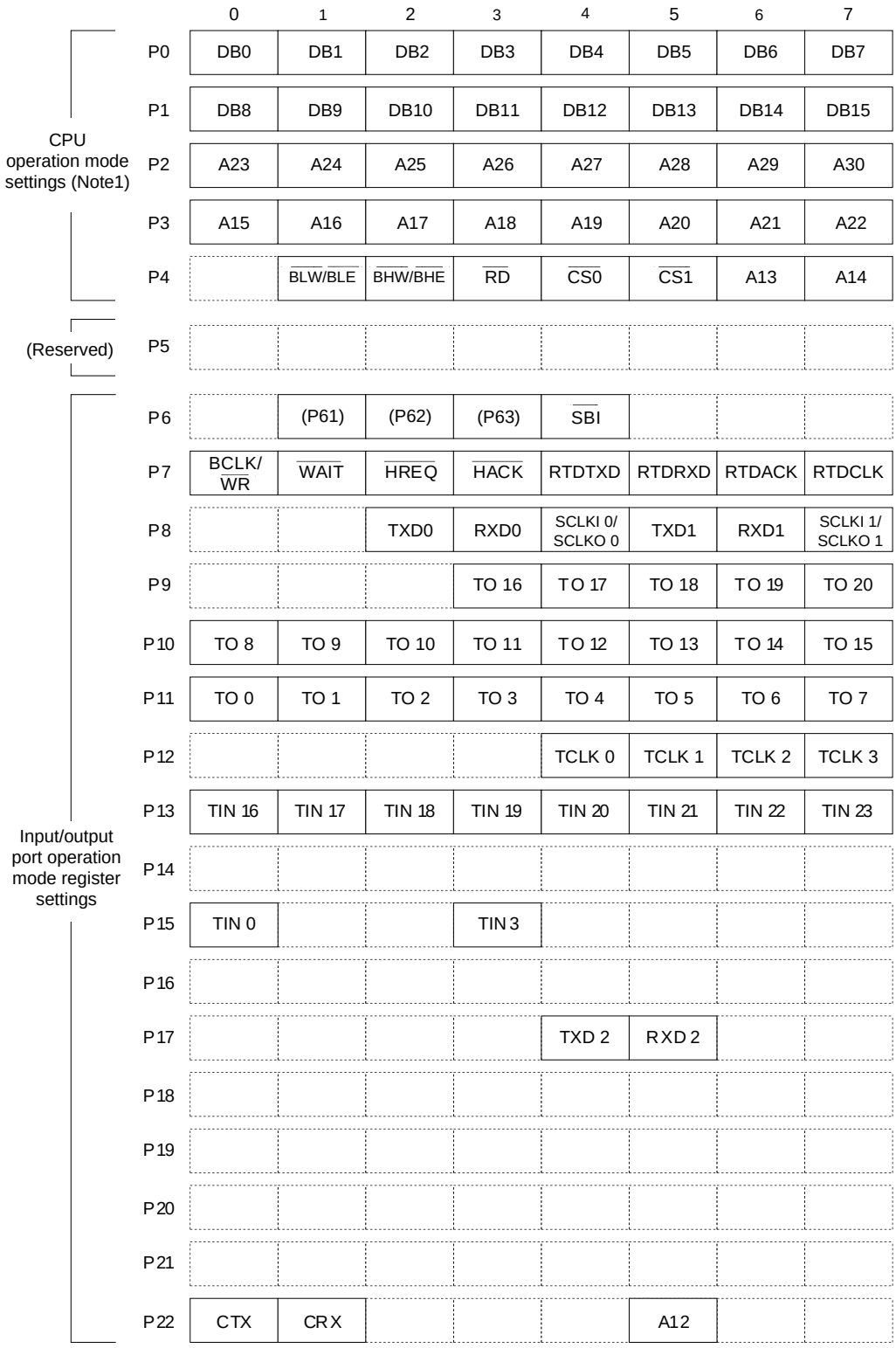
| Item | Specification |
|---|---|
| Number of Port | Total 97 ports<br>P0 : P00 - P07 (8 lines)<br>P1 : P10 - P17 (8 lines)<br>P2 : P20 - P27 (8 lines)<br>P3 : P30 - P37 (8 lines)<br>P4 : P41 - P47 (7 lines)<br>P6 : P61 - P64 (4 lines)<br>P7 : P70 - P77 (8 lines)<br>P8 : P82 - P87 (6 lines)<br>P9 : P93 - P97 (5 lines)<br>P10 : P100 - P107 (8 lines)<br>P11 : P110 - P117 (8 lines)<br>P12 : P124 - P127 (4 lines)<br>P13 : P130 - P137 (8 lines)<br>P15 : P150, P153 (2 lines)<br>P17 : P174, P175 (2 lines)<br>P22 : P220, P221, P225 (3 lines) |
| Port function | The input/output ports can be set for input or output mode bitwise by using the input/output port direction control register. (However, P64 is an $\overline{SBI}$ input-only port, and P221 is CAN input-only port.) |
| Pin function | Dual-functions shared with peripheral I/O or external extended signals (or multi-functions shared with peripheral I/Os which have multiple functions.) |
| Pin function changeover | P0 - P4 : Changed by setting CPU operation mode (MOD0 and MOD1 pins)<br>P6 - 22 : Changed by setting the input/output port operation mode register.<br>(However, peripheral I/O pin functions are selected using the peripheral I/O register.) |

Note: Input/output ports P14, P16, and P18-P21 do not exist.

**Table 10 CPU Operation Modes and P0-P4 Pin Functions**

| MOD0 | MOD1 | Operation mode | Pin functions of P0-P4 |
|---|---|---|---|
| VSS | VSS | Single-chip mode | Input/output port pin |
| VSS | VCCE | External extended mode | External extended signal pin |
| VCCE | VSS | Processor mode (FP pin = VSS) | |
| VCCE | VCCE | Reserved (use inhibited) | – |

Note: VCCE connects to +5V or +3.3V, and VSS connects to GND.




Note 1: The pin function are selected by setting the MOD0 and MOD1 pins.
Note 2: P14, P16, P18, P19, P20, and P21 do not exist.

**Figure 10 Input/output Ports and Pin Function Assignments**

### Built-in 10-Channel DMAC

The microcomputer contains 10 channels of DMAC, allowing for data transfer between internal peripheral I/Os, between internal RAM and internal peripheral I/O, and between internal RAMs.

DMA transfer requests can be issued from the user-cre ated software, as well as can be triggered by a signal generated by the internal peripheral I/O (A-D converter, MJT, or serial I/O).

The microcomputer also supports cascaded connection between DMA channels (starting DMA transfer on a channel at end of transfer on another channel). This makes advanced transfer processing possible without causing any additional CPU load.

**Table 11 Outline of the DMAC**

| Item | Content |
|---|---|
| Number of channels | 10 channels |
| Transfer request | • Software trigger<br>• Request from internal peripheral I/O: A-D converter, multijunction timer, or serial I/O (reception completed, transmit buffer empty)<br>• Cascaded connection between DMA channels possible (Note) |
| Maximum number of times transferred | 256 times |
| Transferable address space | • 64 Kbytes (address space from H'0080 0000 to H'0080 FFFF)<br>• Transfers between internal peripheral I/Os, between internal RAM and internal peripheral IO, and between internal RAMs are supported |
| Transfer data size | 16 bits or 8 bits |
| Transfer method | Single transfer DMA (control of the internal bus is relinquished for each transfer performed), dual-address transfer |
| Transfer mode | Single transfer mode |
| Direction of transfer | One of three modes can be selected for the source and destination of transfer:<br>• Address fixed<br>• Address increment<br>• 32-channel ring buffer |
| Channel priority | Channel 0 > channel 1 > channel 2 > channel 3 > channel 4 > channel 5 > channel 6 > channel 7 > channel 8 > channel 9 (Fixed priority) |
| Maximum transfer rate | 13.3 Mbytes per second (when internal peripheral clock = 20 MHz) |
| Interrupt request | Group interrupt request can be generated when each transfer count register underflows |
| Transfer area | 64 Kbytes from H'0080 0000 to H'0080 FFFF (Transfer is possible in the entire internal RAM/SFR area) |

Note: The following DMA channels can be cascaded.

DMA transfer on channel 1 started at end of one DMA transfer on channel 0
DMA transfer on channel 2 started at end of one DMA transfer on channel 1
DMA transfer on channel 0 started at end of one DMA transfer on channel 2
DMA transfer on channel 4 started at end of one DMA transfer on channel 3
DMA transfer on channel 6 started at end of one DMA transfer on channel 5
DMA transfer on channel 7 started at end of one DMA transfer on channel 6
DMA transfer on channel 5 started at end of one DMA transfer on channel 7
DMA transfer on channel 9 started at end of one DMA transfer on channel 8
DMA transfer on channel 5 started at end of all DMA transfers on channel 0 (underflow of transfer count register)

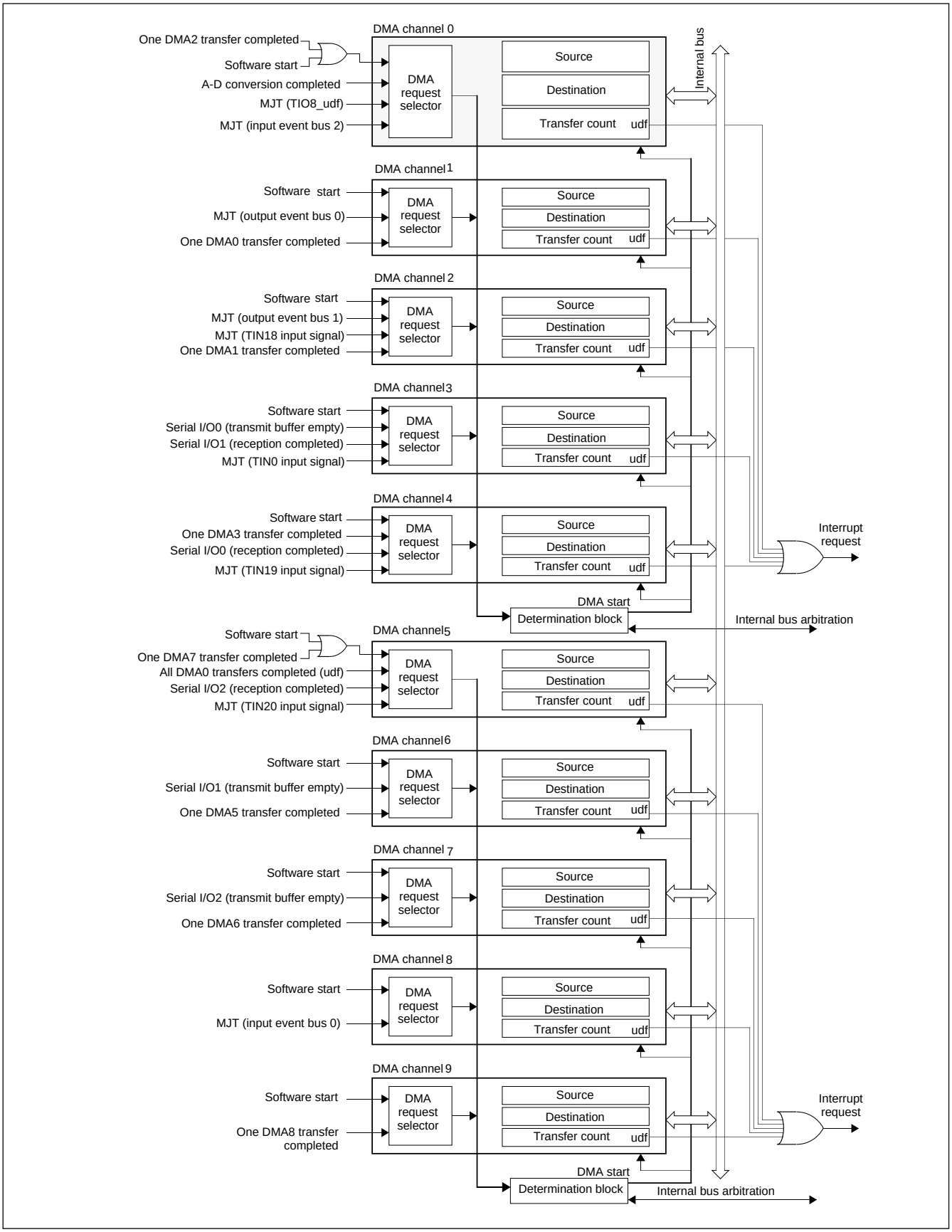



**Figure 11 Block Diagram of the DMAC**

### Built-in 37-Channel Multijunction Timers (MJT)

The microcomputer contains a total of 37 channels of multijunction timers consisting of 11 channels of 16-bit output related timers, 10 channels of 16-bit input/output related timers, eight channels of 16-bit input related timers, eight channels of 32-bit input related timers, Each timer has multiple operation modes to choose from, depending on the purposes of use.

Also, the maltijunction timers internally have a clock bus, input event bus, and an output event bus, so that multiple timers can be used in combination allowing for a flexible timer configuration.

The output related timers have a correcting function that allows the timer's count value to be incremented or decremented as necessary while count is in progress, making real time output control possible.

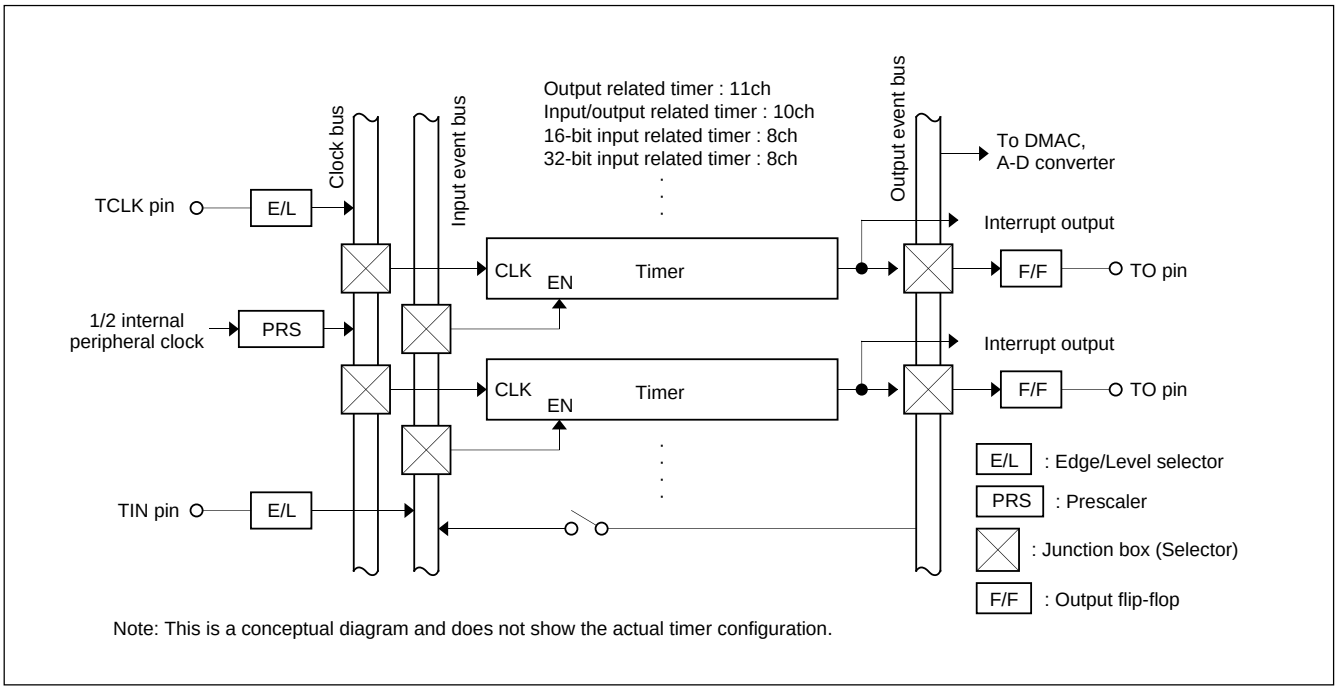



**Figure 12 Conceptual Diagram of the Multijunction Timer (MJT)**

**Table 12 Outline of Multijunction Timers**

| Name | Type | Number of channels | Content |
|---|---|---|---|
| TOP<br>(Timer Output) | Output-related<br>16-bit timer<br>(down-counter) | 11 | One of three input modes can be selected in software.<br>< With correction function ><br>• Single-shot output mode<br>• Delayed single-shot output mode<br>< Without correction function ><br>• Continuous output mode |
| TIO<br>(Timer<br>Input Output) | Input/output-related<br>16-bit timer<br>(down-counter) | 10 | One of three input modes or four output modes can be selected by software.<br>< Input modes ><br>• Measure clear input mode<br>• Measure free-run input mode<br>• Noise processing input mode<br>< Output mode without correction function<br>• PWM output mode<br>• Single-shot output mod<br>• Delayed single-shot output mode<br>• Continuous output mode |
| TMS<br>(Timer<br>Measure Small) | Input-related<br>16-bit timer<br>(up counter) | 8 | 16-bit input measure timer. |
| TML<br>(Timer<br>Measure Large) | Input-related<br>32-bit timer<br>(up counter) | 8 | 32-bit input measure timer. |

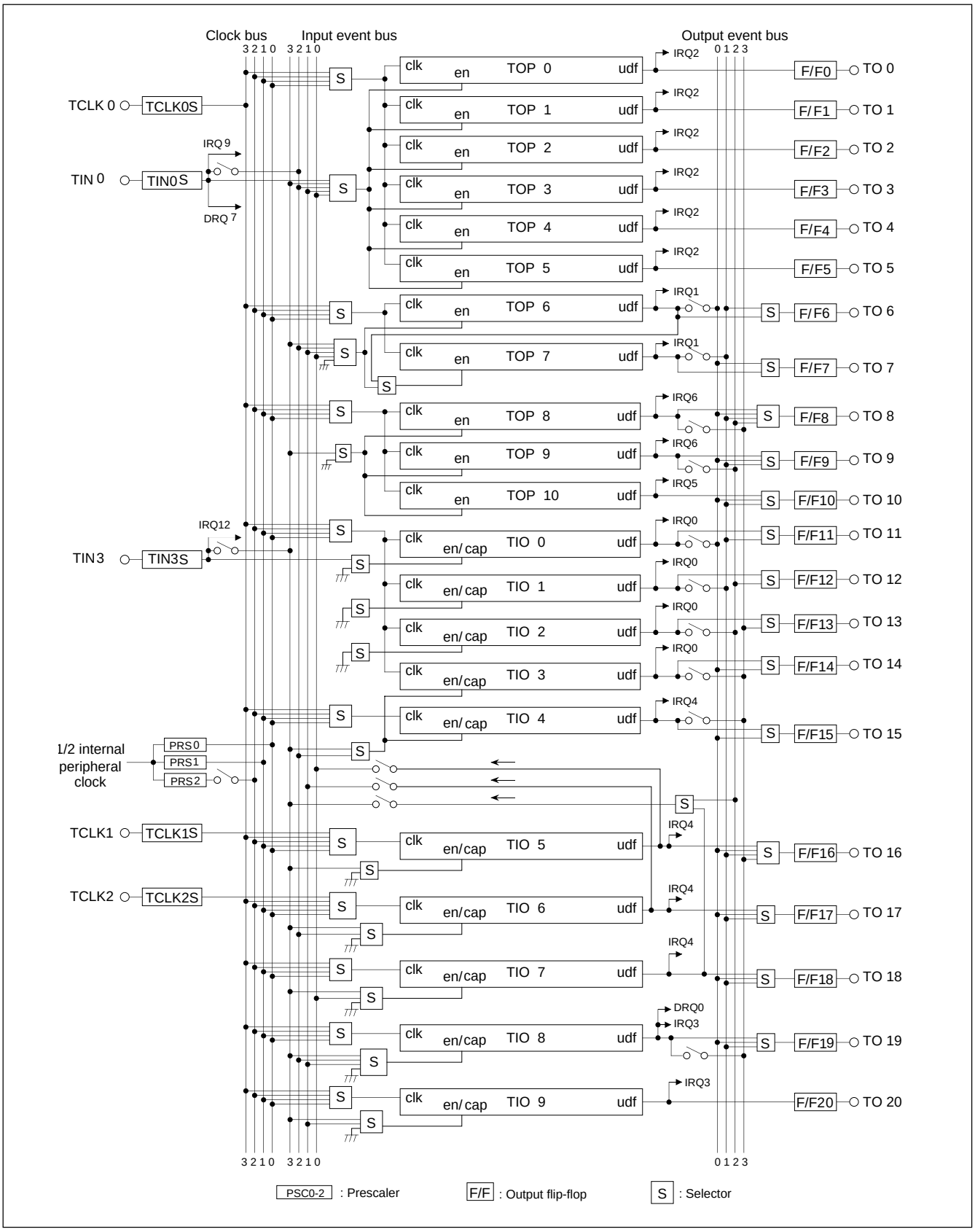



**Figure 13 Block Diagram of Multijunction Timers (MJT) (1/3)**

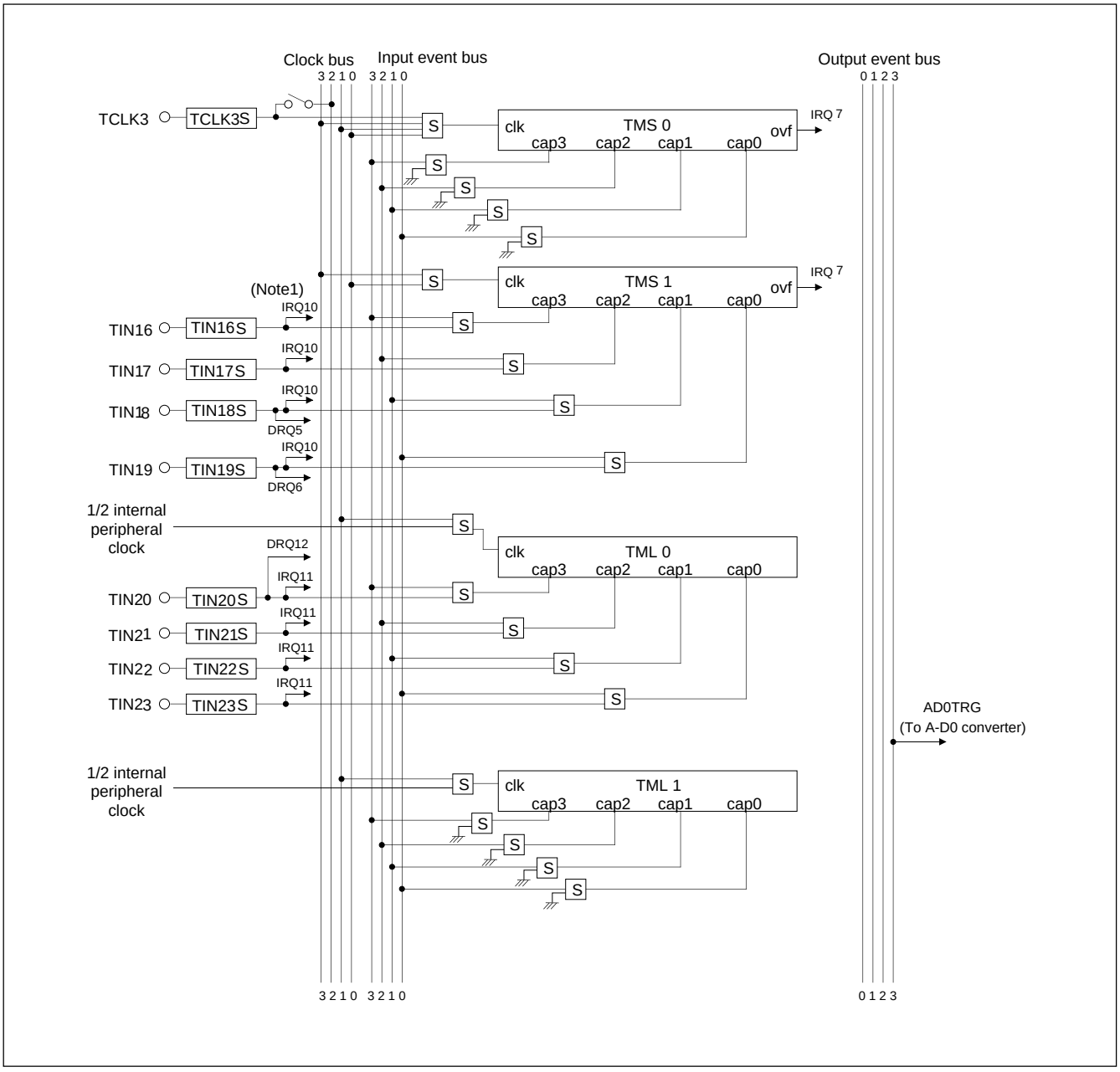



**Figure 14 Block Diagram of Multijunction Timers (MJT) (2/3)**

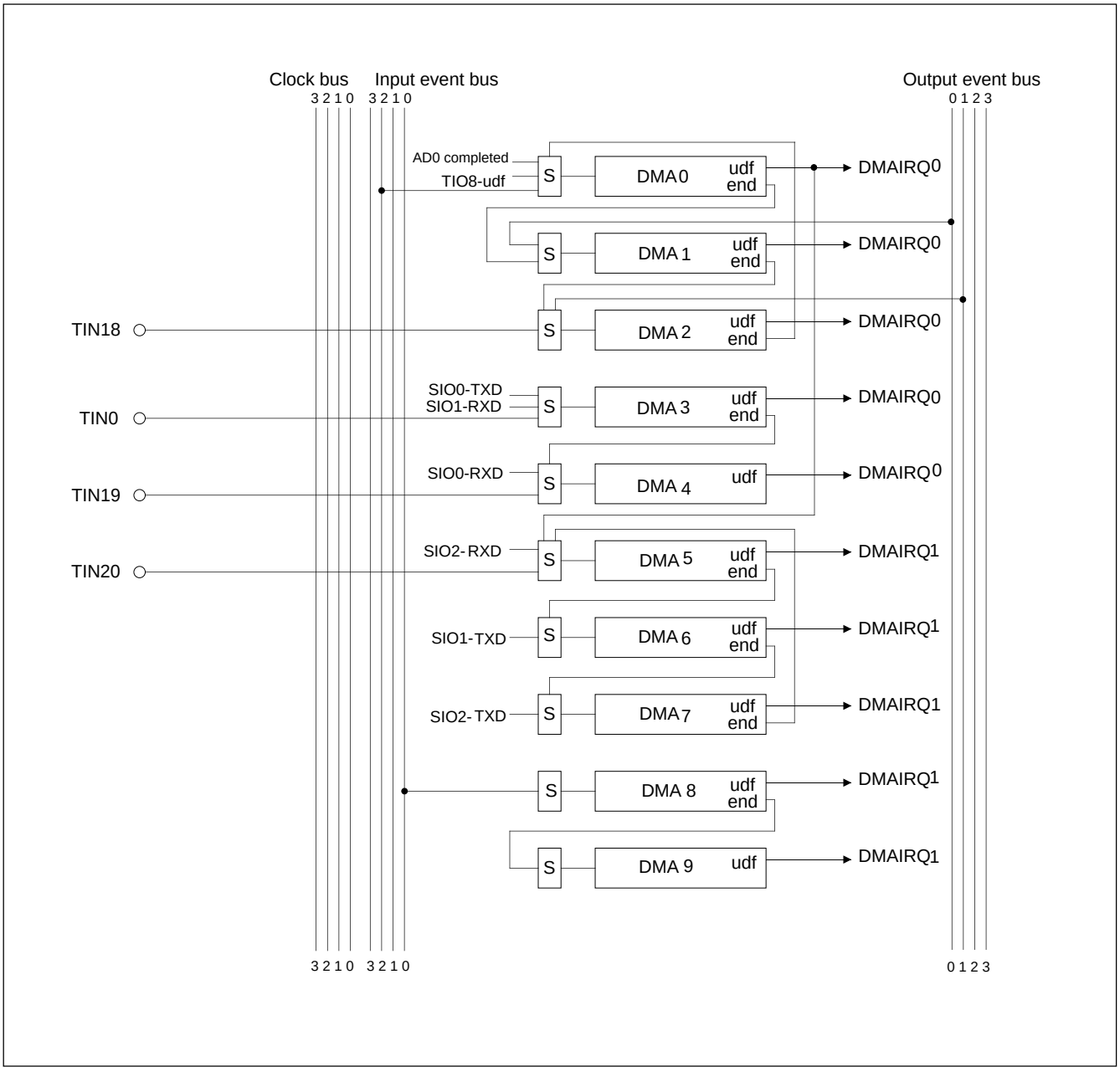



**Figure 15 Block Diagram of Multijunction Timers (MJT) (3/3)**

### Built-in Two Independent A-D Converters

The microcomputer contains two 16-channel converters with 10-bit resolution (A-D0 converter and A-D1 converter). In addition to single conversion on each channel, continuous A-D conversion on a combined group of 4, 8, and 16 channels is possible. The A-D converted value can be read out in either 10 bits or 8 bits.

In addition to ordinary A-D conversion, the converters support comparator mode in which the set value and A-D converted value are compared to determine which is larger or smaller than the other.

When A-D conversion is finished, the converters can generated a DMA transfer request, as well as an interrupt.

The A-D converters are interfaced using a dedicated power supply to allow for connections to the peripheral circuits operating with 5V or 3.3V.

**Table 13 Outline of the A-D Converters**

| Item | Content | | |
|---|---|---|---|
| Analog input | 16 channels | | |
| A-D conversion method | Successive approximation method. | | |
| Resolution | 10 bits (Conversion results can be read out in either 10 or 8 bits.) | | |
| Absolute accuracy (Conditions: Ta = -40 ~ +125°C, AVCC0 = VREF0 = 5.12V) (Note 1) | Normal rate mode | ±2 LSB | |
| | Double rate mode | ±2 LSB | |
| Conversion mode | A-D conversion mode,comparator mode | | |
| Operation mode | Single mode, scan mode | | |
| Scan mode | Single -shot scan mode, continuous scan mode. | | |
| Conversion start trigger | Software start | Started by setting A-D conversion start bit to 1. | |
| | Hardware start | A-D0 converter started by MJT output event bus 3. | |
| Conversion rate f(BCLK) : Internal peripheral clock operating frequency (Note 2) | During single mode (Shortest time ) | Normal | 299 × 1/ f (BCLK) |
| | | Double speed | 173 × 1/ f (BCLK) |
| | During comparator mode (Shortest time ) | Normal | 47 × 1/ f (BCLK) |
| | | Double speed | 29 × 1/ f (BCLK) |
| Interrupt request generation | When A-D conversion is finished, when comparate operation is finished, when single-shot scan is finished, or when one cycle of continuous scan is finished. | | |
| DMA transfer request generation | When A-D conversion is finished, when comparate operation is finished, when single-shot scan is finished, or when one cycle of continuous scan is finished. | | |

Note 1: The rated value of conversion accuracy here is that of the microcomputer's own as a single unit which can be exhibited when the microcomputer is used in an environment where it may not be affected by the power supply wiring or noise on the board.

Note 2: When input clock (XIN) = 10 MHz, f(BCLK) = 20 MHz.

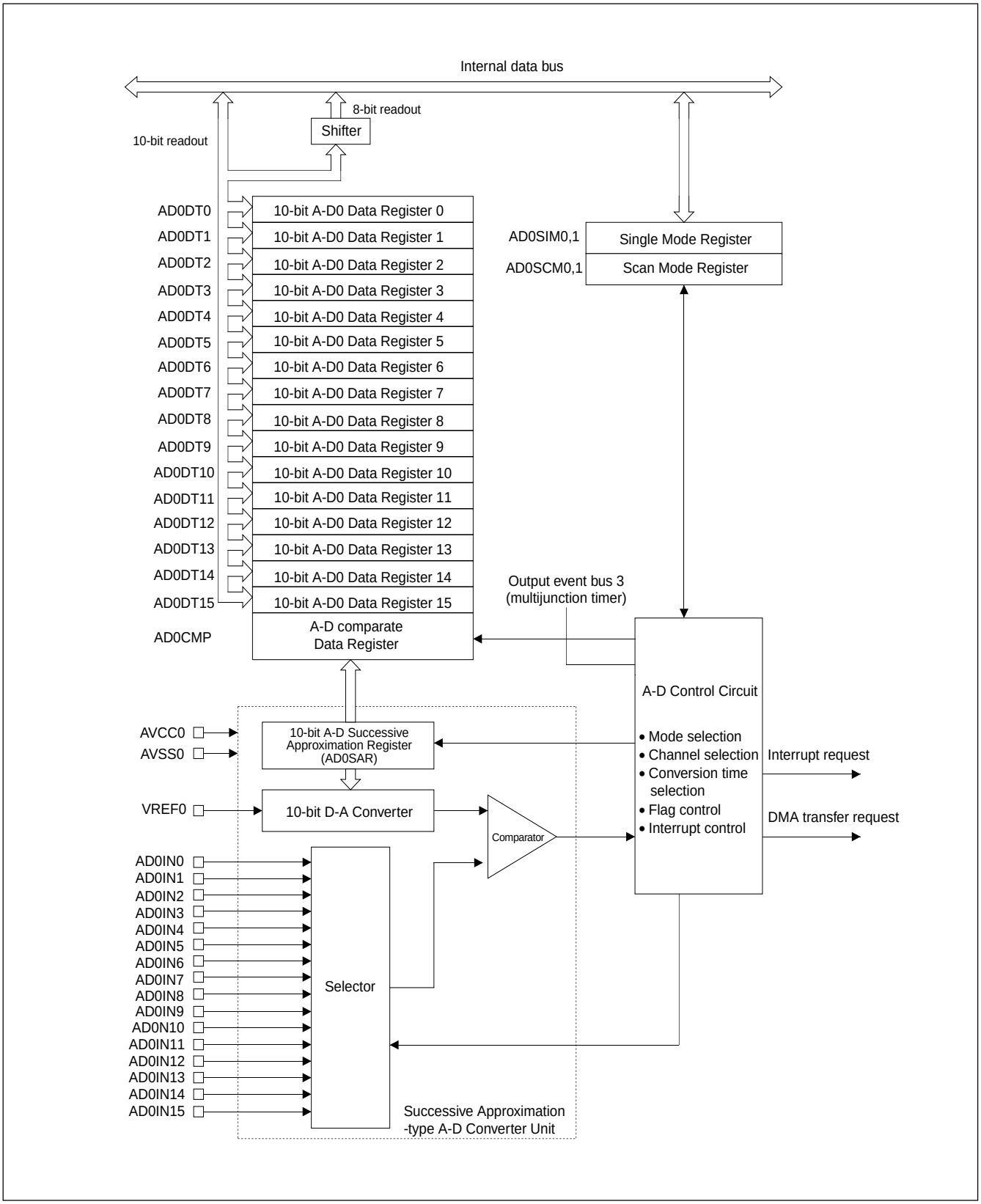



**Figure 16 Block Diagram of the A-D0 Converter**

### 3-channel High-speed Serial I/Os

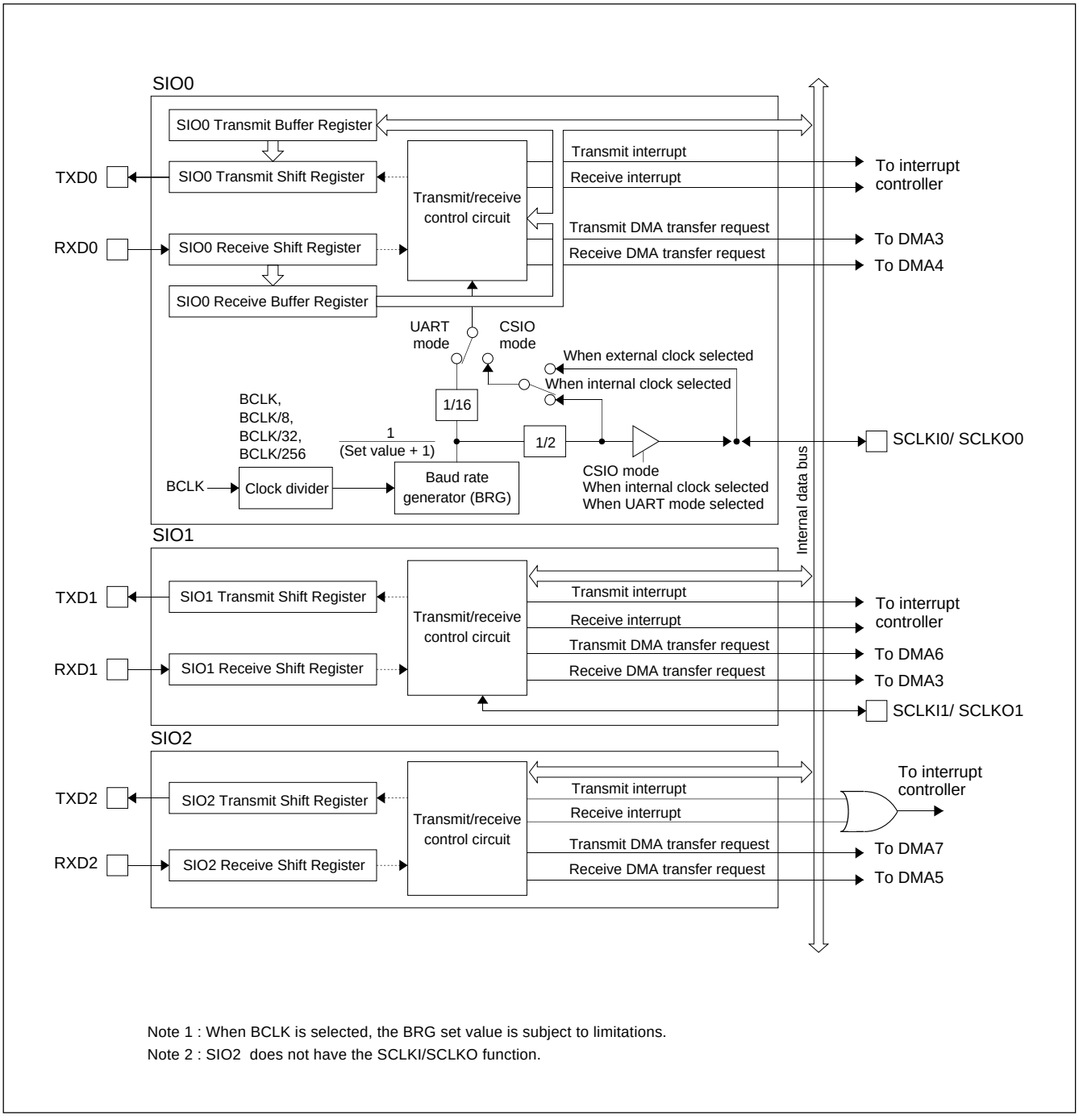
The microcomputer contains three channels of serial I/Os consisting of two channels that can be set for CSIO mode (clock-synchronized serial I/O) or UART mode (asynchronous serial I/O) and one other channel that can only be set for UART mode.

The SIO has the function to generate a DMA transfer request when data reception is completed or the transmit register becomes empty, and is capable of high-speed serial communication without causing any additional CPU load.

**Table 14 Outline of Serial I/O**

| Item | Content |
|---|---|
| Number of channels | CSIO/UART: 2 channels (SIO0,SIO1)<br>UART only : 1 channels (SIO2) |
| Clock | During CSIO mode : Internal clock / external clock, selectable (Note1)<br>During UART mode : Internal clock only |
| Transfer mode | Transmit half-duplex, receive half-duplex, transmit/receive full-duplex |
| BRG count sourcef | (BCLK), f(BCLK)/8, f(BCLK)/32, f(BCLK)/256 (When internal clock is selected) (Note2) |
| Data format | CSIO mode : Data length = Fixed to 8 bits<br>Order of transfer = Fixed to LSB first<br>UARTmode : Start bit = 1 bit<br>Character length = 7, 8, or 9 bits<br>Parity bit = Added or not added (When added, selectable between odd and even parity)<br>Stop bit = 1 or 2 bits<br>Order of transfer = Fixed to LSB first |
| Baud rate | CSIO mode : 152 bits per second to 2 Mbits per second (when operating with f(BCLK) = 20 MHz)<br>UARTmode : 19 bits per second to 156 Kbits per second (when operating with f(BCLK) = 20 MHz) |
| Error detection | CSIO mode : Overrun error only<br>UARTmode : Overrun, parity, and framing errors<br>(The error-sum bit indicates which error has occurred) |
| Fixed cycle clock output function | When using SIO0 and SIO1 as UART, this function outputs a divided-by-2 BRG clock from the SCLK pin. |

Note 1: During CSIO mode, the maximum input frequency of an external clock is f(BCLK) divided by 16.
Note 2: When f(BCLK) is selected for the BRG count source, the BRG set value is subject to limitations.




Note 1 : When BCLK is selected, the BRG set value is subject to limitations.
Note 2 : SIO2 does not have the SCLKI/SCLKO function.

**Figure 17 Block Diagram of Serial I/O**

### CAN Module

The M32171 Group contains two Full CAN modules compliant with CAN Specification V2.0B (CAN0 and CAN1), each of which has 16-channel message slots and three mask registers.

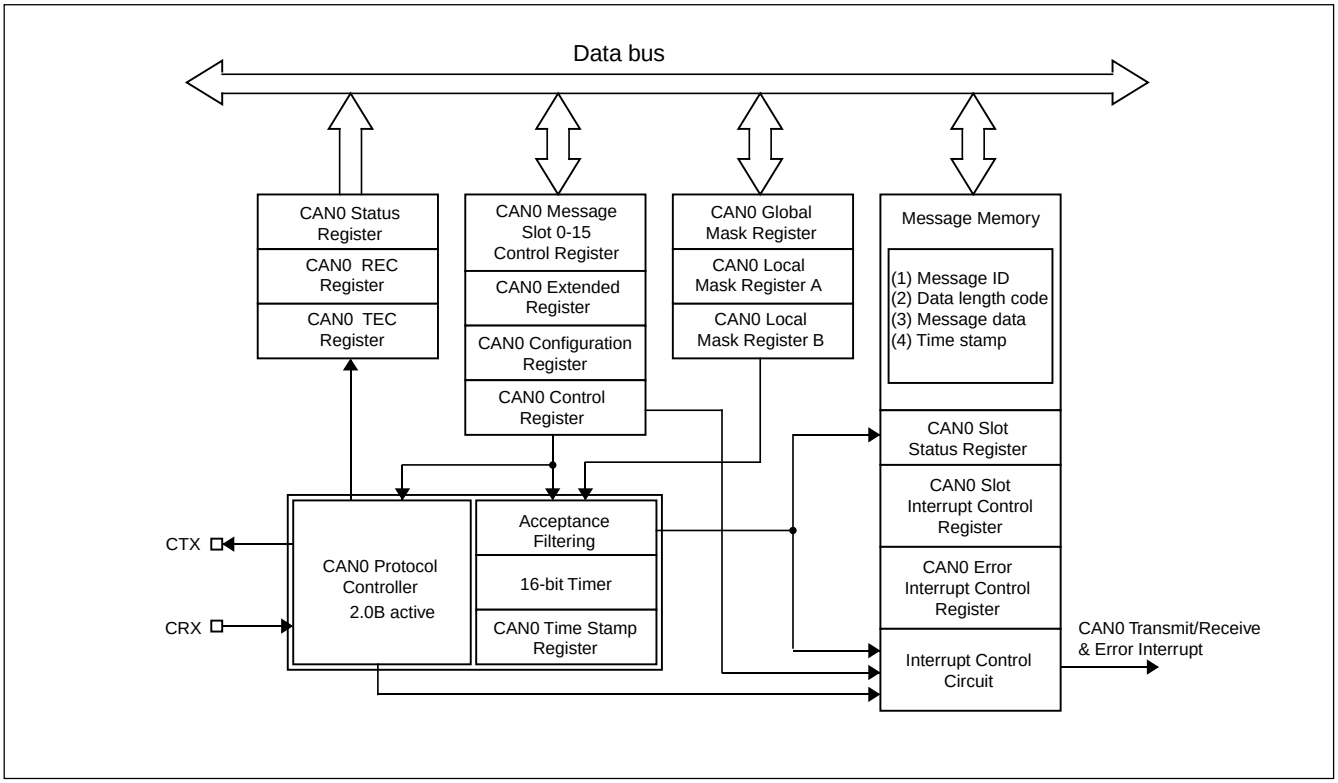



**Figure 18 Block Diagram of the CAN Module**

### 8-level Interrupt Controller

The Interrupt Controller controls interrupt requests from each internal peripheral I/O (31 sources) by using eight priority levels assigned to each interrupt source, including interrupts disabled. In addition to these interrupts, it handles System Break Interrupt (SBI), Reserved Instruction Exception (RIE), and Address Exception (AE) as nonmaskable interrupts.

### Wait Controller

The Wait Controller supports access to external devices.
For access to an external extended area of up to 1 Mbytes (during external extended or processor mode), the Wait Controller controls bus cycle extension by inserting one to four wait cycles or using external $\overline{\text{WAIT}}$ signal input.

### Realtime Debugger (RTD)

The Realtime Debugger (RTD) provides a function for accessing directly from the outside to the internal RAM. It uses a dedicated clock-synchronized serial I/O to communicate with the outside.
Use of the RTD communicating via dedicated serial lines allows the internal RAM to be read out and rewritten without having to halt the CPU.

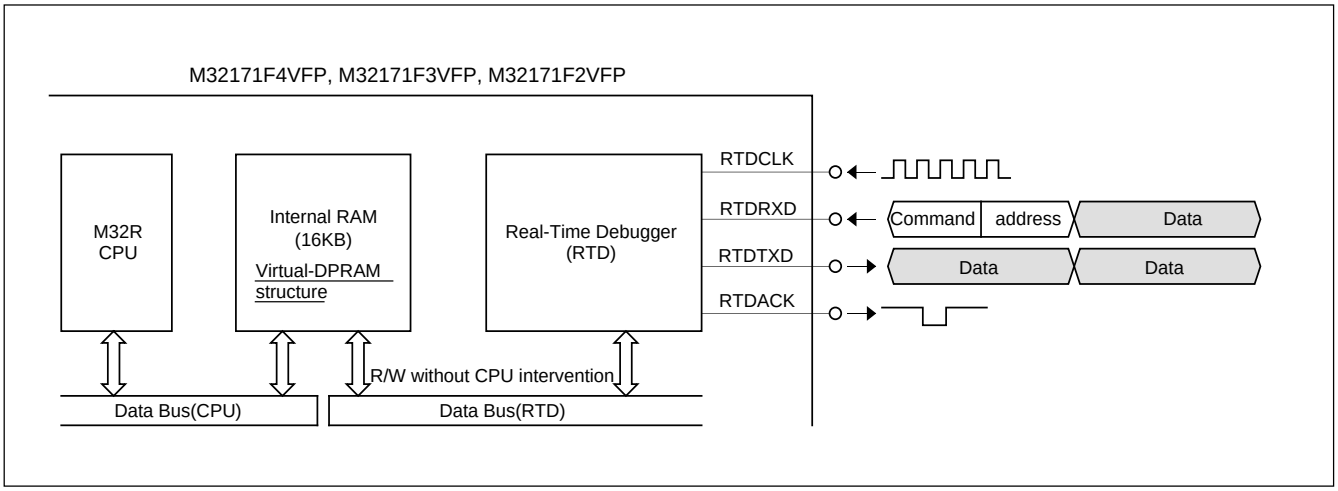



**Figure 19 Conceptual Diagram of the Realtime Debugger (RTD)**

### CPU Instruction Set

The M32R employs a RISC architecture, supporting a total of 83 discrete instructions.

#### (1) Load/store instructions

Perform data transfer between memory and registers.

| | |
|---|---|
| LD | Load |
| LDB | Load byte |
| LDUB | Load unsigned byte |
| LDH | Load halfword |
| LDUH | Load unsigned halfword |
| LOCK | Load locked |
| ST | Store |
| STB | Store byte |
| STH | Store halfword |
| UNLOCK | Store unlocked |

#### (2) Transfer instructions

Perform register to register transfer or register to immediate transfer.

| | |
|---|---|
| LD24 | Load 24-bit immediate |
| LDI | Load immediate |
| MV | Move register |
| MVFC | Move from control register |
| MVTC | Move to control register |
| SETH | Set high-order 16-bit |

#### (3) Branch instructions

Used to change the program flow.

| | |
|---|---|
| BC | Branch on C-bit |
| BEQ | Branch on equal |
| BEQZ | Branch on equal zero |
| BGEZ | Branch on greater than or equal zero |
| BGTZ | Branch on greater than zero |
| BL | Branch and link |
| BLEZ | Branch on less than or equal zero |
| BLTZ | Branch on less than zero |
| BNC | Branch on not C-bit |
| BNE | Branch on not equal |
| BNEZ | Branch on not equal zero |
| BRA | Branch |
| JL | Jump and link |
| JMP | Jump |
| NOP | No operation |

#### (4) Arithmetic/logic instructions

Perform comparison, arithmetic/logic operation, multiplication/division, or shift between registers.

• Comparison

| | |
|---|---|
| CMP | Compare |
| CMPI | Compare immediate |
| CMPU | Compare unsigned |
| CMPUI | Compare unsigned immediate |

• Logical operation

| | |
|---|---|
| AND | AND |
| AND3 | AND 3-operand |
| NOT | Logical NOT |
| OR | OR |
| OR3 | OR 3-operand |
| XOR | Exclusive OR |
| XOR3 | Exclusive OR 3-operand |

• Arithmetic operation

| | |
|---|---|
| ADD | Add |
| ADD3 | Add 3-operand |
| ADDI | Add immediate |
| ADDV | Add (with overflow checking) |
| ADDV3 | Add 3-operand |
| ADDX | Add with carry |
| NEG | Negate |
| SUB | Subtract |
| SUBV | Subtract (with overflow checking) |
| SUBX | Subtract with borrow |

• Multiplication/division

| | |
|---|---|
| DIV | Divide |
| DIVU | Divide unsigned |
| MUL | Multiply |
| REM | Remainder |
| REMU | Remainder unsigned |

• Shift

| | |
|---|---|
| SLL | Shift left logical |
| SLL3 | Shift left logical 3-operand |
| SLLI | Shift left logical immediate |
| SRA | Shift right arithmetic |
| SRA3 | Shift right arithmetic 3-operand |
| SRAI | Shift right arithmetic immediate |
| SRL | Shift right logical |
| SRL3 | Shift right logical 3-operand |
| SRLI | Shift right logical immediate |

#### (5) Instructions for the DSP function

Perform 32 bit × 16 bit or 16 bit × 16 bit multiplication or sum-of-products calculation. These instructions also perform rounding of the accumulator data or transfer between accumulator and general-purpose register.

| | |
|---|---|
| MACHI | Multiply-accumulate high-order halfwords |
| MACLO | Multiply-accumulate low-order halfwords |
| MACWHI | Multiply-accumulate word and high-order halfword |
| MACWLO | Multiply-accumulate word and low-order halfword |
| MULHI | Multiply high-order halfwords |
| MULLO | Multiply low-order halfwords |
| MULWHI | Multiply word and high-order halfword |
| MULWLO | Multiply word and low-order halfword |
| MVFACHI | Move from accumulator high-order word |
| MVFACLO | Move from accumulator low-order word |
| MVFACMI | Move from accumulator middle-order word |
| MVTACHI | Move to accumulator high-order word |
| MVTACLO | Move to accumulator low-order word |
| RAC | Round accumulator |
| RACH | Round accumulator halfword |

#### (6) EIT related instructions

Start trap or return from EIT processing.

| | |
|---|---|
| RTE | Return from EIT |
| TRAP | Trap |

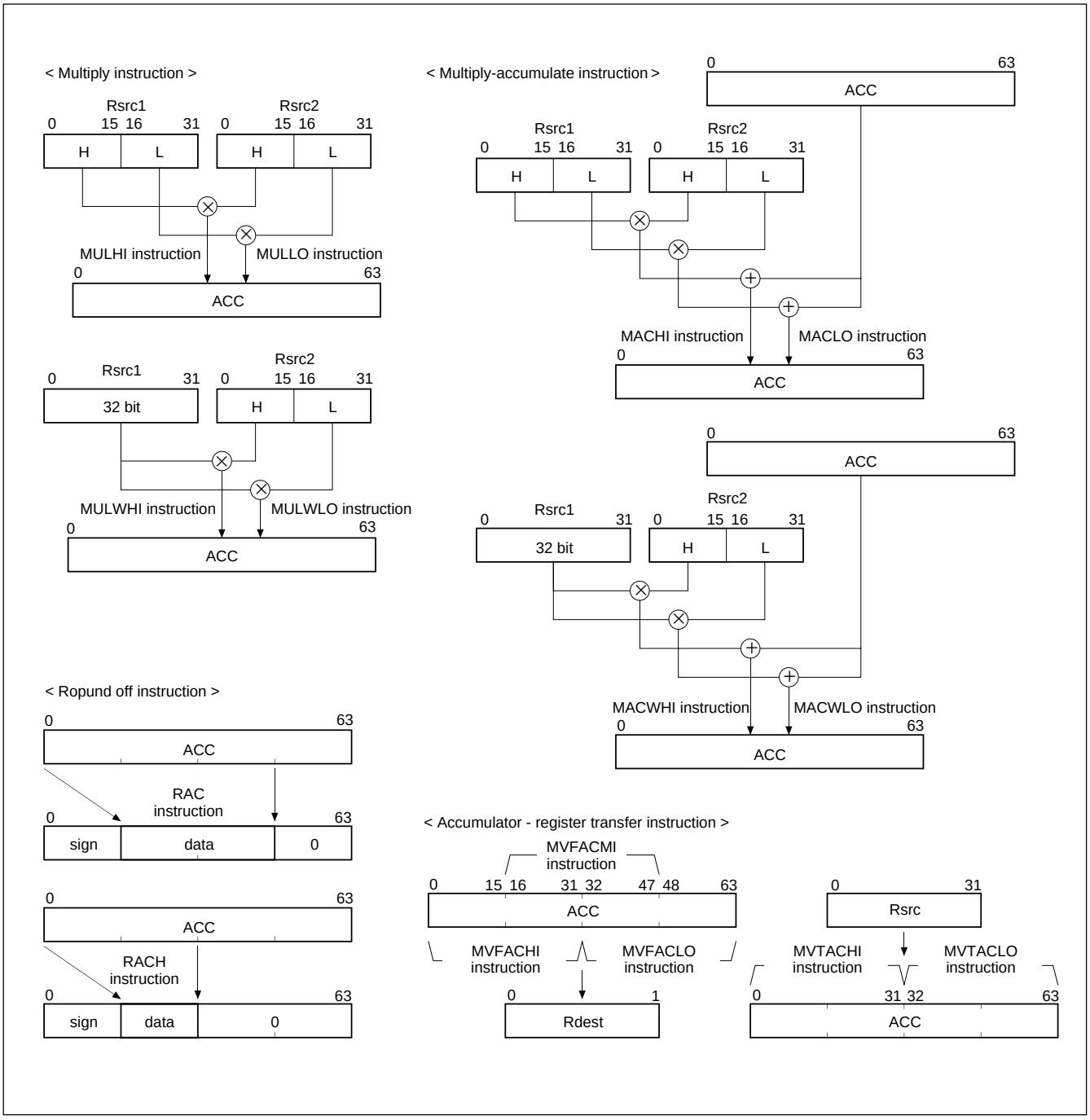


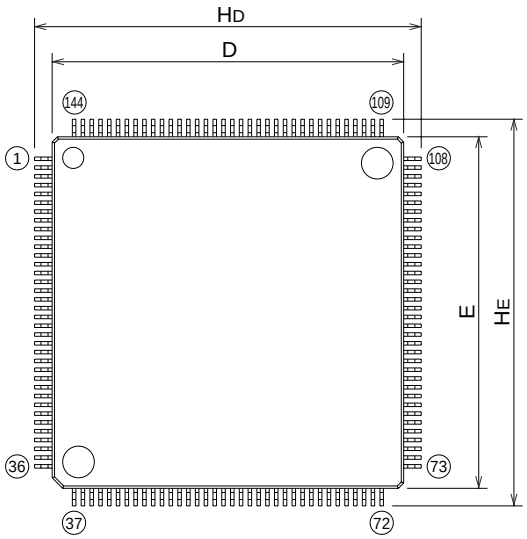

**Figure 20 Instructions for the DSP Function**

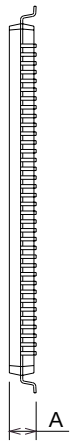
## Package Dimensions Diagram

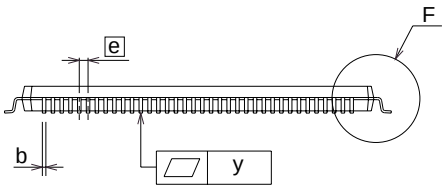
### 144P6Q-A

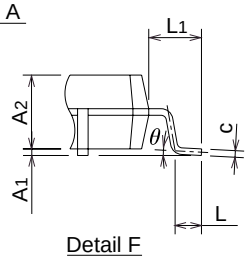
**Plastic 144pin 20×20mm body LQFP**

| EIAJ Package Code | JEDEC Code | Weight(g) | Lead Material |
|---|---|---|---|
| LQFP144-P-2020-0.50 | – | | Cu Alloy |

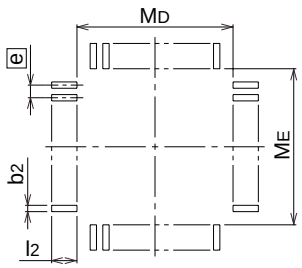



Detail F




Recommended Mount Pad

| Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | – | – | 1.7 |
| A1 | 0.05 | 0.125 | 0.2 |
| A2 | – | 1.4 | – |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.105 | 0.125 | 0.175 |
| D | 19.9 | 20.0 | 20.1 |
| E | 19.9 | 20.0 | 20.1 |
| e | – | 0.5 | – |
| HD | 21.8 | 22.0 | 22.2 |
| HE | 21.8 | 22.0 | 22.2 |
| L | 0.35 | 0.5 | 0.65 |
| L1 | – | 1.0 | – |
| y | – | – | 0.1 |
| θ | 0° | – | 8° |
| b2 | – | 0.225 | – |
| l2 | 1.0 | – | – |
| MD | – | 20.4 | – |
| ME | – | 20.4 | – |

Mitsubishi Microcomputers

# 32171 Group

SINGLE-CHIP 32-BIT CMOS MICROCOMPUTER

MITSUBISHI ELECTRIC CORPORATION
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MITSUBISHI ELECTRIC

| Revision Description List | 32171Group Data Sheet |
|---|---|

| Rev. No. | Revision Description | | Rev. date |
|---|---|---|---|
| | Page | Point | |
| 1.0 | | First Edition | 010514 |
| | | | |