

MITSUBISHI MICROCOMPUTERS M35052-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

The M35052-XXXSP/FP is TV screen display control IC which can be used to display information such as number of channels, the date and messages and program schedules on the TV screen.

In particular, owing to the built-in SYNC-SEP (synchronous separation) circuit, the synchronous correction circuit, the Decoder circuit, and to the Encoder circuit, external circuits can be decrease and character turbulence that occurs when superimposing can be reduced. The processor can conform to the EDS broadcast service and is suitable for AV systems such as VTRs, LDs, and so on.

It is a silicon gate CMOS process and M35052-XXXSP is housed in a 20-pin shrink DIP package, M35052-XXXFP is housed in a 20-pin shrink SOP package.

For M35052-001SP/FP that is a standard ROM version of M35052-XXXSP/FP respectively, the character pattern is also mentioned.

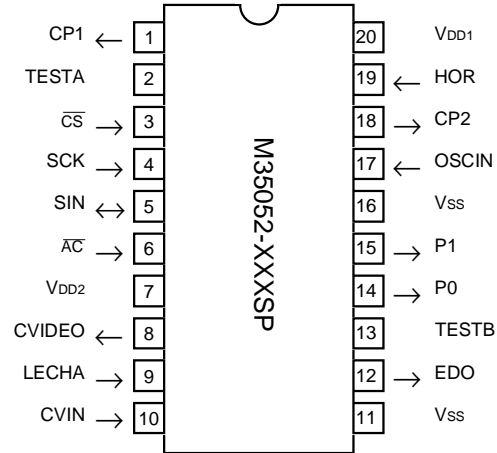
FEATURES

- Screen composition 24 characters X 10 lines,
32 characters X 7 lines
- Number of characters displayed 240 (Max.)
- Character composition 12 X 18 dot matrix
- Characters available 128 characters
- Character sizes available 4 (horizontal) X 4 (vertical)
- Display locations available
Horizontal direction 240 locations
Vertical direction 256 locations
- Blinking Character units
Cycle : approximately 1 second, or approximately 0.5 seconds
Duty : 25%, 50%, or 75%
- Data input By the serial input (16 bits)
- Coloring
Background coloring (composite video signal)
- Blanking
Total blanking (14 X 18 dots)
Border size blanking
Character size blanking
- Synchronizing signal
Composite synchronizing signal generation
(PAL, NTSC, M-PAL)
- 2 output ports (1 digital line)
- Oscillation stop function
It is possible to stop the oscillation for synchronizing signal generation
- Built-in half-tone display function
- Built-in reversed character display function
- Built-in Decoder (NTSC only)
- Built-in Encoder (NTSC only)
- Built-in synchronous correction circuit
- Built-in synchronous separation circuit

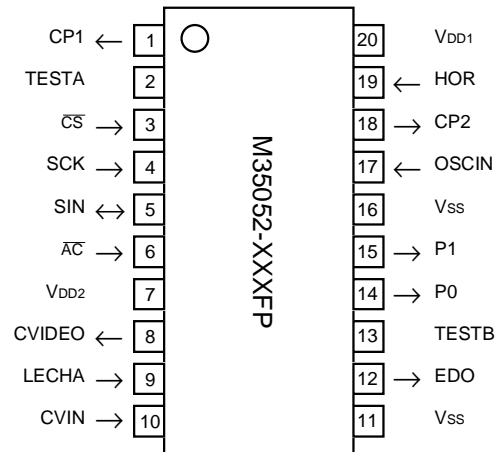
APPLICATION

TV, VCR, Movie

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B

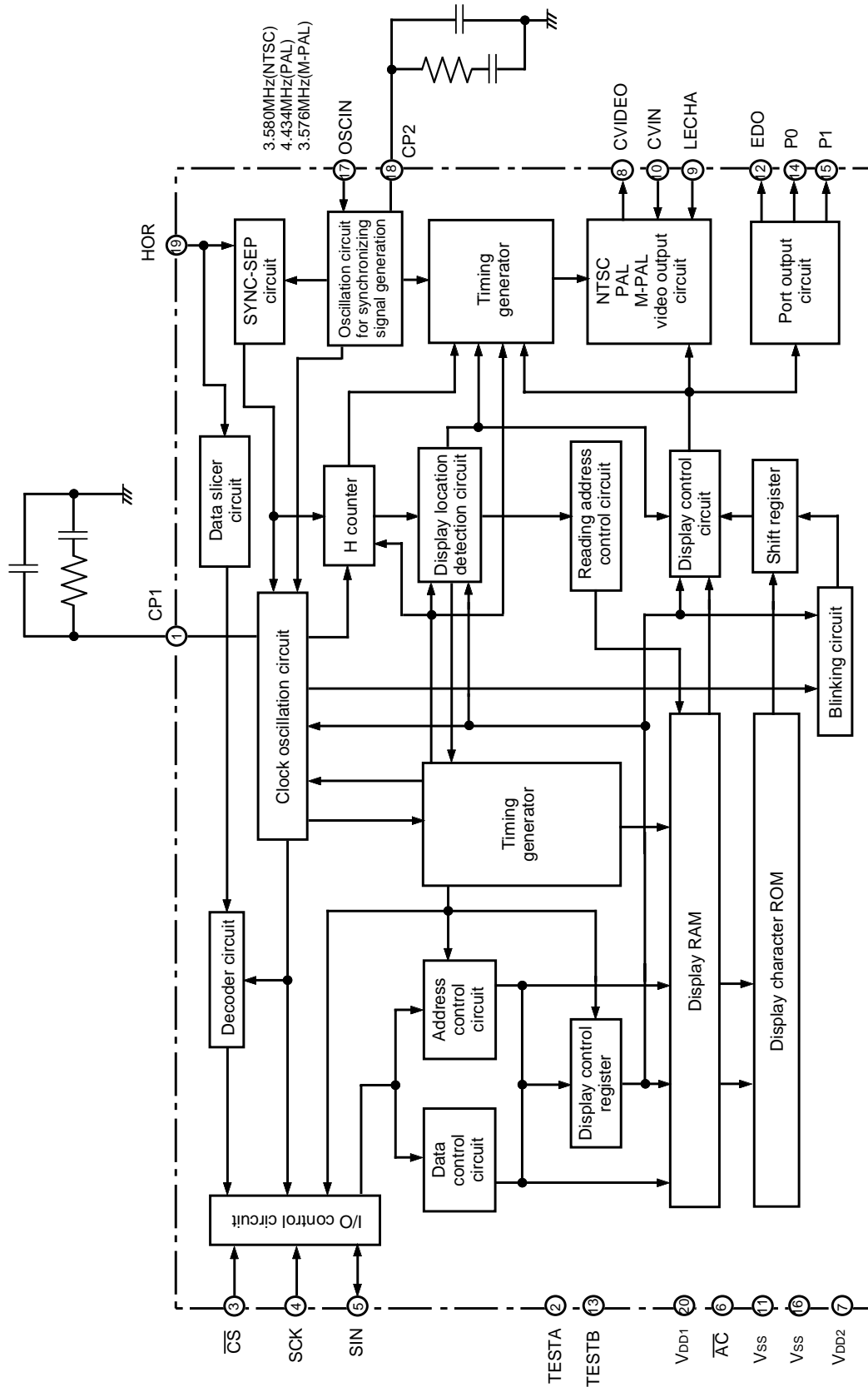


Outline 20P2Q-A

PIN DESCRIPTION

| Symbol | Pin name | Input/Output | Function |
|--------|---|--------------|---|
| OSC1 | Clock input | Input | This is the filter output pin 1. |
| TESTA | Test pin | — | This is the pin for test. Connect this pin to GND during normal operation. |
| CS | Chip select input | Input | This is the chip select pin, and when serial data transmission is being carried out, it goes to "L". Hysteresis input. Includes built-in pull-up resistor. |
| SCK | Serial clock input/output | Input | When CS pin is "L", SIN serial data is taken in when SCK rises. Hysteresis input. Built-in pull-up resistor is included. |
| SIN | Serial data input | Input/Output | This is the pin for serial input of data and addresses for the display control register and the display data memory. Also, serially outputs decode data according to the settings in the relevant registers (serial I/O). |
| AC | Auto-clear input | Input | When "L", this pin resets the internal IC circuit. Hysteresis input. Includes built-in pull-up resistor. |
| VDD2 | Power pin | — | Please connect to +5V with the analog circuit power pin. |
| CVIDEO | Composite video signal output | Output | This is the output pin for composite video signals. It outputs 2VP-P composite video signals. In superimpose mode, character output etc. is superimposed on the external composite video signals from CVIN. |
| LECHA | Character level input | Input | This is the input pin which determines the "white" character color level in the composite video signal. |
| CVIN | Composite video signal input | Input | This is the input pin for external composite video signals. In superimpose mode, character output etc. is superimposed on these external composite video signals. |
| Vss | Earthing pin | — | Please connect to GND using circuit earthing pin. |
| EDO | Encode data output | Output | This is the output pin for encode data. It outputs three-valve data. |
| TESTB | Test pin | — | This is the pin for test. Connect this pin to GND during normal operation. |
| P0 | Port P0 output | Output | This pin outputs the port output or BLNK1 (character background) signal. |
| P1 | Port P1 output | Output | This pin outputs the port output or CO1(character) signal. |
| Vss | Earthing pin | — | Please connect to GND using circuit earthing pin (Analog side). |
| OSCIN | fsc input pin for synchronous signal generation | Input | This is the input pin for the sub-carrier frequency (fsc) for generating a synchronous signal. A frequency of 3.580MHz is needed for NTSC, and a frequency of 4.434MHz is needed for PAL and 3.576MHz is needed for M-PAL. |
| CP2 | Filter output | Output | Filter output pin 2. |
| HOR | Horizontal synchronizing signal input | Input | This is the input pin for external composite video signals. This pin inputs the external video signal clamped sync-chip to 1.5V, and internally carries out synchronous separation. |
| VDD1 | Power pin | — | Please connect to +5V with the digital circuit power pin. |

BLOCK DIAGRAM



SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

MEMORY CONSTITUTION

Address 00₁₆ to EF₁₆ are assigned to the display RAM, address F0₁₆ to F8₁₆ are assigned to the display control registers.

The internal circuit is reset and all display control registers (address F0₁₆ to F8₁₆) are set to "0" and display RAM (address 00₁₆ to EF₁₆) are RAM erased when the AC pin level is "L".

Set "0" in any of DA₇, DAD through DAF of addresses 00₁₆ through EF₁₆, and of DAE and DAF of addresses F0₁₆ through F8₁₆.

Setting the blank code "FF₁₆" as a character code is an exception. TEST_n (n : a number) is MITSUBISHI test memory, so be sure to observe the setting conditions.

| Bit Address | DAF | DAE | DAD | DAC | DAB | DAA | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 | Remarks |
|------------------|-----|-----|--------|--------------------|----------|--------------------------------|---------|----------|--------|----------------|-------|---------|--------|--------|--------|--------|---|
| 00 ₁₆ | 0 | 0 | 0 | REV | BLINK | EC2 | EC1 | EC0 | 0 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | Display RAM |
| } | ⋮ | ⋮ | ⋮ | Reversed character | Blinking | Encode data or character color | | | ⋮ | Character code | | | | | | | |
| | ⋮ | ⋮ | ⋮ | | | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | | |
| EF ₁₆ | 0 | 0 | 0 | REV | BLINK | EC2 | EC1 | EC0 | 0 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | |
| F0 ₁₆ | 0 | 0 | TEST25 | W/R | TEST11 | TEST10 | DECB1 | DECB0 | SYSEP1 | SYSEP0 | SEPV1 | SEPV0 | PTD1 | PTD0 | PTC1 | PTC0 | Port output specify and so on |
| F1 ₁₆ | 0 | 0 | TEST26 | DVP4 | DVP3 | DVP2 | DVP1 | DVP0 | HP7 | HP6 | HP5 | HP4 | HP3 | HP2 | HP1 | HP0 | Horizontal display start position and Decode position specify |
| F2 ₁₆ | 0 | 0 | TEST27 | EVP4 | EVP3 | EVP2 | EVP1 | EVP0 | VP7 | VP6 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 | Vertical display start position and Encode position specify |
| F3 ₁₆ | 0 | 0 | TEST28 | TEST12 | EFLD1 | EFLD0 | DFLD1 | DFLD0 | VSZ21 | VSZ20 | VSZ11 | VSZ10 | HSZ21 | HSZ20 | HSZ11 | HSZ10 | Character size and Encode/Decode specify |
| F4 ₁₆ | 0 | 0 | TEST29 | TEST14 | TEST13 | SPACE | DSP9 | DSP8 | DSP7 | DSP6 | DSP5 | DSP4 | DSP3 | DSP2 | DSP1 | DSP0 | Display mode specify |
| F5 ₁₆ | 0 | 0 | TEST30 | TEST19 | MB/LB | TEST17 | TEST16 | TEST15 | EQP | PALH | MPAL | INT/NON | N/P | BLINK2 | BLINK1 | BLINK0 | Blinking specify and so on |
| F6 ₁₆ | 0 | 0 | TEST31 | TEST2 | TEST1 | TEST0 | LBLACK | LIN24/32 | BLKHF | BB | BG | BR | LEVEL0 | PHASE2 | PHASE1 | PHASE0 | Raster color specify |
| F7 ₁₆ | 0 | 0 | TEST32 | TEST24 | RGBON | TEST22 | CL17/18 | CBLINK | CURS7 | CURS6 | CURS5 | CURS4 | CURS3 | CURS2 | CURS1 | CURS0 | Cursor display specify |
| F8 ₁₆ | 0 | 0 | LEVEL1 | EHP4 | EHP3 | EHP2 | EHP1 | EHP0 | RAMERS | DSPON | STOP1 | STOPIN | SCOR | EX | BLK1 | BLK0 | Control display and so on |

Fig. 1 Memory constitution (M35052-XXXSP/FP)

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM. The screen constitution (24 characters X 10 lines) is shown in Figure 2 the screen constitution (32 characters X 7 lines) is shown in 3.

| Rows/Lines | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| 1 | 00 ₁₆ | 01 ₁₆ | 02 ₁₆ | 03 ₁₆ | 04 ₁₆ | 05 ₁₆ | 06 ₁₆ | 07 ₁₆ | 08 ₁₆ | 09 ₁₆ | 0A ₁₆ | 0B ₁₆ | 0C ₁₆ | 0D ₁₆ | 0E ₁₆ | 0F ₁₆ | 10 ₁₆ | 11 ₁₆ | 12 ₁₆ | 13 ₁₆ | 14 ₁₆ | 15 ₁₆ | 16 ₁₆ | 17 ₁₆ |
| 2 | 18 ₁₆ | 19 ₁₆ | 1A ₁₆ | 1B ₁₆ | 1C ₁₆ | 1D ₁₆ | 1E ₁₆ | 1F ₁₆ | 20 ₁₆ | 21 ₁₆ | 22 ₁₆ | 23 ₁₆ | 24 ₁₆ | 25 ₁₆ | 26 ₁₆ | 27 ₁₆ | 28 ₁₆ | 29 ₁₆ | 2A ₁₆ | 2B ₁₆ | 2C ₁₆ | 2D ₁₆ | 2E ₁₆ | 2F ₁₆ |
| 3 | 30 ₁₆ | 31 ₁₆ | 32 ₁₆ | 33 ₁₆ | 34 ₁₆ | 35 ₁₆ | 36 ₁₆ | 37 ₁₆ | 38 ₁₆ | 39 ₁₆ | 3A ₁₆ | 3B ₁₆ | 3C ₁₆ | 3D ₁₆ | 3E ₁₆ | 3F ₁₆ | 40 ₁₆ | 41 ₁₆ | 42 ₁₆ | 43 ₁₆ | 44 ₁₆ | 45 ₁₆ | 46 ₁₆ | 47 ₁₆ |
| 4 | 48 ₁₆ | 49 ₁₆ | 4A ₁₆ | 4B ₁₆ | 4C ₁₆ | 4D ₁₆ | 4E ₁₆ | 4F ₁₆ | 50 ₁₆ | 51 ₁₆ | 52 ₁₆ | 53 ₁₆ | 54 ₁₆ | 55 ₁₆ | 56 ₁₆ | 57 ₁₆ | 58 ₁₆ | 59 ₁₆ | 5A ₁₆ | 5B ₁₆ | 5C ₁₆ | 5D ₁₆ | 5E ₁₆ | 5F ₁₆ |
| 5 | 60 ₁₆ | 61 ₁₆ | 62 ₁₆ | 63 ₁₆ | 64 ₁₆ | 65 ₁₆ | 66 ₁₆ | 67 ₁₆ | 68 ₁₆ | 69 ₁₆ | 6A ₁₆ | 6B ₁₆ | 6C ₁₆ | 6D ₁₆ | 6E ₁₆ | 6F ₁₆ | 70 ₁₆ | 71 ₁₆ | 72 ₁₆ | 73 ₁₆ | 74 ₁₆ | 75 ₁₆ | 76 ₁₆ | 77 ₁₆ |
| 6 | 78 ₁₆ | 79 ₁₆ | 7A ₁₆ | 7B ₁₆ | 7C ₁₆ | 7D ₁₆ | 7E ₁₆ | 7F ₁₆ | 80 ₁₆ | 81 ₁₆ | 82 ₁₆ | 83 ₁₆ | 84 ₁₆ | 85 ₁₆ | 86 ₁₆ | 87 ₁₆ | 88 ₁₆ | 89 ₁₆ | 8A ₁₆ | 8B ₁₆ | 8C ₁₆ | 8D ₁₆ | 8E ₁₆ | 8F ₁₆ |
| 7 | 90 ₁₆ | 91 ₁₆ | 92 ₁₆ | 93 ₁₆ | 94 ₁₆ | 95 ₁₆ | 96 ₁₆ | 97 ₁₆ | 98 ₁₆ | 99 ₁₆ | 9A ₁₆ | 9B ₁₆ | 9C ₁₆ | 9D ₁₆ | 9E ₁₆ | 9F ₁₆ | A0 ₁₆ | A1 ₁₆ | A2 ₁₆ | A3 ₁₆ | A4 ₁₆ | A5 ₁₆ | A6 ₁₆ | A7 ₁₆ |
| 8 | A8 ₁₆ | A9 ₁₆ | AA ₁₆ | AB ₁₆ | AC ₁₆ | AD ₁₆ | AE ₁₆ | AF ₁₆ | B0 ₁₆ | B1 ₁₆ | B2 ₁₆ | B3 ₁₆ | B4 ₁₆ | B5 ₁₆ | B6 ₁₆ | B7 ₁₆ | B8 ₁₆ | B9 ₁₆ | BA ₁₆ | BB ₁₆ | BC ₁₆ | BD ₁₆ | BE ₁₆ | BF ₁₆ |
| 9 | C0 ₁₆ | C1 ₁₆ | C2 ₁₆ | C3 ₁₆ | C4 ₁₆ | C5 ₁₆ | C6 ₁₆ | C7 ₁₆ | C8 ₁₆ | C9 ₁₆ | CA ₁₆ | CB ₁₆ | CC ₁₆ | CD ₁₆ | CE ₁₆ | CF ₁₆ | D0 ₁₆ | D1 ₁₆ | D2 ₁₆ | D3 ₁₆ | D4 ₁₆ | D5 ₁₆ | D6 ₁₆ | D7 ₁₆ |
| 10 | D8 ₁₆ | D9 ₁₆ | DA ₁₆ | DB ₁₆ | DC ₁₆ | DD ₁₆ | DE ₁₆ | DF ₁₆ | E0 ₁₆ | E1 ₁₆ | E2 ₁₆ | E3 ₁₆ | E4 ₁₆ | E5 ₁₆ | E6 ₁₆ | E7 ₁₆ | E8 ₁₆ | E9 ₁₆ | EA ₁₆ | EB ₁₆ | EC ₁₆ | ED ₁₆ | EE ₁₆ | EF ₁₆ |

Note : The hexadecimal numbers in the boxes show the display RAM address.

Fig. 2 Screen constitution (24 characters X 10 lines)

| Rows/Lines | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
|------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| 1 | 00 ₁₆ | 01 ₁₆ | 02 ₁₆ | 03 ₁₆ | 04 ₁₆ | 05 ₁₆ | 06 ₁₆ | 07 ₁₆ | 08 ₁₆ | 09 ₁₆ | 0A ₁₆ | 0B ₁₆ | 0C ₁₆ | 0D ₁₆ | 0E ₁₆ | 0F ₁₆ | 10 ₁₆ | 11 ₁₆ | 12 ₁₆ | 13 ₁₆ | 14 ₁₆ | 15 ₁₆ | 16 ₁₆ | 17 ₁₆ | 18 ₁₆ | 19 ₁₆ | 1A ₁₆ | 1B ₁₆ | 1C ₁₆ | 1D ₁₆ | 1E ₁₆ | 1F ₁₆ |
| 2 | 20 ₁₆ | 21 ₁₆ | 22 ₁₆ | 23 ₁₆ | 24 ₁₆ | 25 ₁₆ | 26 ₁₆ | 27 ₁₆ | 28 ₁₆ | 29 ₁₆ | 2A ₁₆ | 2B ₁₆ | 2C ₁₆ | 2D ₁₆ | 2E ₁₆ | 2F ₁₆ | 30 ₁₆ | 31 ₁₆ | 32 ₁₆ | 33 ₁₆ | 34 ₁₆ | 35 ₁₆ | 36 ₁₆ | 37 ₁₆ | 38 ₁₆ | 39 ₁₆ | 3A ₁₆ | 3B ₁₆ | 3C ₁₆ | 3D ₁₆ | 3E ₁₆ | 3F ₁₆ |
| 3 | 40 ₁₆ | 41 ₁₆ | 42 ₁₆ | 43 ₁₆ | 44 ₁₆ | 45 ₁₆ | 46 ₁₆ | 47 ₁₆ | 48 ₁₆ | 49 ₁₆ | 4A ₁₆ | 4B ₁₆ | 4C ₁₆ | 4D ₁₆ | 4E ₁₆ | 4F ₁₆ | 50 ₁₆ | 51 ₁₆ | 52 ₁₆ | 53 ₁₆ | 54 ₁₆ | 55 ₁₆ | 56 ₁₆ | 57 ₁₆ | 58 ₁₆ | 59 ₁₆ | 5A ₁₆ | 5B ₁₆ | 5C ₁₆ | 5D ₁₆ | 5E ₁₆ | 5F ₁₆ |
| 4 | 60 ₁₆ | 61 ₁₆ | 62 ₁₆ | 63 ₁₆ | 64 ₁₆ | 65 ₁₆ | 66 ₁₆ | 67 ₁₆ | 68 ₁₆ | 69 ₁₆ | 6A ₁₆ | 6B ₁₆ | 6C ₁₆ | 6D ₁₆ | 6E ₁₆ | 6F ₁₆ | 70 ₁₆ | 71 ₁₆ | 72 ₁₆ | 73 ₁₆ | 74 ₁₆ | 75 ₁₆ | 76 ₁₆ | 77 ₁₆ | 78 ₁₆ | 79 ₁₆ | 7A ₁₆ | 7B ₁₆ | 7C ₁₆ | 7D ₁₆ | 7E ₁₆ | 7F ₁₆ |
| 5 | 80 ₁₆ | 81 ₁₆ | 82 ₁₆ | 83 ₁₆ | 84 ₁₆ | 85 ₁₆ | 86 ₁₆ | 87 ₁₆ | 88 ₁₆ | 89 ₁₆ | 8A ₁₆ | 8B ₁₆ | 8C ₁₆ | 8D ₁₆ | 8E ₁₆ | 8F ₁₆ | 90 ₁₆ | 91 ₁₆ | 92 ₁₆ | 93 ₁₆ | 94 ₁₆ | 95 ₁₆ | 96 ₁₆ | 97 ₁₆ | 98 ₁₆ | 99 ₁₆ | 9A ₁₆ | 9B ₁₆ | 9C ₁₆ | 9D ₁₆ | 9E ₁₆ | 9F ₁₆ |
| 6 | A0 ₁₆ | A1 ₁₆ | A2 ₁₆ | A3 ₁₆ | A4 ₁₆ | A5 ₁₆ | A6 ₁₆ | A7 ₁₆ | A8 ₁₆ | A9 ₁₆ | AA ₁₆ | AB ₁₆ | AC ₁₆ | AD ₁₆ | AE ₁₆ | AF ₁₆ | B0 ₁₆ | B1 ₁₆ | B2 ₁₆ | B3 ₁₆ | B4 ₁₆ | B5 ₁₆ | B6 ₁₆ | B7 ₁₆ | B8 ₁₆ | B9 ₁₆ | BA ₁₆ | BB ₁₆ | BC ₁₆ | BD ₁₆ | BE ₁₆ | BF ₁₆ |
| 7 | C0 ₁₆ | C1 ₁₆ | C2 ₁₆ | C3 ₁₆ | C4 ₁₆ | C5 ₁₆ | C6 ₁₆ | C7 ₁₆ | C8 ₁₆ | C9 ₁₆ | CA ₁₆ | CB ₁₆ | CC ₁₆ | CD ₁₆ | CE ₁₆ | CF ₁₆ | D0 ₁₆ | D1 ₁₆ | D2 ₁₆ | D3 ₁₆ | D4 ₁₆ | D5 ₁₆ | D6 ₁₆ | D7 ₁₆ | D8 ₁₆ | D9 ₁₆ | DA ₁₆ | DB ₁₆ | DC ₁₆ | DD ₁₆ | DE ₁₆ | DF ₁₆ |

Notes 1. The hexadecimal numbers in the boxes show the display RAM address.
2. When 32 characters X 7 lines are displayed, set blank code "FF₁₆" to character code of addresses E0₁₆ to EF₁₆.

Fig. 3 Screen constitution (32 characters X 7 lines)

Display RAM DESCRIPTION

Display RAM Address 0016 to EF16

| DA 0-C | Name | Contents | | Remarks | | |
|-----------|-------------|----------|---|-------------------------------------|---|--|
| | | Status | Function | | | |
| 0 | C0 (LSB) | 0 | Set ROM-held character code of a character needed to display. | | | |
| | | ① | | | | |
| 1 | C1 | 0 | | | | |
| | | ① | | | | |
| 2 | C2 | 0 | | | | |
| | | ① | | | | |
| 3 | C3 | 0 | | | | |
| | | ① | | | | |
| 4 | C4 | 0 | | | | |
| | | ① | | | | |
| 5 | C5 | 0 | | | | |
| | | ① | | | | |
| 6 | C6 (MSB) | 0 | | | | |
| | | ① | | | | |
| 7 | — | 0 | | | Set to "0" during normal operation | (Note 2) |
| | | ① | | | Can not be used | |
| 8 | EC0 | 0 | When EFILD1, 0=1, 0 or 0, 1, set code of the data needed to encode. | Refer to encode function. | | |
| | | ① | | | | |
| 9 | EC1 | 0 | | | When RGBON=1, set background color by character unit. | Refer to supplemental explanation (4). |
| | | ① | | | | |
| A | EC2 | 0 | | | | |
| | | ① | | | | |
| B | BLINK | 0 | No blinking | Refer to BLINK2 to 0 (address F516) | | |
| | | ① | Blinking | | | |
| C | REV | ① | Normal character | | | |
| | | 1 | Reversed character | | | |

Notes 1. Resetting at the $\bar{A}C$ pin RAM-erases the display RAM, and the status turns as indicated by the mark ○ around in the status column.
 2. Set to "1" only when you set a blank code.

Display control register

(1) Address F016

| DA 0-D | Register | Contents | | | Remarks | | | | | | | | | | | | | | | | |
|-----------|----------|------------------|---|----------------|---|--------|--------|----------------|---|---|------------------|---|---|------------------|---|---|------------------|---|---|------------------|---------------------------------------|
| | | Status | Function | | | | | | | | | | | | | | | | | | |
| 0 | PTC0 | ⓪ | P0 output (port 0) | | Port output control | | | | | | | | | | | | | | | | |
| | | 1 | BLNK1 output | | | | | | | | | | | | | | | | | | |
| 1 | PTC1 | ⓪ | P1 output (port 1) | | Refer to supplemental explanation (5). | | | | | | | | | | | | | | | | |
| | | 1 | CO1 output | | | | | | | | | | | | | | | | | | |
| 2 | PTD0 | ⓪ | It is negative polarity at P0 output "L", BLINK1 output. | | Control the port data | | | | | | | | | | | | | | | | |
| | | 1 | It is positive polarity at P0 output "H", BLINK1 output. | | | | | | | | | | | | | | | | | | |
| 3 | PTD1 | ⓪ | It is negative polarity at P01 output "L", CO1 output. | | Refer to supplemental explanation (5). | | | | | | | | | | | | | | | | |
| | | 1 | It is positive polarity at P01 output "H", CO1 output. | | | | | | | | | | | | | | | | | | |
| 4 | SEPV0 | ⓪ | It should be fixed to "0". | | Specifies the vertical synchronous separation criterion | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | |
| 5 | SEPV1 | ⓪ | It should be fixed to "0". | | Refer to supplemental explanation (1). | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | |
| 6 | SYSEP0 | ⓪ | <table border="1"> <thead> <tr> <th>SYSEP1</th> <th>SYSEP0</th> <th>Bias potential</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Can not be used.</td> </tr> <tr> <td>0</td> <td>1</td> <td>Can not be used.</td> </tr> <tr> <td>1</td> <td>0</td> <td>1.75μ</td> </tr> <tr> <td>1</td> <td>1</td> <td>Can not be used.</td> </tr> </tbody> </table> | | | SYSEP1 | SYSEP0 | Bias potential | 0 | 0 | Can not be used. | 0 | 1 | Can not be used. | 1 | 0 | 1.75μ | 1 | 1 | Can not be used. | Specifies the sync-bias potential |
| | | SYSEP1 | SYSEP0 | Bias potential | | | | | | | | | | | | | | | | | |
| 0 | 0 | Can not be used. | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1.75μ | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | | |
| 7 | SYSEP1 | ⓪ | <table border="1"> <thead> <tr> <th>DEC B1</th> <th>DEC B0</th> <th>Bias potential</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>2.35μ</td> </tr> <tr> <td>0</td> <td>1</td> <td>Can not be used.</td> </tr> <tr> <td>1</td> <td>0</td> <td>Can not be used.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Can not be used.</td> </tr> </tbody> </table> | | | DEC B1 | DEC B0 | Bias potential | 0 | 0 | 2.35μ | 0 | 1 | Can not be used. | 1 | 0 | Can not be used. | 1 | 1 | Can not be used. | Specifies the decoding bias potential |
| | | DEC B1 | DEC B0 | Bias potential | | | | | | | | | | | | | | | | | |
| 0 | 0 | 2.35μ | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Can not be used. | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | | |
| 8 | DEC B0 | ⓪ | <table border="1"> <thead> <tr> <th>DEC B1</th> <th>DEC B0</th> <th>Bias potential</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>2.35μ</td> </tr> <tr> <td>0</td> <td>1</td> <td>Can not be used.</td> </tr> <tr> <td>1</td> <td>0</td> <td>Can not be used.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Can not be used.</td> </tr> </tbody> </table> | | | DEC B1 | DEC B0 | Bias potential | 0 | 0 | 2.35μ | 0 | 1 | Can not be used. | 1 | 0 | Can not be used. | 1 | 1 | Can not be used. | Specifies the decoding bias potential |
| | | DEC B1 | DEC B0 | Bias potential | | | | | | | | | | | | | | | | | |
| 0 | 0 | 2.35μ | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Can not be used. | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | | |
| 9 | DEC B1 | ⓪ | <table border="1"> <thead> <tr> <th>DEC B1</th> <th>DEC B0</th> <th>Bias potential</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>2.35μ</td> </tr> <tr> <td>0</td> <td>1</td> <td>Can not be used.</td> </tr> <tr> <td>1</td> <td>0</td> <td>Can not be used.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Can not be used.</td> </tr> </tbody> </table> | | | DEC B1 | DEC B0 | Bias potential | 0 | 0 | 2.35μ | 0 | 1 | Can not be used. | 1 | 0 | Can not be used. | 1 | 1 | Can not be used. | Specifies the decoding bias potential |
| | | DEC B1 | DEC B0 | Bias potential | | | | | | | | | | | | | | | | | |
| 0 | 0 | 2.35μ | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Can not be used. | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | | |
| A | TEST10 | ⓪ | Can not be used. | | | | | | | | | | | | | | | | | | |
| | | 1 | It should be fixed to "1". | | | | | | | | | | | | | | | | | | |
| B | TEST11 | ⓪ | It should be fixed to "0". | | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | |
| C | W/R | ⓪ | Input data from SIN pin | | Control data I/O | | | | | | | | | | | | | | | | |
| | | 1 | Output data from SIN pin (Note 2) | | Refer to decode data output timing. | | | | | | | | | | | | | | | | |
| D | TEST25 | ⓪ | It should be fixed to "0". | | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | |

Notes 1. The mark ⓪ around the status value means the reset status by the "L" level is input to AC pin.

2. Not necessary to release after setting W/R to "1". Turn CS to "H" to switch over to input mode.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(2) Address F116

| DA 0~D | Register | Contents | | Remarks |
|-----------|---------------|----------|---|--|
| | | Status | Function | |
| 0 | HP0 (LSB) | 0 | <p>Let horizontal display start position be HS,</p> $HS = T \times \left(\sum_{n=0}^7 HPn + 6 \right)$ <p>T : The oscillation cycle of display clock</p> | <p>Set the horizontal display start position by use of HP7 through HP0. HP7 to HP0 = (00000000) to (00001111) setting is forbidden.</p> <p>It can be set this up to 240 steps in increments of one T.</p> |
| | | 1 | | |
| 1 | HP1 | 0 | | |
| | | 1 | | |
| 2 | HP2 | 0 | | |
| | | 1 | | |
| 3 | HP3 | 0 | | |
| | | 1 | | |
| 4 | HP4 | 0 | | |
| | | 1 | | |
| 5 | HP5 | 0 | | |
| | | 1 | | |
| 6 | HP6 | 0 | | |
| | | 1 | | |
| 7 | HP7 (MSB) | 0 | | |
| | | 1 | | |
| 8 | DVP0 (LSB) | 0 | <p>Let the slice lines be DVS,</p> $DVS = \sum_{n=0}^4 2^n DVPn + 6$ <p>It should be fixed to "0".</p> | <p>Set the slice lines (horizontal scanning lines) under decoding by use of DVP4 through DVP0. DVP4 to DVP0 = (00000) to (00011) setting is forbidden.</p> <p>Thus, it can be defined a setting up to 26 steps covered by a range from line 10 to line 35.</p> <p>Refer to supplemental explanation (2) about slice lines (DVS).</p> |
| | | 1 | | |
| 9 | DVP1 | 0 | | |
| | | 1 | | |
| A | DVP2 | 0 | | |
| | | 1 | | |
| B | DVP3 | 0 | | |
| | | 1 | | |
| C | DVP4 (MSB) | 0 | | |
| | | 1 | | |
| D | TEST26 | 0 | Can not be used. | |
| | | 1 | | |

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(3) Address F2₁₆

| DA 0~D | Register | Contents | | Remarks |
|-----------|---------------|----------|--|--|
| | | Status | Function | |
| 0 | VP0 (LSB) | 0 | <p>Let vertical display start position be VS,</p> $HS = T \times \sum_{n=0}^7 2^n Vpn$ <p>H : The oscillation cycle of horizontal synchronous signal</p> | <p>Set the vertical display start position by use of VP7 through VP0. VP7 to VP0 = (00000000) to (00000110) setting is forbidden.</p> <p>It can be set this up to 249 steps in increments of one H.</p> <p>VP7 to VP0 = (00000000) to (00100011) setting is forbidden.</p> |
| | | 1 | | |
| 1 | VP1 | 0 | | |
| | | 1 | | |
| 2 | VP2 | 0 | | |
| | | 1 | | |
| 3 | VP3 | 0 | | |
| | | 1 | | |
| 4 | VP4 | 0 | | |
| | | 1 | | |
| 5 | VP5 | 0 | | |
| | | 1 | | |
| 6 | VP6 | 0 | | |
| | | 1 | | |
| 7 | VP7 (MSB) | 0 | | |
| | | 1 | | |
| 8 | EVP0 (LSB) | 0 | <p>Let the encode lines be EVS,</p> $DVS = \sum_{n=0}^4 2^n EVpn + 6$ | <p>Sets the lines (horizontal scanning lines) under encoding by use of EVP4 through EVP0. EVP4 to EVP0 = (00000) to (00011) setting is forbidden.</p> <p>Thus, it can be defined a setting up to 26 steps covered by a range from line 10 to line 35.</p> <p>Refer to supplemental explanation (2) about the encode lines (EVS).</p> |
| | | 1 | | |
| 9 | EVP1 | 0 | | |
| | | 1 | | |
| A | EVP2 | 0 | | |
| | | 1 | | |
| B | EVP3 | 0 | | |
| | | 1 | | |
| C | EVP4 (MSB) | 0 | | |
| | | 1 | | |
| D | TEST27 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(4) Address F316

| DA 0~D | Register | Contents | | | Remarks | | |
|-----------|----------|----------|----------------------------|-------|---------------------------|---|---|
| | | Status | Function | | | | |
| 0 | HSZ10 | 0 | HSZ11 | HSZ10 | Horizontal direction size | Character size setting in the horizontal direction for the first line. | |
| | | 1 | 0 | 0 | | | 1T/dot |
| 1 | HSZ11 | 0 | 0 | 1 | 2T/dot | | |
| | | 1 | 1 | 0 | 3T/dot | | |
| 2 | HSZ20 | 0 | 0 | 1 | 4T/dot | | |
| | | 1 | 1 | 1 | | | |
| 3 | HSZ21 | 0 | HSZ21 | HSZ20 | Horizontal direction size | | Character size setting in the horizontal direction for the 2nd line to 10th line. |
| | | 1 | 0 | 0 | | | |
| 4 | VSZ10 | 0 | 0 | 1 | 2T/dot | | |
| | | 1 | 1 | 0 | 3T/dot | | |
| 5 | VSZ11 | 0 | 0 | 1 | 4T/dot | | |
| | | 1 | 1 | 1 | | | |
| 6 | VSZ20 | 0 | VSZ21 | VSZ20 | Vertical direction size | Character size setting in the vertical direction for the 2nd line to 10th line. | |
| | | 1 | 0 | 0 | | | |
| 7 | VSZ21 | 0 | 0 | 1 | 2H/dot | | |
| | | 1 | 1 | 0 | 3H/dot | | |
| 8 | DFLD0 | 0 | 0 | 1 | 4H/dot | | |
| | | 1 | 1 | 1 | | | |
| 9 | DFLD1 | 0 | DFLD1 | DFLD0 | Field detection | | Specifies the field determination procedure in relation to the Decoding functions. Refer to supplemental explanation (2). |
| | | 1 | 0 | 0 | | | |
| A | EFILD0 | 0 | 0 | 1 | The first field | | |
| | | 1 | 1 | 0 | The second field | | |
| B | EFLD1 | 0 | 0 | 1 | Can not be used | | |
| | | 1 | 1 | 1 | | | |
| C | TEST12 | 0 | It should be fixed to "0". | | | | |
| | | 1 | Can not be used. | | | | |
| D | TEST28 | 0 | It should be fixed to "0". | | | | |
| | | 1 | Can not be used. | | | | |

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(5) Address F416

| DA 0~D | Register | Contents | | Remarks | | | | | | | | | | | | | | | | | | | | |
|-----------|----------|----------------------------|--|---|---------------------------------|-----------|-----------|---|---|----------------------------|---------------------|---|---|-------------|----------------|---|---|---------------------|-------------|---|---|----------------|---------------------|---------------------------------|
| | | Status | Function | | | | | | | | | | | | | | | | | | | | | |
| 0 | DSP0 | ⓪ | <table border="1" style="margin-bottom: 10px;"> <thead> <tr> <th>BLK1</th> <th>BLK0</th> <th>DSPn= "1"</th> <th>DSPn= "0"</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Matrix-outline border size</td> <td>Matrix-outline size</td> </tr> <tr> <td>0</td> <td>1</td> <td>Border size</td> <td>Character size</td> </tr> <tr> <td>1</td> <td>0</td> <td>Matrix-outline size</td> <td>Border size</td> </tr> <tr> <td>1</td> <td>1</td> <td>Character size</td> <td>Matrix-outline size</td> </tr> </tbody> </table> <p>Depends on BLK0 and BLK1 (address F816) DSPn in the generic name for DSP0 to DSP9. DSP0 to DSP9 are each controlled independently.</p> | BLK1 | BLK0 | DSPn= "1" | DSPn= "0" | 0 | 0 | Matrix-outline border size | Matrix-outline size | 0 | 1 | Border size | Character size | 1 | 0 | Matrix-outline size | Border size | 1 | 1 | Character size | Matrix-outline size | Set the display mode of line 1. |
| | | BLK1 | | BLK0 | DSPn= "1" | DSPn= "0" | | | | | | | | | | | | | | | | | | |
| 0 | 0 | Matrix-outline border size | | Matrix-outline size | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Border size | | Character size | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Matrix-outline size | | Border size | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Character size | | Matrix-outline size | | | | | | | | | | | | | | | | | | | | |
| 1 | DSP1 | ⓪ | | | Set the display mode of line 2. | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 2 | DSP2 | ⓪ | | | Set the display mode of line 3. | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 3 | DSP3 | ⓪ | | | Set the display mode of line 4. | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 4 | DSP4 | ⓪ | | | Set the display mode of line 5. | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 5 | DSP5 | ⓪ | | | Set the display mode of line 6. | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 6 | DSP6 | ⓪ | | Set the display mode of line 7. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 7 | DSP7 | ⓪ | | Set the display mode of line 8. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 8 | DSP8 | ⓪ | | Set the display mode of line 9. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| 9 | DSP9 | ⓪ | | Set the display mode of line 10. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | |
| A | SPACE | ⓪ | Normal display | Put a space line between line 2 and line 3 in displaying 32 characters. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Put a space line between line 2 and line 3, and between line 8 and line 9. | | | | | | | | | | | | | | | | | | | | | |
| B | TEST13 | ⓪ | It should be fixed to "0". | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | | | |
| C | TEST14 | ⓪ | It should be fixed to "0". | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | | | |
| D | TEST29 | ⓪ | It should be fixed to "0". | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | | | |

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(6) Address F516

| DA 0~D | Register | Contents | | | Remarks | | | | | | | | | | | | | | | |
|-----------|----------|---------------|---|--------------------------|---|---------|--------------------------|---|---|--------------|---|------------|-------|---|------------|-----|------------|-----------------------------------|---------------|---|
| | | Status | Function | | | | | | | | | | | | | | | | | |
| 0 | BLINK0 | 0 | <table border="1"> <tr> <th>BLINK0</th> <th>BLINK1</th> <th>Duty</th> </tr> <tr> <td>0</td> <td>0</td> <td>Blinking off</td> </tr> <tr> <td>0</td> <td>1</td> <td>25%</td> </tr> <tr> <td>1</td> <td>0</td> <td>50%</td> </tr> <tr> <td>1</td> <td>1</td> <td>75%</td> </tr> </table> | | BLINK0 | BLINK1 | Duty | 0 | 0 | Blinking off | 0 | 1 | 25% | 1 | 0 | 50% | 1 | 1 | 75% | Blinking duty ratio can be altered. (Note) |
| | | BLINK0 | BLINK1 | Duty | | | | | | | | | | | | | | | | |
| 0 | 0 | Blinking off | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 25% | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 50% | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 75% | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | |
| 1 | BLINK1 | 0 | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | |
| 2 | BLINK2 | 0 | Division of vertical synchronizing signal into 1/64. Cycle approximately 1 second. | | Blinking cycle can be altered. | | | | | | | | | | | | | | | |
| | | 1 | Division of vertical synchronizing signal into 1/32. Cycle approximately 0.5 second. | | | | | | | | | | | | | | | | | |
| 3 | N/P | 0 | NTSC, M-PAL mode | | Refer to register MPAL | | | | | | | | | | | | | | | |
| | | 1 | PAL mode | | | | | | | | | | | | | | | | | |
| 4 | INT/NON | 0 | Interlace | | Scanning lines control (only in internal synchronization) | | | | | | | | | | | | | | | |
| | | 1 | Non interlace | | | | | | | | | | | | | | | | | |
| 5 | MPAL | 0 | <table border="1"> <tr> <th>N/P</th> <th>MPAL</th> <th>Synchronous mode</th> </tr> <tr> <td>0</td> <td>0</td> <td>NTSC</td> </tr> <tr> <td>0</td> <td>1</td> <td>M-PAL</td> </tr> <tr> <td>1</td> <td>0</td> <td>PAL</td> </tr> <tr> <td>1</td> <td>1</td> <td>Not available</td> </tr> </table> | | N/P | MPAL | Synchronous mode | 0 | 0 | NTSC | 0 | 1 | M-PAL | 1 | 0 | PAL | 1 | 1 | Not available | Synchronizing signal is selected with this register and N/P register. |
| | | N/P | MPAL | Synchronous mode | | | | | | | | | | | | | | | | |
| 0 | 0 | NTSC | | | | | | | | | | | | | | | | | | |
| 0 | 1 | M-PAL | | | | | | | | | | | | | | | | | | |
| 1 | 0 | PAL | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Not available | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | |
| 6 | PALH | 0 | <table border="1"> <tr> <th>PALH</th> <th>INT/NON</th> <th>Number of scanning lines</th> </tr> <tr> <td rowspan="2">0</td> <td>0</td> <td>625H lines</td> </tr> <tr> <td>1</td> <td>626H lines</td> </tr> <tr> <td rowspan="2">1</td> <td>0</td> <td>627H lines</td> </tr> <tr> <td>1</td> <td>628H lines</td> </tr> </table> | | PALH | INT/NON | Number of scanning lines | 0 | 0 | 625H lines | 1 | 626H lines | 1 | 0 | 627H lines | 1 | 628H lines | It should be fixed to "0" at NTSC | | |
| | | PALH | INT/NON | Number of scanning lines | | | | | | | | | | | | | | | | |
| 0 | 0 | 625H lines | | | | | | | | | | | | | | | | | | |
| | 1 | 626H lines | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 627H lines | | | | | | | | | | | | | | | | | | |
| | 1 | 628H lines | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | |
| 7 | EQP | 0 | Not include the equivalent pulse. | | Effective only at non-interlace | | | | | | | | | | | | | | | |
| | | 1 | Include the equivalent pulse. | | | | | | | | | | | | | | | | | |
| 8 | TEST15 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | |
| 9 | TEST16 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | |
| A | TEST17 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | |
| B | MB/LB | 0 | Output from MSB side | | Setting the decode data output form | | | | | | | | | | | | | | | |
| | | 1 | Output from LSB side | | | | | | | | | | | | | | | | | |
| C | TEST19 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | |
| D | TEST30 | 0 | It should be fixed to "0". | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | |

Note. To flash a character, set 1 to DAB (the flash bit) of the display RAM.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(7) Address F616

| DA 0~D | Register | Contents | | | | Remarks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|-------------------------|----------|--|--|--|---|---------|--------|-----------------------------|-----------------------------|---|---|---|-------|---|---|---|-----|---|---|---|-------|---|---|---|--------|---|---|---|------|---|---|---|---------|---|---|---|------|---|---|---|-------|---|
| | | Status | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | PHASE0 | ① | <table border="1"> <thead> <tr> <th>PHASE2</th> <th>PHASE1</th> <th>PHASE0</th> <th>Raster</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>White</td></tr> </tbody> </table> | | | | PHASE2 | PHASE1 | PHASE0 | Raster | 0 | 0 | 0 | Black | 0 | 0 | 1 | Red | 0 | 1 | 0 | Green | 0 | 1 | 1 | Yellow | 1 | 0 | 0 | Blue | 1 | 0 | 1 | Magenta | 1 | 1 | 0 | Cyan | 1 | 1 | 1 | White | Raster color setting Refer to supplemental explanation (3) about video signal level |
| | | PHASE2 | | | | | PHASE1 | PHASE0 | Raster | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | | | | | Black | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | | | | | Red | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | | | | | Green | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | | | | | Yellow | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | | | | | Blue | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | | | | | Magenta | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | | | | | Cyan | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | | | | | White | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | PHASE1 | ① | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | PHASE2 | ① | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | LEVEL0 | ① | Internal bias off | | | Generates bias potential for composite video signals | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Internal bias on | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | BR | ① | <table border="1"> <thead> <tr> <th>BB</th> <th>BG</th> <th>BR</th> <th>Character back-ground color</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>White</td></tr> </tbody> </table> | | | | BB | BG | BR | Character back-ground color | 0 | 0 | 0 | Black | 0 | 0 | 1 | Red | 0 | 1 | 0 | Green | 0 | 1 | 1 | Yellow | 1 | 0 | 0 | Blue | 1 | 0 | 1 | Magenta | 1 | 1 | 0 | Cyan | 1 | 1 | 1 | White | Character background color setting. Refer to supplemental explanation (3) about video signal level |
| | | BB | | | | | BG | BR | Character back-ground color | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | | | | | Black | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | | | | | Red | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | | | | | Green | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | | | | | Yellow | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | | | | | Blue | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | | | | | Magenta | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | | | | | Cyan | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | | | | | White | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | BG | ① | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | BB | ① | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | BLKHF | ① | The halftone displaying "OFF" in superimpose | | | This register is available in the superimpose displaying only. (Note) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | The halftone displaying "ON" in superimpose | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | LIN $\overline{24}$ /32 | ① | 24 characters X 10 lines display | | | "1" setting is forbidden under encoding. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | 32 characters X 7 lines display | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | LBLACK | ① | Blanking level I 2.3V | | | Set a blackness level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Blanking level II 2.1V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | TEST0 | ① | It should be fixed to "0". | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | TEST1 | ① | It should be fixed to "0". | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | TEST2 | ① | It should be fixed to "0". | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | TEST31 | ① | Can not be used. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | It should to be fixed to "1". | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Note. It is necessary to input the external composite video signal to the CVIN pin, and externally connect a 100 to 200Ω register in series.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(8) Address F716

| DA 0~D | Register | Contents | | Remarks |
|-----------|----------|----------|---|--|
| | | Status | Function | |
| 0 | CUR0 | 0 | Let cursor displaying address be CURS, CURS = T x $\sum_{n=0}^7 2^n \text{CURn}$ | Set the cursor displaying address by use of CUR7 through CUR0. CUR7 to CUR0 (11110000) setting is forbidden under 24 characters display. CUR7 to CUR0 (11100000) setting is forbidden under 32 characters display. Set CUR7 to CUR0 = (11111111) under cursor is not be displayed. The cursor displaying address (CURS) is correspond to display construction. |
| | | 1 | | |
| 1 | CUR1 | 0 | | |
| | | 1 | | |
| 2 | CUR2 | 0 | | |
| | | 1 | | |
| 3 | CUR3 | 0 | | |
| | | 1 | | |
| 4 | CUR4 | 0 | | |
| | | 1 | | |
| 5 | CUR5 | 0 | | |
| | | 1 | | |
| 6 | CUR6 | 0 | | |
| | | 1 | | |
| 7 | CUR7 | 0 | | |
| | | 1 | | |
| 8 | CBLINK | 0 | No blinking | The cursor blinking setting |
| | | 1 | Blinking | |
| 9 | CL17/18 | 0 | Cursor displaying at the 17th dot by vertical direction. | Refer to character construction. |
| | | 1 | Cursor displaying at the 18th dot by vertical direction. | |
| A | TEST22 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| B | RGBON | 0 | Normal | Refer to supplemental explanation (4). |
| | | 1 | Character background coloring | |
| C | TEST24 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |
| D | TEST32 | 0 | It should be fixed to "0". | |
| | | 1 | Can not be used. | |

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(9) Address F816

| DA 0~D | Register | Contents | | | | Remarks | | | | | | | | | | | | | | | | | | | | |
|-----------|----------|----------------------------|---|--|--|---|---------------------|-----------|-----------|-----------|---|---|----------------------------|---------------------|---|---|-------------|----------------|---|---|---------------------|-------------|---|---|----------------|---------------------|
| | | Status | Function | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | BLK0 | 0 | <table border="1"> <tr> <td>BLK1</td> <td>BLK0</td> <td>DSPn= "1"</td> <td>DSPn= "0"</td> </tr> <tr> <td>0</td> <td>0</td> <td>Matrix-outline border size</td> <td>Matrix-outline size</td> </tr> <tr> <td>0</td> <td>1</td> <td>Border size</td> <td>Character size</td> </tr> <tr> <td>1</td> <td>0</td> <td>Matrix-outline size</td> <td>Border size</td> </tr> <tr> <td>1</td> <td>1</td> <td>Character size</td> <td>Matrix-outline size</td> </tr> </table> | | | | BLK1 | BLK0 | DSPn= "1" | DSPn= "0" | 0 | 0 | Matrix-outline border size | Matrix-outline size | 0 | 1 | Border size | Character size | 1 | 0 | Matrix-outline size | Border size | 1 | 1 | Character size | Matrix-outline size |
| | | BLK1 | | | | | BLK0 | DSPn= "1" | DSPn= "0" | | | | | | | | | | | | | | | | | |
| 0 | 0 | Matrix-outline border size | | | | | Matrix-outline size | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Border size | | | | | Character size | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Matrix-outline size | | | | | Border size | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Character size | | | | | Matrix-outline size | | | | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | BLK1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | EX | 0 | External synchronization | | | Synchronizing signal switching (Note1) | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Internal synchronization | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | SCOR | 0 | Superimpose monotone display | | | "1" setting is forbidden at internal synchronous or PAL, M-PAL mode displaying. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Superimpose coloring display (only NTSC) | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | STOPIN | 0 | fsc input mode | | | OSCIN oscillation control | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Can not be used. | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | STOP1 | 0 | Oscillation VCO for display | | | Control oscillation VCO for display | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Stop oscillation VCO for display | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | DSPON | 0 | Display OFF | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Display ON | | | | | | | | | | | | | | | | | | | | | | | |
| 7 | RAMERS | 0 | RAM not erased | | | This register does not exist (Note 3). | | | | | | | | | | | | | | | | | | | | |
| | | 1 | RAM erased | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | EHP0 | 0 | Let encode data programming start position be EHS, $EHS = T \times \sum_{n=0}^4 2^n EHPn + 6$ | | | Set encode start position by use of EHP4 through EHP0. EHP4 to EHP0 = (00000) to (01111) is setting forbidden. Refer to encode function (3) | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | |
| 9 | EHP1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | |
| A | EHP2 | 0 | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | |
| B | EHP3 | 0 | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | |
| C | EHP4 | 0 | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | | | | | | | | | |
| D | LEVEL1 | 0 | Internal bias OFF | | | Generates bias potential for decoding and synchronous separation. | | | | | | | | | | | | | | | | | | | | |
| | | 1 | Internal bias ON | | | | | | | | | | | | | | | | | | | | | | | |

- Notes 1.** In dealing with the internal synchronization, cut off external video signals outside the IC. The leakage of external input video signals can be avoided.
- 2.** In displaying color superimposition, enter into the OSCIN pin the fsc signal that phase-synchronizes with the color burst of the composite video signals (input to the CVIN pin).
- 3.** Erases all the display RAM. The character code turns to blank-FF16, the encode data bit and the blinking bit turn to "1" respectively, and reversed character bit turns to "0".

Supplemental explanation about display control register

(1) How to effect synchronous separation from composite video signals

Synchronous separation is effected as follows depending on the width of L-level of the vertical synchronous period.

1. Less than 8.4 μs Not to be determined to be a vertical synchronous signal.
2. Equal to or higher than 8.4 μs but less than 15.6 μs When two clocks continue, if take place, it is "L" period is determined to be a vertical synchronization signal.
3. Equal to or higher than 15.6 μs It is "L" period is determined to be a vertical synchronous signal with no condition.

The determination is made at the timing indicated by V in Fig.3 either in case 2 or in case 3.

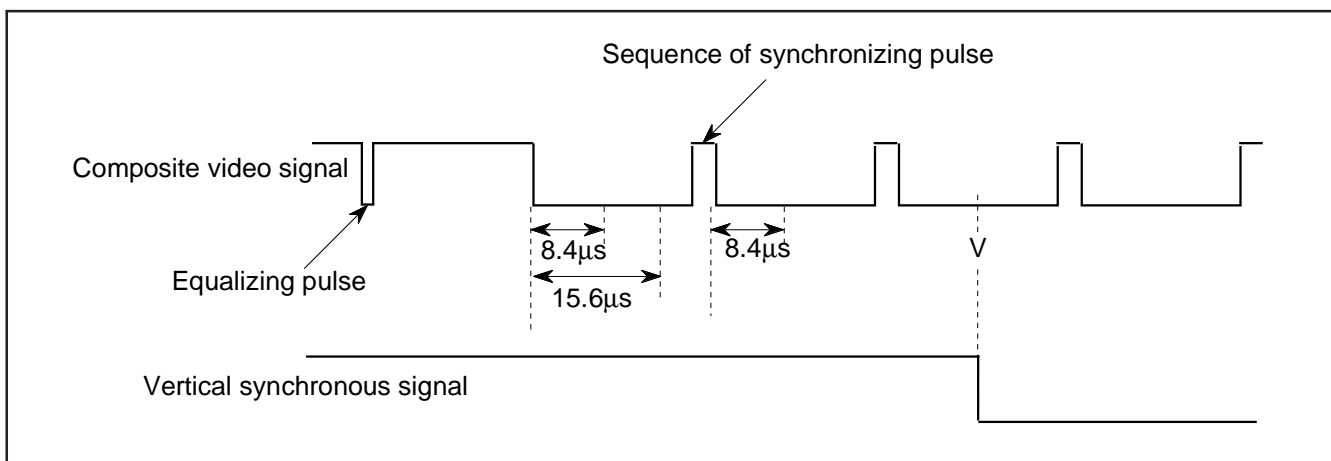


Fig. 4 The method of synchronous separation from composite video signal.

(2) Field definition

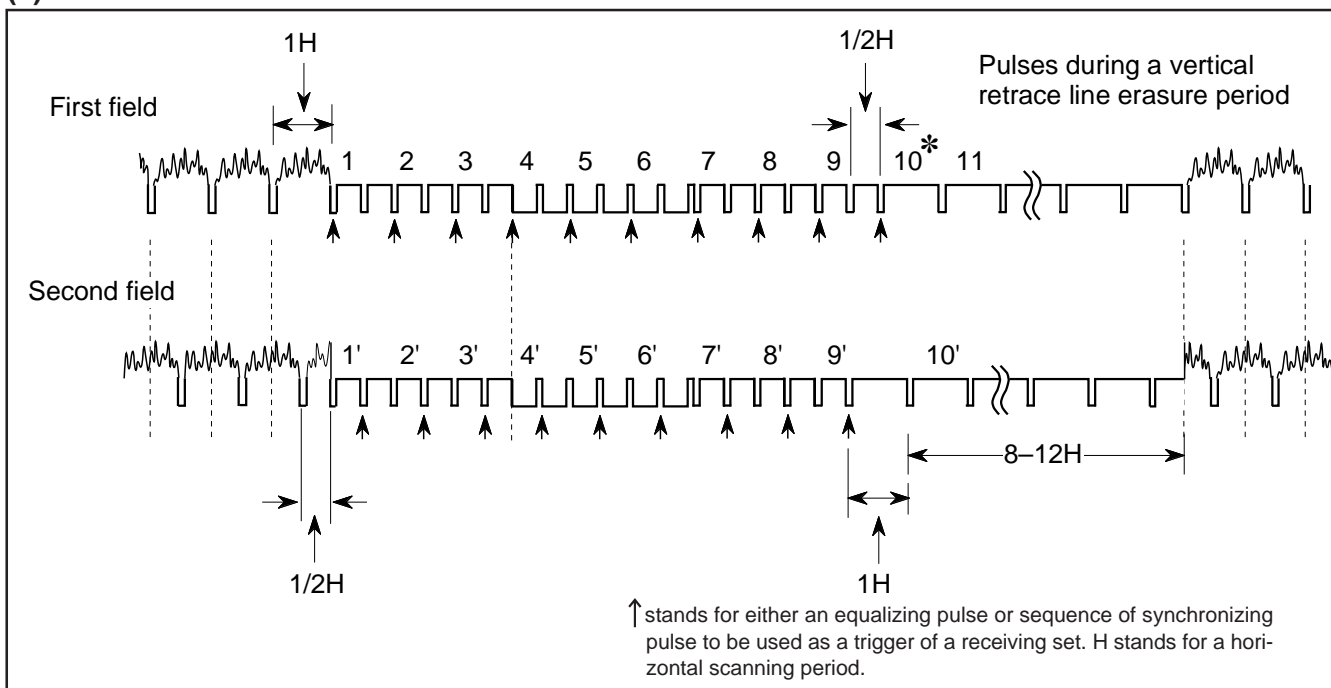


Fig. 5 Field definition

*A horizontal scanning line number corresponds to slice lines DVP4 through DVP0 (address F116) and to encode lines EVP4 through EVP0 (address F216).

(3) Video signal level

VDD : 5.0V, Ta : 25°C

| Color | Phase angle (rad) | | Brightness level (V) | | | Amplitude ratio (to color burst) | | |
|-------------|------------------------|----------------------------|----------------------|------|------|----------------------------------|------|------|
| | NTSC method | PAL, M-PAL method | Min. | Typ. | Max. | Min. | Typ. | Max. |
| Sync-chip | – | – | 1.3 | 1.5 | 1.7 | – | – | – |
| Pedestal | – | – | 1.9 | 2.1 | 2.3 | – | – | – |
| Color burst | 0 | $\pm 4\pi/16$ | 1.9 | 2.1 | 2.3 | – | 1.0 | – |
| Black | – | – | 2.1 | 2.3 | 2.5 | – | – | – |
| Red | $7\pi/16 \pm 2\pi/16$ | $\pm 7\pi/16 \pm 2\pi/16$ | 2.3 | 2.5 | 2.7 | 1.5 | 3.0 | 4.5 |
| Green | $27\pi/16 \pm 2\pi/16$ | $\mp 5\pi/16 \pm 2\pi/16$ | 2.7 | 2.9 | 3.1 | 1.4 | 2.8 | 4.2 |
| Yellow | $\pi/16 \pm 2\pi/16$ | $\pm \pi/16 \pm 2\pi/16$ | 3.1 | 3.3 | 3.5 | 1.0 | 2.0 | 3.0 |
| Blue | $17\pi/16 \pm 2\pi/16$ | $\mp 15\pi/16 \pm 2\pi/16$ | 2.0 | 2.2 | 2.4 | 1.0 | 2.0 | 3.0 |
| Magenta | $11\pi/16 \pm 2\pi/16$ | $\pm 11\pi/16 \pm 2\pi/16$ | 2.5 | 2.7 | 2.9 | 1.4 | 2.8 | 4.2 |
| Cyan | $23\pi/16 \pm 2\pi/16$ | $\mp 9\pi/16 \pm 2\pi/16$ | 2.9 | 3.1 | 3.3 | 1.5 | 3.0 | 4.5 |
| White | – | – | 3.1 | 3.3 | 3.5 | – | – | – |

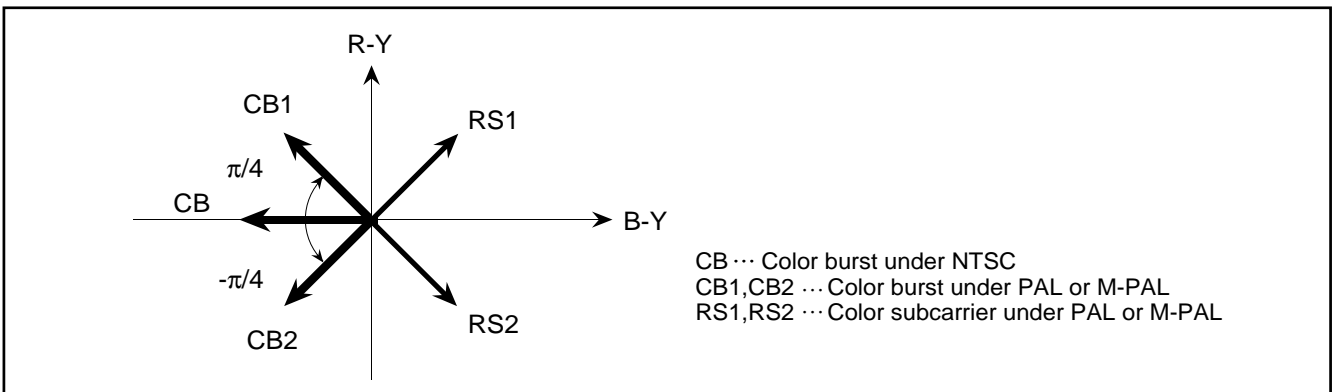


Fig. 6 Bector phases

(4) Setting RGBON (address F716)

- a) When encode is off ... EFILD1, 0 (address F316) = 0, 0
 Encode setting ... Not effected
 RGBON = "0" Sets background colors depending on BB, BG, and BR (address F616), screen by screen.
 RGBON = "1" Sets background colors depending on EC2 to EC0 (address 0016 to EF16), character by character. The color setting is shown below.
- b) When encode is on ... EFILD1, 0 (address F316) = 0, 1 or 1, 0
 Encode setting ... Sets encode data depending on EC2 through EC0. (Refer to the encode functions for details.)
 RGBON = "0" Sets background colors depending on BB, BG and BR (address F616) screen by screen.
 RGBON = "1" This setting can not be used.
 (When encode is on, setting RGBON to "1" results in setting both encode data and background colors depending on the same memory (EC2 through EC0), so this setting can not be used.

Color Setting

| EC2 | EC1 | EC0 | Color |
|-----|-----|-----|---------|
| 0 | 0 | 0 | Black |
| 0 | 0 | 1 | Red |
| 0 | 1 | 0 | Green |
| 0 | 1 | 1 | Yellow |
| 1 | 0 | 0 | Blue |
| 1 | 0 | 1 | Magenta |
| 1 | 1 | 0 | Cyan |
| 1 | 1 | 1 | White |

(5) Port output and BLNK1, CO1 output

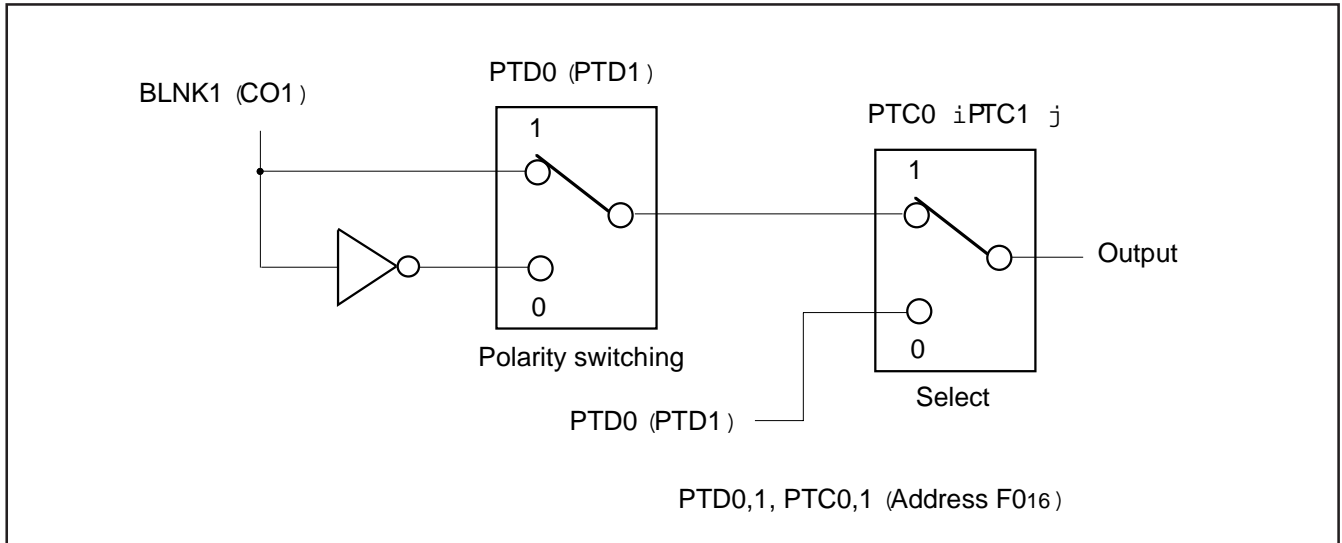


Fig. 7 Example of port control

(6) Setting conditions for oscillating or stopping the display clock

| | at display clock operating | at display clock stop |
|--------|----------------------------|-----------------------|
| STOP1 | 0 | 1 |
| DSPON | 1 | 0 |
| CS pin | L | H |

STOP1, DSPON (Address F816)

(7) Setting condition at LEVEL0,1

| | Operation state (Character display) | | Now-working condition (no characters are displayed) |
|--------|-------------------------------------|----------------------|--|
| | Internal synchronous | External synchronous | |
| LEVEL0 | 1 | 1 | 0 |
| LEVEL1 | 0 | 1 | 0 |

LEVEL0 (address F616), LEVEL1 (address F816)

DISPLAY FORMS

M35052-XXXSP/FP has the following four display forms as the blanking function, when CO1 and BLNK1 are output.

- (1) Character size : Blanking same as the character size.
- (2) Border size : Blanking the background as a size from character.
- (3) Matrix-outline size: Blanking the background as a size from all character font size.
- (4) Matrix-outline border size : Blanking the background as a size from all character font size.
Border display.

This display format allows each line to be controlled independently, so that two kinds of display formats can be combined on the same screen.

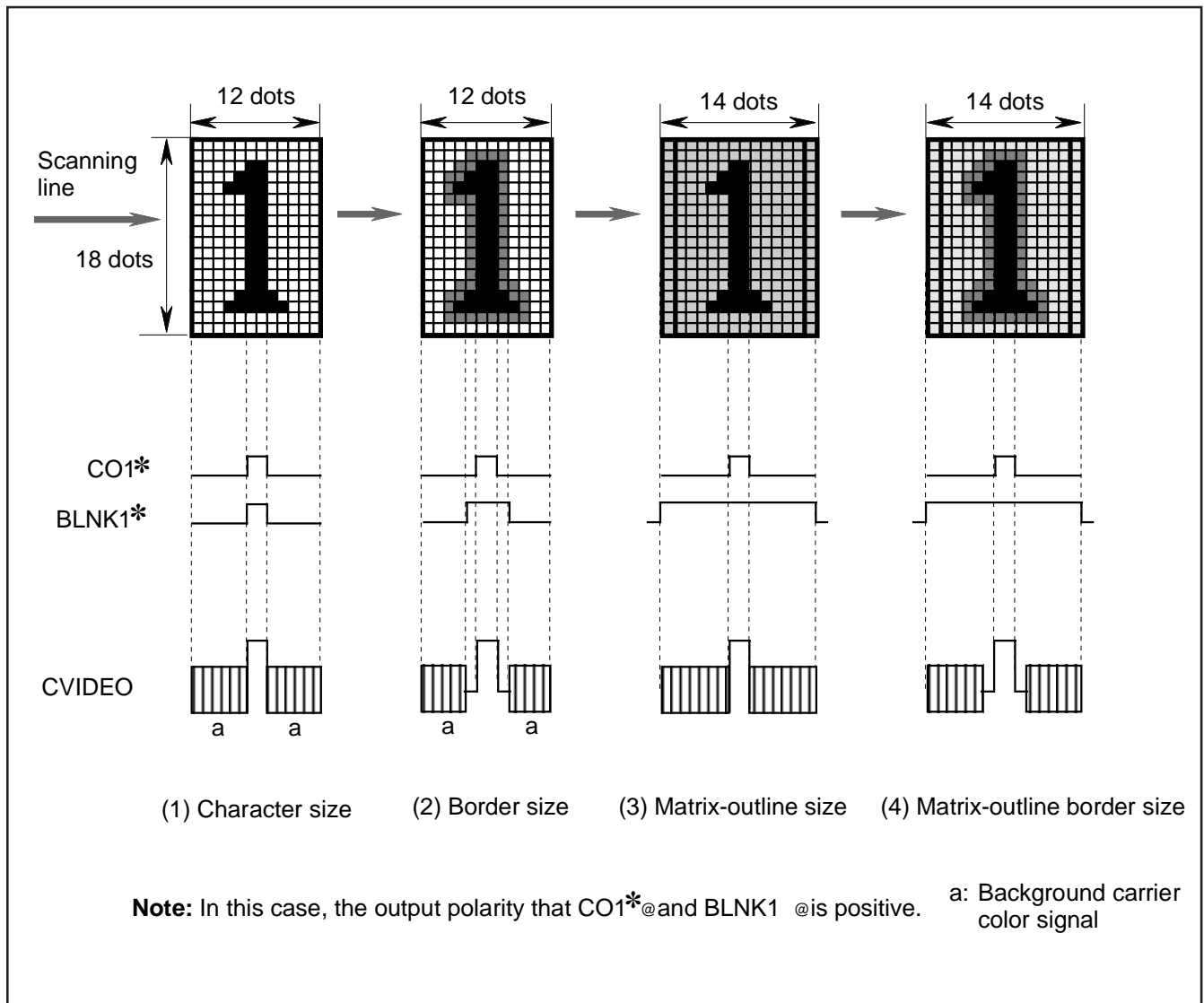


Fig. 8 Display forms at each display mode

DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by then serial input function. Example of data setting is shown in Figure 9.

Owing to automatic address increment, not necessary to enter addresses for the second and subsequent data.

In automatically, the next of address F8₁₆ is assigned to address 00₁₆.

Fig. 9 shows an example of data serially entered.

| | DA F | DA E | DA D | DA C | DA B | DA A | DA 9 | DA 8 | DA 7 | DA 6 | DA 5 | DA 4 | DA 3 | DA 2 | DA 1 | DA 0 | Remarks |
|-----------------------------|------|------|---------|-------|--------|--------|----------|-----------|---------|--------|--------|----------|---------|---------|---------|---------|---|
| Address (F8 ₁₆) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | Specify address |
| Data (F8 ₁₆) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Display OFF |
| | 0 | 0 | 0 | REV | BLINK | EC2 | EC1 | EC0 | 0 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | Specify address display RAM 0 to EF ₁₆ . |
| Data (01 ₁₆) | 0 | 0 | 0 | REV | BLINK | EC2 | EC1 | EC0 | 0 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | |
| } | } | | | | | | | | } | | | | | | | | |
| Data (EE ₁₆) | 0 | 0 | 0 | REV | BLINK | EC2 | EC1 | EC0 | 0 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | |
| Data (EF ₁₆) | 0 | 0 | 0 | REV | BLINK | EC2 | EC1 | EC0 | 0 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | Specify address register F0 ₁₆ to F7 ₁₆ . |
| Data (F0 ₁₆) | 0 | 0 | 0 | W/R | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | PTD 1 | PTD 0 | PTC 1 | PTC 0 | |
| Data (F1 ₁₆) | 0 | 0 | 0 | DVP 4 | DVP 3 | DVP 2 | DVP 1 | DVP 0 | HP 7 | HP 6 | HP 5 | HP 4 | HP 3 | HP 2 | HP 1 | HP 0 | |
| Data (F2 ₁₆) | 0 | 0 | 0 | EVP 4 | EVP 3 | EVP 2 | EVP 1 | EVP 0 | VP 7 | VP 6 | VP 5 | VP 4 | VP 3 | VP 2 | VP 1 | VP 0 | |
| Data (F3 ₁₆) | 0 | 0 | 0 | 0 | EFLD 1 | EFLD 0 | DFLD 1 | DFLD 0 | VSZ 21 | VSZ 20 | VSZ 11 | VSZ 10 | HSZ 21 | HSZ 20 | HSZ 11 | HSZ 10 | |
| Data (F4 ₁₆) | 0 | 0 | 0 | 0 | 0 | SPACE | DSP 9 | DSP 8 | DSP 7 | DSP 6 | DSP 5 | DSP 4 | DSP 3 | DSP 2 | DSP 1 | DSP 0 | |
| Data (F5 ₁₆) | 0 | 0 | 0 | 0 | MB/LB | 0 | 0 | 0 | EQP | PALH | MPAL | INT /NON | N/P | BLINK 2 | BLINK 1 | BLINK 0 | |
| Data (F6 ₁₆) | 0 | 0 | 1 | 0 | 0 | 0 | LBLACK | LIN 24/32 | BLKHF | BB | BG | BR | LEVEL 0 | PHASE 2 | PHASE 1 | PHASE 0 | |
| Data (F7 ₁₆) | 0 | 0 | 0 | 0 | RGBON | 0 | CL 17/18 | CBLINK | CURS 7 | CURS 6 | CURS 5 | CURS 4 | CURS 3 | CURS 2 | CURS 1 | CURS 0 | |
| Data (F8 ₁₆) | 0 | 0 | LEVEL 1 | EHP 4 | EHP 3 | EHP 2 | EHP 1 | EHP 0 | RAM ERS | DSPON | STOP 1 | STOP IN | SCOR | EX | BLK 1 | BLK 0 | |

Fig. 9 Example of data setting serial input function

SERIAL DATA INPUT TIMING

- (1) The address consists of 16 bits.
- (2) The data consists of 16 bits.
- (3) The 16 bits in the SCK after the CS signal has fallen are the address, and for succeeding input data, the address is incremented every 16 bits.

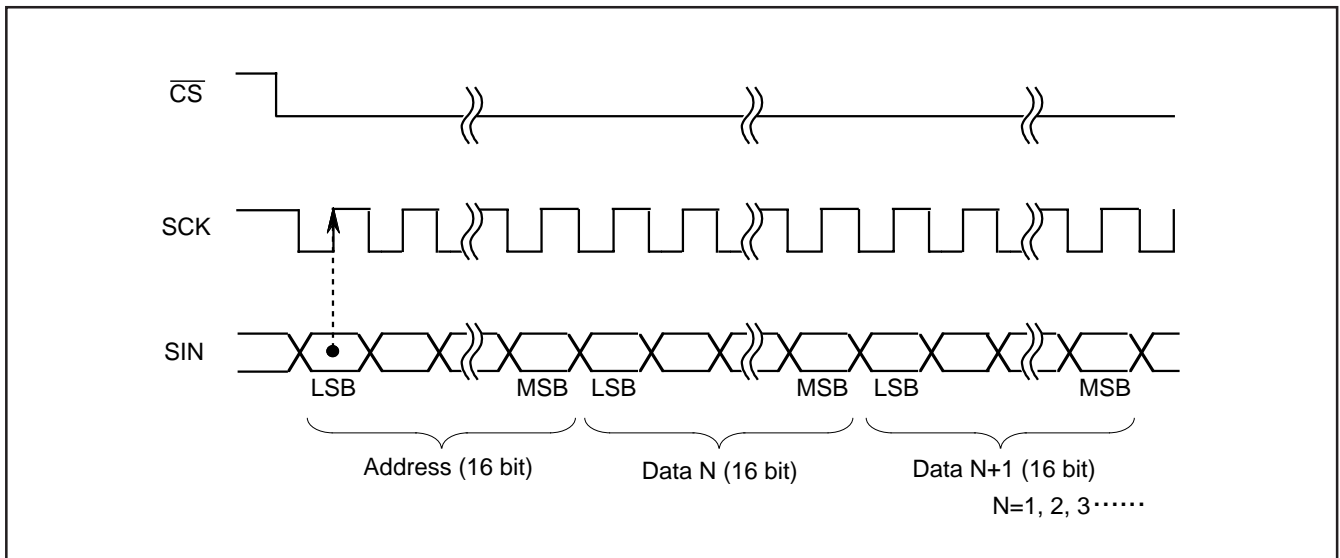


Fig. 10 Serial input timing

Output timing of decode data

- (1) Setting "1" in the $\overline{W/R}$ register activates output mode.
- (2) Outputs decode data in 16 clocks of the SCK after switching over to output mode. (Don't enter the SCK for more than 16 clocks.)
- (3) Raising the \overline{CS} signal deactivates output mode. (To switch over to input mode, cause \overline{CS} to fall.)
- (4) If no data are present, or if data have already been read, 0000₁₆ is output.

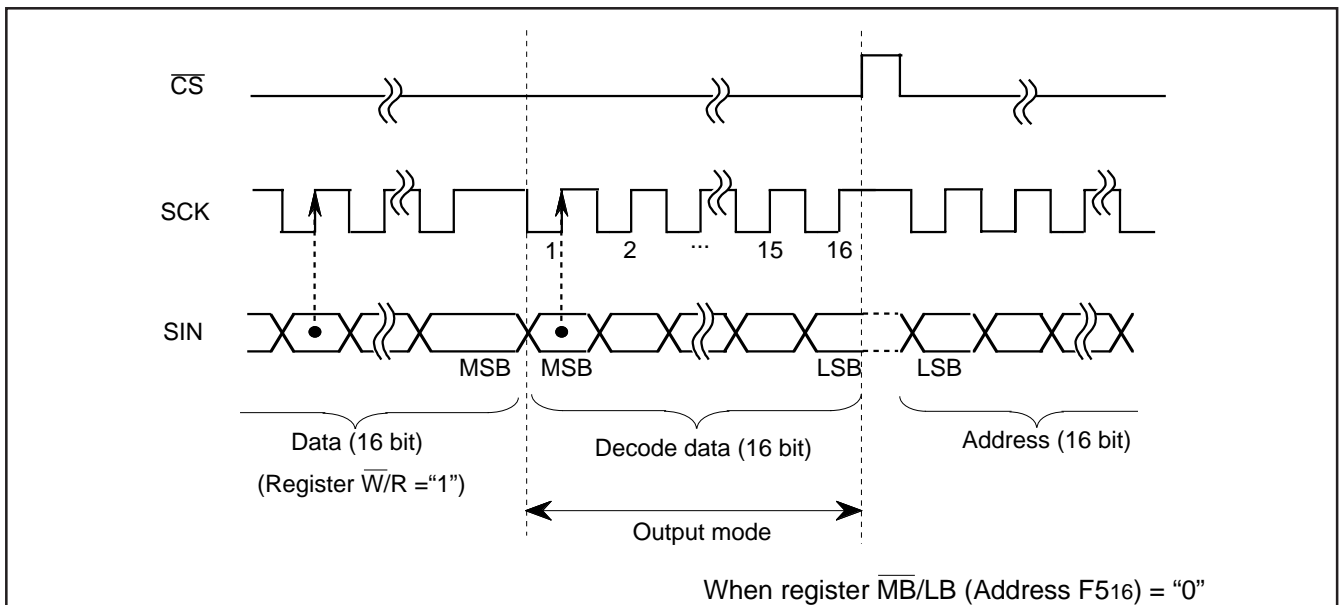


Fig. 11 Decode data output timing

Encode functions (effective for NTSC only)

(1) Setting encode data

Setting data code (000 – 111) in EC0 through EC2 (bits DA8 through DAA) of the display RAM (addresses 0 through EF16) encodes. A sample setting and data code are shown below.

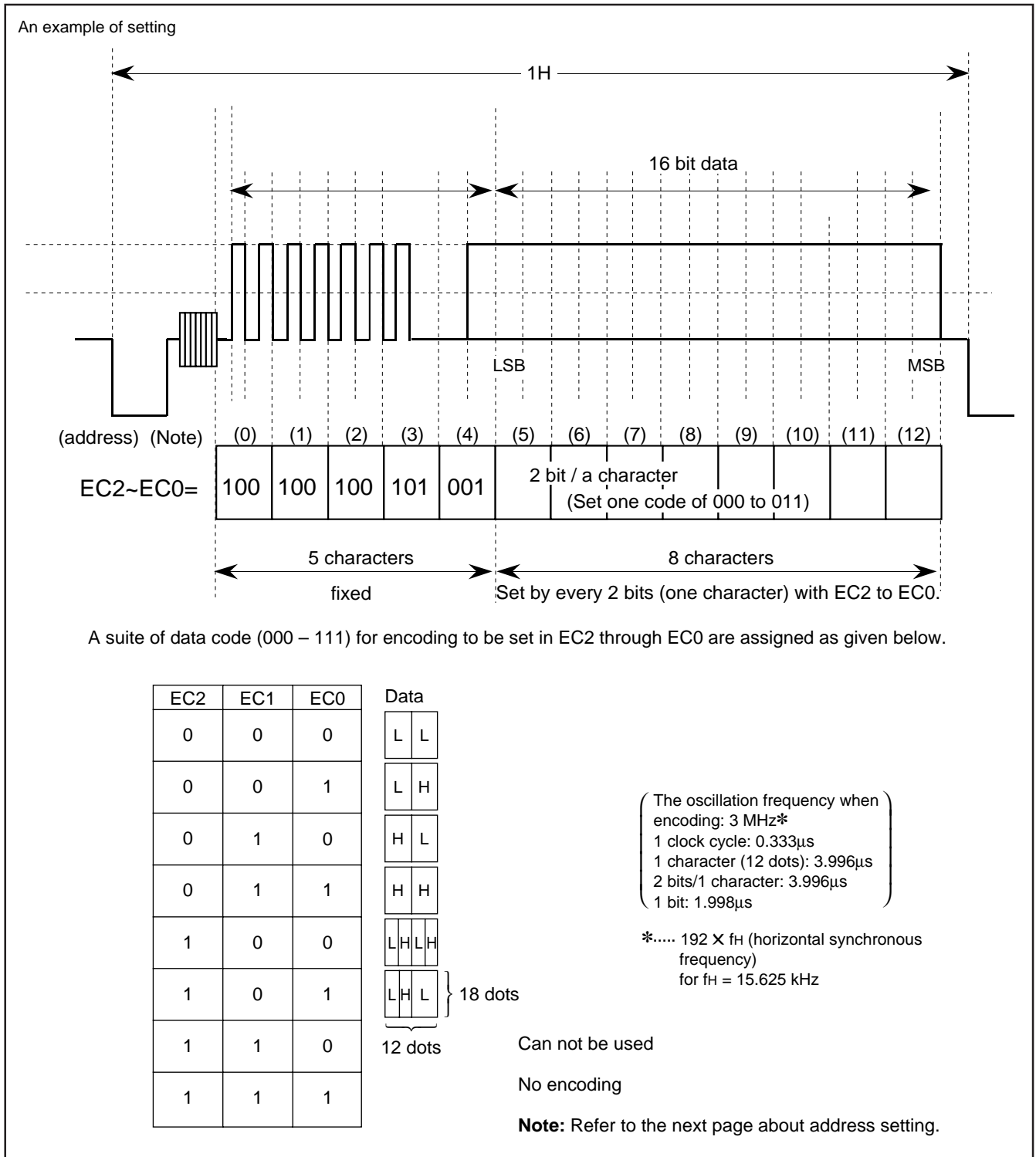


Fig. 12 An example of data code setting

(2) Setting addresses

Set encode data in EC0 through EC2 of addresses (that correspond to an extent from the first character to the thirteenth character in each line as appearing on the screen.) Set "111" to EC2 through EC0 of all the addresses in which you set no encode data.

Screen

| | The first character | | | | | | | | | | | | | The 13th character | | | | | | The 24th character | | | | |
|---------|---------------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|--------------------------|------------------|------------------|------------------|------------------|------------------|--------------------|------------------|------------------|------------------|------------------|
| line 1 | 00 ₁₆ | 01 ₁₆ | 02 ₁₆ | 03 ₁₆ | 04 ₁₆ | 05 ₁₆ | 06 ₁₆ | 07 ₁₆ | 08 ₁₆ | 09 ₁₆ | 0A ₁₆ | 0B ₁₆ | 0C ₁₆ | 0D ₁₆ | 0E ₁₆ | 0F ₁₆ | 10 ₁₆ | 11 ₁₆ | 12 ₁₆ | 13 ₁₆ | 14 ₁₆ | 15 ₁₆ | 16 ₁₆ | 17 ₁₆ |
| line 2 | 18 ₁₆ | 19 ₁₆ | 1A ₁₆ | 1B ₁₆ | 1C ₁₆ | 1D ₁₆ | 1E ₁₆ | 1F ₁₆ | 20 ₁₆ | 21 ₁₆ | 22 ₁₆ | 23 ₁₆ | 24 ₁₆ | 25 ₁₆ | 26 ₁₆ | 27 ₁₆ | 28 ₁₆ | 29 ₁₆ | 2A ₁₆ | 2B ₁₆ | 2C ₁₆ | 2D ₁₆ | 2E ₁₆ | 2F ₁₆ |
| line 3 | 30 ₁₆ | 31 ₁₆ | 32 ₁₆ | 33 ₁₆ | 34 ₁₆ | 35 ₁₆ | 36 ₁₆ | 37 ₁₆ | 38 ₁₆ | 39 ₁₆ | 3A ₁₆ | 3B ₁₆ | 3C ₁₆ | 3D ₁₆ | 3E ₁₆ | 3F ₁₆ | 40 ₁₆ | 41 ₁₆ | 42 ₁₆ | 43 ₁₆ | 44 ₁₆ | 45 ₁₆ | 46 ₁₆ | 47 ₁₆ |
| line 4 | 48 ₁₆ | 49 ₁₆ | 4A ₁₆ | 4B ₁₆ | 4C ₁₆ | 4D ₁₆ | 4E ₁₆ | 4F ₁₆ | 50 ₁₆ | 51 ₁₆ | 52 ₁₆ | 53 ₁₆ | 54 ₁₆ | 55 ₁₆ | 56 ₁₆ | 57 ₁₆ | 58 ₁₆ | 59 ₁₆ | 5A ₁₆ | 5B ₁₆ | 5C ₁₆ | 5D ₁₆ | 5E ₁₆ | 5F ₁₆ |
| line 5 | 60 ₁₆ | 61 ₁₆ | 62 ₁₆ | 63 ₁₆ | 64 ₁₆ | 65 ₁₆ | 66 ₁₆ | 67 ₁₆ | 68 ₁₆ | 69 ₁₆ | 6A ₁₆ | 6B ₁₆ | 6C ₁₆ | 6D ₁₆ | 6E ₁₆ | 6F ₁₆ | 70 ₁₆ | 71 ₁₆ | 72 ₁₆ | 73 ₁₆ | 74 ₁₆ | 75 ₁₆ | 76 ₁₆ | 77 ₁₆ |
| line 6 | 78 ₁₆ | 79 ₁₆ | 7A ₁₆ | 7B ₁₆ | 7C ₁₆ | 7D ₁₆ | 7E ₁₆ | 7F ₁₆ | 80 ₁₆ | 81 ₁₆ | 82 ₁₆ | 83 ₁₆ | 84 ₁₆ | 85 ₁₆ | 86 ₁₆ | 87 ₁₆ | 88 ₁₆ | 89 ₁₆ | 8A ₁₆ | 8B ₁₆ | 8C ₁₆ | 8D ₁₆ | 8E ₁₆ | 8F ₁₆ |
| line 7 | 90 ₁₆ | 91 ₁₆ | 92 ₁₆ | 93 ₁₆ | 94 ₁₆ | 95 ₁₆ | 96 ₁₆ | 97 ₁₆ | 98 ₁₆ | 99 ₁₆ | 9A ₁₆ | 9B ₁₆ | 9C ₁₆ | 9D ₁₆ | 9E ₁₆ | 9F ₁₆ | A0 ₁₆ | A1 ₁₆ | A2 ₁₆ | A3 ₁₆ | A4 ₁₆ | A5 ₁₆ | A6 ₁₆ | A7 ₁₆ |
| line 8 | A8 ₁₆ | A9 ₁₆ | AA ₁₆ | AB ₁₆ | AC ₁₆ | AD ₁₆ | AE ₁₆ | AF ₁₆ | B0 ₁₆ | B1 ₁₆ | B2 ₁₆ | B3 ₁₆ | B4 ₁₆ | B5 ₁₆ | B6 ₁₆ | B7 ₁₆ | B8 ₁₆ | B9 ₁₆ | BA ₁₆ | BB ₁₆ | BC ₁₆ | BD ₁₆ | BE ₁₆ | BF ₁₆ |
| line 9 | C0 ₁₆ | C1 ₁₆ | C2 ₁₆ | C3 ₁₆ | C4 ₁₆ | C5 ₁₆ | C6 ₁₆ | C7 ₁₆ | C8 ₁₆ | C9 ₁₆ | CA ₁₆ | CB ₁₆ | CC ₁₆ | CD ₁₆ | CE ₁₆ | CF ₁₆ | D0 ₁₆ | D1 ₁₆ | D2 ₁₆ | D3 ₁₆ | D4 ₁₆ | D5 ₁₆ | D6 ₁₆ | D7 ₁₆ |
| line 10 | D8 ₁₆ | D9 ₁₆ | DA ₁₆ | DB ₁₆ | DC ₁₆ | DD ₁₆ | DE ₁₆ | DF ₁₆ | E0 ₁₆ | E1 ₁₆ | E2 ₁₆ | E3 ₁₆ | E4 ₁₆ | E5 ₁₆ | E6 ₁₆ | E7 ₁₆ | E8 ₁₆ | E9 ₁₆ | EA ₁₆ | EB ₁₆ | EC ₁₆ | ED ₁₆ | EE ₁₆ | EF ₁₆ |

Using area for encode data setting
Useless area

Start setting data from the first line. Data set in the lines specified by registers EVP0 through EVP3 (address F2₁₆) will be encoded.

Setting data in the second and subsequent lines, it is possible to set encode data to ten consecutive lines from those specified by registers EVP0 to EVP2.

Similarly to encode line N specified by registers EVP0 through EVP2, extending encode lines to line N-1 and to line N+1, it is possible to read encode data more certainly.

Fig.13 Display monitor

(3) Encode data output

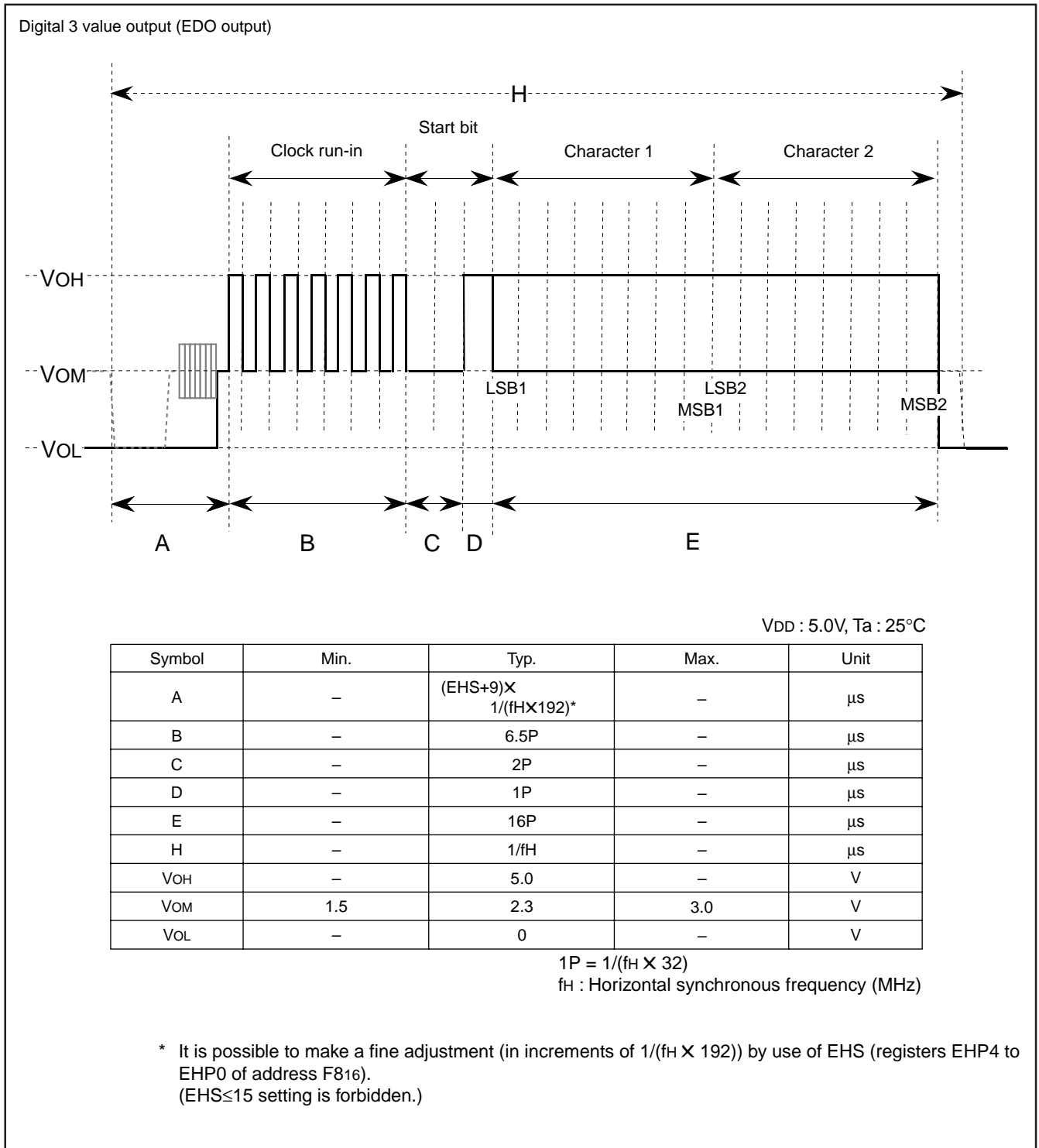


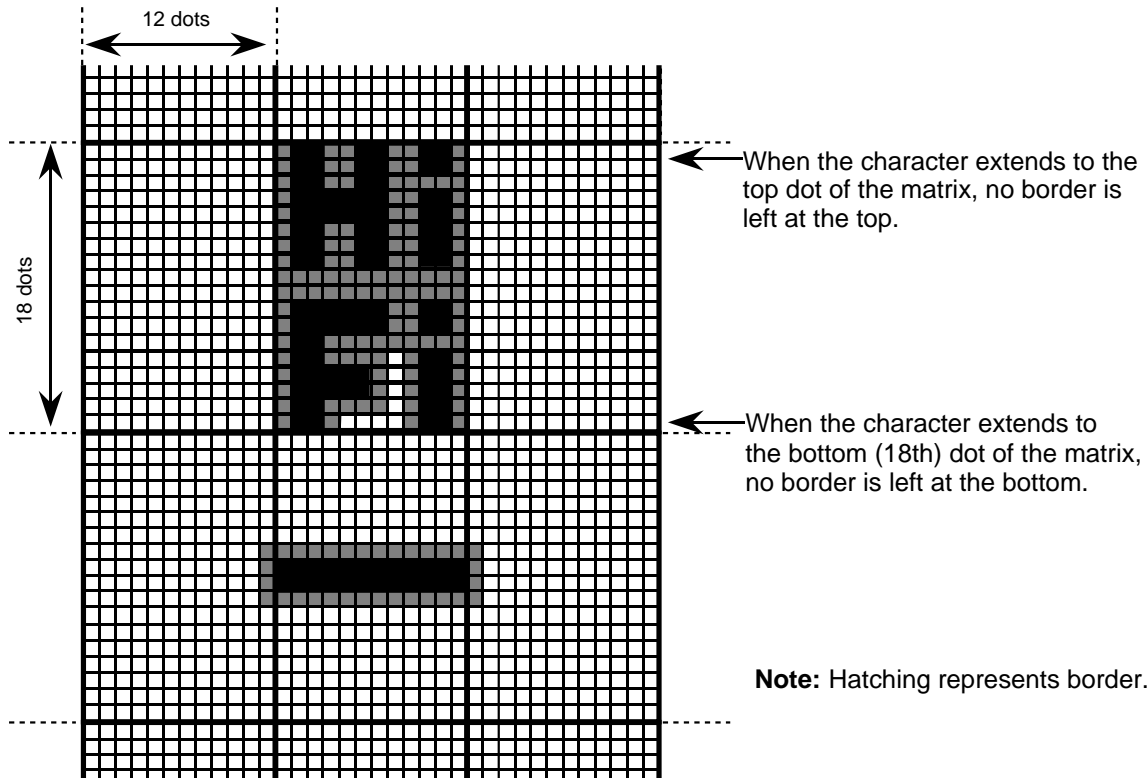
Fig. 14 Encode data output

CHARACTER FONT

Images are composed on a 12 X 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

Character code "FF16" is so fixed as to be blank and to have no background, thus cannot assign a character font to this code.

(1) Border display (set by register BLK0, 1 (address F816))



(2) Cursor display (Border display)

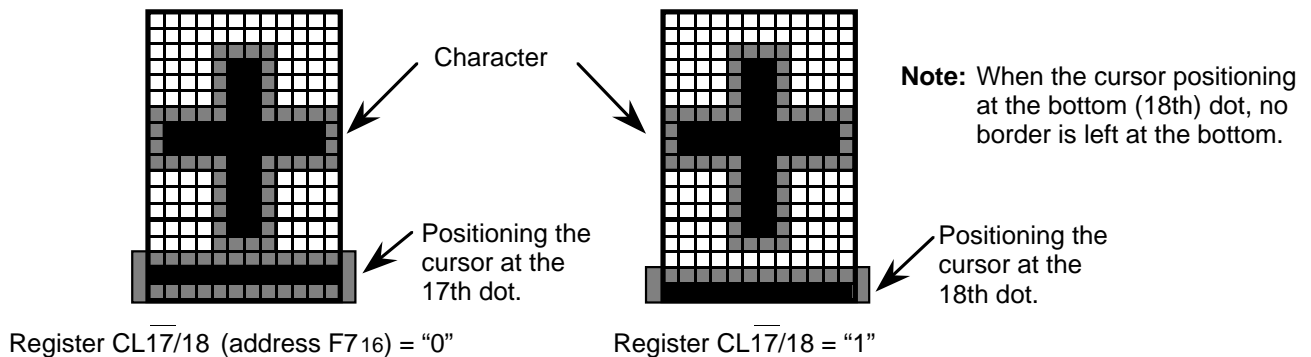


Fig. 15 Character font and border

M35052-XXXSP/FP PERIPHERAL CIRCUIT

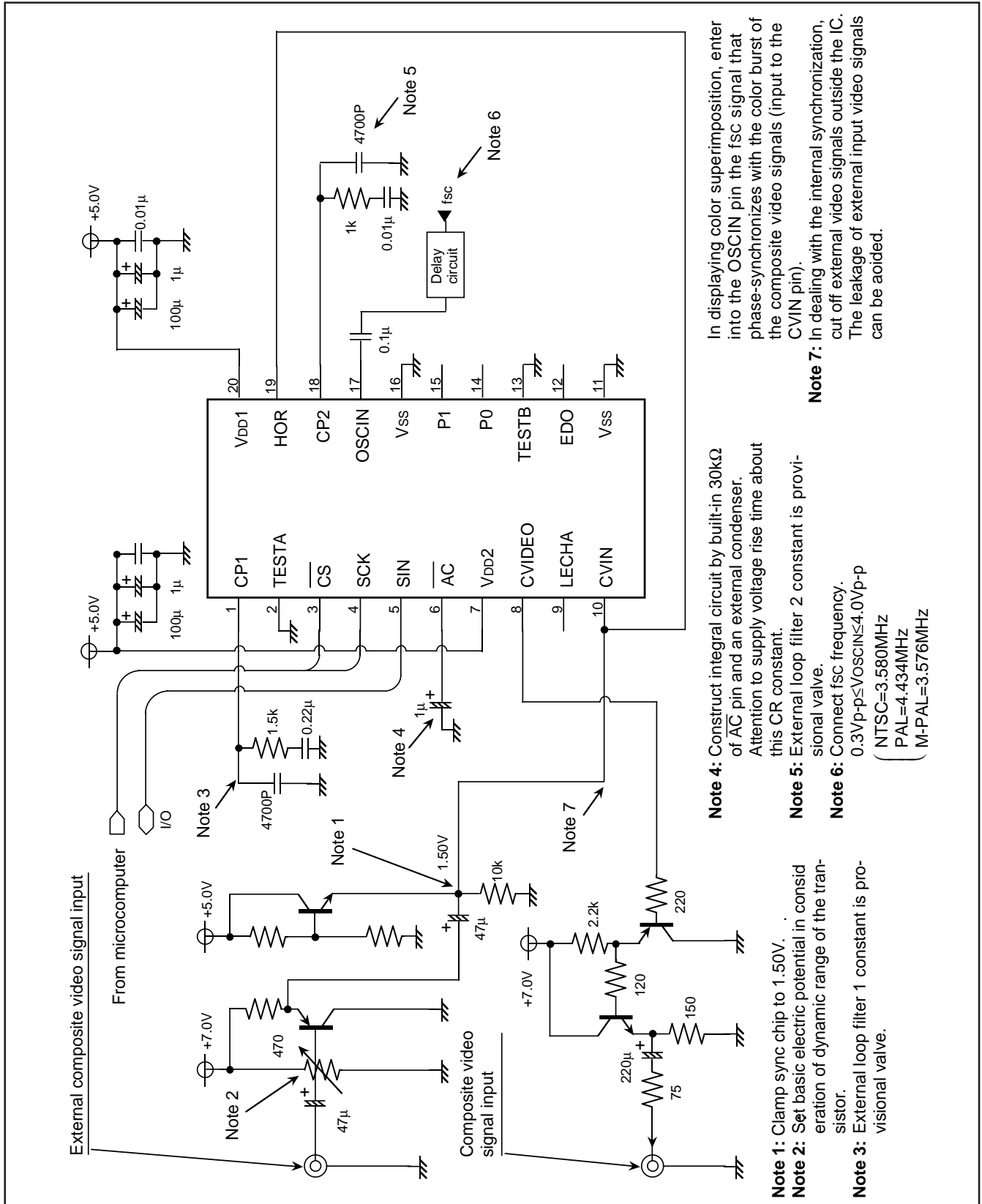


Fig. 16 M35052-XXXSP/FP example of peripheral circuit

Precautions

(1) Points to note in setting the display RAMs

- a) Be careful to the edges may sway depending on the combination of character's background color and raster color.

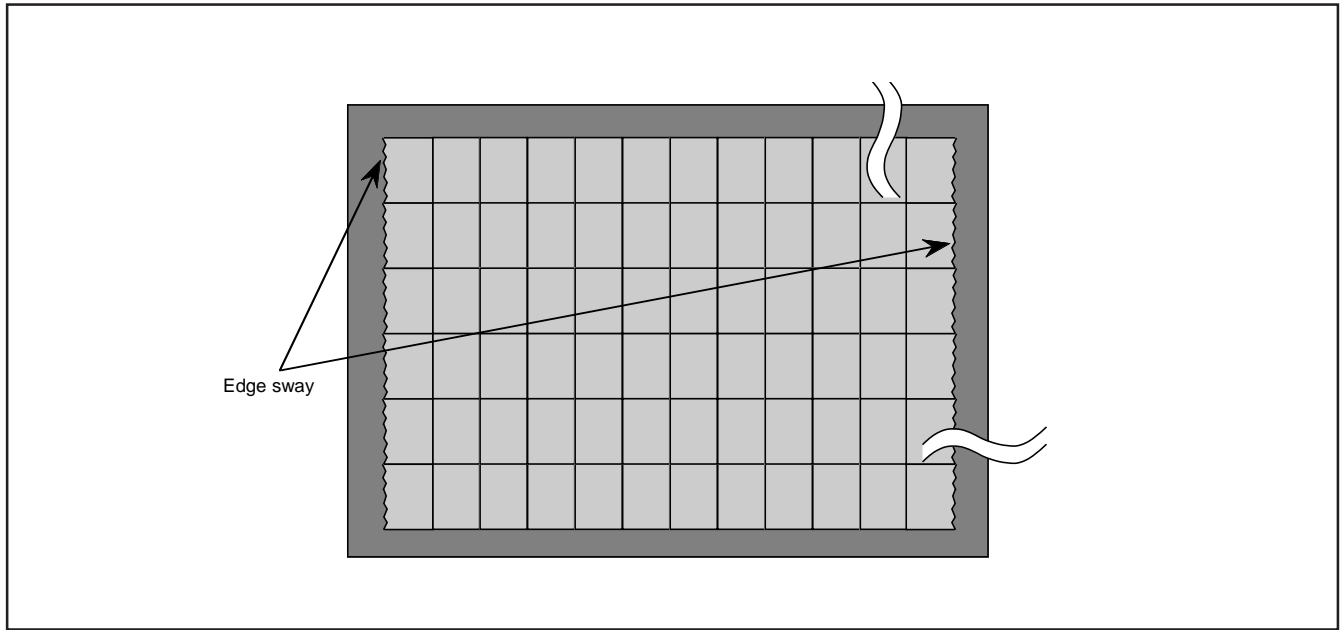


Fig. 17 Example of display

- b) If what display exceeds the display area in dealing with external synchronization, (if use double - size characters), set the character code of the addresses lying outside that display area blank code – "FF₁₆".

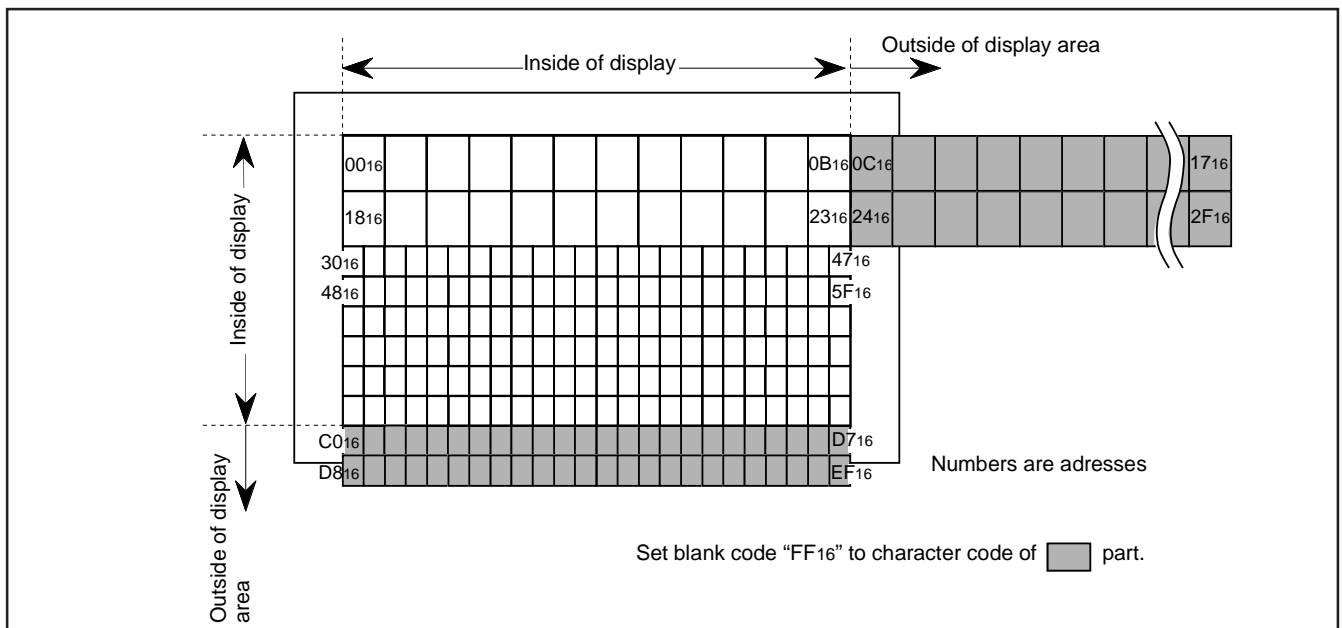


Fig. 18 Example of display

- (2) Before setting registers at the starting of system, be sure to reset the M35052-XXXSP/FP by applying "L" level to the $\bar{A}C$ pin.

(3) Power supply noise

When power supply noise is generated, the internal oscillator circuit does not stabilize, whereby causing horizontal jitters across the picture display. Therefore, connect a bypass capacitor between the power supply and GND.

- 3) Wait 20 ms (the period necessary for the internal oscillation circuit to stabilize) before entering data.
4) Set necessary data in other registers, and make the display RAM ready.

(4) Synchronous correction action

When switching channel or in the special playback mode (quick playback, rewinding, and so on) of VTR, effect of synchronous correction becomes strong, and distortion of a character is apt to occur because the continuity of video signal is suddenly switched. When the continuity of video signal is out of order, erasure of displayed characters is recommended in a extreme short time to raise the quality of displayed characters.

(5) Notes on fsc signal input

This IC amplifies the subcarrier frequency (fsc) signal (NTSC, M-PAL system: 3.58MHz, PAL system: 4.43MHz) input to the OSCIN pin (17-pin) and generates the composite video signal internally. The amplified fsc signal can be destabilized in the following cases.

- a) When the fsc signal is outside of recommended operating conditions.
b) When the waveform of the fsc signal is distorted.
c) When DC level in the fsc waveform fluctuates.

When the amplified signal is unstable, the composite video signal generated inside the IC is also unstable in terms of synchronization with the subcarrier and phase.

Consequently, this results in color flicker and lost synchronization when the composite video signal is generated. Make note of the fact that this may prevent a stable blue background from being formed.

(6) Forbidding to stop entering the fsc signal

This IC doesn't properly work if the fsc signal is not entered into the OSCIN pin (pin 17), so don't stop the fsc signal so as to work the IC. To stop the IC, turn the display off (set 0 in the register DSPON (address F816).)

(7) Forbidding to set data during the period in which the internal oscillation circuit stabilizes

- a) To start entering the fsc signal when its input is stopped.
b) To start oscillating the oscillation circuit for display when its oscillation is stopped. (to assign "1" to the register STOP1 (address F816) when it is assigned "0", or the like.)
c) To turn on the internal bias when it is turned off. (to assign "1" to the register LEVEL1 (address F816) when it is assigned "0".)

There can be instances in which data are not properly set in the registers until the internal oscillation circuit stabilizes, so follow the steps in sequence as given below.

- 1) Set "0" in the register DSPON (address F816). (the display is turned off)
2) Effect the settings a), b), and c) given above.

TIMING REQUIREMENTS ($T_a = -20^{\circ}\text{C}$ to 70°C , $V_{DD} = 5 \pm 0.25\text{V}$, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|--------------------------------|-----------------------------------|--------|------|------|---------------|
| | | Min. | Typ. | Max. | |
| $t_w(\text{SCK})$ | SCK width | 400 | – | – | ns |
| $t_{su}(\overline{\text{CS}})$ | $\overline{\text{CS}}$ setup time | 200 | – | – | ns |
| $t_h(\overline{\text{CS}})$ | $\overline{\text{CS}}$ hold time | 2 | – | – | μs |
| $t_{su}(\text{SIN})$ | SIN setup time | 200 | – | – | ns |
| $t_h(\text{SIN})$ | SIN hold time | 200 | – | – | ns |
| t_{word} | 1 word writing time | 12.8 | – | – | μs |

Note. When oscillation stop at register STOR1 (address F816), 1V (field term) or more of $t_{su}(\overline{\text{CS}})$ and $t_h(\overline{\text{CS}})$ are needed.

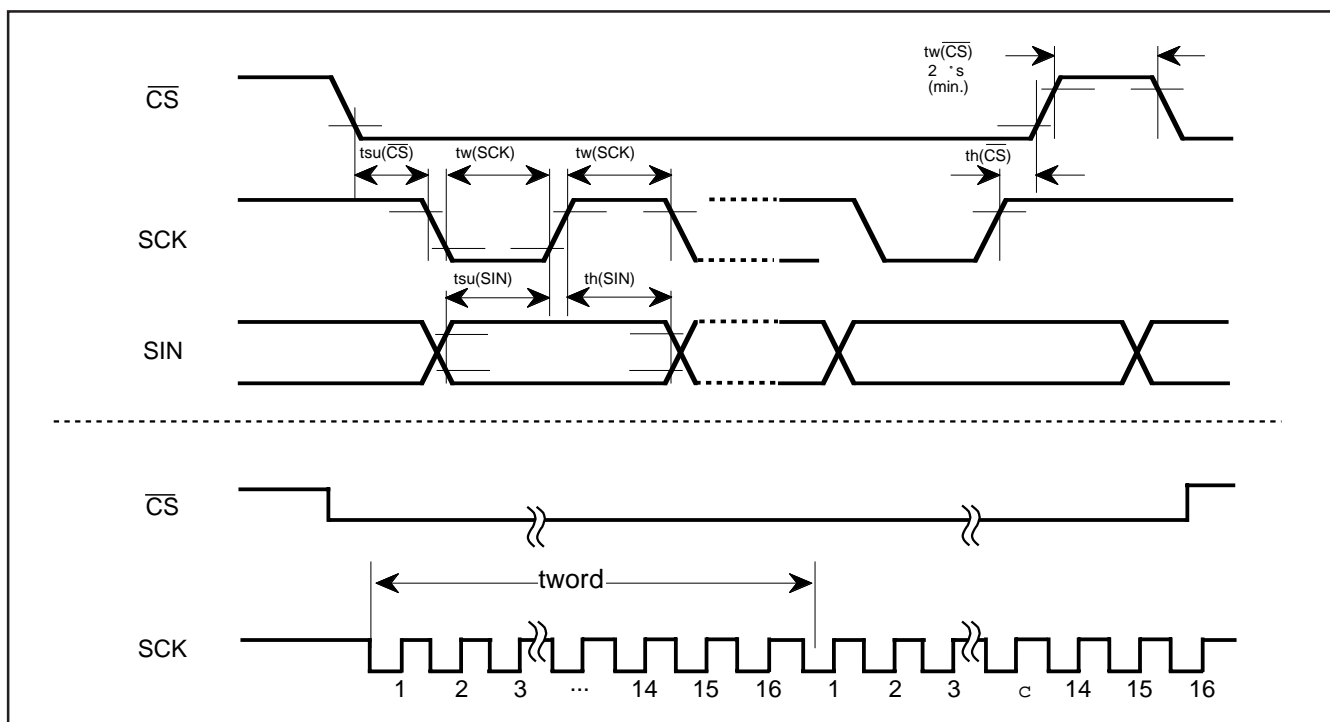


Fig. 19 Serial input timing requirements

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

ABSOLUTE MAXIMUM RATINGS (V_{DD} = 5V, Ta = -20 to 70°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Ratings | Unit |
|------------------|-----------------------|---------------------------------|---|------|
| V _{DD} | Supply voltage | With respect to V _{SS} | -0.3~6.0 | V |
| V _I | Input voltage | | V _{SS} -0.3≤V _I ≤V _{DD} +0.3 | V |
| V _O | Output voltage | | V _{SS} ≤V _O ≤V _{DD} | V |
| P _d | Power dissipation | Ta=25°C | 300 | mW |
| T _{opr} | Operating temperature | | -20~70 | °C |
| T _{stg} | Storage temperature | | -40~125 | °C |

RECOMMENDED OPERATING CONDITIONS (V_{DD} = 5V, Ta = -20 to 70°C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit | |
|--------------------|--|------------------------|-------------------------|---------------------|------|-----|
| | | Min. | Typ. | Max. | | |
| V _{DD} | Supply voltage | 4.75 | 5.00 | 5.25 | V | |
| V _{IH} | "H" level input voltage \overline{AC} , \overline{CS} , SIN, SCK, TESTA, TESTB | 0.8XV _{DD} | V _{DD} | V _{DD} | V | |
| V _{IL} | "L" level input voltage \overline{AC} , \overline{CS} , SIN, SCK, TESTA, TESTB | 0 | 0 | 0.2XV _{DD} | V | |
| V _{CVIN} | CVIN, HOR | - | 2.0V _{P-P} | - | V | |
| V _{OSCIN} | Input voltage OSCIN (Note) | 0.3V _{P-P} | - | 4.0V _{P-P} | V | |
| f _{OSCIN} | Synchronous signal oscillation frequency (Duty 40~60%) | - | 3.580 4.434 3.576 | - | MHz | |
| f _{OSC1} | Display oscillation frequency | 24 charactersX10 lines | - | 480Xf _H | - | MHz |
| f _{OSC2} | | 32 charactersX7 lines | - | 640Xf _H | - | MHz |

Notes 1. Noise component is within 30mV.

2. f_H: Horizontal synchronous frequency (MHz).

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, Ta = 25°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-----------------|---|--|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{DD} | Supply voltage | Ta=-20~70°C | 4.75 | 5.00 | 5.25 | V |
| I _{DD} | Supply current | V _{DD} =5.00V | - | 30 | 50 | mA |
| V _{OH} | "H" level output voltage P0, P1, SIN | V _{DD} =4.75V, I _{OH} =-0.4mA | 3.75 | - | - | V |
| V _{OL} | "L" level output voltage P0, P1, SIN | V _{DD} =4.75V, I _{OL} =-0.4mA | - | - | 0.4 | V |
| R _I | Pull-up resistance \overline{AC} , \overline{CS} , SCK, SIN, TESTB | V _{DD} =5.00V | 10 | 30 | 100 | kΩ |
| V _{OH} | "H" level output voltage EDO | V _{DD} =5.00V, I _{OH} =-0.04mA | 4.0 | - | - | V |
| V _{OM} | "M" level output voltage EDO | V _{DD} =5.00V, I _{OM} =±0.04mA | 1.5 | 2.3 | 3.0 | V |
| V _{OL} | "L" level output voltage EDO | V _{DD} =5.00V, I _{OL} =0.04mA | - | - | 0.4 | V |

VIDEO SIGNAL INPUT CONDITIONS (V_{DD} = 5V, Ta = -20 to 70°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|--------------------|--|-------------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{IN-SC} | Composite video signal input clamp voltage | Sync-chip voltage | - | 1.5 | - | V |

Note for Supplying Power

(1) Timing of power supplying to AC pin

The internal circuit of M35052-XXXSP/FP is reset when the level of the auto clear input pin AC is "L". This pin is hysteresis input with the pull-up resistor. The timing about power supplying of AC pin is shown in Figure 20. t_w is the interval after the supply voltage becomes $0.8 \times V_{DD}$ or more and before the supply voltage to the AC pin (V_{AC}) becomes $0.2 \times V_{DD}$ or more.

After supplying the power (V_{DD} and V_{SS}) to M35052-XXXSP/FP, the t_w time must be reserved for 1ms or more. Before starting

input from the microcomputer, the waiting time (t_s) must be reserved for 500ms after the supply voltage to the AC pin becomes $0.8 \times V_{DD}$ or more.

(2) Timing of power supplying to VDD1 pin and VDD2 pin

The power need to supply to VDD1 and VDD2 at a time, though it is separated perfectly between the VDD1 as the digital line and the VDD2 as the analog line.

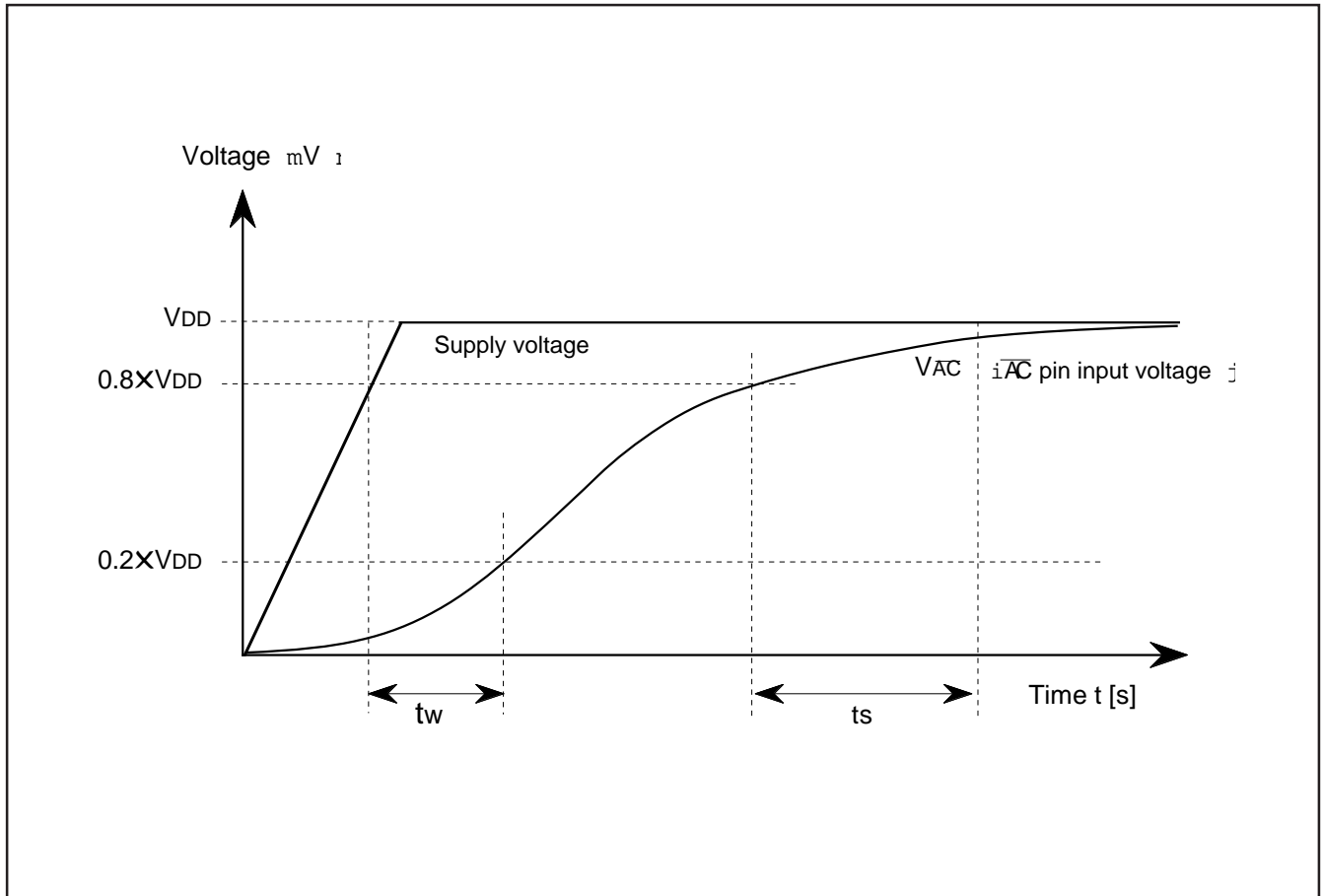


Fig. 20 Timing of power supplying to AC pin

PRECAUTION FOR USE

Notes on noise and latch-up

Connect a capacitor (approx. $0.1 \mu F$) between pins VDD and VSS at the shortest distance using relatively thick wire to prevent noise and latch up.

ROM ORDERING METHOD

Please submit the information described below when ordering Mask ROM.

- (1) ROM Order Confirmation Form 1
- (2) Data to be written into mask ROM EPROM
(three sets containing the identical data)
- (3) Mark Specification Form 1
- (4) Program for character font generating + floppy disk in which character data is input

STANDARD ROM TYPE : M35052-001SP/FP

M35052-001SP/FP is a standard ROM type of M35052-XXXSP/FP
 Character patterns are fixed to the contents of Figure 21 to 23.

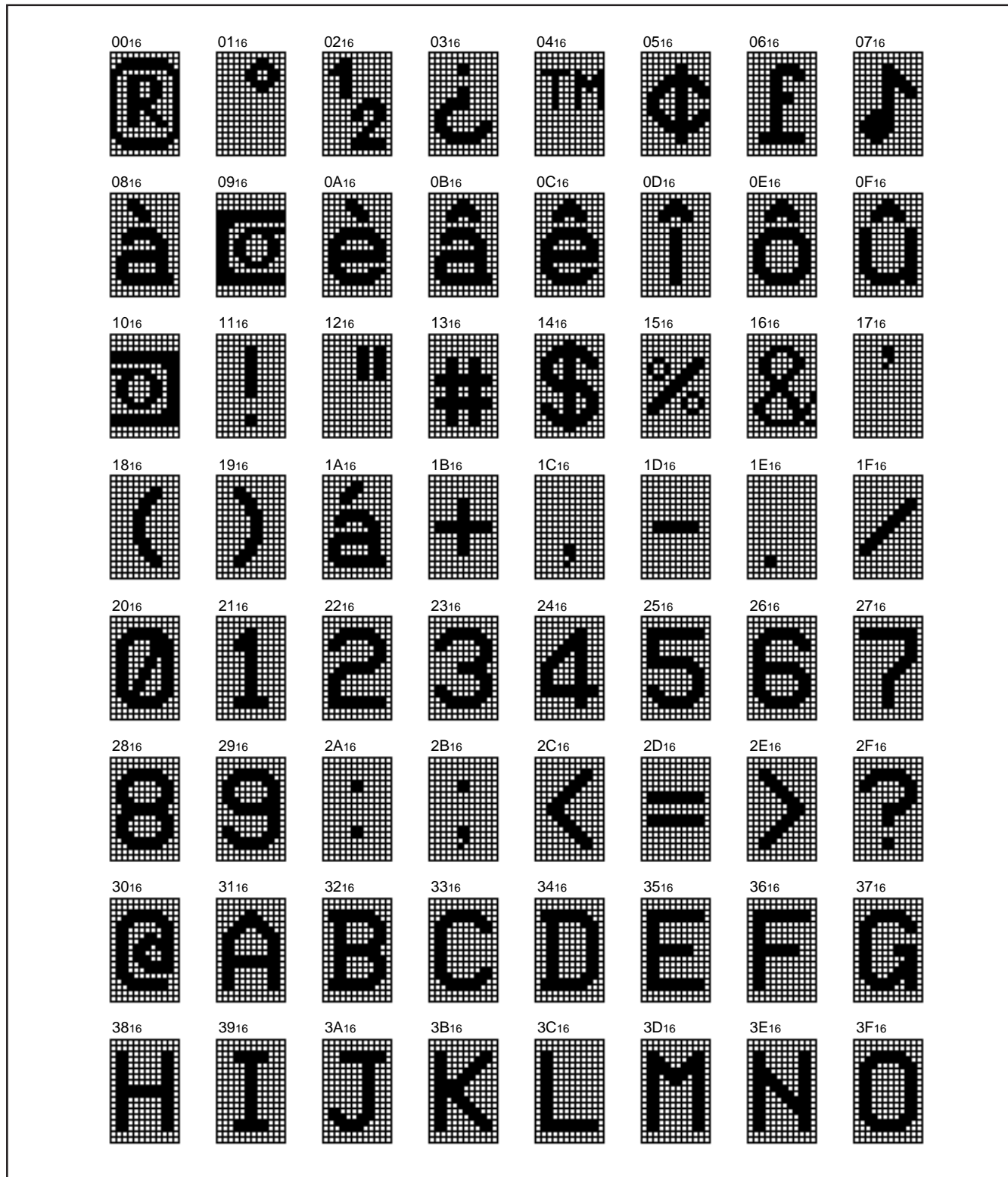


Fig. 21 M35052-001SP/FP character patterns (1)

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

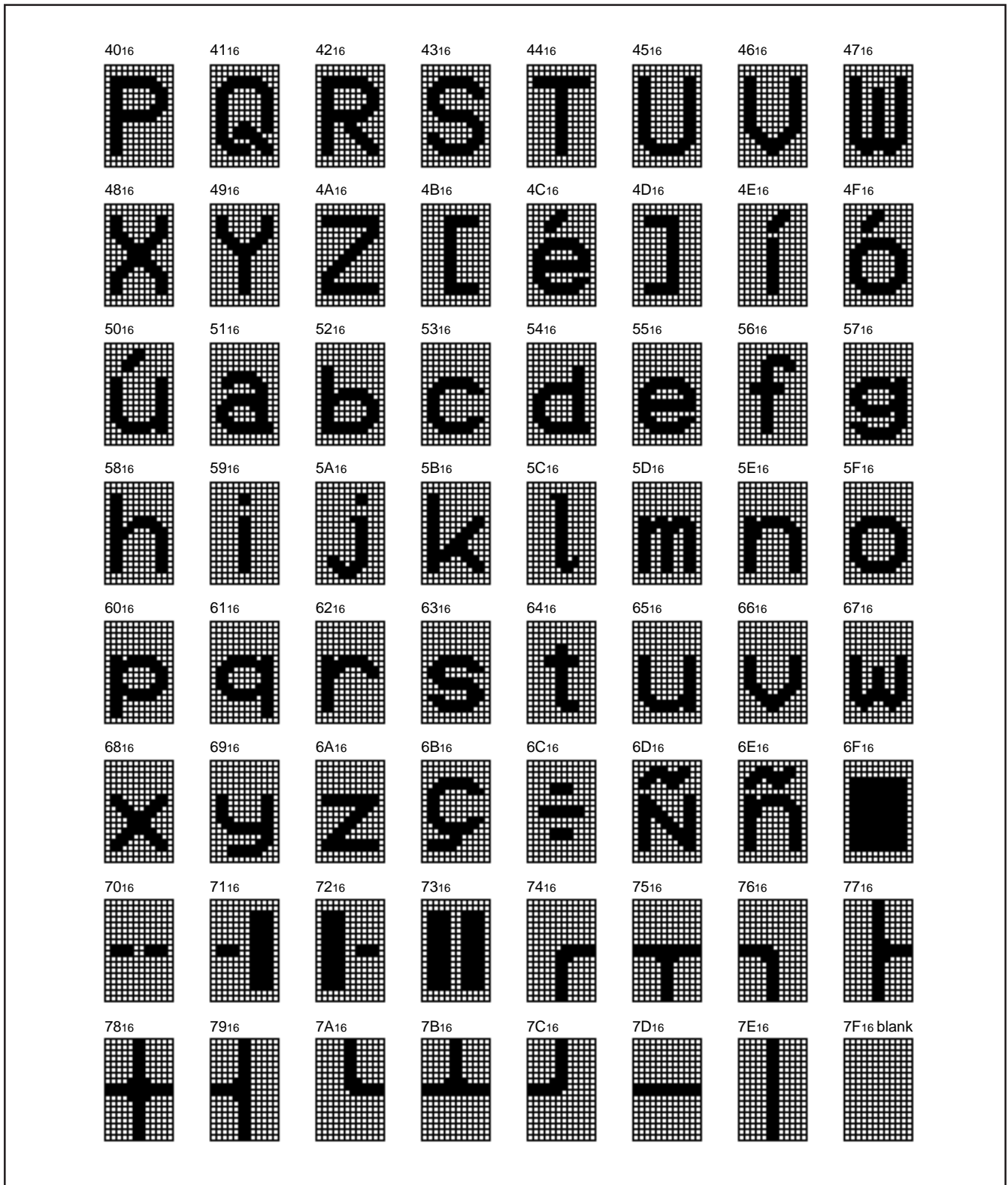
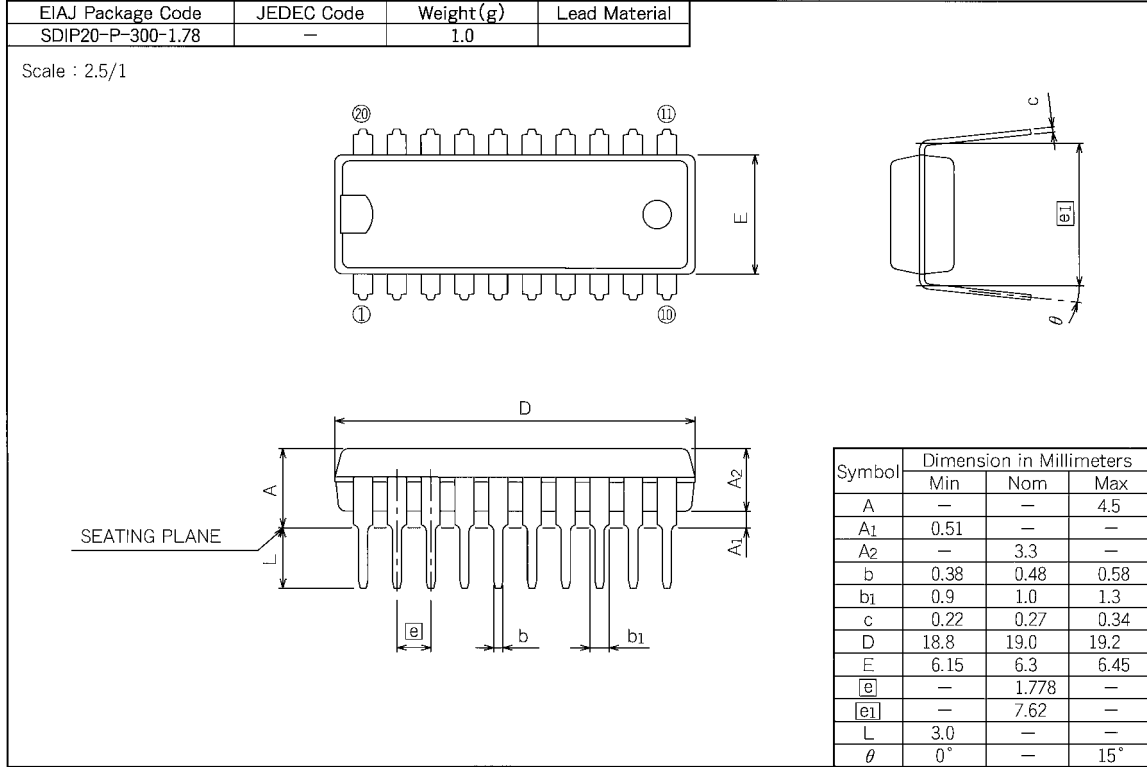


Fig. 22 M35052-001SP/FP character patterns (2)

PACKAGE OUTLINE

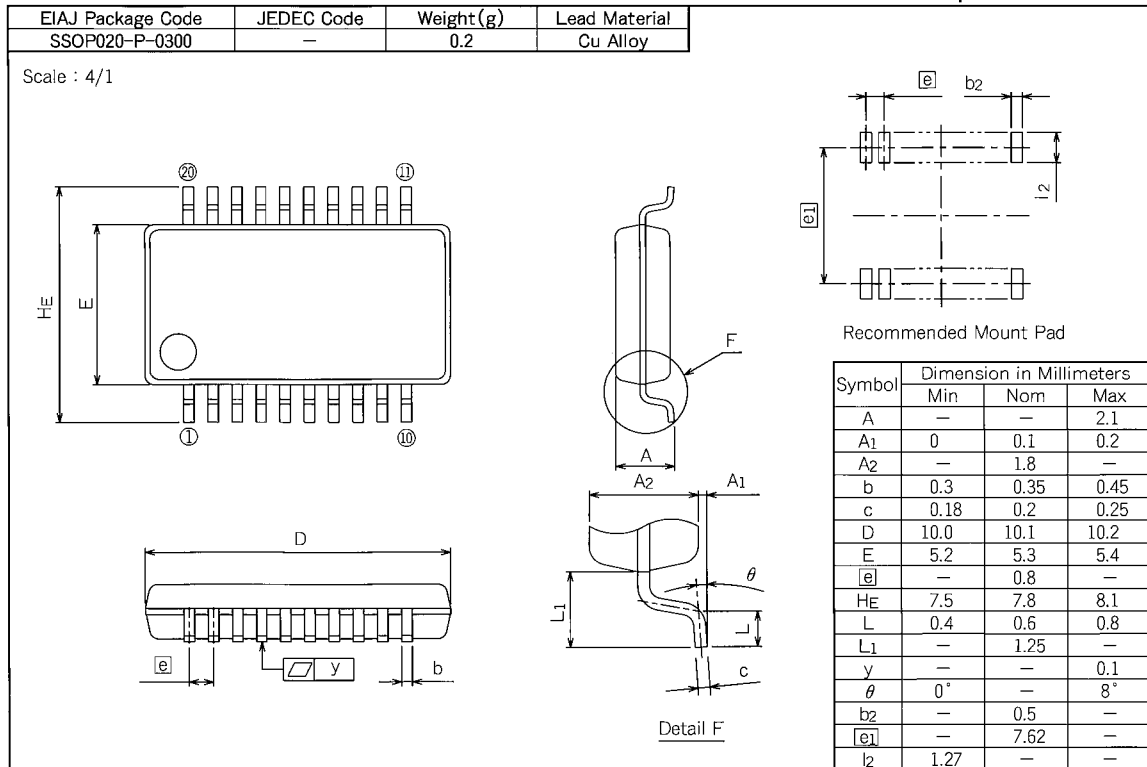
20P4B

Plastic 20pin 300mil SDIP



20P2Q-A

Plastic 20pin 300mil SSOP





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REVISION DESCRIPTION LIST

M35052-XXXSP/FP DATA SHEET

| Rev. No. | Revision Description | Rev. date |
|----------|--|-----------|
| 1.0 | First Edition | 980402 |
| 1.1 | P41 20P2Q-A (20-PIN SSOP) MARK SPECIFICATION FORM B: Note 4 added | 000707 |
| 1.2 | Delete Mask ROM ORDER CONFIRMATION FORM and MASK SPECIFICATION FORM | 000829 |
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