

# M62370GP

3V TYPE 8-BIT 36CH SELECTOR SW BUILT-IN D-A CONVERTER WITH BUFFER AMPLIFIERS

## DESCRIPTION

The M62370GP is a CMOS semiconductor IC, containing 36 channels of 8-bit D-A converters. It is operable with a low supply voltage between 2.7~3.6V, and is easy to use due to serial data input, and 3-pin(DI,CLK,LD) connection with microcomputer. The IC also contains Do pin terminal, enabling cascade connection, and therefore is suitable for automatic control in combination with a microcomputer.

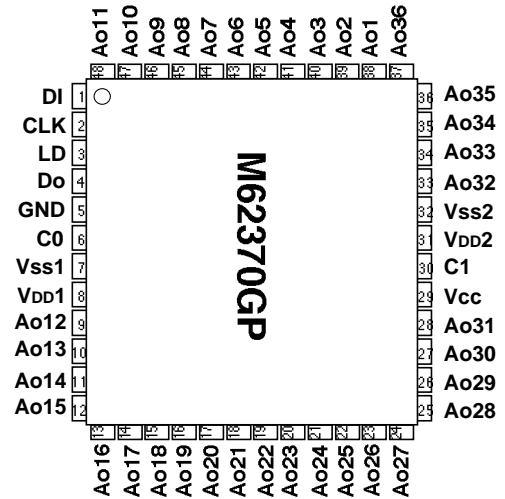
## FEATURES

- Operable with a low voltage between 2.7~3.6V
- 16-bit serial data input(connected via 3 pins:DI,CLK,LD)
- 36 channels built-in of 8-bit D-A converter
- 6 channels of D-A converters capable of selecting and outputting 4 data stored in each converter, through 2 control terminals

## APPLICATION

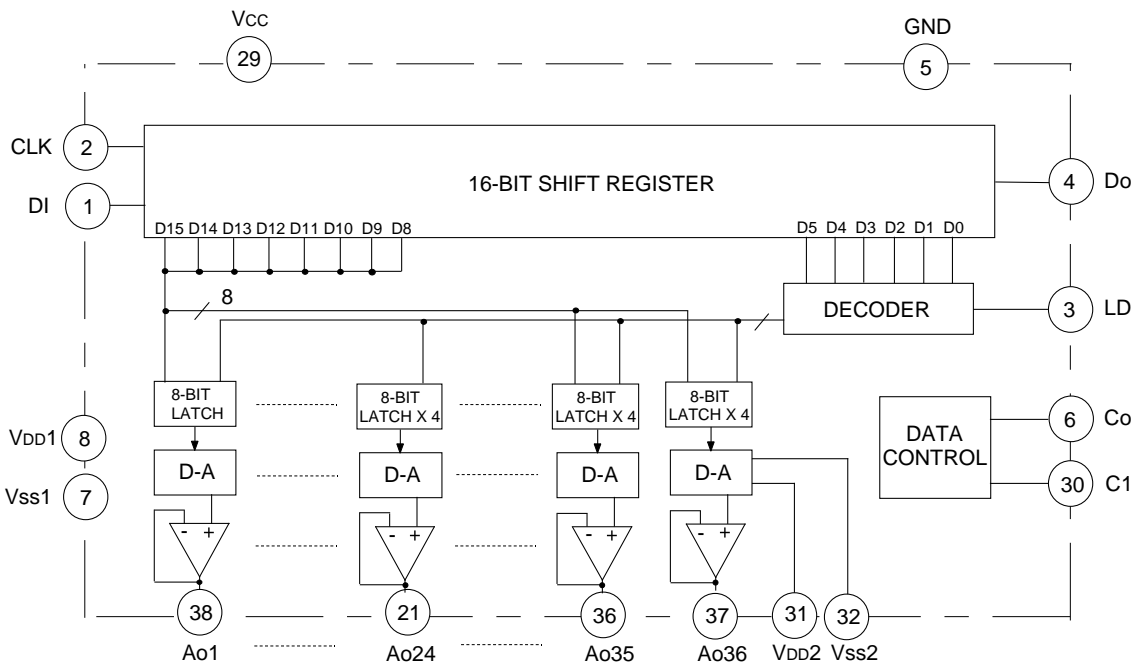
Digital-analog conversion in industrial or home-use electronic equipment.  
Automatic control in combination with EEPROM and microcomputer(Substitute for conventional semi-fixed resistor)

## PIN CONFIGURATION (TOP VIEW)



Outline 48P6D-A

## BLOCK DIAGRAM



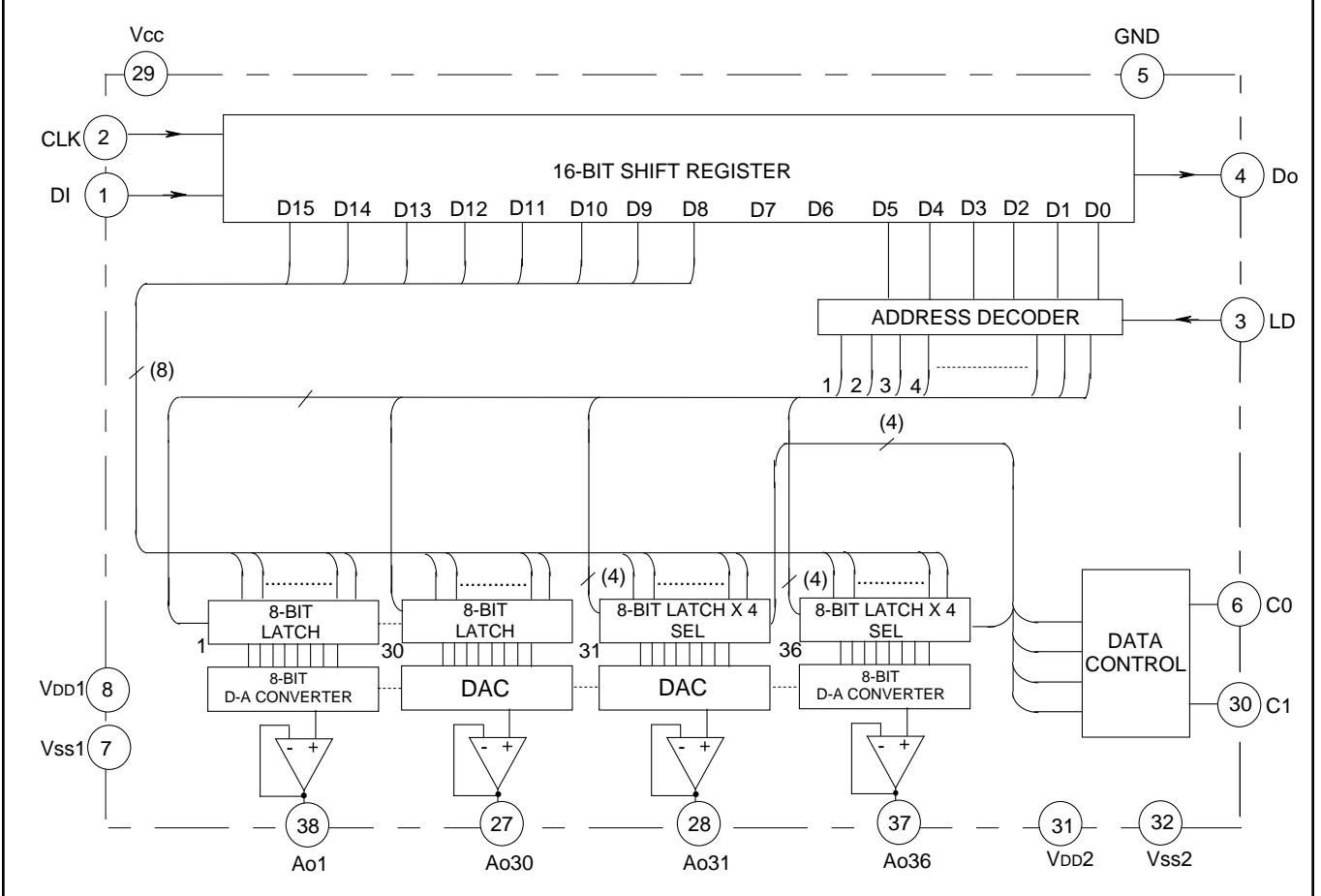
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### EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
①	DI	Serial data input terminal to input 16-bit long serial data
④	Do	Terminal to output MSB data of 16-bit shift register
②	CLK	Shift clock input terminal. Input signal at DI pin is input to 16-bit shift register at rise of shift clock pulse
③	LD	When H-level signal is input to this terminal, the value stored in 16-bit shift register is loaded in decoder and D-A converter output register
⑳	Ao1	8-bit D-A converter output terminal
⋮	⋮	
④⑧	Ao11	
⑨	Ao12	
⋮	⋮	
⑳	Ao31	
③③	Ao32	
⋮	⋮	
③⑦	Ao36	
⑳	Vcc	Power supply terminal
⑤	GND	GND terminal
⑥	C0	Data select signal input terminal 1 for channel No.31 through 36
⑩	C1	Data select signal input terminal 2 for channel No.1 through 24
⑧	VDD1	Upper reference voltage input terminal and power supply to operational amplifier for channel No.1 through 24
⑦	VSS1	Lower reference voltage input terminal for channel No.1 through 24
⑩①	VDD2	Upper reference voltage input terminal and power supply to operational amplifier for channel No.25 through 36
⑩②	VSS2	Lower reference voltage input terminal for channel No.25 through 36

### BLOCK DIAGRAM FOR EXPLANATION OF TERMINALS



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### DIGITAL DATA FORMAT

FIRST LSB LAST MSB

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
← DAC DATA →								← DAC SELECT DATA →							

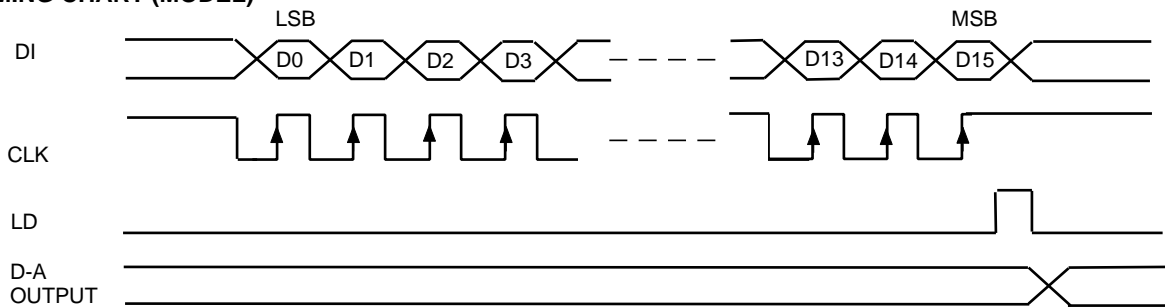
D8	D9	D10	D11	D12	D13	D14	D15	D-A output
0	0	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 1 + V_{refL}$
1	0	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 2 + V_{refL}$
0	1	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 3 + V_{refL}$
1	1	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 4 + V_{refL}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	$(V_{refU}-V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	VrefU

D5	D4	D3	D2	D1	D0	DAC selection
0	0	0	0	0	0	Don't care
0	0	0	0	0	1	Ao1 selection
0	0	0	0	1	0	Ao2 selection
⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	0	Ao30 selection
0	1	1	1	1	1	Ao31(0) selection
1	0	0	0	0	0	Ao32(0) selection
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	0	1	0	0	Ao36(0) selection
1	0	0	1	0	1	Ao31(1) selection
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	1	0	1	0	Ao36(1) selection
1	0	1	0	1	1	Ao31(2) selection
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	0	0	0	0	Ao36(2) selection
1	1	0	0	0	1	Ao31(3) selection
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	0	1	1	0	Ao36(3) selection
1	1	0	1	1	1	Don't care
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	Don't care

C0	C1	Ao31 through Ao36 data selected
0	0	Address 0 selected
0	1	Address 1 selected
1	0	Address 2 selected
1	1	Address 3 selected

\* VrefU=VDD1,VDD2  
VrefL=Vss1,Vss2

### TIMING CHART (MODEL)



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### ABSOLUTE MAXIMUM RATINGS(Ta=25°C,unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage		-0.3~+7.0	V
V <sub>O</sub>	Output voltage		-0.3~V <sub>CC</sub> +0.3	V
P <sub>d</sub>	Power dissipation		400	mW
K <sub>θ</sub>	Terminal derating	Ta 25°C	4	mW/°C
T <sub>opr</sub>	Operating temperature		-20~+85	°C
T <sub>stg</sub>	Storage temperature		-40~+125	°C

### ELECTRICAL CHARACTERISTICS

#### Digital part(V<sub>CC</sub>=+3V±10%, V<sub>CC</sub>=V<sub>DD</sub>,Ta=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V <sub>CC</sub>	Supply voltage		2.7	3.0	5.5	V
I <sub>CC</sub>	Circuit current	CLK=1MHz operation,V <sub>CC</sub> =3V,I <sub>AO</sub> =0μA		1.0		mA
I <sub>ILK</sub>	Input leak current		-10		10	μA
V <sub>IL</sub>	Input low voltage				0.6	V
V <sub>IH</sub>	Input high voltage		2.4			V
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> =2.5mA			0.4	V
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> =-400μA	V <sub>CC</sub> -0.4			V

Note.Standard value is at Ta=25°C

#### Analog part(V<sub>CC</sub>=+3V±10%, V<sub>CC</sub>=V<sub>DD</sub>,Ta=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I <sub>DD</sub>	Current dissipation			5.0		mA
V <sub>DD</sub>	D-A converter upper reference voltage range		2.7	3.0	5.5	V
V <sub>SS</sub>	D-A converter lower reference voltage range		GND		V <sub>DD</sub> -2	V
V <sub>AO</sub>	Buffer amplifier output voltage range	I <sub>AO</sub> =±100μA	0.1		V <sub>DD</sub> -0.1	V
		I <sub>AO</sub> =+300μA -200μA	0.2		V <sub>DD</sub> -0.2	
I <sub>AO</sub>	Buffer amplifier output driving range	Upper saturation voltage=0.4V Lower saturation voltage=0.3V	-300		500	μA
SD <sub>L</sub>	Differential nonlinearity error	V <sub>CC</sub> =2.700V V <sub>DD</sub> =2.700V	-1.0		1.0	LSB
SL	Nonlinearity error	V <sub>CC</sub> =2.700V V <sub>DD</sub> =2.700V	-1.5		1.5	LSB
S <sub>ZERO</sub>	Zero code error	V <sub>SS</sub> =0.050V	-2		2	LSB
S <sub>FULL</sub>	Full scale error	No load(I <sub>AO</sub> =±0)	-2		2	LSB
C <sub>O</sub>	Output capacitive load				0.1	μF
R <sub>O</sub>	Buffer amplifier output impedance			50		

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### AC CHARACTERISTICS ( $V_{CC}=V_{DD}, T_a=-20 \sim +85^{\circ}\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
tCKL	Clock "L" pulse width		200			ns
tCKH	Clock "H" pulse width		200			ns
tCR	Clock rise time				200	ns
tCF	Clock fall time				200	ns
tDCH	Data set up time		30			ns
tCHD	Data hold time		60			ns
tCHL	LD set up time		200			ns
tLDC	LD hold time		100			ns
tLDH	LD "H" pulse duration		100			ns
tDo	Data output delay time	$C_L=100\text{pF}$	70		350	ns
tLDD	D-A converter output setting time	$C_L=100\text{pF}, V_{AO}:0.3 \rightarrow 2.7\text{V}$ The time until the output becomes the final value of $\pm 2$ LSB			100	$\mu\text{s}$

### TIMING CHART

