M62381FP

8-BIT 8CH MULTIPLYING D-A CONVERTER WITH BUFFER AMPLIFIERS

DESCRIPTION

The M62381FP is an integrated circuit semiconductor of CMOS structure with 8 channels of built-in 8-bit resolution multiplication type D-A converters.

The input data is a easy-to-use 3-wire serial transfer method and it is able to cascading serial use with Do terminal.

This device is capable of 4 quadrant multiplication because of built-in inverting type amplifier.

FEATURES

- Digital data transfer method
  3-wire 12-bit serial data transfer method(DI,CLK,LD)
- High pressure proof(V_{DD}±5V)
- Short setting time
- Built-in reset terminal,all the buffer amplifier outputs forces zero volts.

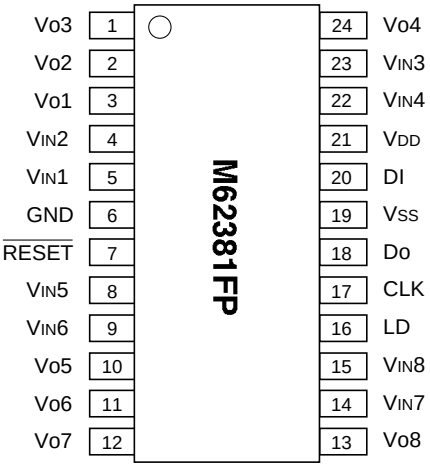
APPLICATION

Signal gain control of DISPLAY-MONITOR or CTV.

Conversion from digital control data analog control data for form-use and industrial equipment.

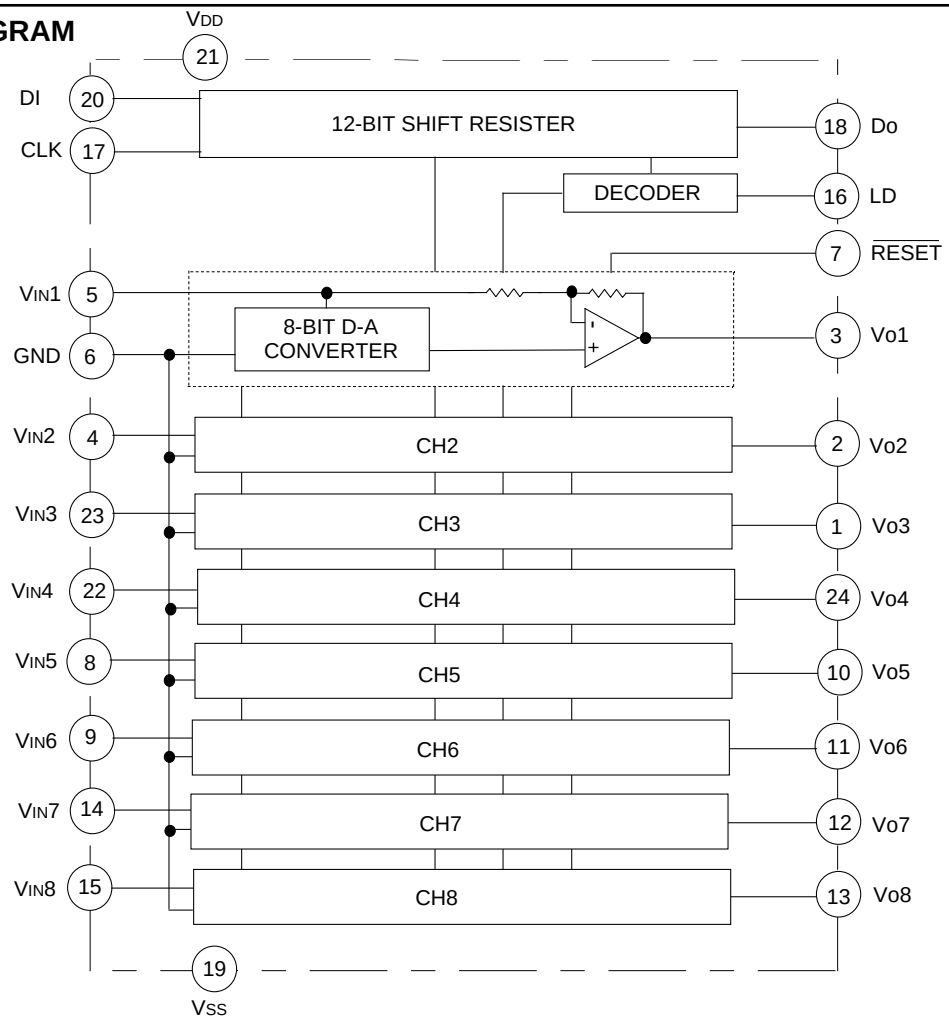
Automatic adjustment by combination with EEPROM and micro-computer.
(replacement of conventional half-fixed resistor.)

PIN CONFIGURATION (TOP VIEW)



Outline 24P2V-A

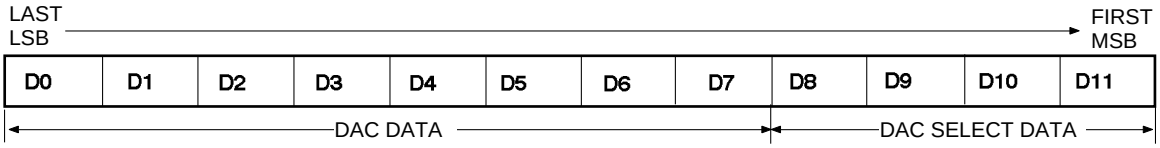
BLOCK DIAGRAM



EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
⑳	DI	Serial data input terminal
⑱	Do	Serial data output terminal
⑰	CLK	Serial clock input terminal
⑯	LD	When LD terminal level is "H",latch circuit data is load
③	Vo1	8-bit resolution D-A converter output terminal
②	Vo2	
①	Vo3	
㉔	Vo4	
⑩	Vo5	
⑪	Vo6	
⑫	Vo7	
⑬	Vo8	
㉑	V_{DD}	Analog and digital common power supply terminal
⑲	V_{SS}	Analog negative power supply terminal
⑥	GND	GND terminal
⑤	$V_{IN}1$	D-A converter reference input terminal
④	$V_{IN}2$	
㉓	$V_{IN}3$	
㉒	$V_{IN}4$	
⑧	$V_{IN}5$	
⑨	$V_{IN}6$	
⑭	$V_{IN}7$	
⑮	$V_{IN}8$	
⑦	$\overline{\text{RESET}}$	When $\overline{\text{RESET}}$ terminal level is "H",all D-A output terminal became "0V"

DIGITAL DATA FORMAT



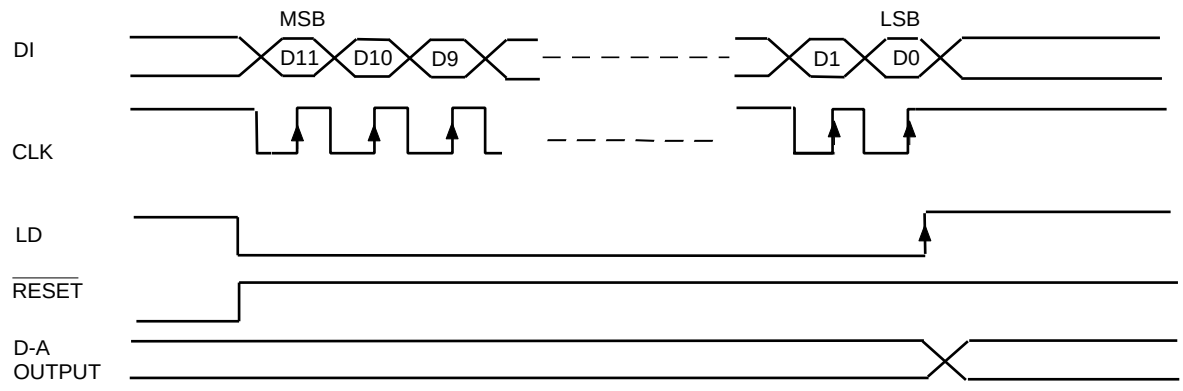
(1)DAC set up data

MSB							LSB	
D7	D6	D5	D4	D3	D2	D1	D0	D-A output
0	0	0	0	0	0	0	0	$-V_{IN}$
0	0	0	0	0	0	0	1	(1/128-1) X V_{IN}
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	(127/128-1) X V_{IN}
1	0	0	0	0	0	0	0	(128/128-1) X V_{IN}
1	0	0	0	0	0	0	1	(129/128-1) X V_{IN}
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	(254/128-1) X V_{IN}
1	1	1	1	1	1	1	1	(255/128-1) X V_{IN}

(2)DAC select data

MSB			LSB	
D11	D10	D9	D8	DAC selection
0	0	0	0	Don't care
0	0	0	1	ch1 selection
0	0	1	0	ch2 selection
⋮	⋮	⋮	⋮	⋮
0	1	1	1	ch7 selection
1	0	0	0	ch8 selection
1	0	0	1	Don't care
⋮	⋮	⋮	⋮	⋮
1	1	1	1	Don't care

TIMING CHART (MODEL)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage		-0.3 to +6.0	V
V_{IN}	Digital input voltage		-0.3 to +6.0	V
Vss	Analog negative supply voltage		-6.0 to +3.0	V
V_{IN}	Input voltage		Vss+0.3 to V_{DD}-0.3	V
Vo	Output voltage		Vss+0.3 to V_{DD}-0.3	V
Topr	Operating temperature		-20 to +85	°C
Tstg	Storage temperature		-40 to +125	°C

ELECTRICAL CHARACTERISTICS

Digital part(V_{DD}=+5V, V_{SS}=-5V,$V_{DD}\geq V_{IN}\geq$Vss,GND=0V,Ta=-20 to +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage		4.5	5.0	5.5	V
I_{ILK}	Input leak current	V_{IN}=0 to Vcc	-10		10	µA
V_{IL}	Input low voltage				0.2V_{DD}	V
V_{IH}	Input high voltage		0.8V_{DD}			V
V_{OL}	Output low voltage	I_{OL}=2.5mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=-400µA	V_{DD}-0.4			V

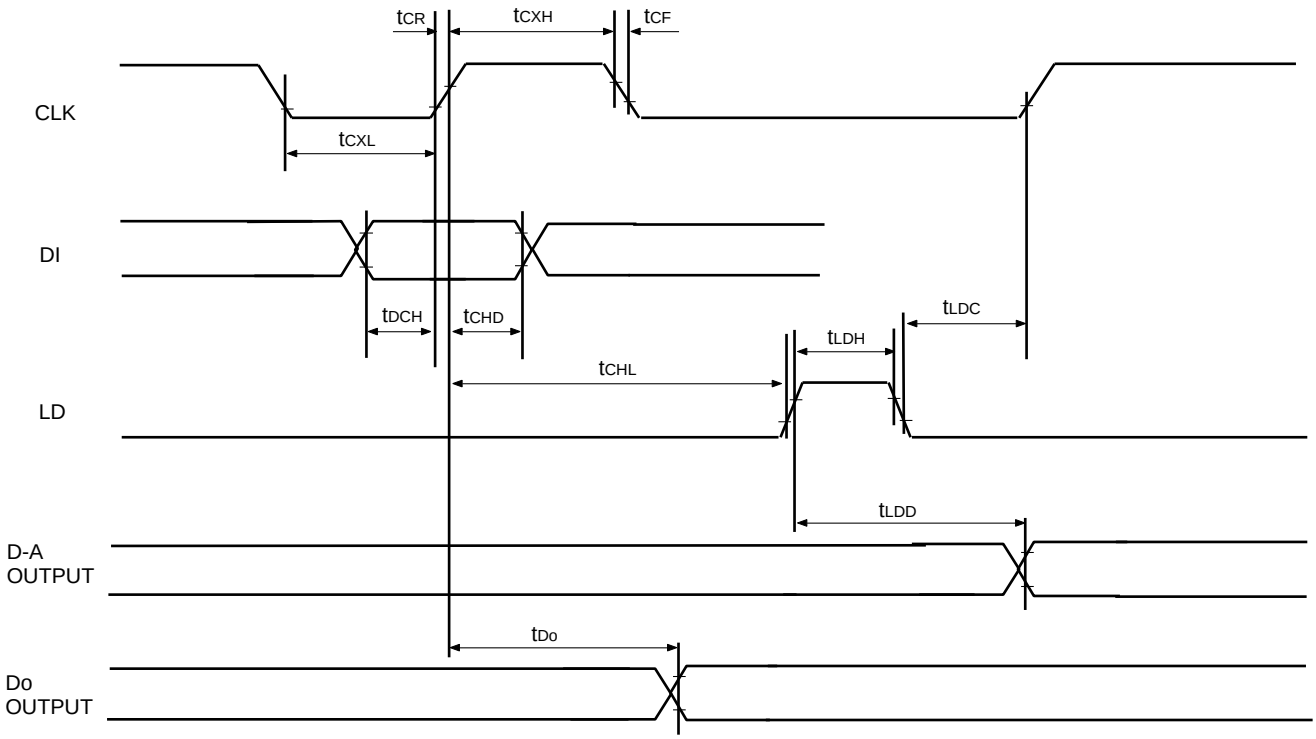
Analog part(V_{DD}=+5V, V_{SS}=-5V,$V_{DD}\geq V_{IN}\geq$Vss,GND=0V,Ta=-20 to +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{IN}	D-A converter reference input current			0.2	0.4	mA
V_{AO}	Buffer amplifier output voltage range	I_{AO}=±500µA	V_{AOZERO} +0.15		V_{AOFULL} -0.15	V
		I_{AO}=±1mA	V_{AOZERO} +0.3		V_{AOFULL} -0.3	
I_{AO}	Buffer amplifier output current range	V_{AO}=V_{AOZERO}+0.3 to V_{AOFULL}-0.3	-1.0		1.0	mA
RES	Resolution		8			bit
DNL	Differential nonlinearity	V_{DD}-0.5≥V_{IN}≥V_{SS}+0.5	-1.0		1.0	LSB
NL	Nonlinearity		-1.5		1.5	LSB
EG	Gain error		-3		3	%FS

AC CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{CXL}	Clock "L"pulse width		200			ns
t_{CXH}	Clock "H"pulse width		200			ns
t_{CR}	Clock rise time				200	ns
t_{CF}	Clock fall time				200	ns
t_{DCH}	Data set up time		30			ns
t_{CHD}	Data hold time		60			ns
t_{CHL}	LD set up time		200			ns
t_{LDH}	LD hold time		100			ns
t_{LDC}	LD "H" pulse width		100			ns
t_{Do}	Data output delay time	C_L=100pF	70		350	ns
t_{LDD}	D-A output setting time	Without load				ns

TIMING CHART



APPLICATION EXAMPLE