

9 Jul, 1997  
**MITSUBISHI LSIs**  
**M5M51016BTP,RT-12VL-I,**  
**-12VLL-I**  
**1048576-BIT(65536-WORD BY 16-BIT)CMOS STATIC RAM**

**DESCRIPTION**

The M5M51016BTP, RT are a 1048576-bit CMOS static RAM organized as 65536 word by 16-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low stand-by current and low operation current and ideal for the battery back-up application.

The M5M51016BTP,RT are packaged in a 44-pin thin small outline package which is a high reliability and high density surface mount device (SMD). Two types of devices are available. M5M51016BTP(normal lead bend type package), M5M51016BRT (reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

**FEATURES**

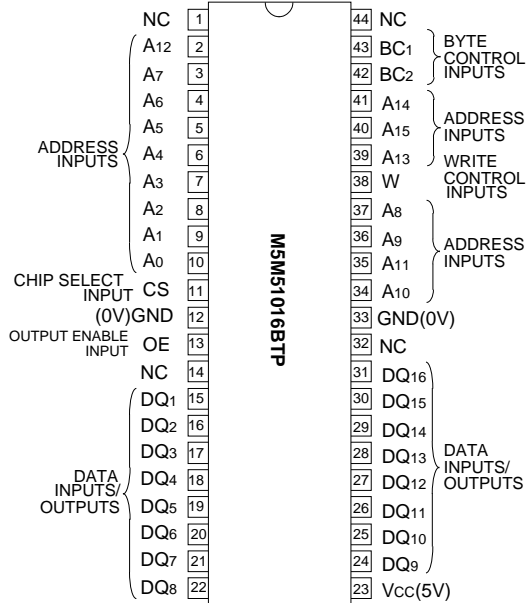
Type name	Access time (max)	Power supply current	
		Active (max)	stand-by (max)
M5M51016BTP,RT-12VL	120ns	12mA (1MHz)	120µA (V <sub>cc</sub> = 3.6V)
M5M51016BTP,RT-12VLL	120ns		24µA (V <sub>cc</sub> = 3.6V) 0.3µA (V <sub>cc</sub> = 3.0V, typ)

- Single +3.0V power supply
- Low stand-by current 0.3E A (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by CS, BC<sub>1</sub> & BC<sub>2</sub>
- Data hold on +2V power supply
- Three-state outputs : OR-tie capability
- OE prevents data contention in the I/O bus
- Common data I/O
- Package  
M5M51016BTP,RT ..... 44pin 400mil TSOP(II)

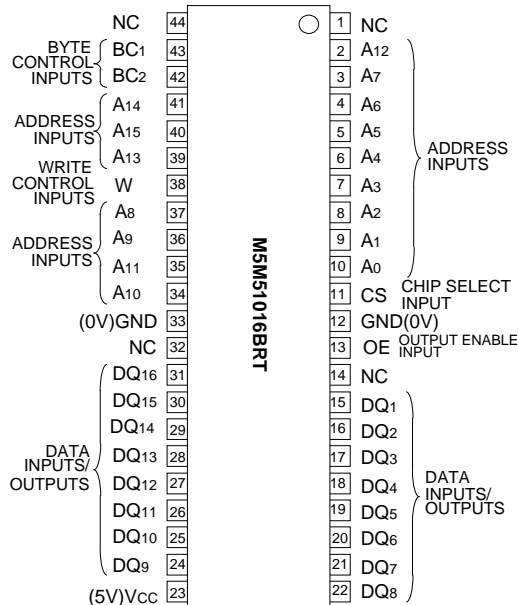
**APPLICATION**

Small capacity memory units

**PIN CONFIGURATION (TOP VIEW)**



Outline 44P3W - H (400mil TSOP Normal Bend)



Outline 44P3W - J (400mil TSOP Reverse Bend)

NC : NO CONNECTION

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**FUNCTION**

The operation mode of the M5M51016B series are determined by a combination of the device control inputs  $\overline{BC1}$ ,  $\overline{BC2}$ , CS, W and  $\overline{OE}$ . Each mode is summarized in the function table.

A write cycle is executed whenever the low level W overlaps with the low level  $\overline{BC1}$  and/or  $\overline{BC2}$  and the high level CS. The address must be set up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of W,  $\overline{BC1}$ ,  $\overline{BC2}$  or CS, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input  $\overline{OE}$  directly controls the output stage. Setting the  $\overline{OE}$  at a high level, the output stage is in a high-impedance state, and the databus contention problem in the write cycle is eliminated.

A read cycle is executed by setting W at a high level and  $\overline{OE}$  at a low level while  $\overline{BC1}$  and/or  $\overline{BC2}$  and CS are in an active state. ( $\overline{BC1}$  and/or  $\overline{BC2}=\overline{L}$ , CS=H)

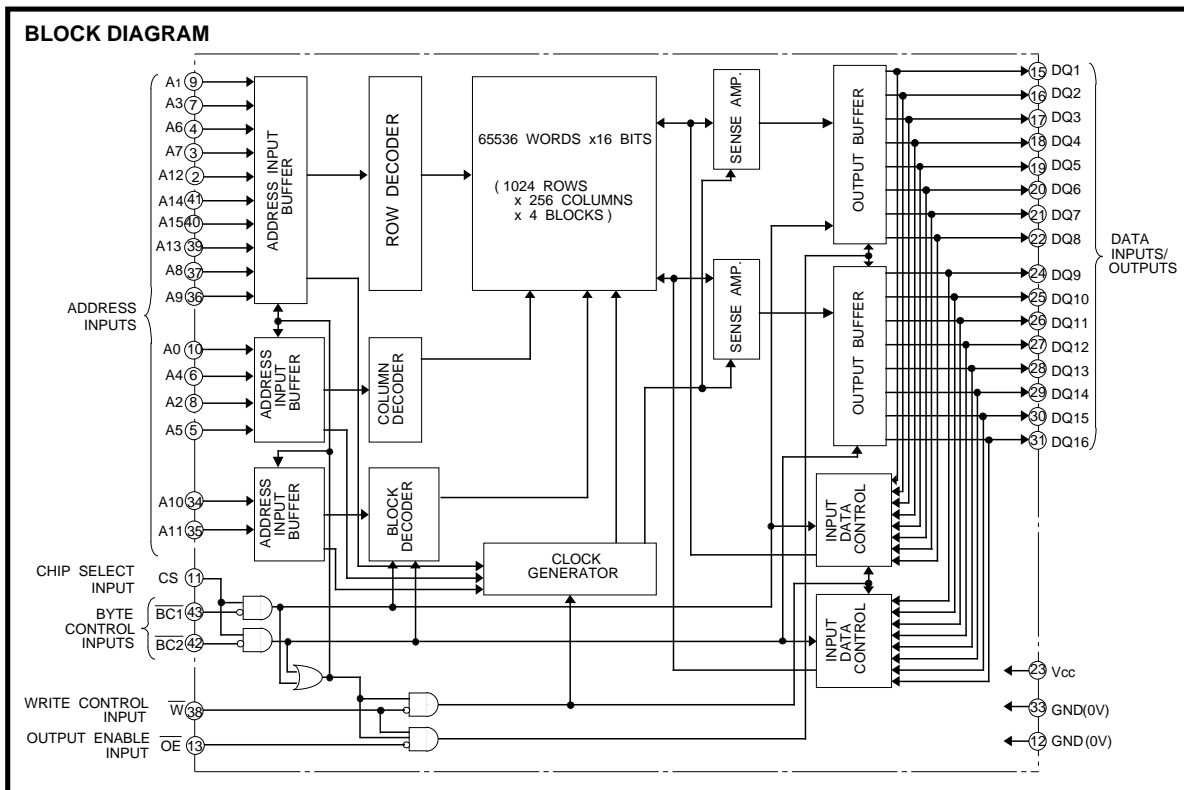
When setting  $\overline{BC1}$  at a high level and the other pins are in an active state, upper-Byte are in a selectable mode in which both reading and writing are enabled, and lower-Byte are in a non-selectable mode. And when setting  $\overline{BC2}$  at a high level and the other pins are in an active state, lower-Byte are in a selectable mode and upper -Byte are in a non-selectable mode.

When setting  $\overline{BC1}$  and  $\overline{BC2}$  at a high level or CS at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled.

In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by  $\overline{BC1}$ ,  $\overline{BC2}$  and CS. The power supply current is reduced as low as the stand-by current which is specified as  $I_{CC3}$  or  $I_{CC4}$ , and the memory data can be held at +2V power supply, enabling battery back-up operation during powerfailure or power-down operation in the non-selected mode.

CS	$\overline{BC1}$	$\overline{BC2}$	W	$\overline{OE}$	Mode	DQ1~8	DQ9~16	$I_{CC}$
L	X	X	X	X	Non selection	High-Z	High-Z	Stand-by
X	H	H	X	X	Non selection	High-Z	High-Z	Stand-by
H	H	L	L	X	Upper-Byte Write	High-Z	Din	Active
H	H	L	H	L	Upper-Byte Read	High-Z	Dout	Active
H	H	L	H	H	—	High-Z	High-Z	Active
H	L	H	L	X	Lower-Byte Write	Din	High-Z	Active
H	L	H	H	L	Lower-Byte Read	Dout	High-Z	Active
H	L	H	H	H	—	High-Z	High-Z	Active
H	L	L	L	X	Word Write	Din	Din	Active
H	L	L	H	L	Word Read	Dout	Dout	Active
H	L	L	H	H	—	High-Z	High-Z	Active

(High-Z=High-impedance)



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**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage	With respect to GND	- 0.3 ~ 4.6	V
V <sub>I</sub>	Input voltage		- 0.3* ~ V <sub>CC</sub> + 0.3	V
V <sub>O</sub>	Output voltage		0 ~ V <sub>CC</sub>	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =25 °C	1	W
T <sub>opr</sub>	Operating temperature		- 40 ~ 85	°C
T <sub>stg</sub>	Storage temperature		- 65 ~ 150	°C

\* -3.0V in case of AC ( Pulse width ≤ 50ns )

**DC ELECTRICAL CHARACTERISTICS** (T<sub>a</sub>=- 40 ~ 85°C , V<sub>CC</sub>=2.7V ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>IH</sub>	High-level input voltage		2.0		V <sub>CC</sub> +0.3V	V
V <sub>IL</sub>	Low-level input voltage		- 0.3*		0.6	V
V <sub>OH1</sub>	High-level output voltage 1	I <sub>OH</sub> = -1mA	2.4			V
V <sub>OH2</sub>	High-level output voltage 2	I <sub>OH</sub> = - 0.1mA	V <sub>CC</sub> -0.5V			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 2mA			0.4	V
I <sub>I</sub>	Input current	V <sub>I</sub> = 0 ~ V <sub>CC</sub>			±1	µA
I <sub>O</sub>	Output current in off-state	BC <sub>1</sub> and BC <sub>2</sub> = V <sub>IH</sub> or CS = V <sub>IL</sub> or OE = V <sub>IH</sub> , V <sub>I/O</sub> = 0 ~ V <sub>CC</sub>			±1	µA
I <sub>CC1W</sub>	Word operation (16bit) Active supply current (AC, TTL level)	BC <sub>1</sub> and BC <sub>2</sub> = V <sub>IL</sub> , CS = V <sub>IH</sub> other inputs = V <sub>IH</sub> or V <sub>IL</sub> Output-open(duty 100%)	Min cycle	27	50	mA
I <sub>CC2W</sub>			1MHz	5	12	mA
I <sub>CC1B</sub>	Byte operation (8bit) Active supply current (AC, TTL level)	(BC <sub>1</sub> = V <sub>IH</sub> and BC <sub>2</sub> = V <sub>IL</sub> ) or (BC <sub>1</sub> = V <sub>IL</sub> and BC <sub>2</sub> = V <sub>IH</sub> ), CS = V <sub>IH</sub> other inputs = V <sub>IH</sub> or V <sub>IL</sub> Output-open(duty 100%)	Min cycle	20	30	mA
I <sub>CC2B</sub>			1MHz	3	10	mA
I <sub>CC3</sub>	Stand-by current	1) CS ≤ 0.2V, other inputs = 0~V <sub>CC</sub> 2) BC <sub>1</sub> , BC <sub>2</sub> ≥ V <sub>CC</sub> - 0.2V, CS ≥ V <sub>CC</sub> - 0.2V other inputs = 0~V <sub>CC</sub>	-VL		120	µA
			-VLL		24	µA
I <sub>CC4</sub>	Stand-by current	BC <sub>1</sub> and BC <sub>2</sub> = V <sub>IH</sub> or CS = V <sub>IL</sub> , other inputs = 0~V <sub>CC</sub>			1	mA

\* -3.0V in case of AC ( Pulse width ≤ 30ns )

**CAPACITANCE** (T<sub>a</sub>=- 40 ~ 85°C , V<sub>CC</sub>=2.7V ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>I</sub>	Input capacitance ( except BC <sub>1</sub> , BC <sub>2</sub> )	V <sub>I</sub> =GND, V <sub>I</sub> =25mVrms, f=1MHz			6	pF
C <sub>I(BC)</sub>	Input capacitance ( BC <sub>1</sub> , BC <sub>2</sub> )	V <sub>I</sub> =GND, V <sub>I</sub> =25mVrms, f=1MHz			9	pF
C <sub>O</sub>	Output capacitance	V <sub>O</sub> =GND, V <sub>O</sub> =25mVrms, f=1MHz			8	pF

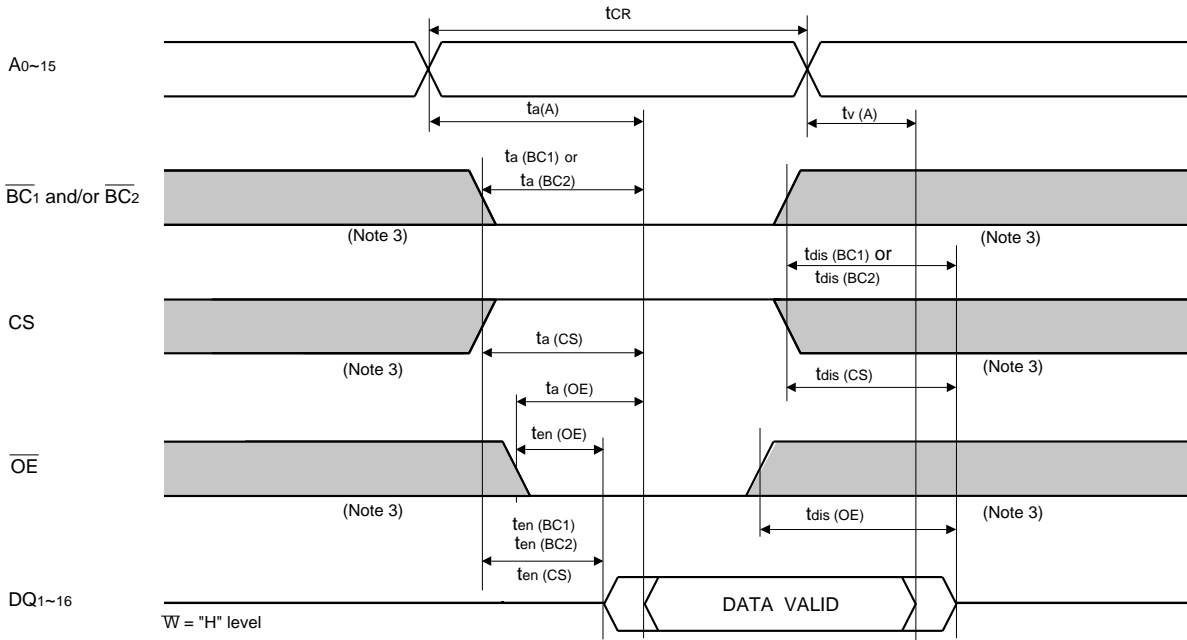
Note 1: Direction for current flowing into an IC is positive (no mark).

2: Typical value is V<sub>CC</sub> = 3.3V, T<sub>a</sub> = 25°C

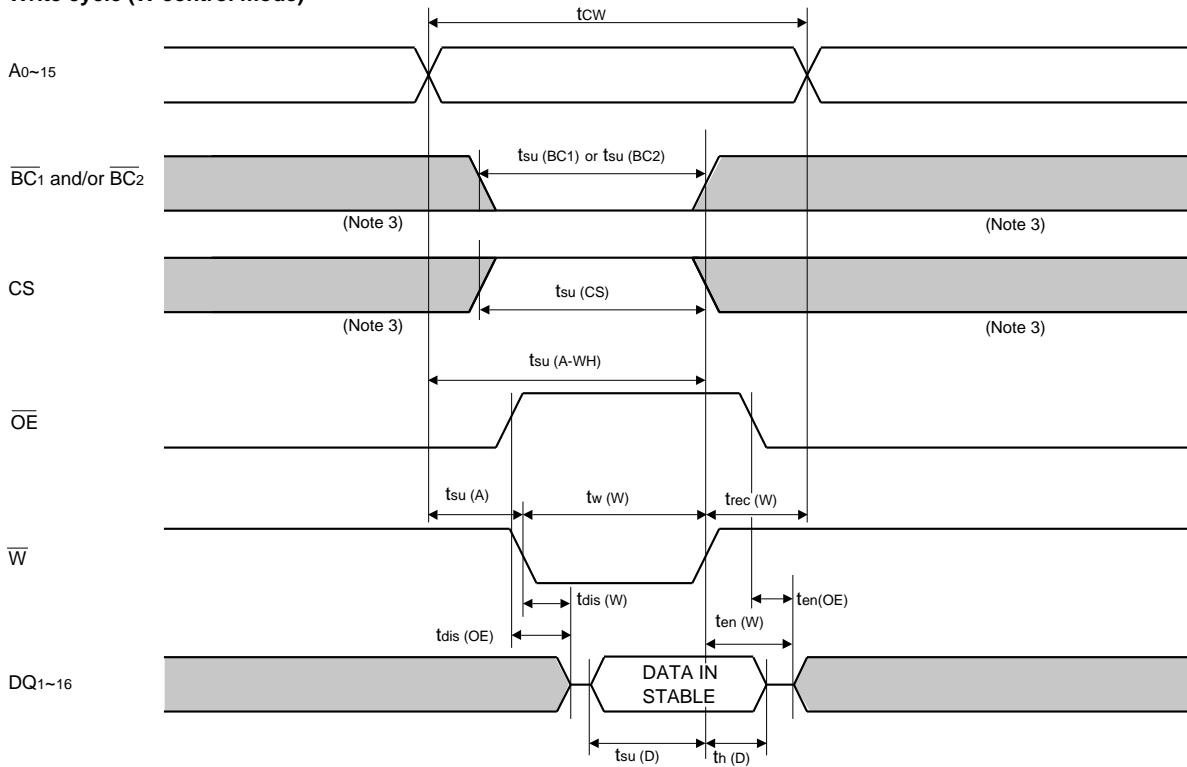


**(4) TIMING DIAGRAMS**

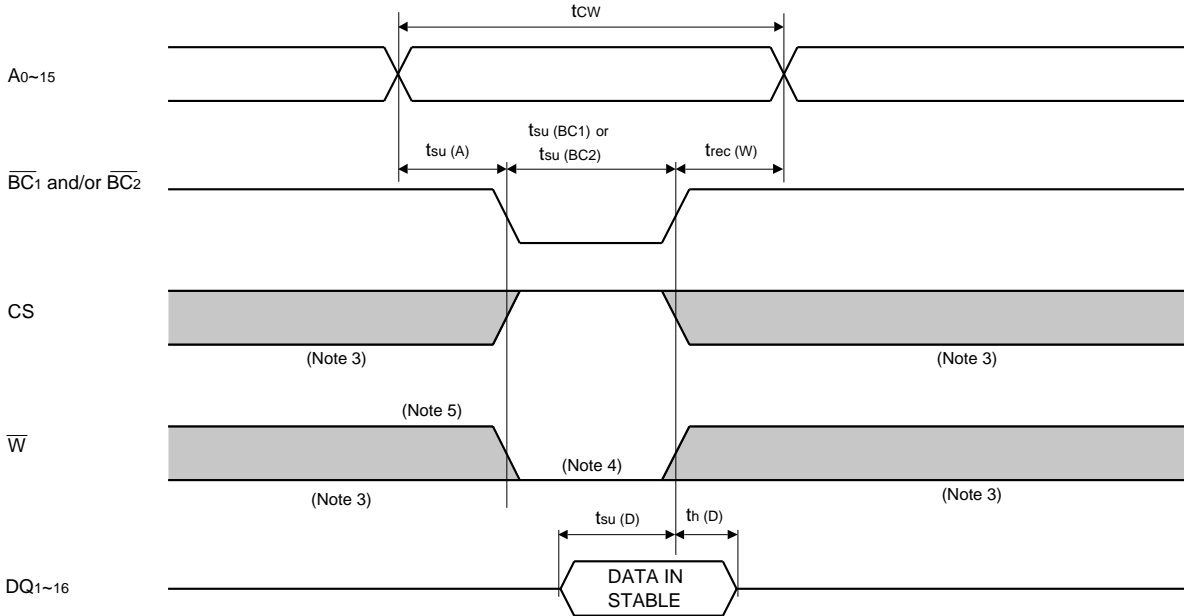
**Read cycle**



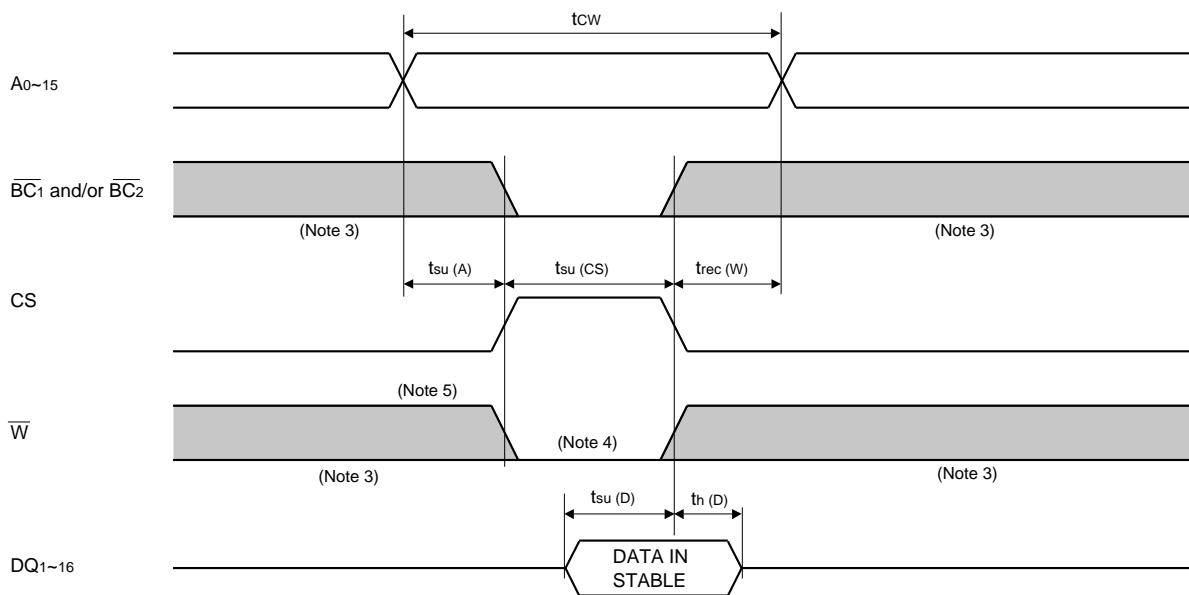
**Write cycle ( $\overline{W}$  control mode)**



**Write cycle ( $\overline{BC}$  control mode)**



**Write cycle (CS control mode)**



- Note 3: Hatching indicates the state is "don't care".  
 4: Writing is executed while CS high overlaps  $\overline{BC}_1$  and/or  $\overline{BC}_2$  low and  $\overline{W}$  low.  
 5: When the falling edge of  $\overline{W}$  is simultaneously or prior to the falling edge of  $\overline{BC}_1$  and/or  $\overline{BC}_2$  or rising edge of CS, the outputs are maintained in the high impedance state.  
 6: Don't apply inverted phase signal externally when DQ pin is output mode.

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**POWER DOWN CHARACTERISTICS**

**(1) ELECTRICAL CHARACTERISTICS** ( $T_a = -40 \sim 85^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_I(BC)$	Byte control input $\overline{BC}_1$ & $\overline{BC}_2$		2.0			V
$V_I(CS)$	Chip select input CS	$2.7V \leq V_{CC(PD)}$			0.6	V
		$V_{CC(PD)} < 2.7V$			0.2	
$I_{CC(PD)}$	Power down supply current	$V_{CC} = 3V$ 1) $CS \leq 0.2V$ other inputs = 0 ~ 3V 2) $BC_1$ & $BC_2 \geq V_{CC} - 0.2V$ , $CS \geq V_{CC} - 0.2V$ , other inputs=0~3V	-VL		100	$\mu\text{A}$
			-VLL	0.3	20 (Note 7)	

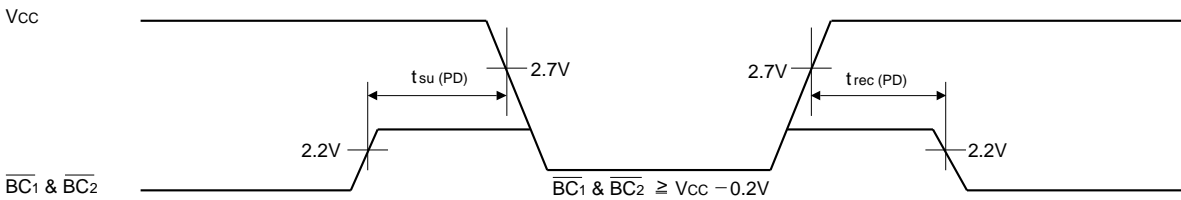
Note7.  $I_{CC(PD)} = 1\mu\text{A}$  in case of  $T_a = 25^\circ\text{C}$

**(2) TIMING REQUIREMENTS** ( $T_a = -40 \sim 85^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

**(3) POWER DOWN CHARACTERISTICS**

**$\overline{BC}$  control mode**



**CS control mode**

