

M5M5V416CWG -70HI

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V416C is a family of low voltage 4-Mbit static RAMs organized as 262144-words by 16-bit, fabricated by Mitsubishi's high-performance 0.18µm CMOS technology.

The M5M5V416C is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

M5M5V416CWG is packaged in a CSP (chip scale package), with the outline of 7.0mm x 8.5mm, ball matrix of 6 x 8 (48ball) and ball pitch of 0.75mm. It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

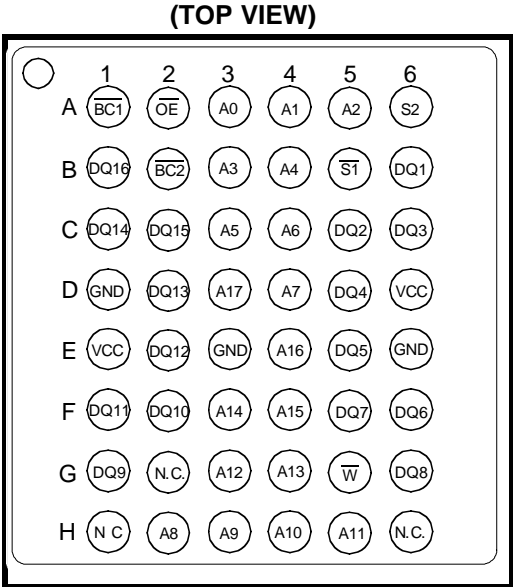
FEATURES

- Single 2.7~3.0V power supply
- Small stand-by current: 0.1µA (2.85V, typ.)
- No clocks, No refresh
- Data retention supply voltage = 2.0V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by $\overline{S1}$, $S2$, $\overline{BC1}$ and $\overline{BC2}$
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE prevents data contention in the I/O bus
- Process technology: 0.18µm CMOS
- Package: 48ball 7.0mm x 8.5mm CSP

| Version, Operating temperature | Part name | Power Supply | Access time max. | Stand-by current (Vcc=3.0V) | | | | | Active current Icc1 (3.0V, typ.) |
|--------------------------------------|-------------------|-----------------|---------------------|-----------------------------|------|----------------|------|------|---|
| | | | | * Typical | | Ratings (max.) | | | |
| | | | | 25°C | 40°C | 25°C | 40°C | 85°C | |
| I-version -40 ~ +85°C | M5M5V416CWG -70HI | 2.7 ~ 3.0V | 70ns | 0.2 | 0.4 | 1 | 2 | 20 | 30mA (10MHz) 5mA (1MHz) |

* Typical parameter indicates the value for the center of distribution, and not 100% tested.

PIN CONFIGURATION



| Pin | Function |
|------------------|-----------------------|
| A0 ~ A17 | Address input |
| DQ1 ~ DQ16 | Data input / output |
| $\overline{S1}$ | Chip select input 1 |
| S2 | Chip select input 2 |
| \overline{W} | Write control input |
| \overline{OE} | Output enable input |
| $\overline{BC1}$ | Lower Byte (DQ1 ~ 8) |
| $\overline{BC2}$ | Upper Byte (DQ9 ~ 16) |
| Vcc | Power supply |
| GND | Ground supply |

Outline: 48FJA
NC: No Connection

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FUNCTION

The M5M5V416CWG is organized as 262144-words by 16-bit. These devices operate on a single +2.7~3.0V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

The operation mode are determined by a combination of the device control inputs $\overline{BC1}$, $\overline{BC2}$, $S1$, $S2$, \overline{W} and \overline{OE} . Each mode is summarized in the function table.

A write operation is executed whenever the low level \overline{W} overlaps with the low level $\overline{BC1}$ and/or $\overline{BC2}$ and the low level $\overline{S1}$ and the high level $S2$. The address(A0~A17) must be set up before the write cycle and must be stable during the entire cycle.

A read operation is executed by setting \overline{W} at a high level and \overline{OE} at a low level while $\overline{BC1}$ and/or $\overline{BC2}$ and $\overline{S1}$ and $S2$ are in an active state($\overline{S1}=L, S2=H$).

When setting $\overline{BC1}$ at the high level and other pins are in an active stage, upper-byte are in a selectable mode in which both reading and writing are enabled, and lower-byte are in a non-selectable mode. And when setting $\overline{BC2}$ at a high level and other pins are in an active stage, lower-

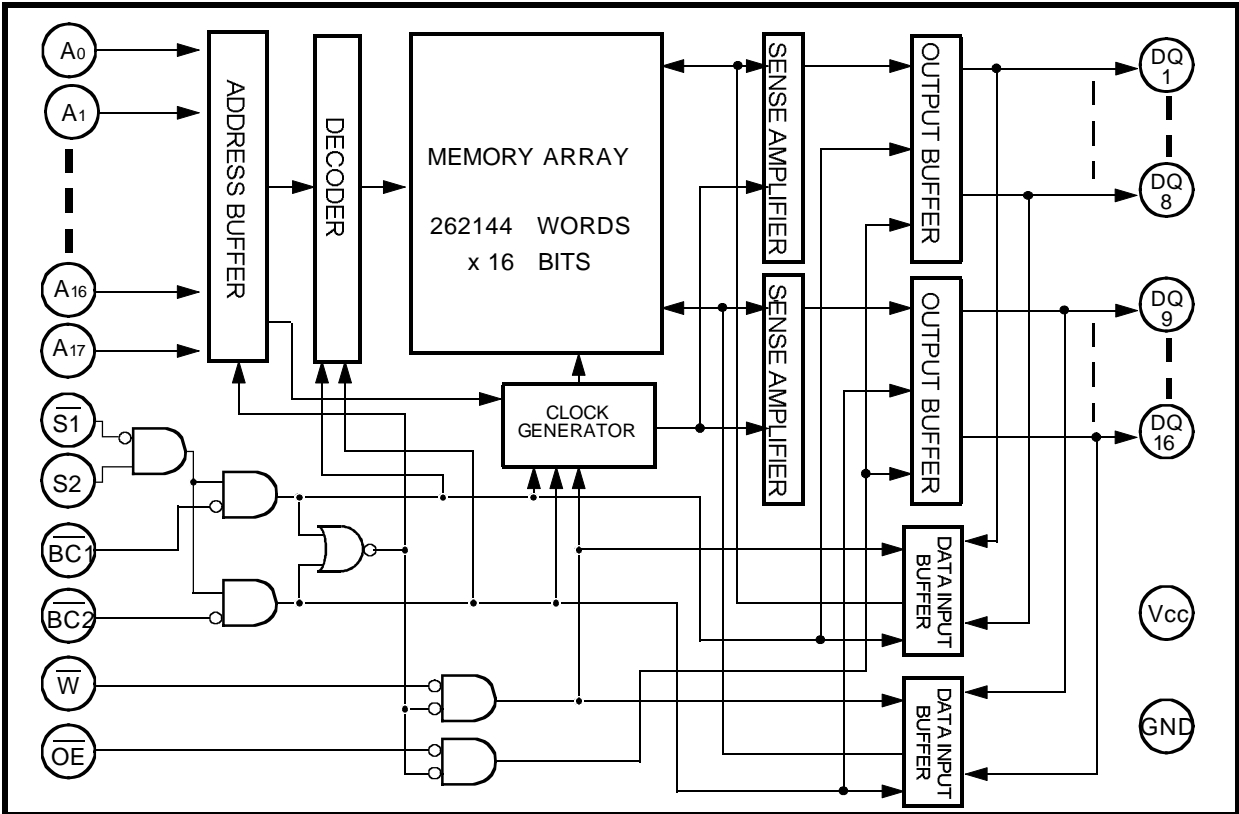
When setting $\overline{BC1}$ and $\overline{BC2}$ at a high level or $\overline{S1}$ at a high level or $S2$ at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{BC1}$, $\overline{BC2}$ and $\overline{S1}$, $S2$.

The power supply current is reduced as low as 0.1 μ A(25°C, typical), and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

| $\overline{S1}$ | $S2$ | $\overline{BC1}$ | $\overline{BC2}$ | \overline{W} | \overline{OE} | Mode | DQ1~8 | DQ9~16 | I _{cc} |
|-----------------|------|------------------|------------------|----------------|-----------------|---------------|--------|--------|-----------------|
| X | L | X | X | X | X | Non selection | High-Z | High-Z | Standby |
| H | H | X | X | X | X | Non selection | High-Z | High-Z | Standby |
| X | X | H | H | X | X | Non selection | High-Z | High-Z | Standby |
| L | H | L | H | L | X | Write | Din | High-Z | Active |
| L | H | L | H | H | L | Read | Dout | High-Z | Active |
| L | H | L | H | H | H | ———— | High-Z | High-Z | Active |
| L | H | H | L | L | X | Write | High-Z | Din | Active |
| L | H | H | L | H | L | Read | High-Z | Dout | Active |
| L | H | H | L | H | H | ———— | High-Z | High-Z | Active |
| L | L | L | L | X | X | Write | Din | Din | Active |
| L | L | L | L | L | L | Read | Dout | Dout | Active |
| L | L | L | L | H | H | ———— | High-Z | High-Z | Active |

BLOCK DIAGRAM



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4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Units |
|------------------|-----------------------|----------------------|-------------------------------|-------|
| V _{CC} | Supply voltage | With respect to GND | -0.5* ~ +4.6 | V |
| V _I | Input voltage | With respect to GND | -0.3* ~ V _{CC} + 0.3 | |
| V _O | Output voltage | With respect to GND | 0 ~ V _{CC} | |
| P _d | Power dissipation | T _a =25°C | 700 | mW |
| T _a | Operating temperature | I-version | - 40 ~ +85 | °C |
| T _{stg} | Storage temperature | | - 65 ~ +150 | °C |

* -3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=2.7 ~ 3.0V, unless noted.)

| Symbol | Parameter | Conditions | Limits | | | Units | |
|------------------|---------------------------------------|---|-----------|-----|-----------------------|-------|----|
| | | | Min | Typ | Max | | |
| V _{IH} | High-level input voltage | | 2.2 | | V _{CC} +0.2V | V | |
| V _{IL} | Low-level input voltage | | -0.2* | | 0.4 | | |
| V _{OH} | High-level output voltage | I _{OH} = -0.5mA | 2.4 | | | | |
| V _{OL} | Low-level output voltage | I _{OL} =2mA | | | 0.4 | | |
| I _I | Input leakage current | V _I =0 ~ V _{CC} | | | ±1 | μA | |
| I _O | Output leakage current | $\overline{BC1}$ and $\overline{BC2}$ =V _{IH} or $\overline{S1}$ =V _{IH} or $\overline{S2}$ =V _{IL} or \overline{OE} =V _{IH} , V _{I/O} =0 ~ V _{CC} | | | ±1 | μA | |
| I _{CC1} | Active supply current (AC, MOS level) | $\overline{BC1}$ and $\overline{BC2}$ ≤ 0.2V, $\overline{S1}$ ≤ 0.2V, $\overline{S2}$ ≥ V _{CC} -0.2V other inputs ≤ 0.2V or ≥ V _{CC} -0.2V Output - open (duty 100%) | f = 10MHz | - | 30 | 40 | mA |
| | | | f = 1MHz | - | 5 | 10 | |
| I _{CC2} | Active supply current (AC, TTL level) | $\overline{BC1}$ and $\overline{BC2}$ =V _{IL} , $\overline{S1}$ =V _{IL} , $\overline{S2}$ =V _{IH} other pins =V _{IH} or V _{IL} Output - open (duty 100%) | f = 10MHz | - | 30 | 40 | mA |
| | | | f = 1MHz | - | 5 | 10 | |
| I _{CC3} | Stand by supply current (MOS level) | (1) $\overline{S1}$ ≥ V _{CC} - 0.2V, $\overline{S2}$ ≥ V _{CC} - 0.2V, other inputs = 0 ~ V _{CC} (2) $\overline{S2}$ ≤ 0.2V, other inputs = 0 ~ V _{CC} (3) $\overline{BC1}$ and $\overline{BC2}$ ≥ V _{CC} - 0.2V $\overline{S1}$ ≤ 0.2V, $\overline{S2}$ ≥ V _{CC} - 0.2V other inputs = 0 ~ V _{CC} | ~ +25°C | - | 0.1 | 1 | μA |
| | | | ~ +40°C | - | 0.2 | 2 | |
| | | | ~ +85°C | - | - | 20 | |
| I _{CC4} | Stand by supply current (TTL level) | $\overline{BC1}$ and $\overline{BC2}$ =V _{IH} or $\overline{S1}$ =V _{IH} or $\overline{S2}$ =V _{IL} Other inputs=0 ~ V _{CC} | - | - | 0.5 | mA | |

Note 1: Direction for current flowing into IC is indicated as positive (no mark)

* -1.0V in case of AC (Pulse width ≤ 30ns)

Note 2: Typical parameter indicates the value for the center of distribution at 2.85V, and is not 100% tested.

CAPACITANCE

(V_{CC}=2.7 ~ 3.0V, unless noted.)

| Symbol | Parameter | Conditions | Limits | | | Units |
|----------------|--------------------|--|--------|-----|-----|-------|
| | | | Min | Typ | Max | |
| C _I | Input capacitance | V _I =GND, V _I =25mVrms, f=1MHz | | | 10 | pF |
| C _O | Output capacitance | V _O =GND, V _O =25mVrms, f=1MHz | | | 10 | |

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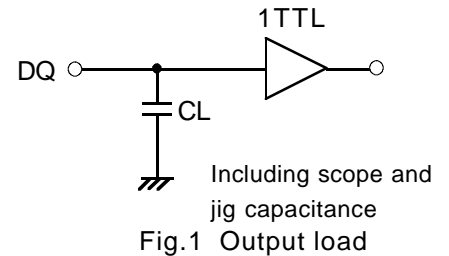
4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

AC ELECTRICAL CHARACTERISTICS

(V_{CC}=2.7 ~ 3.0V, unless noted.)

(1) TEST CONDITIONS

| | |
|-------------------------------|---|
| Supply voltage | 2.7~3.0V |
| Input pulse | V _{IH} =2.4V, V _{IL} =0.2V |
| Input rise time and fall time | 5ns |
| Reference level | V _{OH} =V _{OL} =1.5V <small>Transition is measured ±200mV from steady state voltage.(for t_{en},t_{dis})</small> |
| Output loads | Fig.1,CL=30pF CL=5pF (for t _{en} ,t _{dis}) |



(2) READ CYCLE

| Symbol | Parameter | Limits | | Units |
|-----------------------|---|--------|-----|-------|
| | | 70HI | | |
| | | Min | Max | |
| t _{CR} | Read cycle time | 70 | | ns |
| t _{a(A)} | Address access time | | 70 | ns |
| t _{a(S1)} | Chip select 1 access time | | 70 | ns |
| t _{a(S2)} | Chip select 2 access time | | 70 | ns |
| t _{a(BC1)} | Byte control 1 access time | | 70 | ns |
| t _{a(BC2)} | Byte control 2 access time | | 70 | ns |
| t _{a(OE)} | Output enable access time | | 35 | ns |
| t _{dis(S1)} | Output disable time after $\overline{S1}$ high | | 25 | ns |
| t _{dis(S2)} | Output disable time after $\overline{S2}$ low | | 25 | ns |
| t _{dis(BC1)} | Output disable time after $\overline{BC1}$ high | | 25 | ns |
| t _{dis(BC2)} | Output disable time after $\overline{BC2}$ high | | 25 | ns |
| t _{dis(OE)} | Output disable time after \overline{OE} high | | 25 | ns |
| t _{en(S1)} | Output enable time after $\overline{S1}$ low | 10 | | ns |
| t _{en(S2)} | Output enable time after $\overline{S2}$ high | 10 | | ns |
| t _{en(BC1)} | Output enable time after $\overline{BC1}$ low | 5 | | ns |
| t _{en(BC2)} | Output enable time after $\overline{BC2}$ low | 5 | | ns |
| t _{en(OE)} | Output enable time after \overline{OE} low | 5 | | ns |
| t _{v(A)} | Data valid time after address | 10 | | ns |

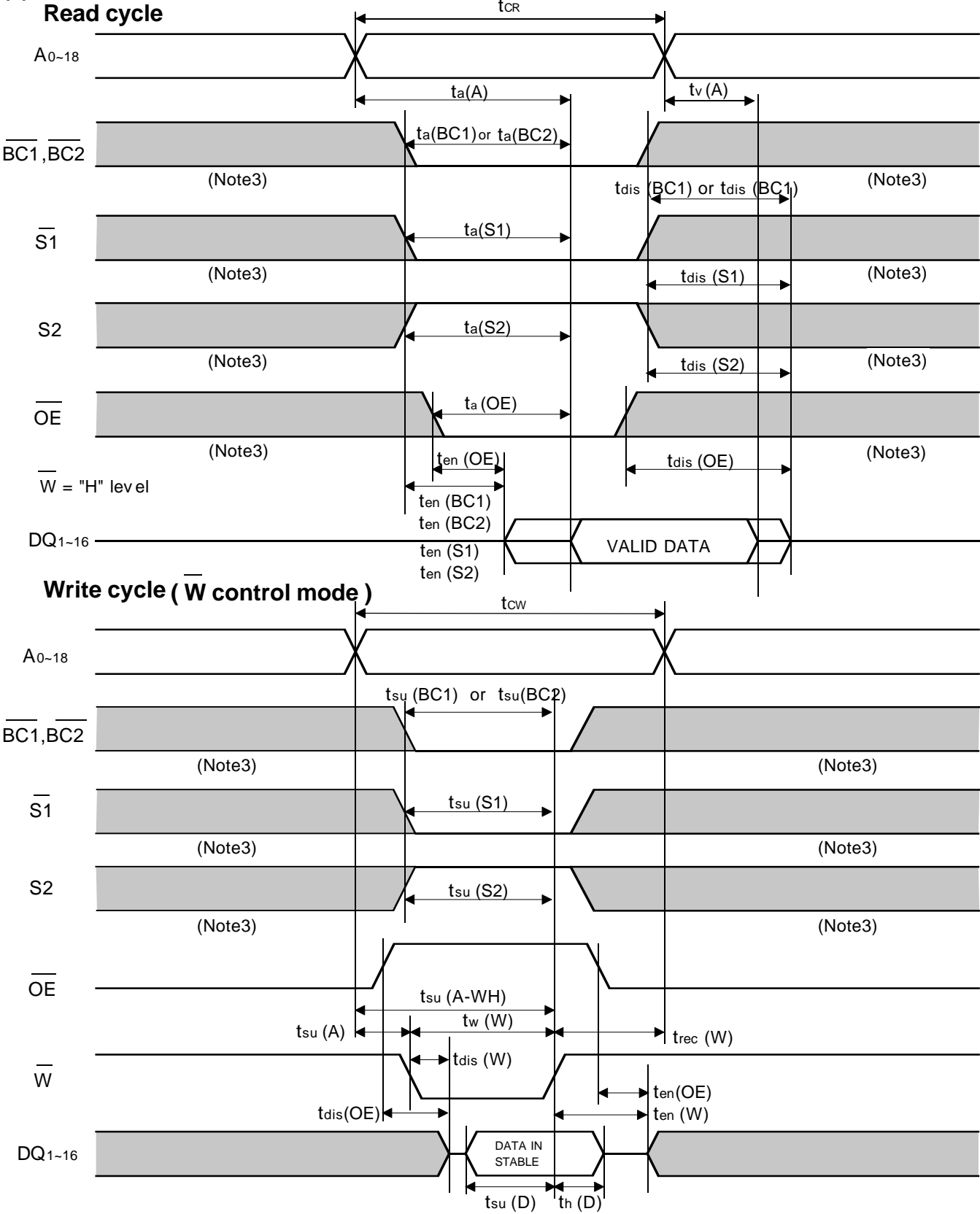
(3) WRITE CYCLE

| Symbol | Parameter | Limits | | Units |
|-----------------------|---|--------|-----|-------|
| | | 70HI | | |
| | | Min | Max | |
| t _{cw} | Write cycle time | 70 | | ns |
| t _{w(W)} | Write pulse width | 55 | | ns |
| t _{su(A)} | Address setup time | 0 | | ns |
| t _{su(A-WH)} | Address setup time with respect to \overline{W} | 60 | | ns |
| t _{su(BC1)} | Byte control 1 setup time | 60 | | ns |
| t _{su(BC2)} | Byte control 2 setup time | 60 | | ns |
| t _{su(S1)} | Chip select 1 setup time | 60 | | ns |
| t _{su(S2)} | Chip select 2 setup time | 60 | | ns |
| t _{su(D)} | Data setup time | 35 | | ns |
| t _{h(D)} | Data hold time | 0 | | ns |
| t _{rec(W)} | Write recovery time | 0 | | ns |
| t _{dis(W)} | Output disable time from \overline{W} low | | 25 | ns |
| t _{dis(OE)} | Output disable time from \overline{OE} high | | 25 | ns |
| t _{en(W)} | Output enable time from \overline{W} high | 5 | | ns |
| t _{en(OE)} | Output enable time from \overline{OE} low | 5 | | ns |

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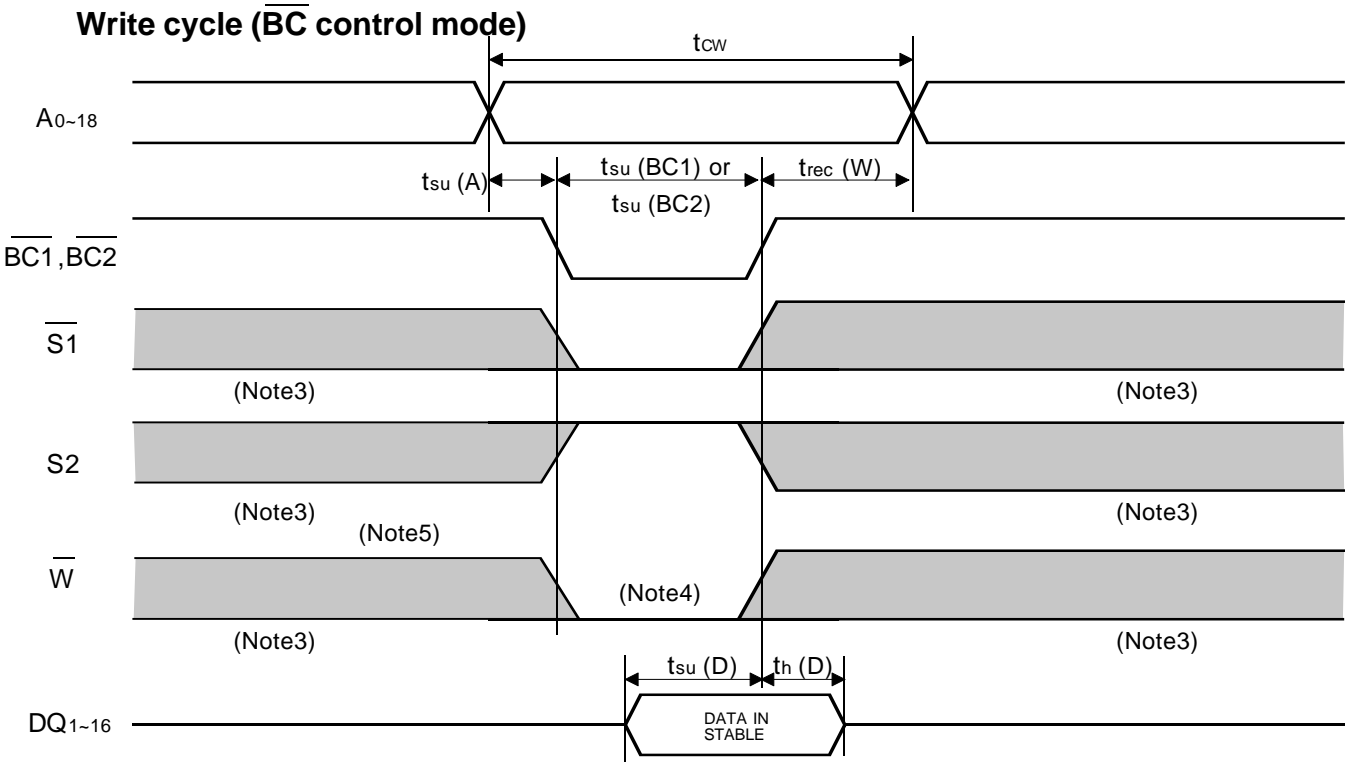
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(4)TIMING DIAGRAMS



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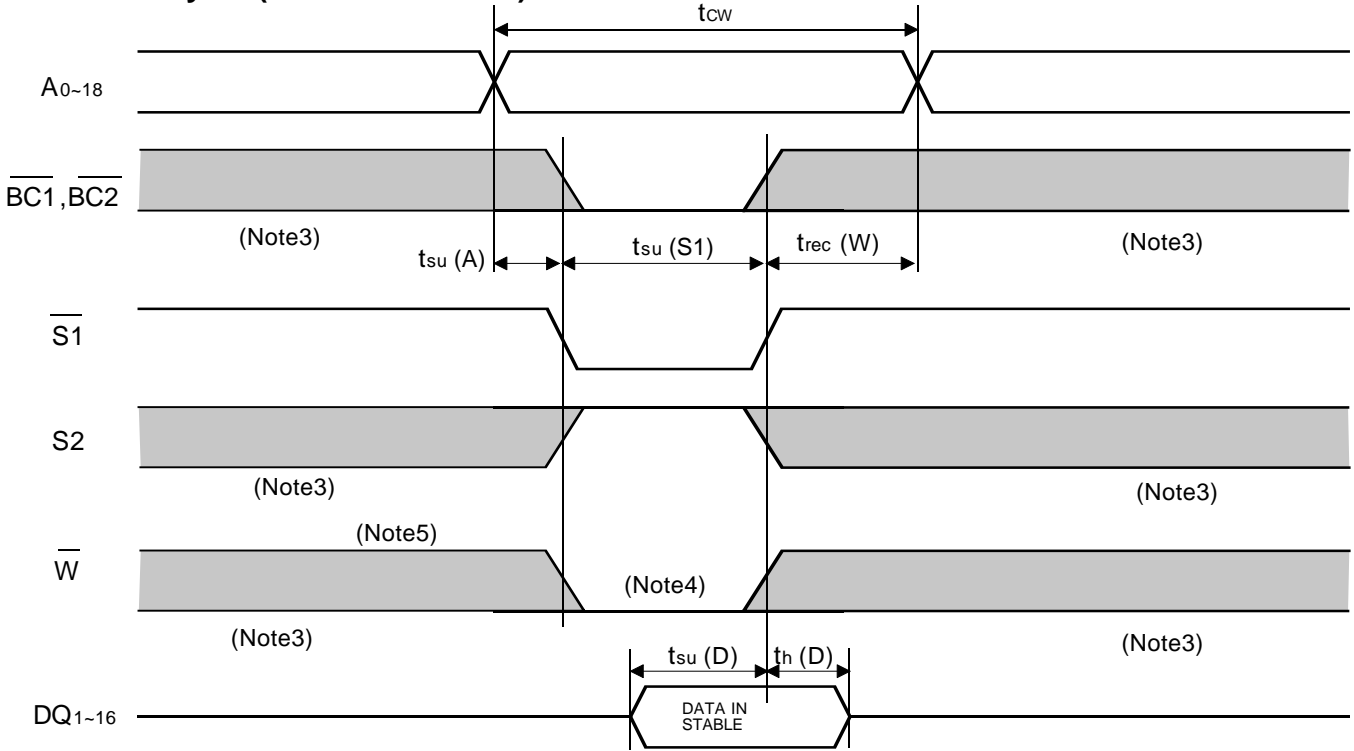


- Note 3: Hatching indicates the state is "don't care".
- Note 4: A Write occurs during S1 low, S2 high overlaps BC1 and/or BC2 low and W low.
- Note 5: When the falling edge of W is simultaneously or prior to the falling edge of BC1 and/or BC2 or the falling edge of S1 or rising edge of S2, the outputs are maintained in the high impedance state.
- Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.

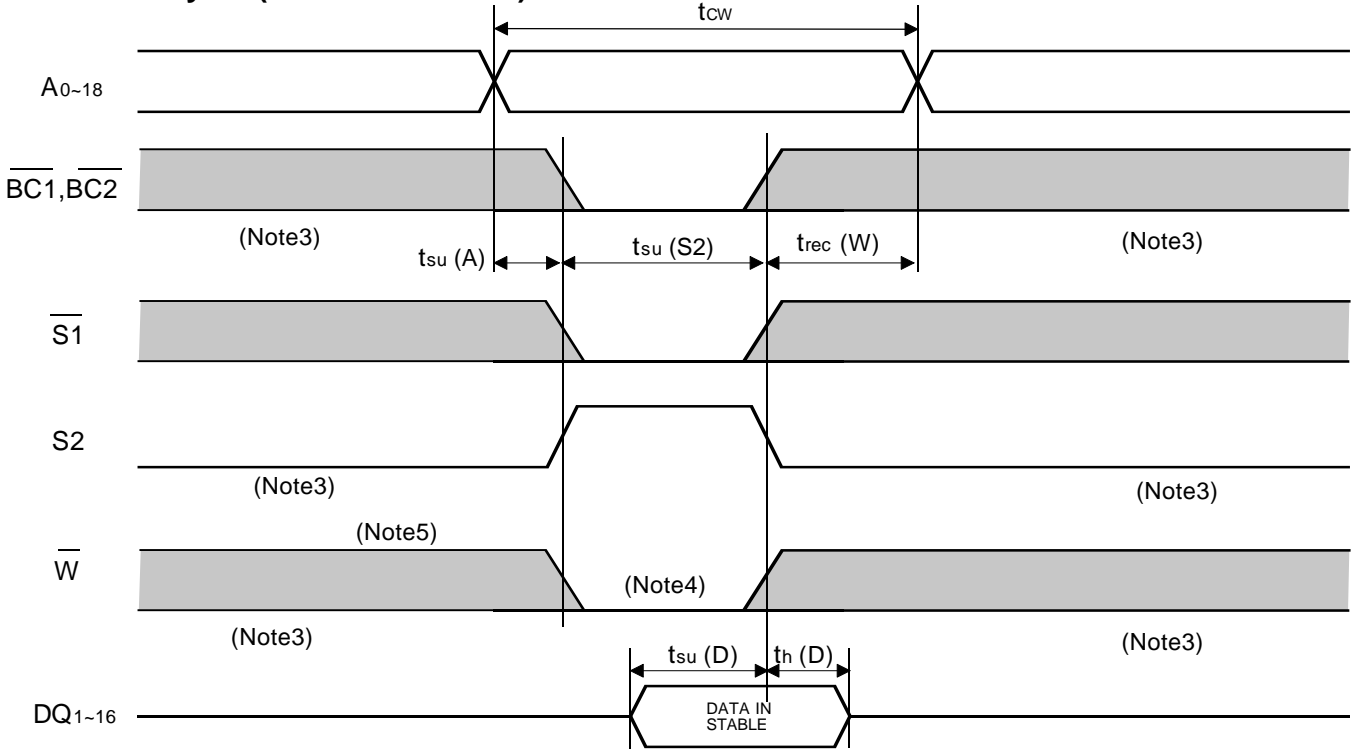
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Write cycle ($\overline{S1}$ control mode)



Write cycle ($\overline{S2}$ control mode)



M5M5V416CWG -70HI

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test conditions | Limits | | | Units | |
|------------------------------------|--|--|---------|-----|-----|-------|----|
| | | | Min | Typ | Max | | |
| V _{CC} (PD) | Power down supply voltage | | 2.0 | | | V | |
| V _I (BC) | Byte control input $\overline{BC}1$ & $\overline{BC}2$ | $2.7V \leq V_{CC}(PD)$ $2.0V \leq V_{CC}(PD) \leq 2.7V$ | 2.2 | | | V | |
| V _I ($\overline{S}1$) | Chip select input $\overline{S}1$ | $2.7V \leq V_{CC}(PD)$ $2.0V \leq V_{CC}(PD) \leq 2.7V$ | 2.2 | | | V | |
| V _I (S2) | Chip select input S2 | | | | 0.2 | V | |
| I _{CC} (PD) | Power down supply current | V _{CC} =2.0V (1) $\overline{S}1 \geq V_{CC} - 0.2V$, other inputs = 0 - V _{CC} (2) $S2 \leq 0.2V$, other inputs = 0 - V _{CC} (3) $\overline{BC}1$ and $\overline{BC}2 \geq V_{CC} - 0.2V$, $\overline{S}1 \leq 0.2V$, $S2 \geq V_{CC} - 0.2V$, other inputs = 0 - V _{CC} | ~ +25°C | - | 0.1 | 0.8 | μA |
| | | | ~ +40°C | - | 0.2 | 1.5 | |
| | | | ~ +85°C | - | - | 15 | |

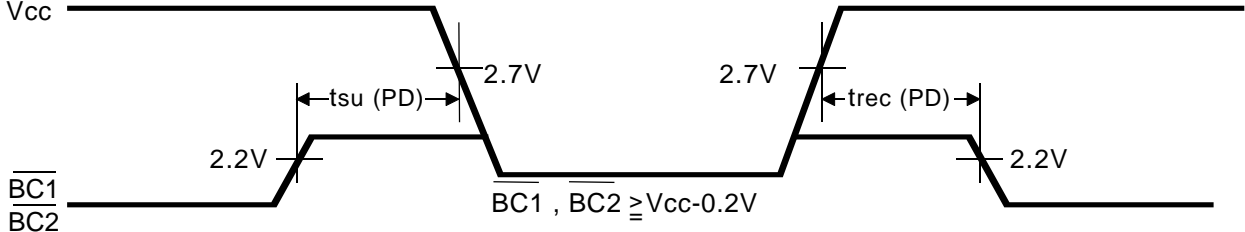
Note 2: Typical parameter of I_{CC}(PD) indicates the value for the center of distribution at 2.0V, and not 100% tested.

(2) TIMING REQUIREMENTS

| Symbol | Parameter | Test conditions | Limits | | | Units |
|-----------------------|--------------------------|-----------------|--------|-----|-----|-------|
| | | | Min | Typ | Max | |
| t _{SU} (PD) | Power down set up time | | 0 | | | ns |
| t _{REC} (PD) | Power down recovery time | | 5 | | | ms |

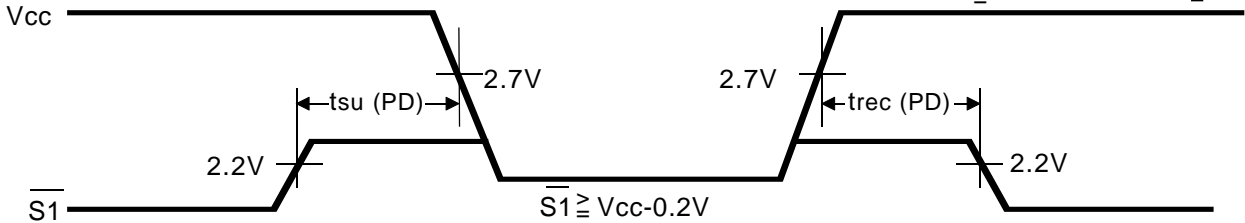
(3) TIMING DIAGRAM

BC control mode

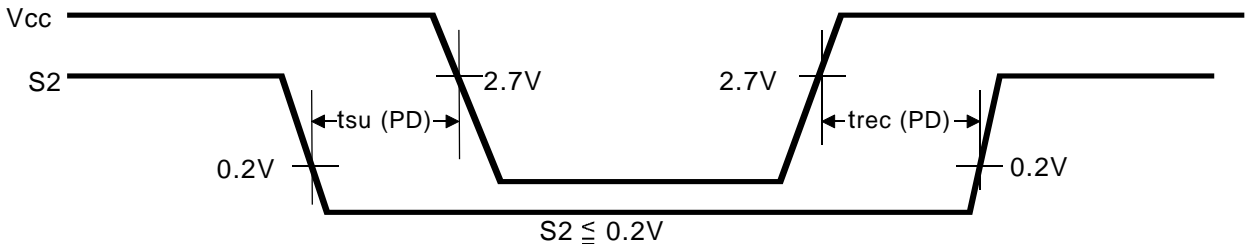


$\overline{S}1$ control mode

note7 : On the S1 mode, the level of $\overline{S}2$ must be fixed at $S2 \geq V_{CC} - 0.2V$ or $S2 \leq 0.2V$.



S2 control mode



Keep safety first in your circuit designs!

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