M5M4V4405CJ,TP-6,-7,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 4-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.

The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

Self or extended refresh current is low enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V4405CXX-6, -6S	60	15	30	15	110	264
M5M4V4405CXX-7, -7S	70	20	35	20	130	231

XX=J, TP

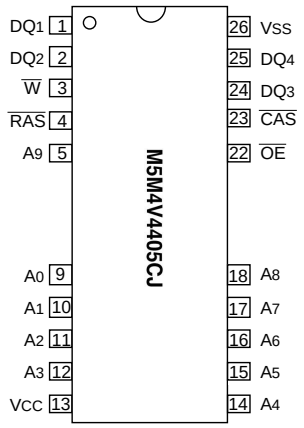
- Standard 26 pin SOJ, 26 pin TSOP(II)
- Single 3.3V±0.3V supply
- Low stand-by power dissipation
  - CMOS Input level .....1.8mW(Max)*
  - CMOS Input level .....180µW(Max)
- Low operating power dissipation
  - M5M4V4405Cxx-6, -6S .....288.0mW (Max)
  - M5M4V4405Cxx-7, -7S .....252.0mW (Max)
- Self refresh capabiility*
  - Self refresh current .....100µA(max)
- Extended refresh capability*
  - Extended refresh current .....100µA(max)
- Hyper-page mode (1024-bit random access), Read-modify- write, $\overline{RAS}$-only refresh $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, CBR self refresh(-6S,-7S) capabilities.
- Early-write mode and $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- 1024 refresh cycles every 16.4ms (A_0~A_9)
- 1024refresh cycle every128ms (A_0~A_9)*

*: Applicable to self refresh version (M5M4V4405Cxx-6S,-7S: option) only

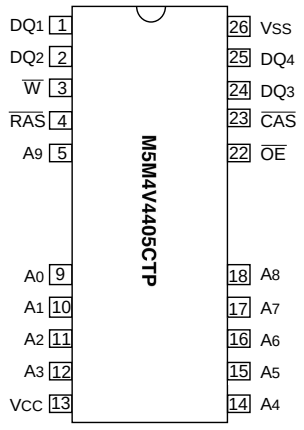
APPLICATION

Lap top personal computer,Solid state disc, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Outline 26P0J (300mil SOJ)



Outline 26P3Z-E (300mil TSOP)

PIN DESCRIPTION

Pin name	Function
A_0~A_9	Address inputs
DQ_1~DQ_4	Data inputs / outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
V_{CC}	Power supply (+3.3V)
V_{SS}	Ground (0V)

EDO (HYPER PAGE MODE) 4194304-BIT(1048576-WORD BY 4-BIT) DYNAMIC RAM

FUNCTION

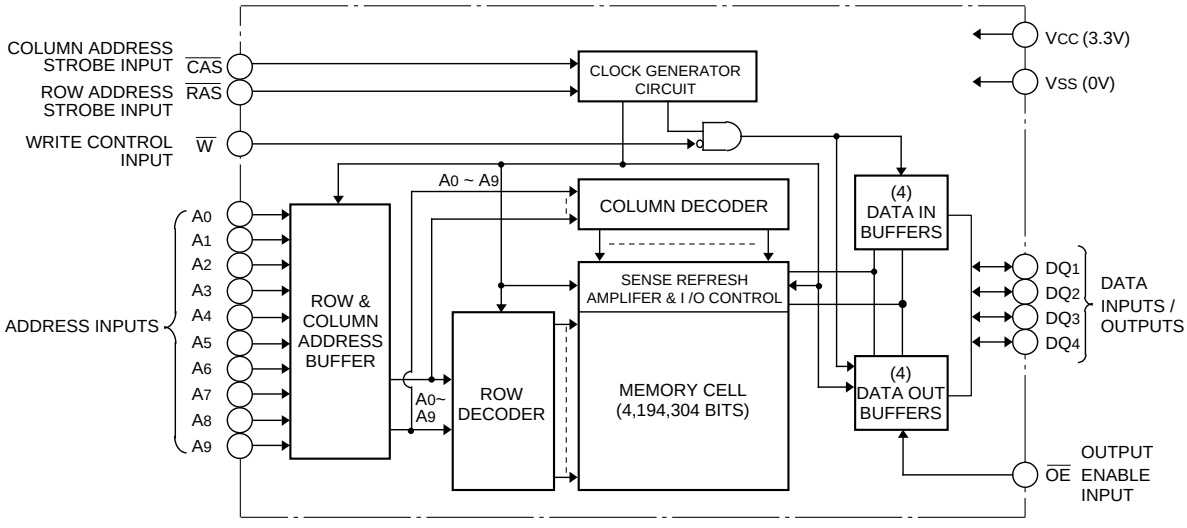
In addition to normal read, write, and read-modify-write operations the M5M4V4405CJ,TP provide, a number of other functions, e.g., Hyper Page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Hyper Page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	APD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	NAC	APD	AP	APD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Self refresh*	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	-0.5 ~ 4.6	V
V_I	Input voltage		-0.5 ~ 4.6	V
V_O	Output voltage		-0.5 ~ 4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter		Limits			Unit
			Min	Nom	Max	
V_{CC}	Supply voltage		3.0	3.3	3.6	V
V_{SS}	Supply voltage		0	0	0	V
V_{IH}	High-level input voltage, all inputs		2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage	DQ_1~DQ_4	-0.3		0.8	V
		others	-0.3		0.8	V

Note 1 : All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=3.3V± 0.3V, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≤V_{OUT}≤V_{CC}	-5		5	µA
I_I	Input current		0V≤V_{IN}≤V_{CC}+0.3V, Other inputs pins=0V	-5		5	µA
I_{CC1} (AV)	Average supply current from V_{CC} operating (Note 3,4,5)	**M5M4V4405C-6,-6S**	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			80	mA
		M5M4V4405C-7,-7S				70	
I_{CC2} (AV)	Supply current from V_{CC}, stand-by (Note 6)		$\overline{RAS}$=$\overline{CAS}$ =V_{IH}, output open			2	mA
		M5M4V4405C	$\overline{RAS}$=$\overline{CAS}$≥V_{CC} -0.2V output open			0.5	
		M5M4V4405C(S)				0.05 *	
I_{CC3} (AV)	Average supply current from V_{CC} refreshing (Note 3,5)	**M5M4V4405C-6,-6S**	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			80	mA
		M5M4V4405C-7,-7S				70	
I_{CC4}(AV)	Average supply current from V_{CC} Hyper-Page-Mode (Note 3,4,5)	**M5M4V4405C-6,-6S**	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			80	mA
		M5M4V4405C-7,-7S				70	
I_{CC6}(AV)	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	**M5M4V4405C-6,-6S**	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			70	mA
		M5M4V4405C-7,-7S				60	
I_{CC8}(AV)*	Average supply current from V_{CC} Extended-Refresh cycle (Note 6)		$\overline{RAS}$ cycling $\overline{CAS}$≤0.2V or CAS before RAS refresh cycling $\overline{RAS}$≤0.2V or ≥V_{CC}-0.2V $\overline{CAS}$≤0.2V or ≥V_{CC}-0.2V $\overline{W}$≤0.2V (Except for $\overline{RAS}$ falling edge) or ≥V_{CC}-0.2V $\overline{OE}$≤0.2V or ≥V_{CC}-0.2V A_0~A_9 ≤0.2V or≥V_{CC}-0.2V DQ=open t_{RC}=125µs, t_{RAS}=t_{RAS} min ~1µs			100	µA
I_{CC9}(AV)*	Average supply current from V_{CC} Self-Refresh cycle (Note 6)	**M5M4V4405C(S)**	$\overline{RAS}$=$\overline{CAS}$≤0.2V output open			100	µA

Note 2: Current flowing into an IC is positive, out is negative.
3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Addres can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}.

CAPACITANCE (Ta=0~70˚C, V_{CC}=3.3V±0.3V, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I\ (A)}$	Input capacitance, address inputs	V_I=V_{SS}			5	pF
$C_{I\ (CLK)}$	Input capacitance, clock inputs	f=1MHz			7	pF
$C_{I\ /\ O}$	Input/Output capacitance, data ports	V_I=25mVrms			7	pF

SWITCHING CHARACTERISTICS (Ta=0~70˚C, V_{CC}=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits				Unit
			M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		60		70	ns
t_{AA}	Column address access time	(Note 7,10)		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		33		38	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		15		20	ns
t_{OHC}	Output hold time from $\overline{CAS}$		5		5		ns
t_{OHR}	Output hold time from $\overline{RAS}$	(Note 13)	5		5		ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)		15		20	ns
t_{WEZ}	Output disable time after $\overline{WE}$ low	(Note 12)		15		20	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12,13)		15		20	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high	(Note 12,13)		15		20	ns

Note 6: An initial pause of 200µs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh cycles)D@@@@@@@@@@@@@ @
Note the $\overline{RAS}$ may be cycled during the initial pause. And eight initialization cycles are required after prolonged periods (greater than $t_{REF(max)}$) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to 100pF, V_{OH}=2.4V(I_{OH}=-2mA) and V_{OL}=0.4V(I_{OL}=2mA).
The reference levels for measuring of output signals are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$ and $t_{CP} \geq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12: $t_{OEZ\ (max)}$, $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$ defines the time at which the output achieves the high impedance state($I_{OUT} \leq$ | ±10µA |) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Hyper-Page Mode Cycles)

(Ta=0~70°C, V_{CC} = 3.3V±0.3V, V_{SS} =0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
t_{REF}	Refresh cycle time		16.4		16.4	ms
t_{REF}	Refresh cycle time*		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width	40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note 16)	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	10		13		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note 17)	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note 18)	0	13	0	13	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	10		10		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low (Note 19)	0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low (Note 19)	0		0		ns
t_{RDD}	Delay time, $\overline{RAS}$ high to data (Note 20)	15		20		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data (Note 20)	15		20		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data (Note 20)	15		20		ns
t_T	Transition time (Note 21)	1	50	1	50	ns

Note 14: The timing requirements are assumed t_T =2ns.

@ 15: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

@ 16: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}.

@ 17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.

@ 18: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

@ 19: Either t_{DZC} or t_{DZO} must be satisfied.

@ 20: Either t_{RDD} or t_{CDD} or t_{ODD} must be satisfied.

@ 21: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
t_{RC}	Read cycle time	110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	10	10000	13	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	48		55		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low	0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 22)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 22)	0		0		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	30		35		ns
t_{CAL}	Column address to $\overline{CAS}$ hold time	18		23		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	15		20		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	15		20		ns

Note 22: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
t_{WC}	Write cycle time	110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	10	10000	13	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	48		55		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	10		13		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 24)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	10		13		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	10		13		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	10		13		ns
t_{WP}	Write pulse width	10		13		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note 23)	133		161		ns
t_{RAS}	$\overline{RAS}$ low pulse width	89	10000	107	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	44	10000	57	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	89		107		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	44		57		ns
t_{RCS}	Read setup time before0 $\overline{CAS}$ low	0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 24)	32		42		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 24)	77		92		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note 24)	47		57		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	15		20		ns

Note 23: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

@ 24: t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD}, and t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Hyper page Mode Cycle
(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter		Limits				Unit
			M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
			Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time	(Note 26)	25		30		ns
t_{HPRWC}	Hyper Page Mode read write / read modify write cycle time		66		79		ns
t_{DOH}	Output hold time from $\overline{CAS}$ low		5		5		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read or write cycle	(Note 27)	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note 28)	10	16	13	16	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		33		38		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to W low	(Note 24)	50		60		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access		7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse Width (Hi-Z control)		7		7		ns
t_{WPE}	$\overline{W}$ Pulse Width (Hi-Z control)		7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read		32		42		ns
t_{HAWD}	Delay time, Address to $\overline{W}$ low after read		47		57		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read		50		60		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read		15		20		ns
t_{HAOD}	Delay time, Address to $\overline{OE}$ high after read		30		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read		33		38		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26: $t_{HPC(min)}$ is specified in the case of read-only and early write-only in Hyper page Mode.
27: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
28: $t_{CP(max))}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 29)

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHP}	Read hold time after $\overline{RAS}$ low	10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	17		22		ns

Note 29: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle* (Note 30)

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
t_{RASS}	CBR self refresh $\overline{RAS}$ low pulse width	100		100		µs
t_{RPS}	CBR self refresh $\overline{RAS}$ high precharge time	110		130		ns
t_{CHS}	CBR self refresh $\overline{CAS}$ hold time	-50		-50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		ns

Test Mode Specification (Note 31)

ELECTRICAL CHARACTERISTICS (T_a=0~70˚C, V_{CC}=3.3V±0.3V, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC1} (AV)	Average supply current from V_{CC} operating (Note 3,4,5)	M5M4V4405C-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			85	mA
		M5M4V4405C-7,-7S				75	
I_{CC3} (AV)	Average supply current from V_{CC} refreshing (Note 3,5)	M5M4V4405C-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			85	mA
		M5M4V4405C-7,-7S				75	
I_{CC4}(AV)	Average supply current from V_{CC} Hyper-Page-Mode (Note 3,4,5)	M5M4V4405C-6,-6S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			85	mA
		M5M4V4405C-7,-7S				75	
I_{CC6}(AV)	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V4405C-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			75	mA
		M5M4V4405C-7,-7S				65	

Note 31: All previously specified electrical characteristics, switing characteristics, and timing requirements are applicable to that of test mode.

SWITCHING CHARACTERISTICS (T_a=0~70˚C, V_{CC}=3.3V±0.3V, V_{SS}=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits				Unit
			M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
			Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		20		25	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		65		75	ns
t_{AA}	Column address access time	(Note 7,10)		35		40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		38		43	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		20		25	ns

TIMING REQUIREMENTS (T_a=0~70˚C, V_{CC}=3.3V±0.3V, V_{SS}=0V, unless otherwise noted, see notes 14,15)

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
t_{RC}	Read cycle time	115		135		ns
t_{RAS}	$\overline{RAS}$ low pulse width	65	10000	75	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	15	10000	18	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	53		60		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	20		25		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	35		40		ns
t_{CAL}	Column address to $\overline{CAS}$ hold time	23		28		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	20		25		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	20		25		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
			Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note 23)	138		166		ns
t_{RAS}	$\overline{RAS}$ low pulse width		94	10000	112	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		49	10000	62	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		94		112		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		49		62		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 24)	37		47		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 24)	82		97		ns
t_{AWD}	Delay time, address to $\overline{W}$ low	(Note 24)	52		62		ns

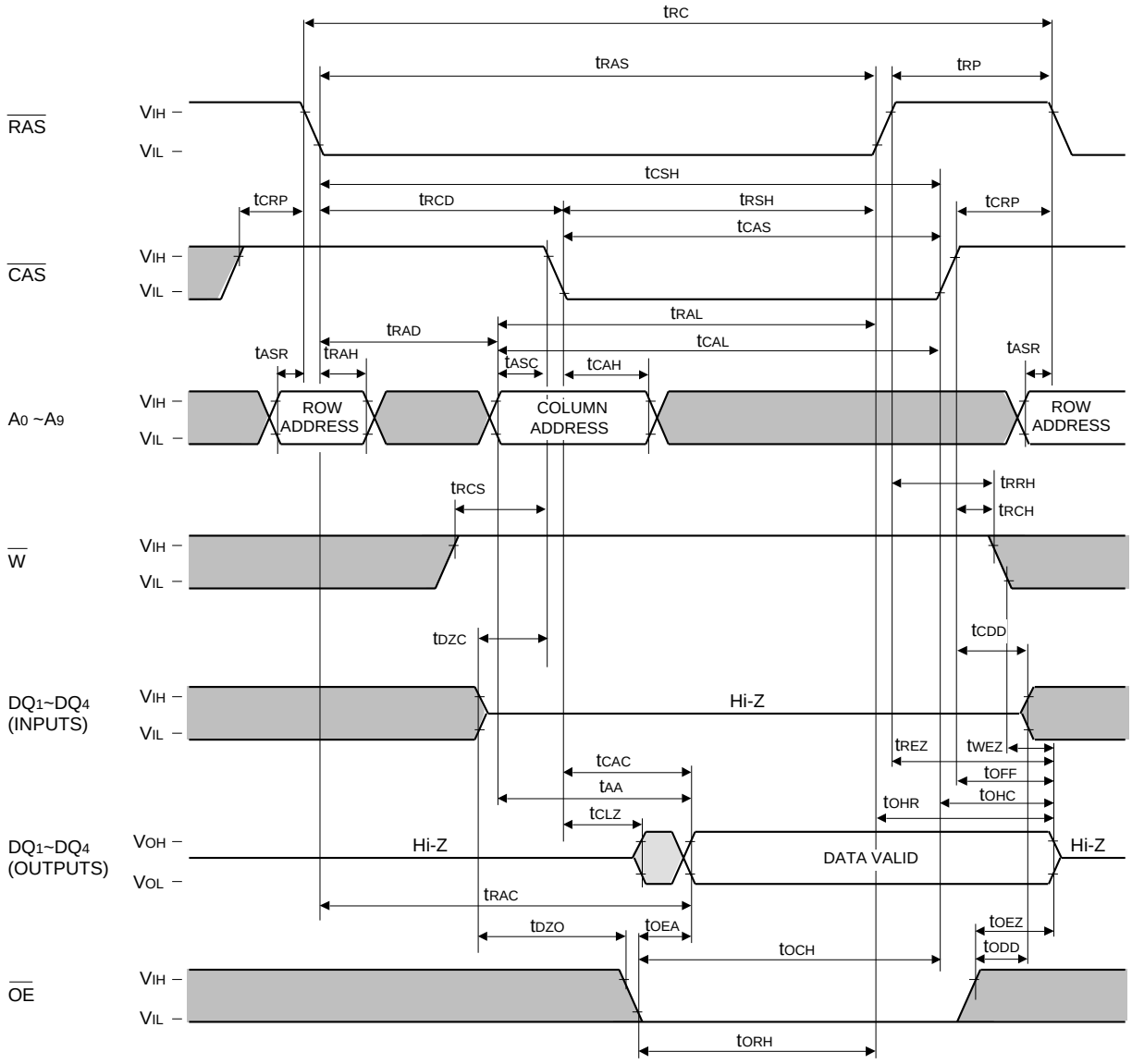
Hyper page Mode Cycle
(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time (Note 26)	30		35		ns
t_{HPRWC}	Hyper Page Mode read write / read modify write cycle time	71		84		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read or write cycle (Note 27)	82	100000	97	100000	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	38		43		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 24)	55		65		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	37		47		ns
t_{HAWD}	Delay time, Address to $\overline{W}$ low after read	52		62		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	55		65		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	20		25		ns
t_{HAOD}	Delay time, Address to $\overline{OE}$ high after read	35		40		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	38		43		ns

Test Mode Set Cycle

Symbol	Parameter	Limits				Unit
		M5M4V4405C-6,-6S		M5M4V4405C-7,-7S		
		Min	Max	Min	Max	
t_{WSR}	Write setup time before $\overline{RAS}$ low	10		10		ns
t_{WHR}	Write hold time after $\overline{RAS}$ low	10		15		ns

Timing Diagrams (Note 32)
Read Cycle

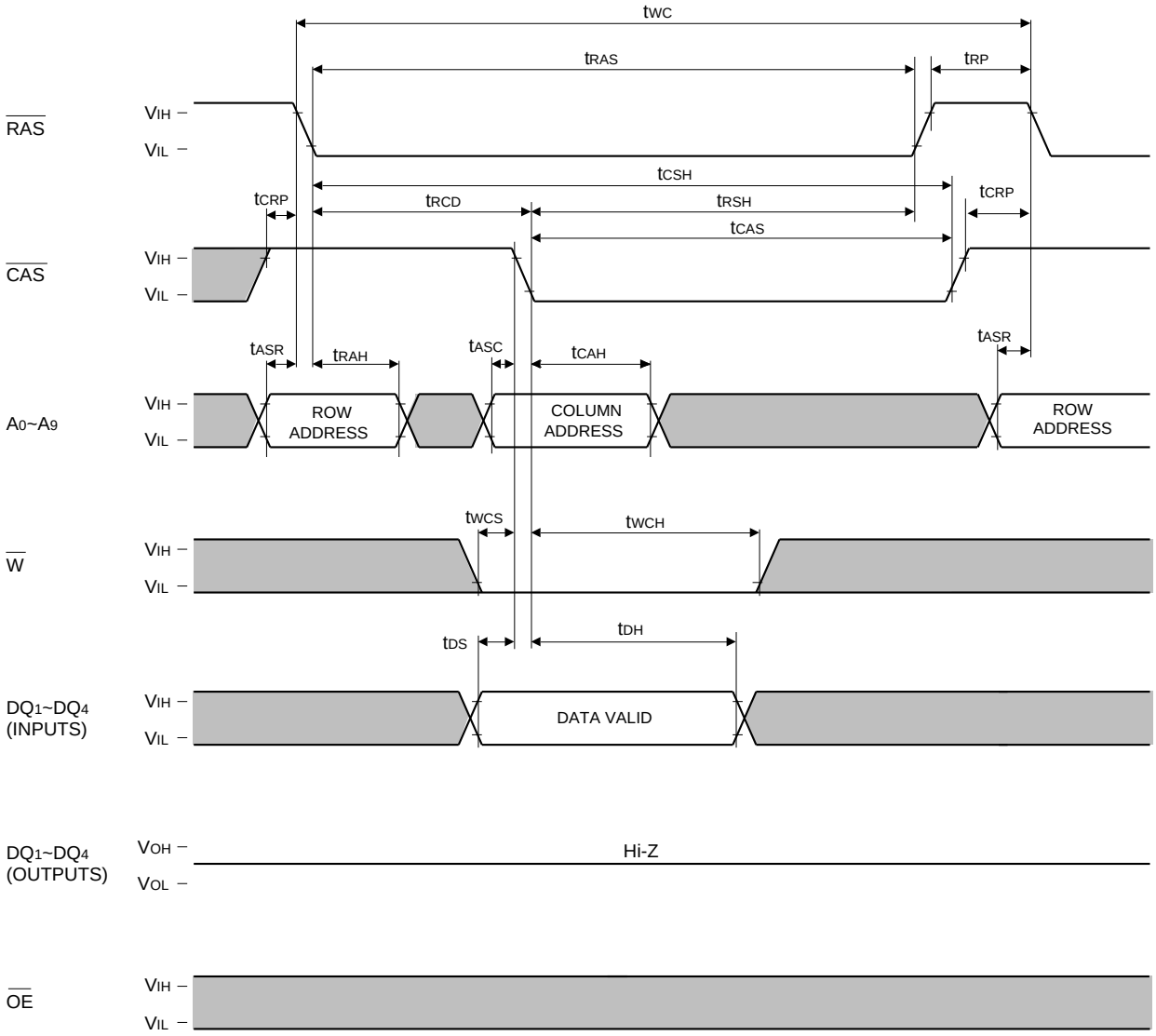


Note 32

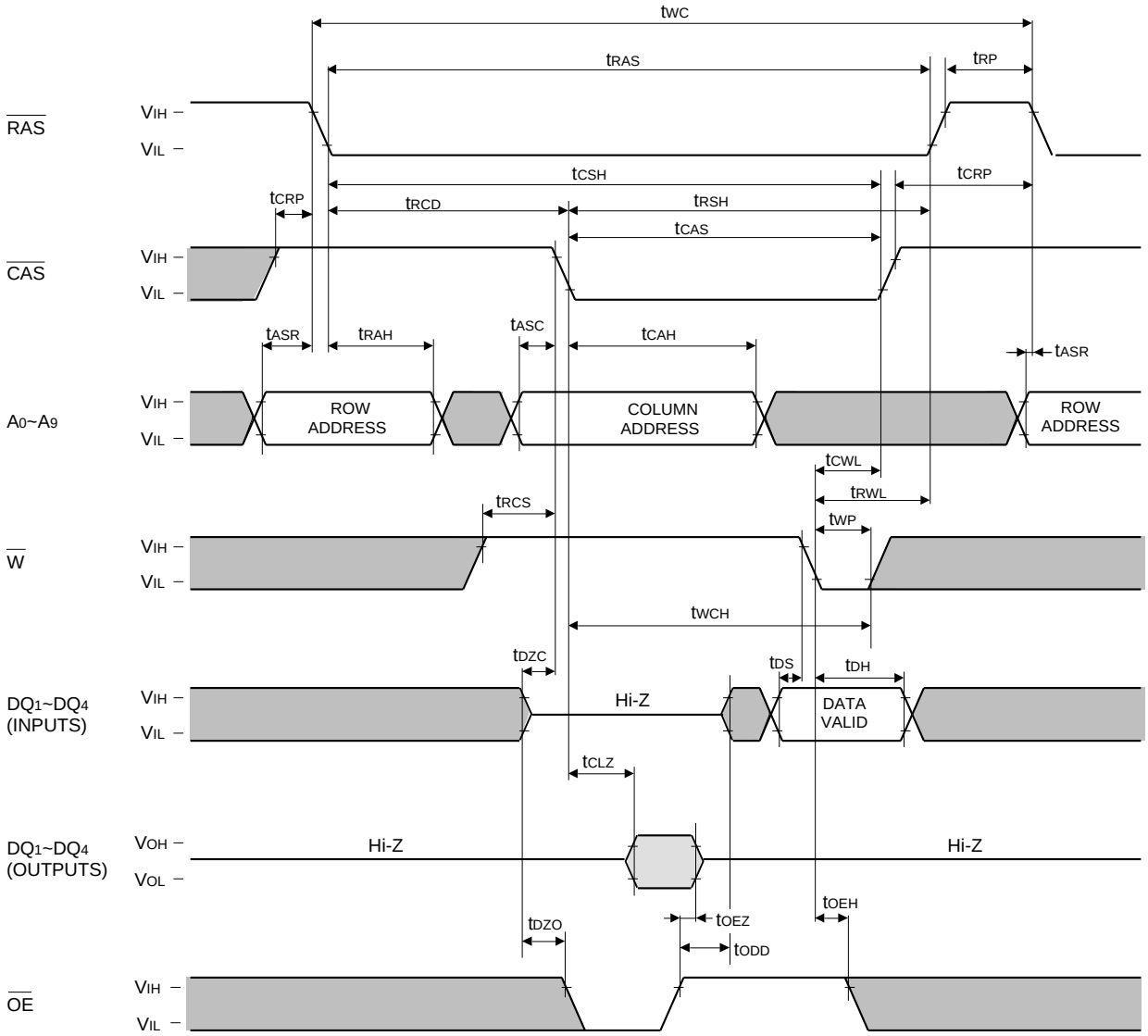
Indicates the don't care input.
VIH(min)≤VIN≤VIH(max) or VIL(min)≤VIN≤VIL(max)

Indicates the invalid output.

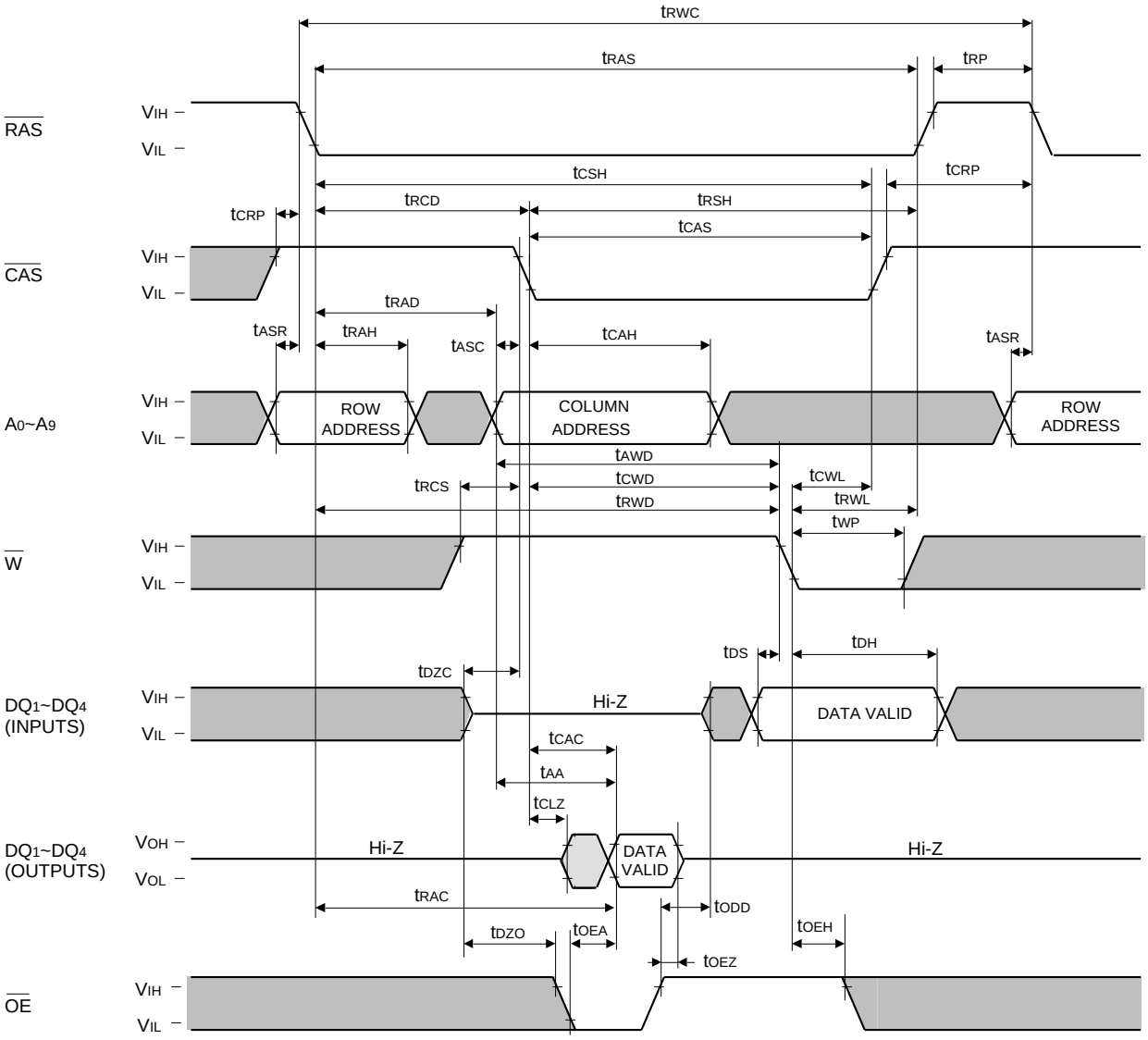
Early Write Cycle



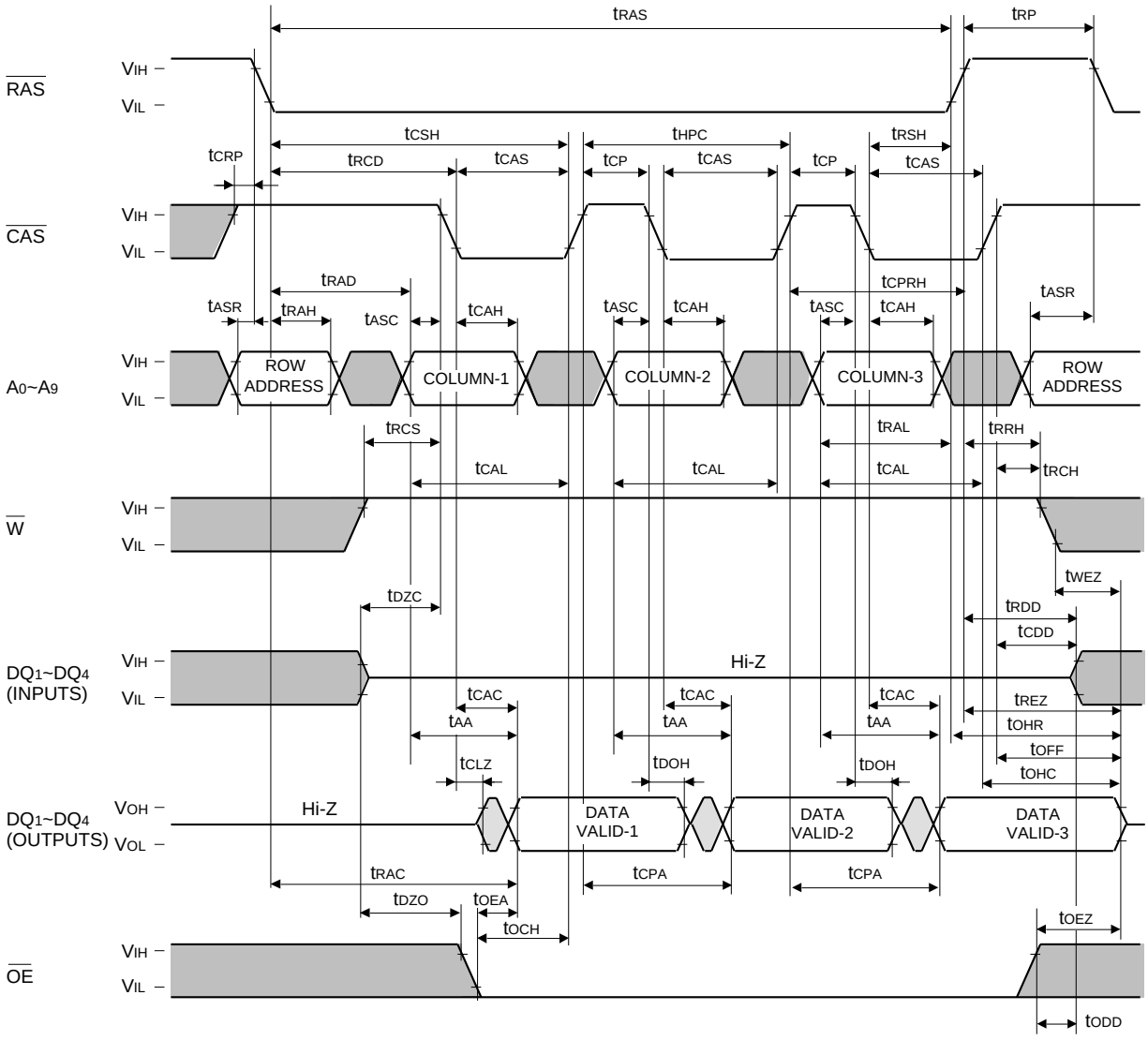
Delayed Write Cycle



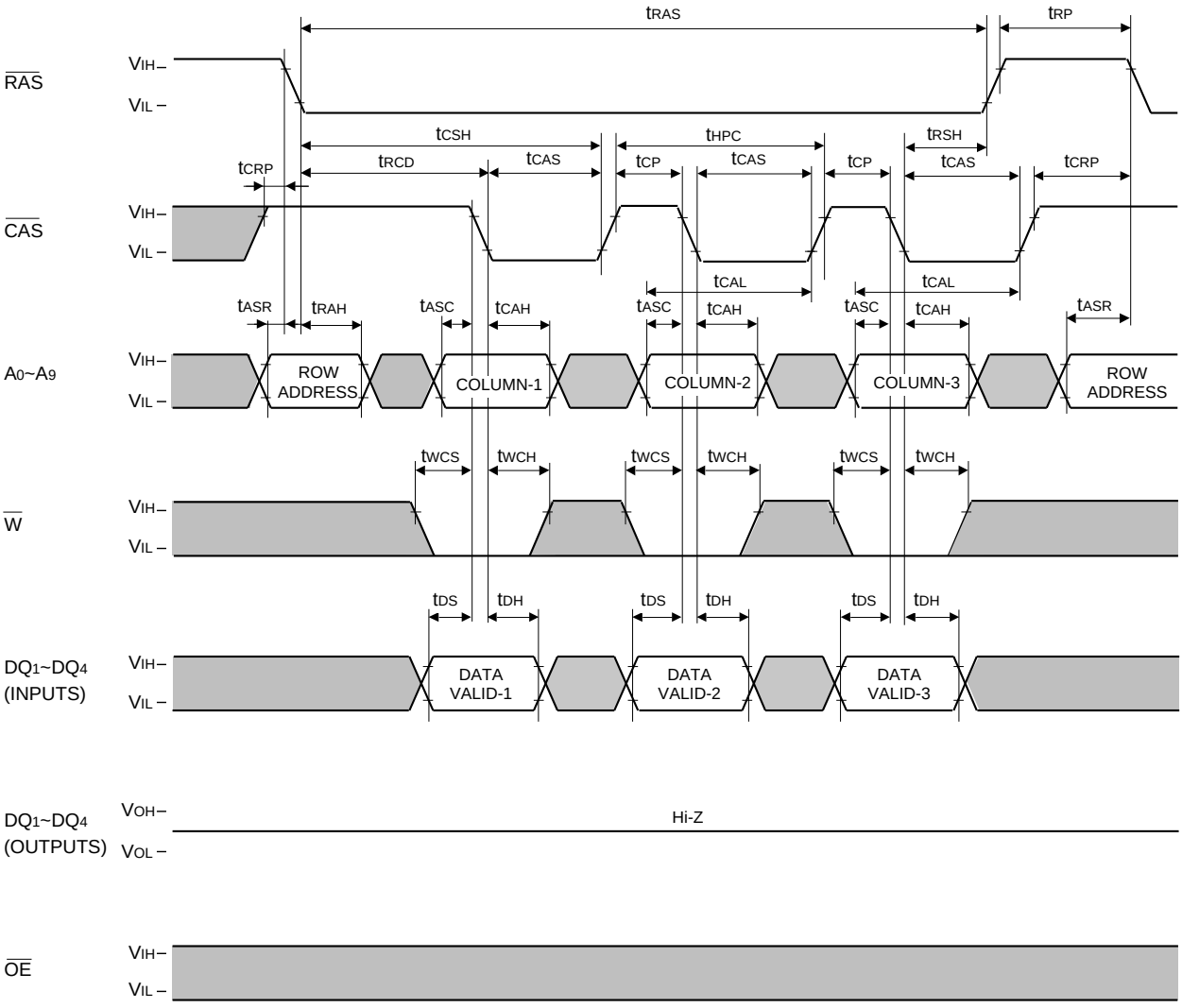
Read-Write, Read-Modify-Write Cycle



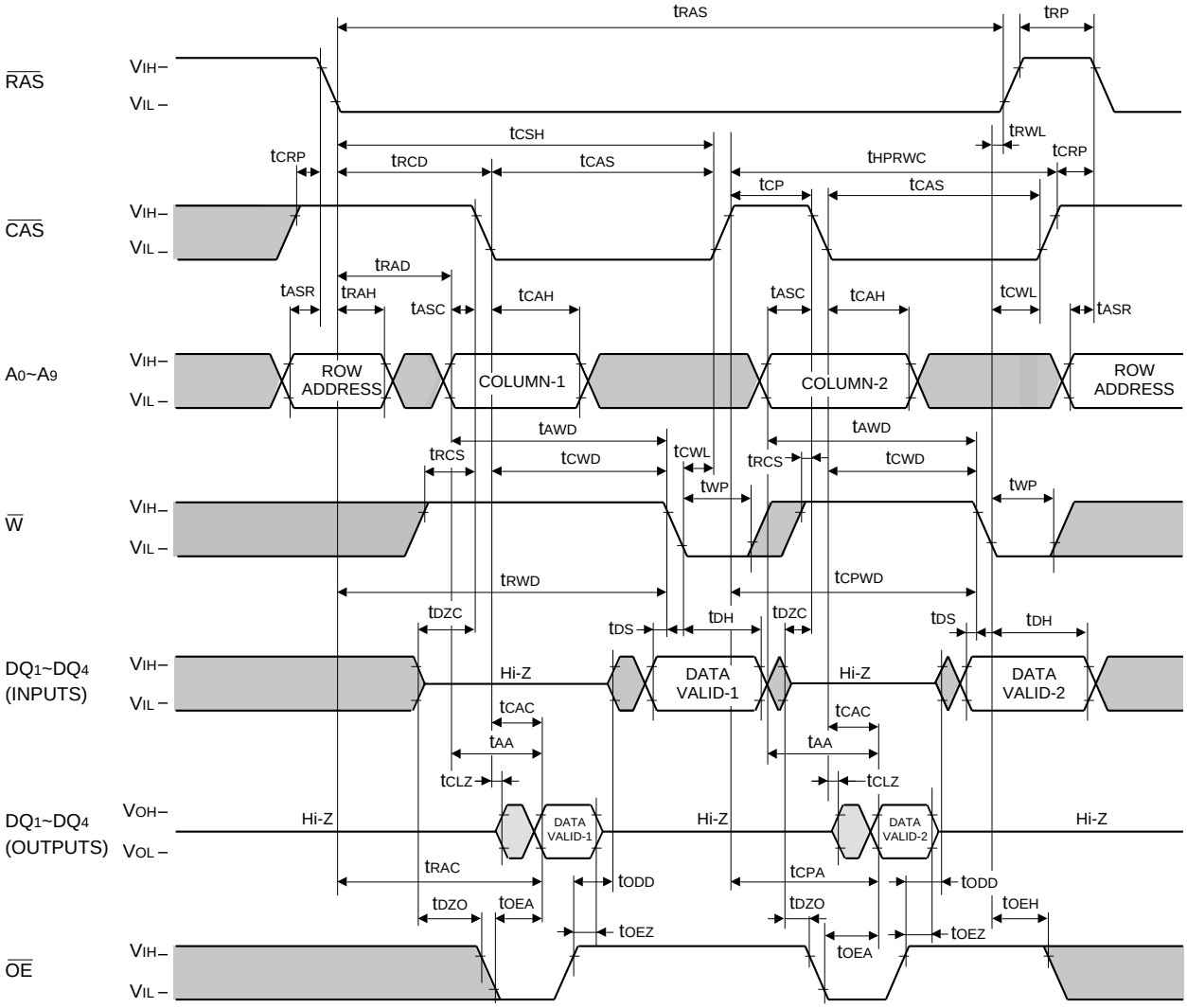
Hyper Page Mode Read Cycle



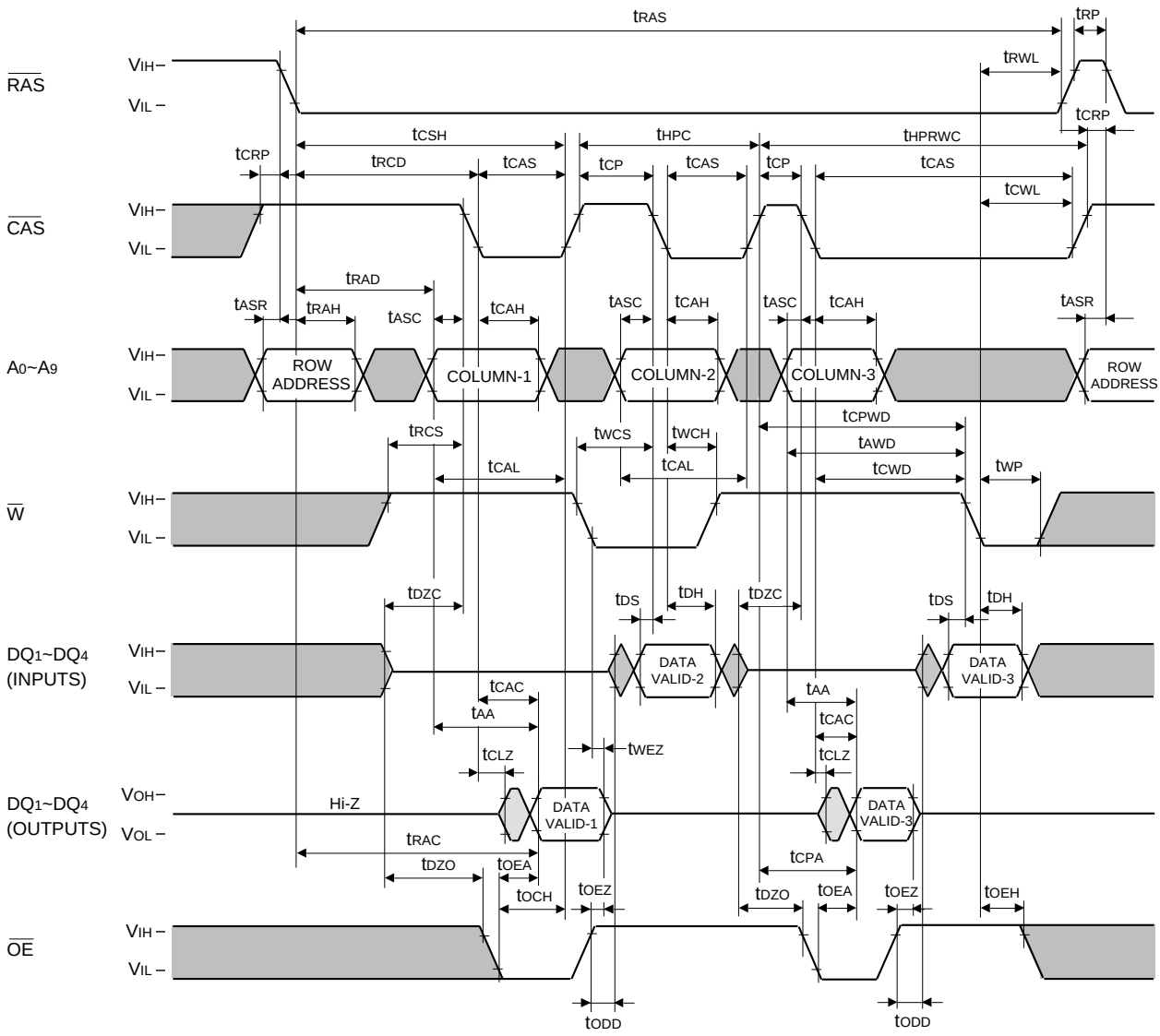
Hyper Page Mode Early Write Cycle



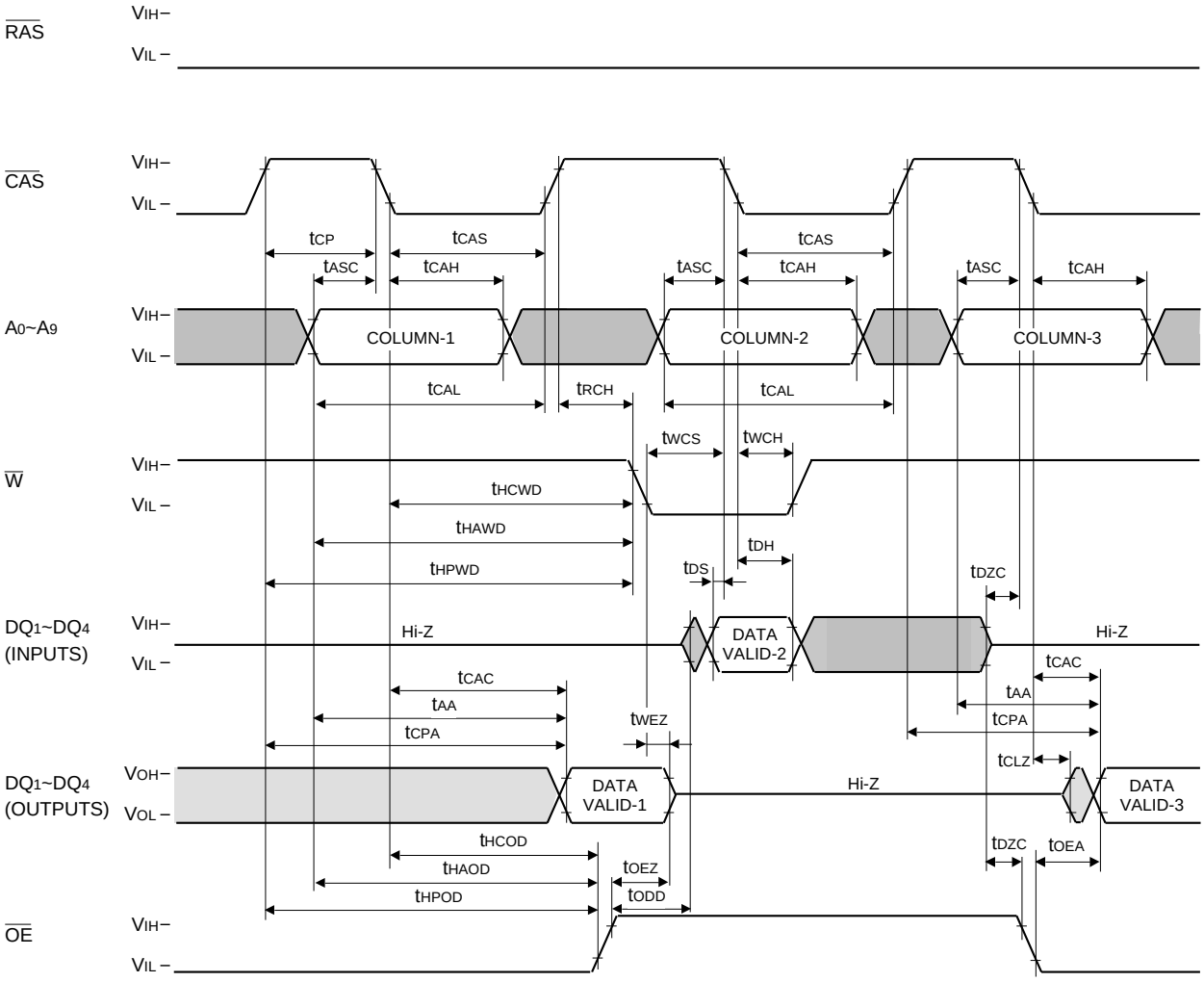
Hyper Page Mode Read-Write, Read-Modify-Write Cycle



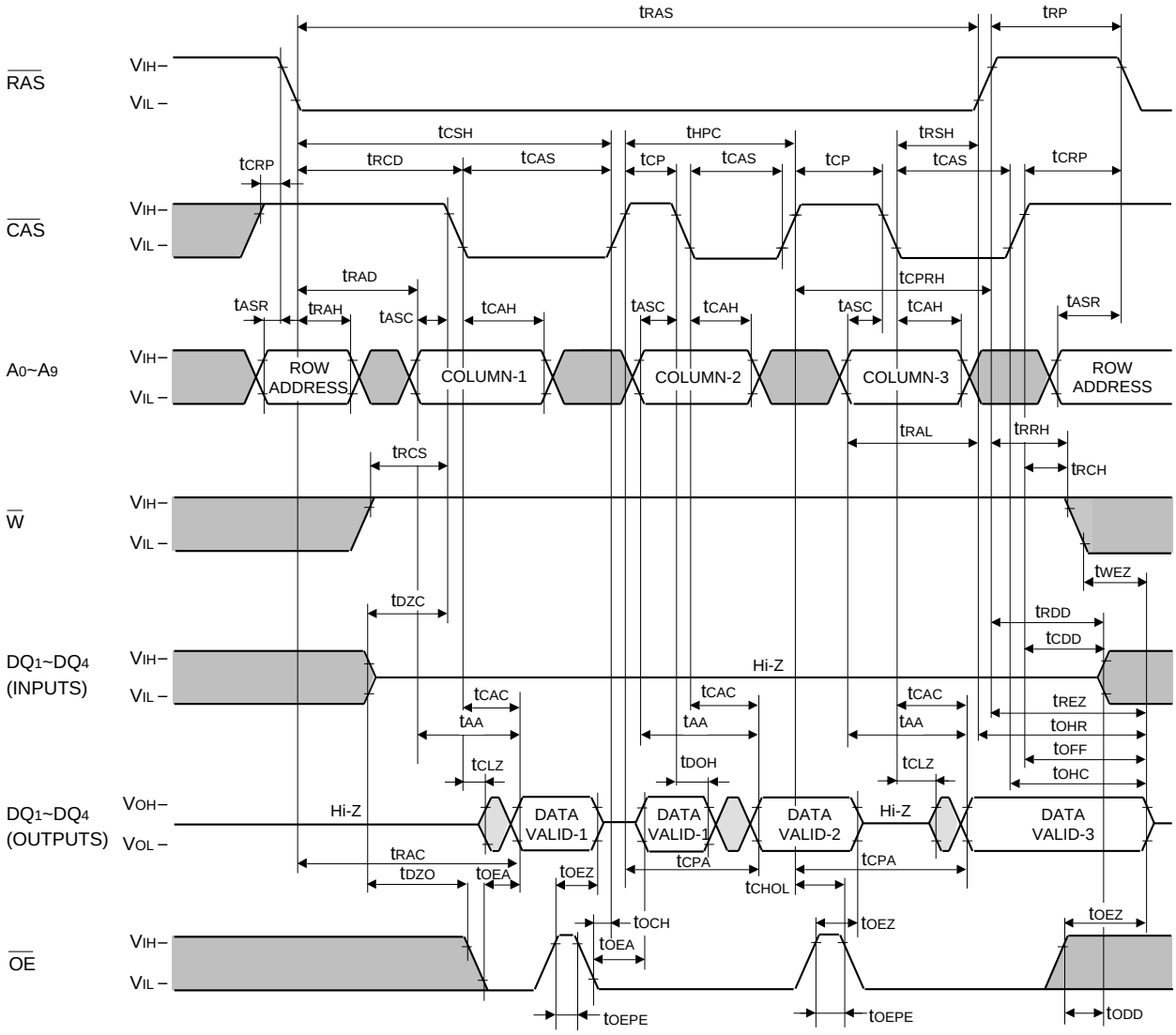
Hyper Page Mode Mix Cycle (1)



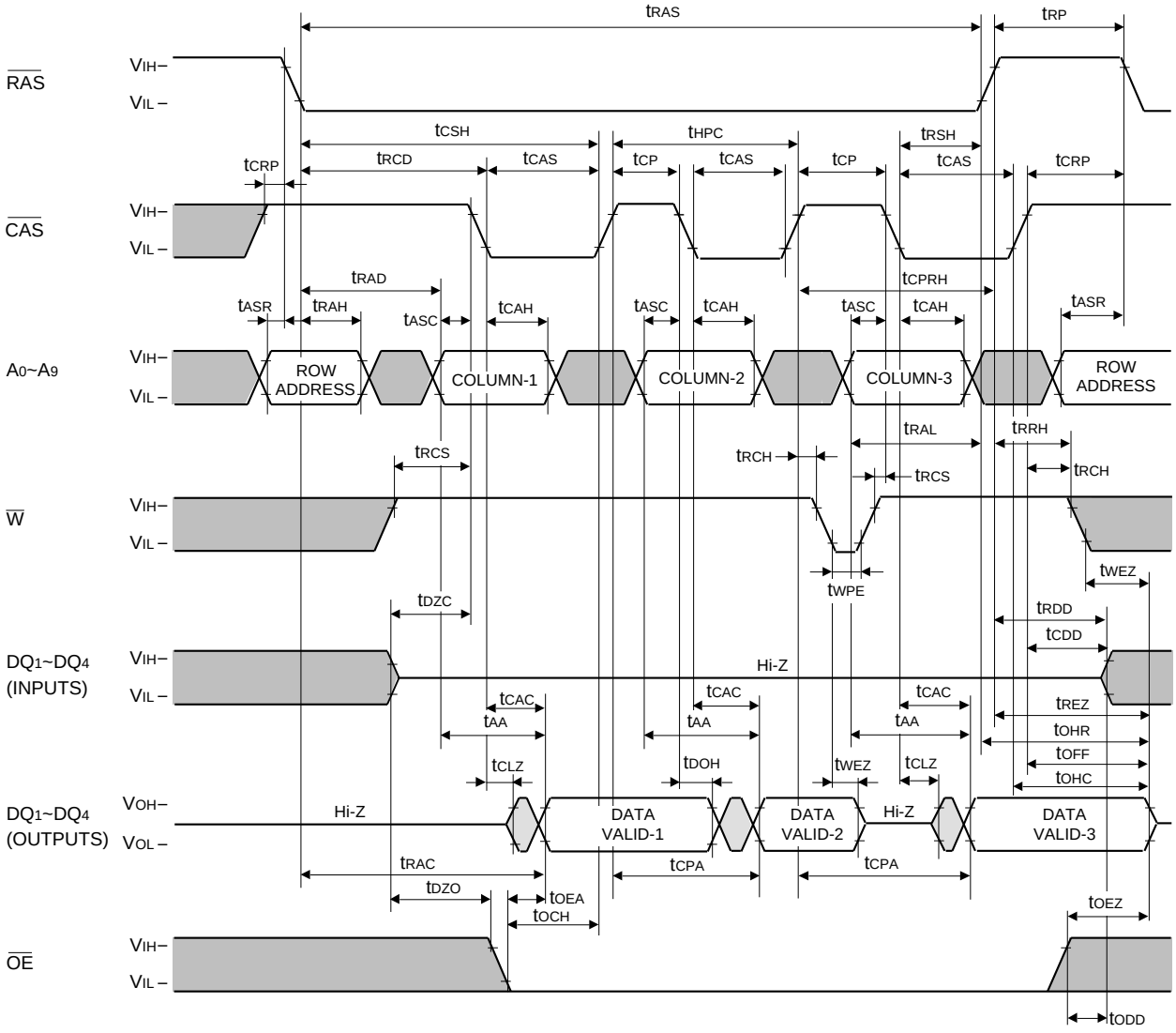
Hyper Page Mode Mix Cycle (2)



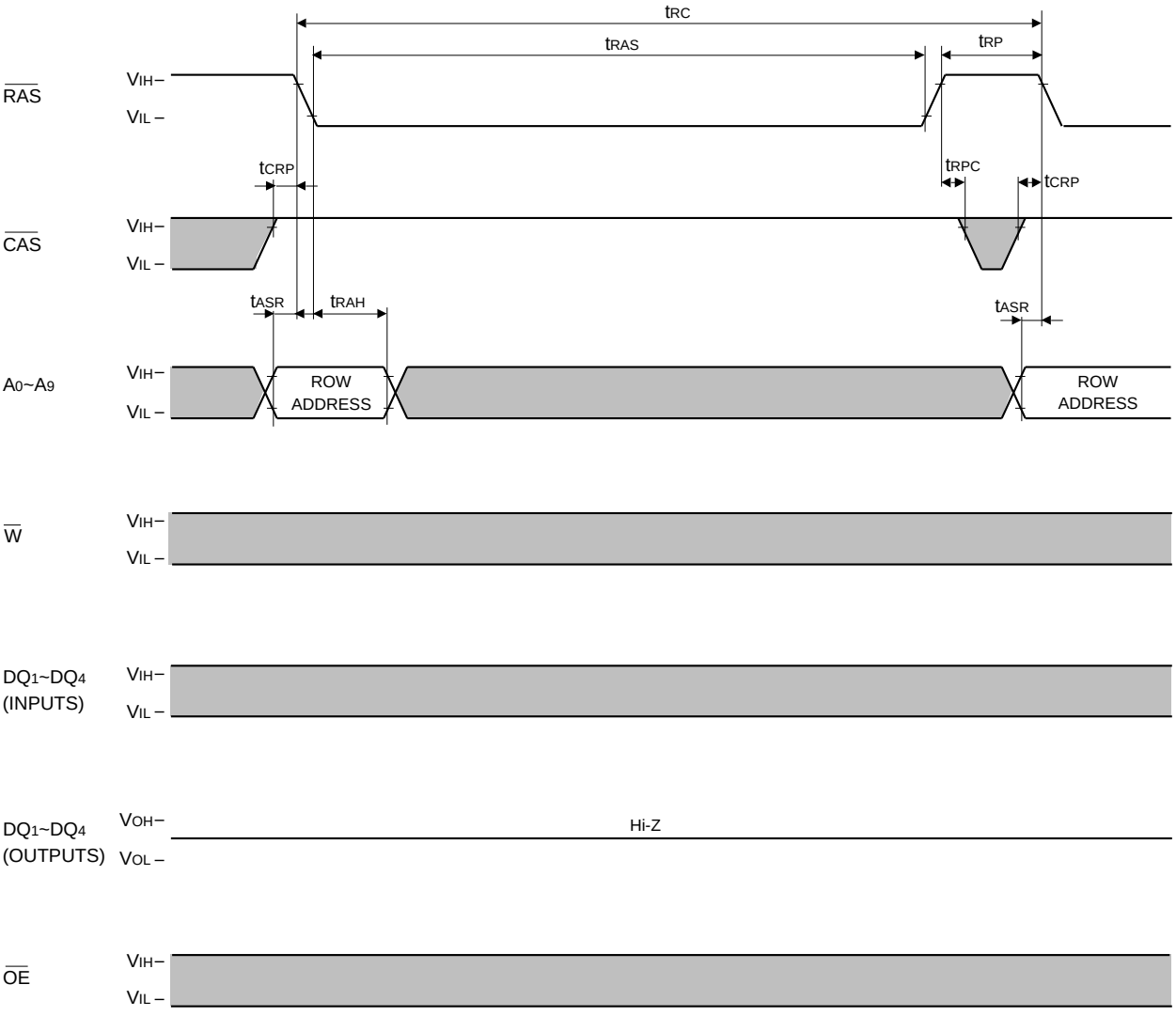
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)



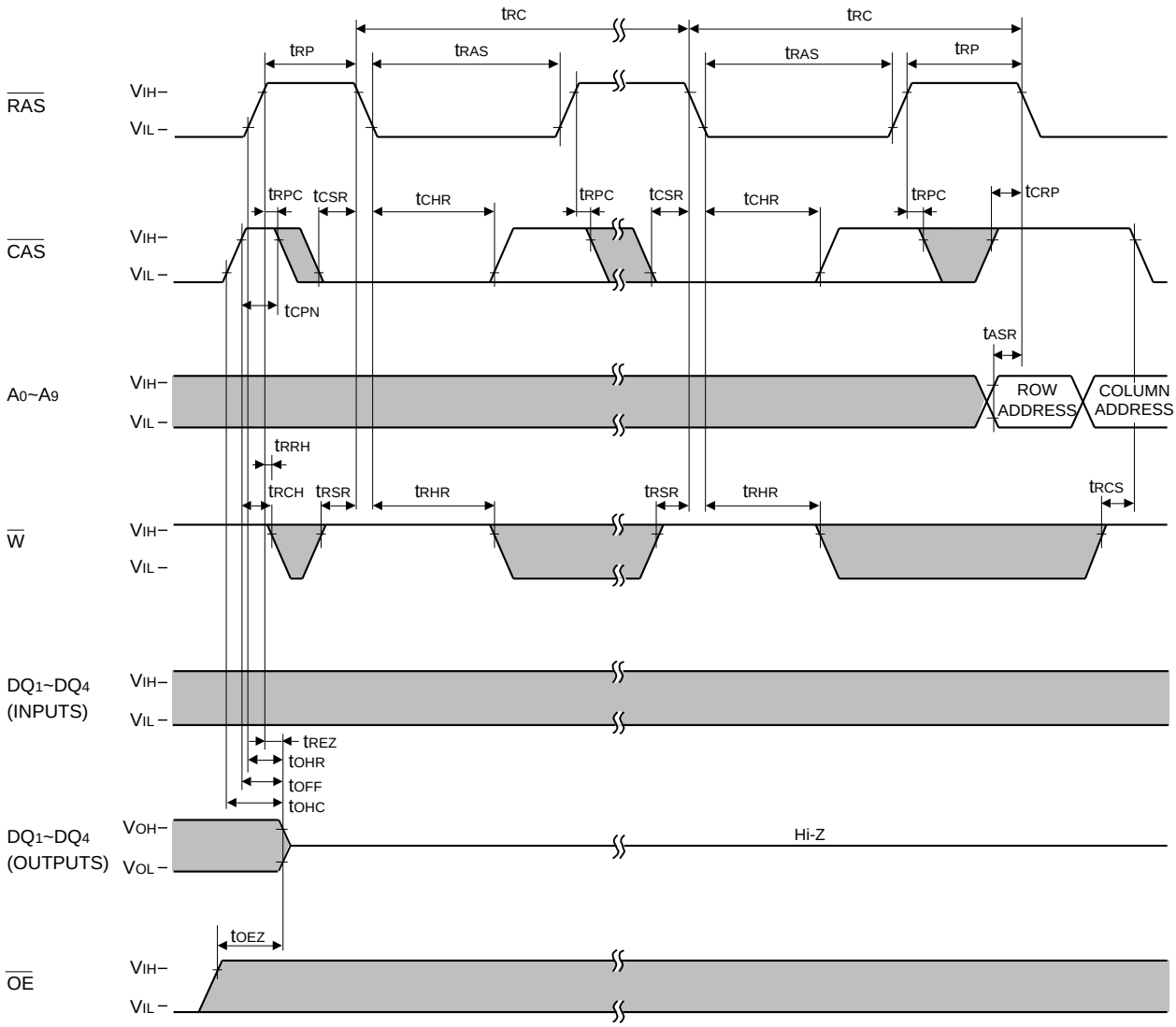
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



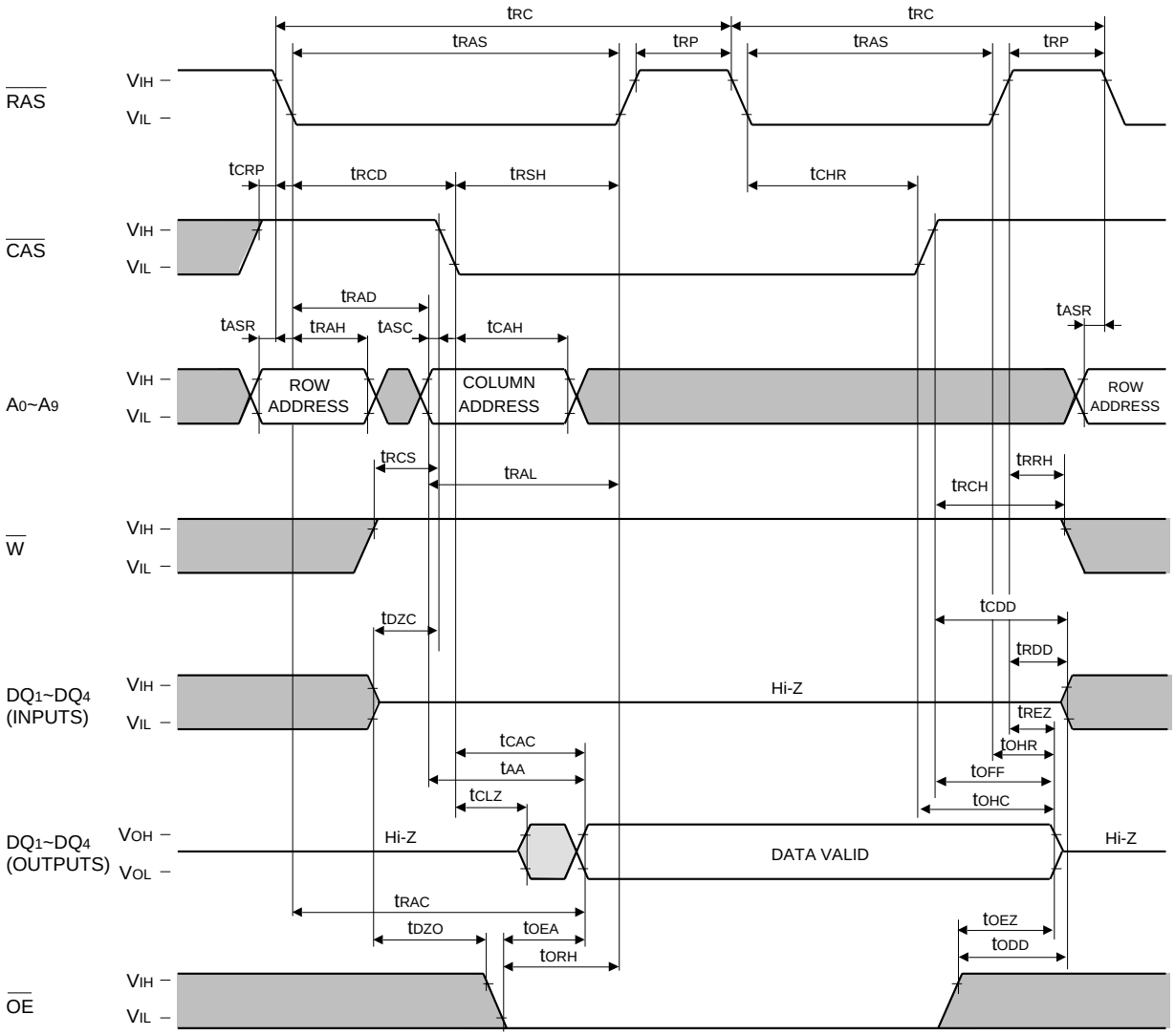
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*

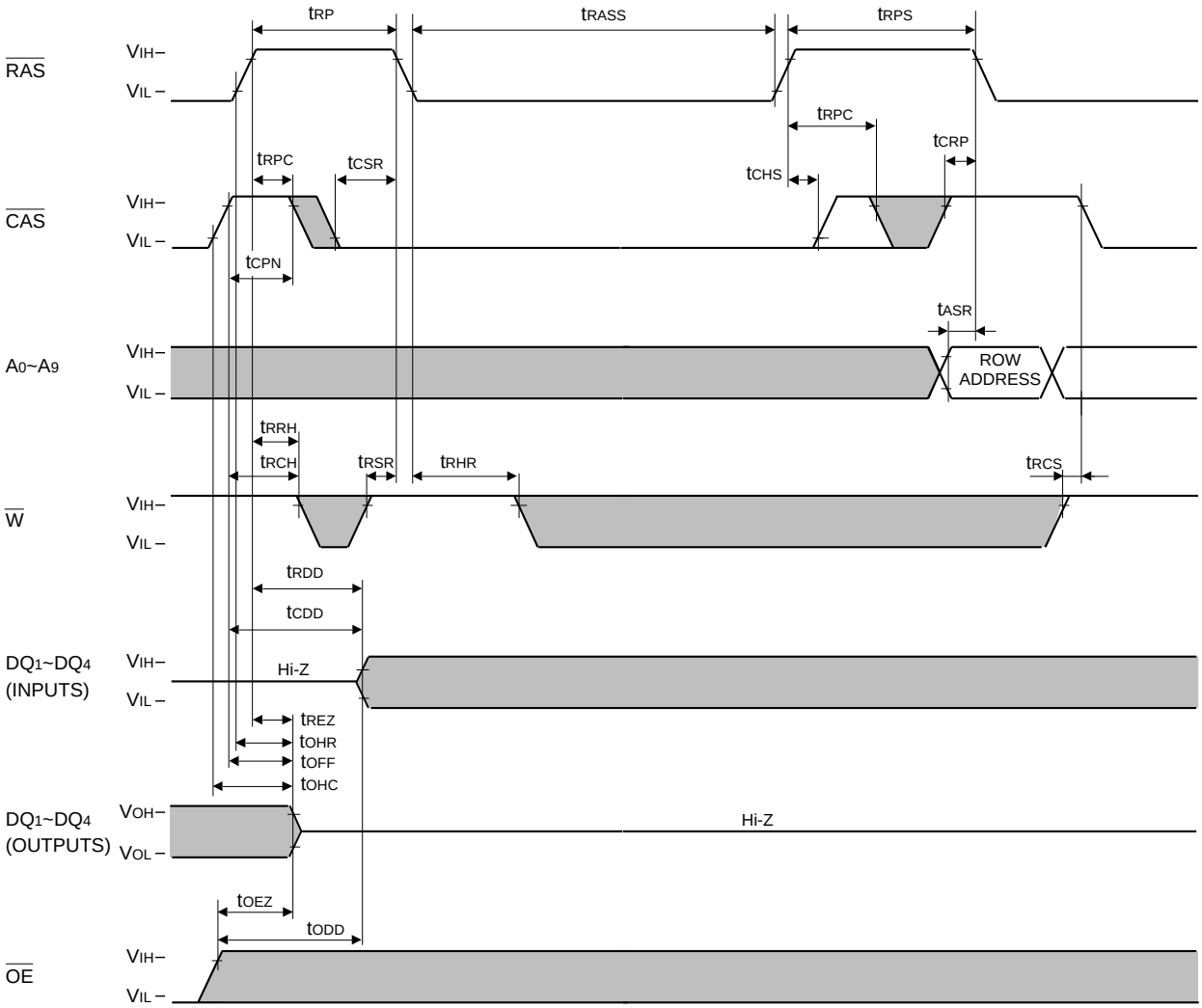


Hidden Refresh Cycle (Read) (Note 33)

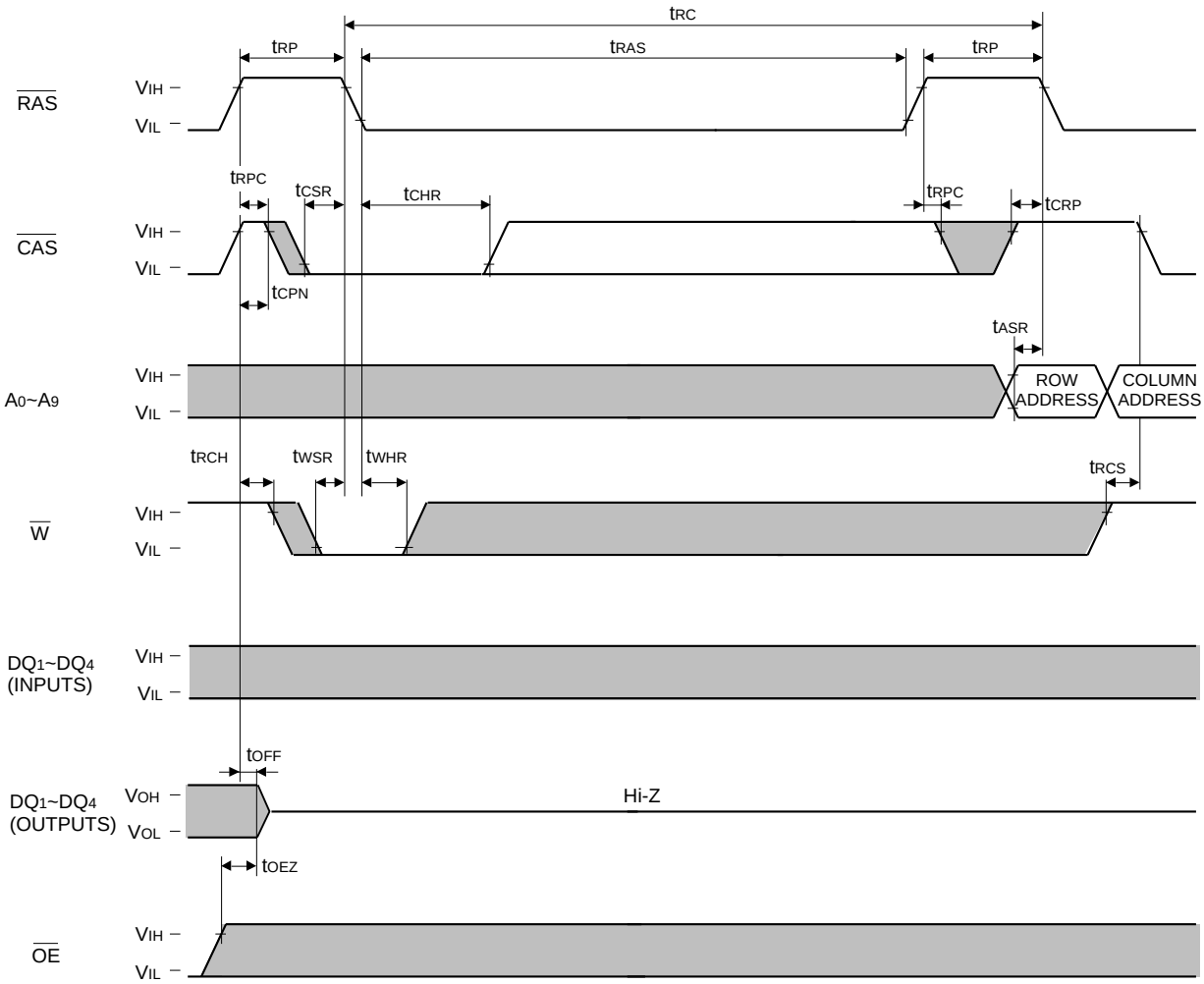


Note 33: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Self Refresh Cycle* (Note 30)



Test Mode Set Cycle (Note 34)



Note 34: The cycle is also avaiilable for initialization cycle, but in this case device enters test mode.
The test mode function is initiated with a W and CAS before RAS cycle(WCBR cycle) as specified above timing diagram.
The test mode function is terminated by either a CAS before RAS(CBR) refresh or a RAS only refresh cycle.
During the test mode, the device is internally organized as 4-bits wide (256 kilobytes deep) for each DQ (input / output) port.
No addressing of A0, A1(column only) is required.
During a write cycle, data on the each DQ (input) pin is written in parallel into all 4-bits for each DQ port and can be written independently for each DQ port.
During a read cycle, the each DQ (output) pin indicates independently a HIGH state if all 4-bits are equal, and a LOW state if any bits differ.
During the test mode operation, a WCBR cycle is used to perform refresh.

Note 30 : Self refresh sequence
Two refreshing methods should be used properly depending on the low pulse width(t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. Distributed refresh during Read / Write operation
(A) Timing Diagram

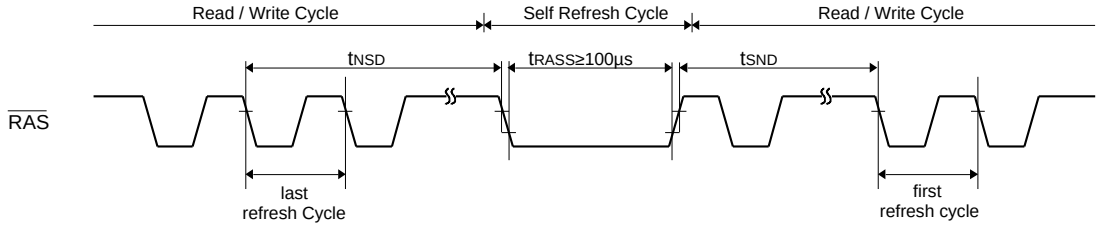
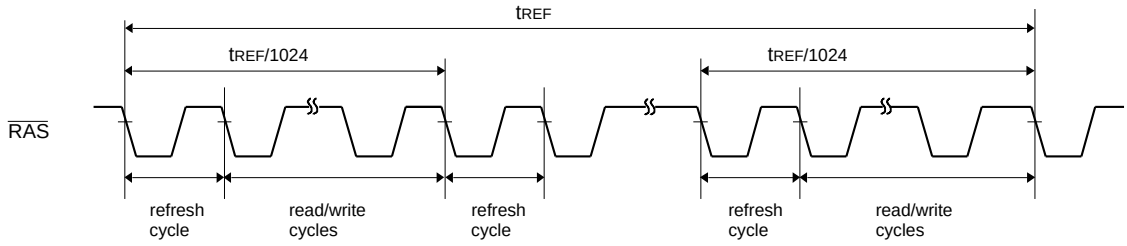


Table 2

Read / Write Cycle	Read / Write → Self Refresh	Self Refresh → Read / Write
CBR distributed refresh	t_{NSD}≤125µs	t_{SND}≤125µs
$\overline{RAS}$ only distributed refresh	t_{NSD}≤16µs	t_{SND}≤16µs

(B) Definition of distributed refresh



Definition of CBR distributed refresh
(Including extended refresh)

The CBR distributed refresh performs more than 1024 constant period(125µs max.) CBR cycles within 128 ms.

Definition of $\overline{RAS}$ only distributed refresh

All combinations of nine row address signals (A_0~A_9) are selected during 1024 constant period(16µs max.) $\overline{RAS}$ only refresh cycles within 16.4 ms.

Note:
Hidden refresh may be used instead of CBR refresh.
RAS/CAS refresh may be used instead of RAS only refresh.

1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval from the falling edge of RAS signal in the last CBR refresh cycle during read/write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation.
  The time interval from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND}(shown in table 2).

1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation.
  The time interval t_{NSD} from the falling edge of RAS signal in the last RAS only refresh cycle during read/write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within 16µs.
- Switching from self refresh operation to read/write operation.
  The time interval t_{SND} from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the first CBR refresh cycle during read/write operation period should be set within 16µs.

2. Burst refresh during Read/Write operation
(A) Timing diagram

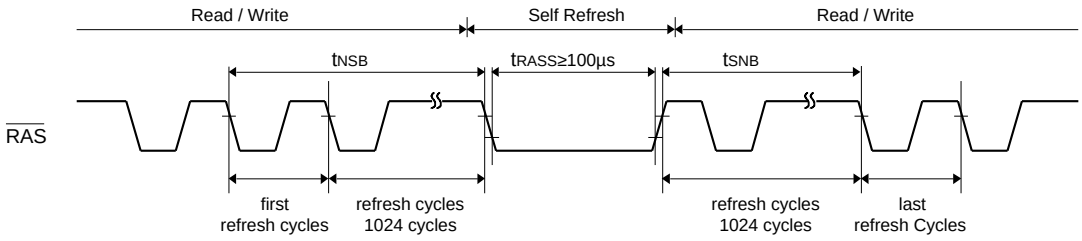
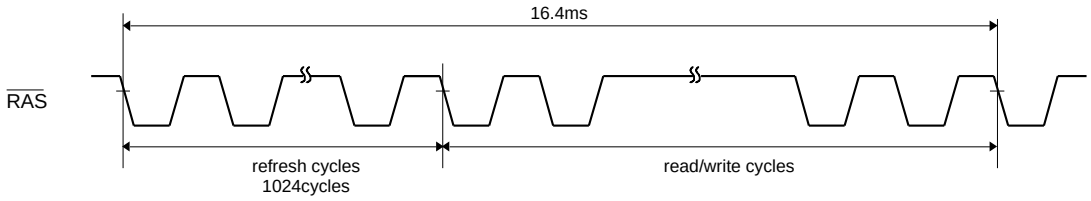


Table 3

Read / Write Cycle	Read / Write→ Self Refresh	Self Refresh→ Read / Write
CBR burst refresh	t_{NSB}≤16.4ms	t_{SNB}≤16.4ms
$\overline{RAS}$ only burst refresh	$t_{NSB}+t_{SNB}$≤16.4ms	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 1024 continuous CBR cycles within 16.4 ms.

Definition of $\overline{RAS}$ only burst refresh

All combination of nine row address signals (A_0 ~A_9) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4 ms.

2.1 CBR burst refresh

- Switching from read/write operation to self refresh operation.
  The time interval ns from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4 ms.
- Switching from self refresh operation to read/write operation.
  The time interval snob from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period should be set within 16.4 ms.

2.2 $\overline{RAS}$ only burst refresh

- Switching from read/write operation to self refresh operation.
  The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB}(Shown in table 3).
- Switching from self refresh operation to read/write operation.
  The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period should be set within t_{SNB}(shown in table 3).