M62009L,P,FP

LOW POWER 2 OUTPUT SYSTEM RESET IC WITH EXTERNAL INPUT

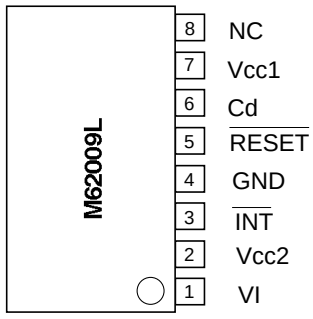
DESCRIPTION

As applications for microcomputers are increasing,a desire has arisen for a RAM backup function.Let us introduce Mitsubishi Electric new low power dissipation,high-performance system reset IC,which is suitable for such RAM backup.

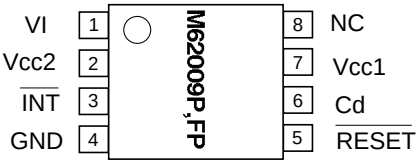
The M62009,which is a low power-dissipation 2-output microcomputer system reset IC,is a 2-output system reset IC which provides for RAM backup in microcomputers,and reduces power dissipation by using the Bi-CMOS process.The M62009 considerably reduces the number of components in the reset circuit.

The M62009 performs two-stage detection of normal supply voltage and backup supply voltage required for backup mode.When the supply voltage is switched from normal supply voltage to back up supply voltage the interruption output,which is one of the two outputs,gives the interruption signal to a microcomputer,in this way,the microcomputer reduces power dissipation and enters in the backup mode. If the backup supply voltage goes lower than the voltage required for backup,the reset output(RESET output)which is different from the INT output gives the reset signal (forced reset) to the microcomputer.The interruption signal from the INT output recovers the microcomputer from the backup mode. To recover from reset, RESET output is canceled when the specified interval of time (delay time) elapses after the signal is given from the INT output.

PIN CONFIGURATION (TOP VIEW)



Outline 8P5(L)



Outline 8P4(P)
8P2S-A(FP)

NC:NO CONNECTION

FEATURES

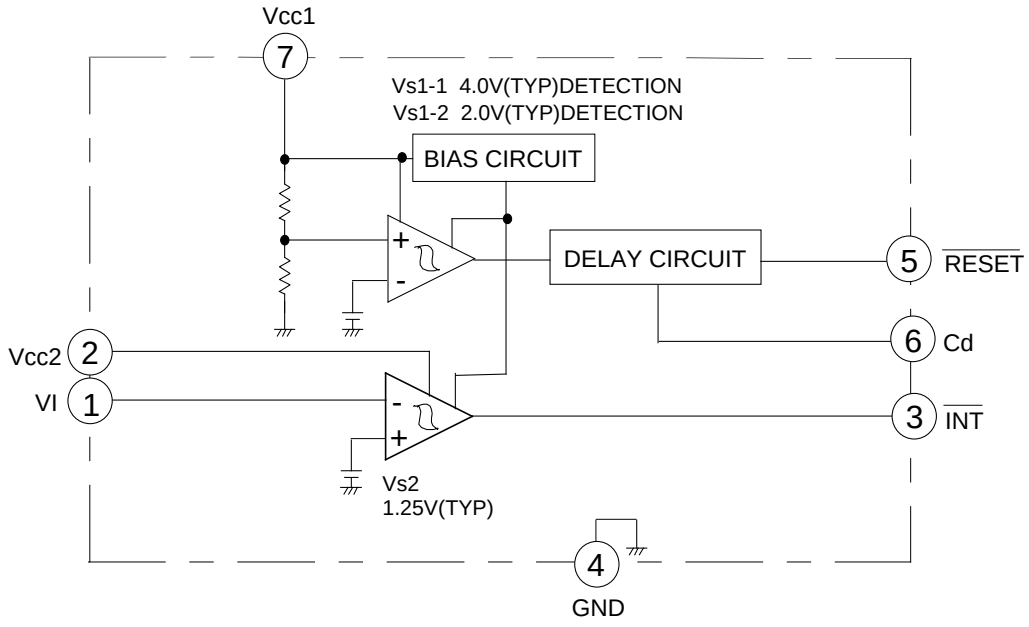
•Bi-CMOS process low power dissipation circuit configuration
Icc=7μA(Typ.) (Normal mode Vcc1=Vcc2=5.0V)
Icc=5μA(Typ.) (Backup mode Vcc1=5.0V)
Icc=1μA(Typ.) (Backup mode Vcc1=2.5V)
•Two supply detection
Vcc1(RESET) Vcc1-1=4.0V(typ):Increase of Vcc1
Vs1-2=2.0V(typ):Decrease of Vcc1
Vcc2(INT) Free set up
•Two outputs(open drain type)
Reset output (RESET):Forced reset signal output
Interruption output(INT):Output of the signal for interruption processing
(output of the switching signal for backup mode)

•Packages 2 types
5-pin SIP (single in-line)
8-pin SOP (mini flat)

APPLICATION

Prevention of errors in microcomputer system in electronic equipment that requires RAM backup,such as office,industrial,and home-use equipment.

BLOCK DIAGRAM



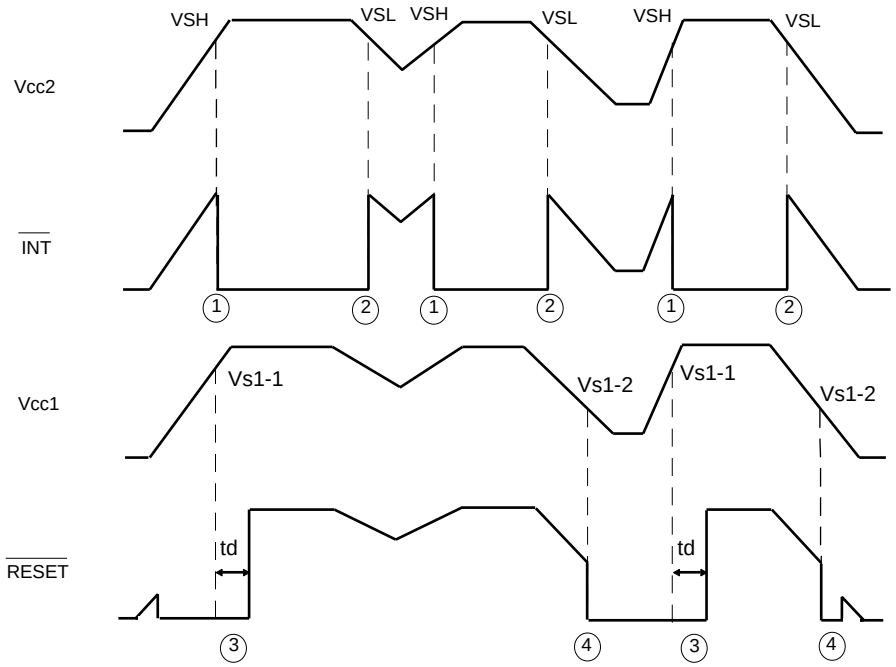
ABSOLUTE MAXIMUM RATINGS(Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		8	V
I_{SINK}	Output sink current		5	mA
Pd	Power dissipation		800(SIP)/625(DIP)/440(FP)	mW
K_Θ	Thermal derating	(Ta≥25°C)	8(SIP)/6.25(DIP)/4.4(FP)	mW/°C
T_{opr}	Operating temperature		-20 ~ +75	°C
T_{stg}	Storage temperature		-55 ~ +125	°C

ELECTRICAL CHARACTERISTICS(Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$V_{S\,1\text{-}1}$	Detection voltage	Increase of Vcc1	3.8	4.0	4.2	V
$V_{S\,1\text{-}2}$	Detection voltage	Decrease of Vcc1	1.85	2.00	2.15	V
$V_{S\,2}$	Reference voltage	Decrease of VI	1.20	1.25	1.30	V
ΔVs	Hysteresis voltage	Vcc2=Detection voltage of hysteresis voltage (Detection voltage=4V set up)		87		mV
I_{CC}	Circuit Current	Vcc1=Vcc2=5V		7	30	µA
$I_{CC2\text{-}1}$	Circuit Current	Vcc1=5V Vcc2=0V		5	20	µA
$I_{CC2\text{-}2}$	Circuit Current	Vcc1=2.5V Vcc2=0V		1	4.5	µA
td	Delay time	Cd=0.33µF		50		mS
Vsat	Output saturation voltage	V_{IN}=5V Ic=4mA(NMOS)		0.2	0.4	V

TIMING CHART



① Vcc2=VSH(Increase of Vcc2)INT output →Low
② Vcc2=VSL(Decrease of Vcc2)INT output→High
③ Delay time obtained from Vs1-1.td=50msec(Cd=0.33µF):td=1.52X10⁵XCd(sec)
RESET output:reset cancel(cancel)
④ Vcc1=VS1-2(Vcc1 Decrease)
RESET output:forced reset output(L reset)

APPLICATION CIRCUIT EXAMPLE