M62393P/FP

8-BIT 8CH I^{2}C-BUS D-A CONVERTER WITH BUFFER AMPLIFIERS

DESCRIPTION

The M62393 is an integrated circuit semiconductor of CMOS structure with 8 channels of built-in D-A converters with output buffer operational amplifiers.

The input is 2-wires serial method is used for the transfer format of digital data to allow connection with a microcomputer with minimum wiring.

The output buffer operational amplifier employs AB class output circuit with sync and source drive capacity of 1.0mA or more,and it operates in the whole voltage range from VrefU to ground.

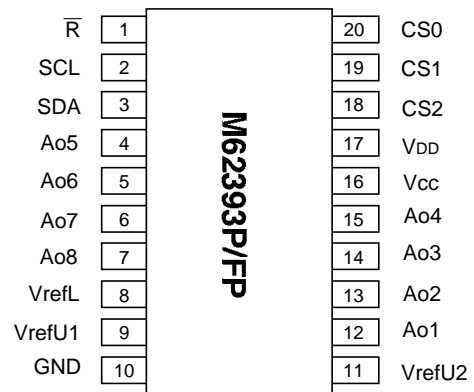And because of connects maximum 8 pieces to 64 channels control.

FEATURES

- Digital data transfer format
  I^{2}C-bus serial data method
- Output buffer operational amplifier
  it operates in the whole voltage range from VrefU(0 to 5V)to ground.
- High output current drive capacity
  ±1.0mA over
- Preparation two high level reference voltage terminal because there are two high level reference voltage terminal,it can set up two kinds differ voltage range.

APPLICATION

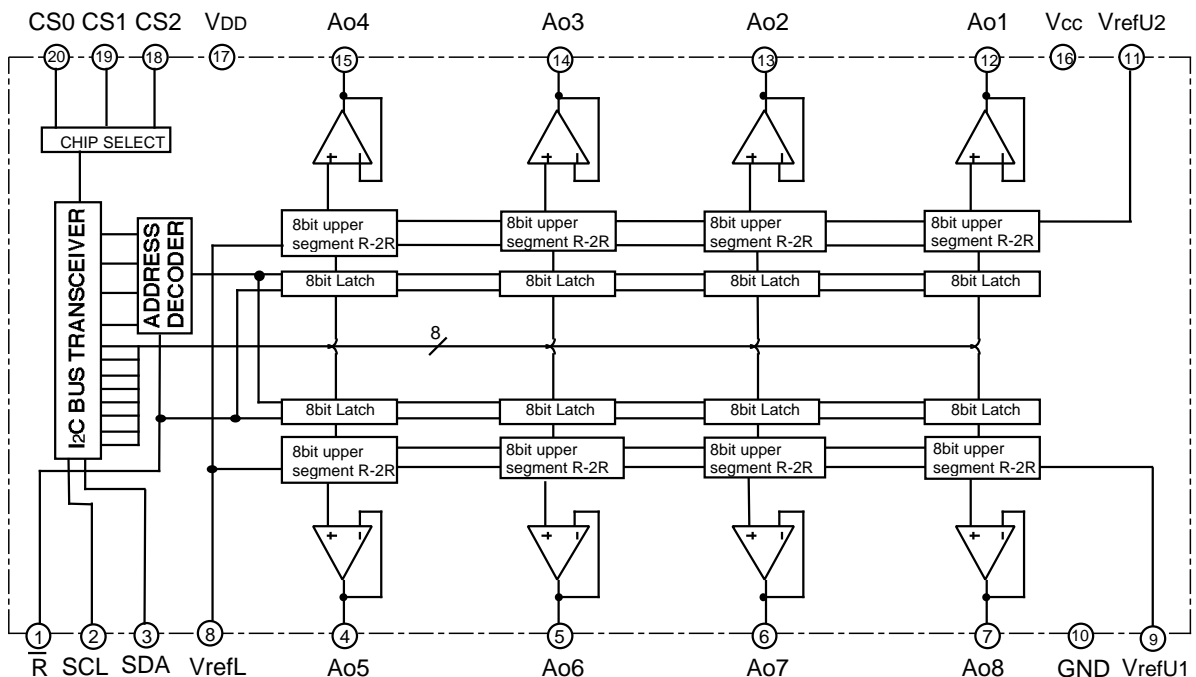Conversion from digital control data to analog control data for home-use and industrial equipment.

Signal gain control or automatic adjustment of DISPLAY-MONITOR or CTV.

PIN CONFIGURATION (TOP VIEW)

$\overline{R}$	1	20 CS0
SCL	2	19 CS1
SDA	3	18 CS2
Ao5	4	17 V$_{DD}$
Ao6	5	16 Vcc
Ao7	6	15 Ao4
Ao8	7	14 Ao3
VrefL	8	13 Ao2
VrefU1	9	12 Ao1
GND	10	11 VrefU2

M62393P/FP

Outline 20P4(P)
         20P2N-A(FP)

BLOCK DIAGRAM

8-BIT 8CH I^{2}C-BUS D-A CONVERTER WITH BUFFER AMPLIFIERS

EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
③	SDA	Serial data input terminal
①	$\overline{R}$	Reset signal input terminal
②	SCL	Serial clock input terminal
⑫	Ao1	
⑬	Ao2	
⑭	Ao3	
⑮	Ao4	8-bit D-A converter output terminal
④	Ao5	
⑤	Ao6	
⑥	Ao7	
⑦	Ao8	
⑯	V_{CC}	Analog power supply terminal
⑰	V_{DD}	Digital power supply terminal
⑩	GND	Analog and digital common GND
⑧	VrefL	D-A converter low level reference voltage input terminal
⑨	VrefU1	D-A converter high level reference voltage input terminal 1
⑪	VrefU2	D-A converter high level reference voltage input terminal 2
⑱	CS2	Chip select data input terminal 2
⑲	CS1	Chip select data input terminal 1
⑳	CS0	Chip select data input terminal 0

M62393P/FP

8-BIT 8CH I^{2}C-BUS D-A CONVERTER WITH BUFFER AMPLIFIERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.3 to +7.0	V
VDD	Supply voltage		-0.3 to +7.0	V
VrefU1,2	D-A converter high level reference voltage		-0.3 to +7.0	V
VIN	Input voltage		-0.3 to VDD+0.3	V
Vo	Output voltage		-0.3 to VDD+0.3	V
Pd	Power dissipation		990(DIP)/590(FP)	mW
Topr	Operating temperature		-20 to +85	°C
Tstg	Storage temperature		-55 to +125	°C

ELECTRICAL CHARACTERISTICS

Digital part(Vcc,VDD,VrefU1,2=+5V±10%,Vcc VrefU1,2,GND=VrefL=0V,Ta=-20 to +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VDD	Supply voltage		4.5	5.0	5.5	V
IDD	Supply current	CLK=1MHz operation IAO=0µA				mA
IILK	Input leak current	VIN=0 to Vcc	-10		10	µA
VIL	Input low voltage				0.2Vcc	V
VIH	Input high voltage		0.8Vcc			V

Analog part(Vcc,VDD,VrefU1,2=+5V±10%,Vcc VrefU1,2,GND=VrefL=0V,Ta=-20 to +85°C,unless otherwise noted)

| Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
Vcc	Supply voltage		4.5	5.0	5.5	V
Icc	Supply current	CLK=1MHz operation IAO=0µA				mA
IrefU	D-A converter high level reference voltage input current	VrefU=5V VrefL=0V Data condition:at maximum current				mA
VrefU	D-A converter high level reference voltage range	The output does not necessarily be the values within the reference voltage setting range.	3.5		Vcc	V
VrefL	D-A converter low level reference voltage range		GND		Vcc-3.5	V
VAO	Buffer amplifier output voltage range	IAO=±100µA	0.1		Vcc-0.1	V
		IAO=±500µA	0.2		Vcc-0.2	
IAO	Buffer amplifier output current range	Upper side saturation voltage=0.3V Lower side saturation voltage=0.2V	-1.0		1.0	mA
SDL	Differential nonlinearity	VrefU=4.79V VrefL=0.95V Vcc=5.5V(15mV/LSB) without load(IAO=0)	-1.0		1.0	LSB
SL	Nonlinearity		-1.5		1.5	LSB
SZERO	Zero code error		-2.0		2.0	LSB
SFULL	Full scale error		-2.0		2.0	LSB
Co	Output capacitative load				0.1	µF
Ro	Buffer amplifier output impedance			5.0		

8-BIT 8CH I^{2}C-BUS D-A CONVERTER WITH BUFFER AMPLIFIERS

I^{2}C-BUS LINE CHARACTERISTICS

Symbol	Parameter	Normal mode		High speed mode		Unit
		Min	Max	Min	Max	
f$_{SCL}$	SCL clock frequency	0	100	0	400	kHz
t$_{BUF}$	Time the bus must be free before a new transmission can start	4.7	—	1.3	—	µs
t$_{HD:STA}$	Hold time start condition.After this period.The first clock pulse is generated	4.0	—	0.6	—	µs
t$_{LOW}$	The low period of the clock	4.7	—	1.3	—	µs
t$_{HIGH}$	The high period of the clock	4.0	—	0.6	—	µs
t$_{SU:STA}$	Set up time for start condition(only relevant for a repeated start condition)	4.7	—	4.7	—	µs
t$_{HD:DAT}$	Hold time data	0	—	0	0.9	µs
t$_{SU:DAT}$	Set up time data	250	—	100		ns
t$_R$	Rise time of both SDA and SCL lines		1000	20	300	ns
t$_F$	Fall time of both SDA and SCL lines		300	20	300	ns
t$_{SU:STO}$	Set up time for stop condition	4.0	—	0.6	—	µs

*Note that transmitter must internally at reset a hold time to bridge the undefined region(max.300ns)of the falling edge of SCL.
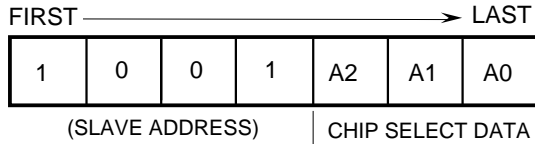
TIMING CHART
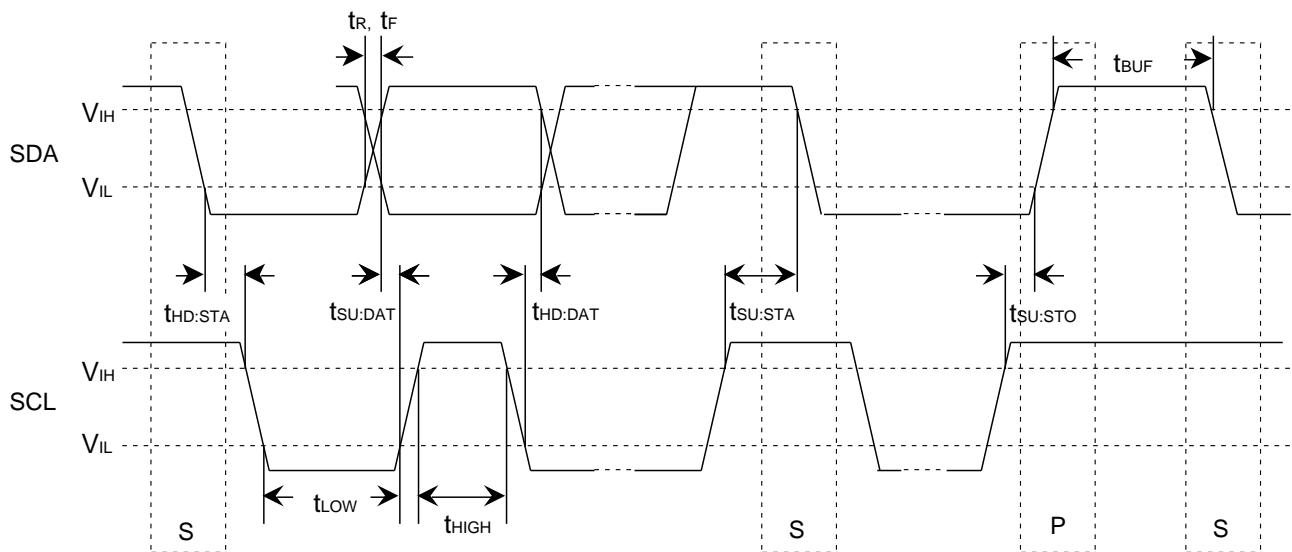
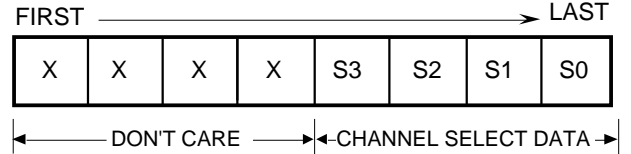**8-BIT 8CH I^{2}C-BUS D-A CONVERTER WITH BUFFER AMPLIFIERS**

I2C BUS FORMAT

STA	SLAVE ADDRESS	W	A	SUB ADDRESS	A	DAC DATA	A	STP

DIGITAL DATA FORMAT

•SLAVE ADDRESS

FIRST ⟶ LAST

1	0	0	1	A2	A1	A0

(SLAVE ADDRESS)   CHIP SELECT DATA

•SUB ADDRESS

FIRST ⟶ LAST

X	X	X	X	S3	S2	S1	S0

◄— DON'T CARE —►◄—CHANNEL SELECT DATA—►

•DAC DATA

FIRST   LAST

MSB ⟶ LSB

D7	D6	D5	D4	D3	D2	D1	D0
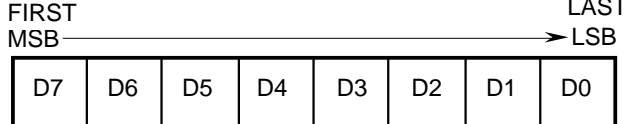
(1)CHIP SELECT DATA

MSB   LSB

A2	A1	A0	CS2	CS1	CS0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1

(2)CHANNEL SELECT DATA

MSB   LSB

S3	S2	S1	S0	Channel selection
0	0	0	0	Don't care.
0	0	0	1	ch1 selection
0	0	1	0	ch2 selection
⋮	⋮	⋮	⋮	⋮
0	1	1	1	ch11 selection
1	0	0	0	ch12 selection
1	0	0	1	Don't care.
⋮	⋮	⋮	⋮	⋮
1	1	1	1	Don't care.

(3)DAC DATA

FIRST   LAST

MSB ⟶ LSB

D7	D6	D5	D4	D3	D2	D1	D0	DAC output
0	0	0	0	0	0	0	0	(VrefU-VrefL)/256 x 1+VrefL
0	0	0	0	0	0	0	1	(VrefU-VrefL)/256 x 2+VrefL
0	0	0	0	0	0	1	0	(VrefU-VrefL)/256 x 3+VrefL
0	0	0	0	0	0	1	1	(VrefU-VrefL)/256 x 4+VrefL
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	(VrefU-VrefL)/256 x 255+VrefL
1	1	1	1	1	1	1	1	VrefU