System Reset
Monolithic IC PST623

Outline

This low reset type IC functions in CPU and other logic systems to detect input voltage and reset the system accurately when power is turned on or interruped.

Features

1. Detection voltage can be set easily (2 external resistors)
2. High percision voltage detection Internal reference voltage 1.25±2%
3. Enables high voltage check (at stage before Reg)
4. Low operating limit voltage 0.65V typ.
5. High output current during ON 10mA min.
6. Low current consumption 40μA typ.
7. Built-in delay circuit (1 external capacitor)

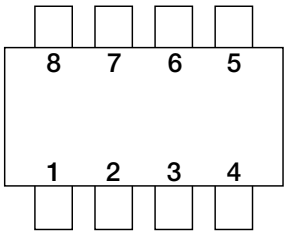
Applications

1. Reset circuits in microcomputers, CPUs and MPUs
2. Logic circuit reset circuits
3. Level detection circuits

Package

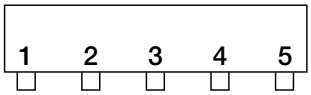
VSOP-8A (PST623XS)
SIP-5A (PST623XW)

Pin Assignment



VSOP-8A

1	Vs
2	NC
3	TC
4	GND
5	RESET
6	NC
7	NC
8	Vcc



SIP-5A

1	Vcc
2	Vs
3	TC
4	GND
5	RESET

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Units
Storage temperature	T_{STG}	–40~+125	℃
Maximum power supply voltage	V_{CC} max.	10	V
Allowable power consumption	Pd max.	300	mW
Input pin voltage	V_{ID}	–0.3~V_{CC}	V

Recommended Operating Conditions

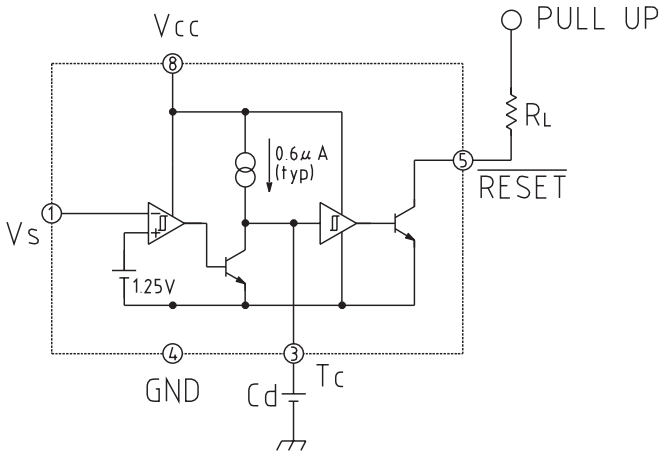
Item	Symbol	Rating	Units
Power supply voltage	V_{CCOP}	2.0~10.0	V
Operating temperature	T_{OPG}	–25~+75	℃

Electrical Characteristics (Except where noted otherwise, V_{CC}=5V, Ta=25°C)

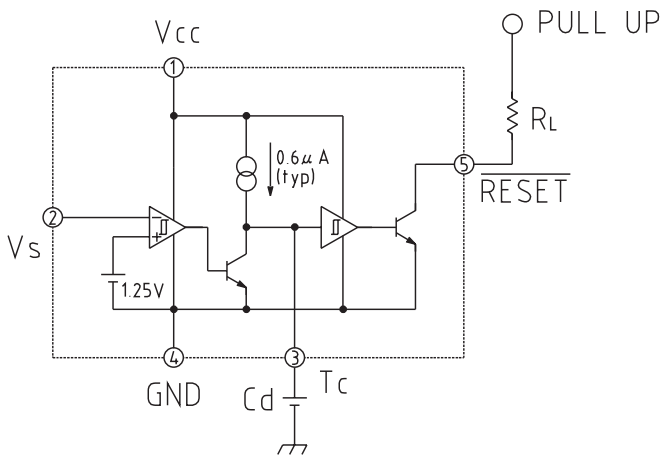
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Detection reference voltage	V_S	R_L=470Ω, V_{IN}=H→L	1.225	1.25	1.275	V
Hysteresis voltage	⊿V_S	R_L=470Ω, V_{IN}=L→H→L	12	25	50	mV
Detection reference voltage temperature coefficient	$\frac{V_S}{\Delta T}$	R_L=470Ω, Ta=–25~+75℃		±0.01		%/℃
L level output voltage	V_{OL}	V_{IN}=1.0V, R_L=470Ω		0.3	0.45	V
Output leakage current	I_{OH}	V_{IN}=1.5V, V_{OUT}=10V			±0.1	μA
Circuit current while on	I_{CCL}	V_{IN}=1.0V, R_L=∞		50	90	μA
Circuit current while off	I_{CCH}	V_{IN}=1.5V, R_L=∞		42	70	μA
"H" transport delay time	tpLH	R_L=4.7kΩ, Cd=0.047uF		110		mS
"L" transport delay time	tpHL	R_L=4.7kΩ, Cd=0.047uF		15		μS
Operation limit voltage	V_{OPL}	R_L=4.7kΩ, V_{OL} ≦ 0.4V Minimum power supply voltage for which output can maintain Lo.		0.65	0.85	V
Output current while on	I_{OL}	V_{IN}=1.0V, R_L=0	10			mA
Delay time setting comparator Threshold level	Vtsh	R_L=470Ω, V_{TC}=L→H	1.25	1.4	1.55	V
Capacitor charging current	I_{TC}	V_{IN}=1.5V, V_{TC}=0.2V	0.39	0.60	0.81	μA
Vs input current	I_{IN}	V_{IN}=1.35V		40		nA

Equivalent Circuit Diagram

■ VSOP-8A

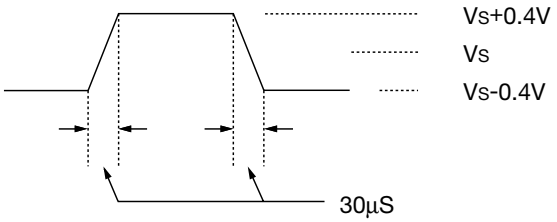


■ SIP-5A



Notes on Using PST623

1. Input voltage rise and fall

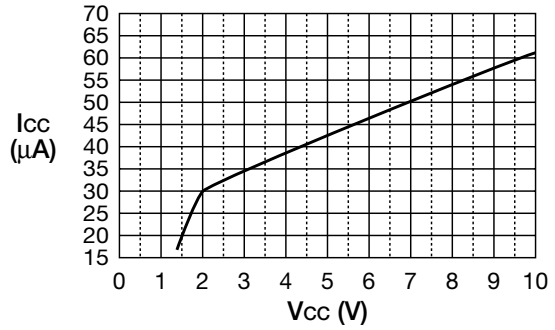


Be sure to give an incline of more than 30μS to rise and fall for input with varied power supply voltage (V_{CC}) and bleeder resistance.
Also, when setting input bleeder resistance, VS pin input current is affected and the detection voltage setting will differ from the set value if current on the bleeder resistor is too low.
Use input bleeder resistor R2 at 250kΩ or less.

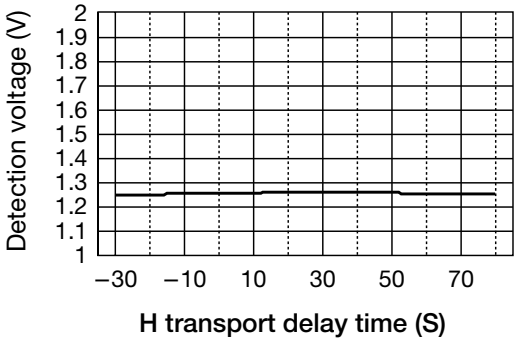
2. Delay time setting
H transmission delay time can be set easily as follows from the TC pin, using the external capacitor.
T = Cd × (2.33 × 106) [S]
Use the external capacitor at 1μF (approx. 2.33S) or less.

Characteristics

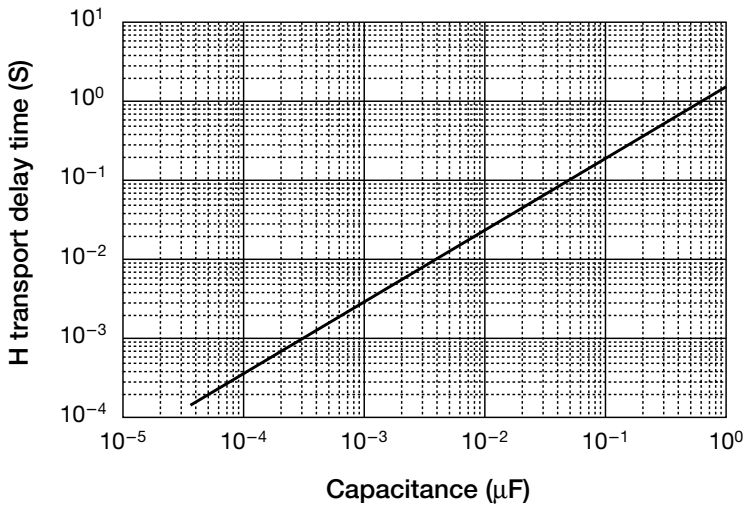
Current consumption for OFF



Detection voltage

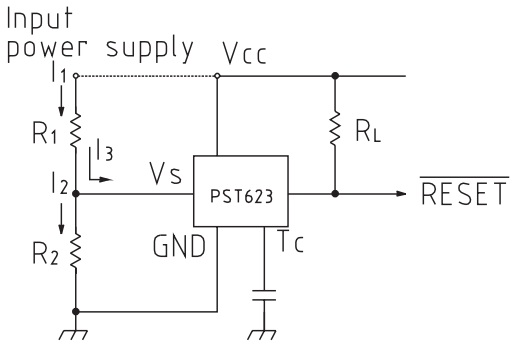


H transport delay time



Application Circuits

1. Circuit Diagram

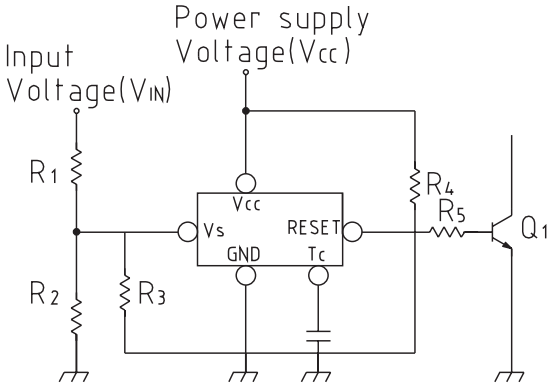


2. Detection Voltage Setting

$$V_S \fallingdotseq 1.25 \cdot \frac{R1+R2}{R2}$$

* Note
The value of I2 should be sufficient to ignore I3.
Make I2 > 5μA.
R2 < 250kΩ

3. How to widen hysteresis



Voltage $V_{IN}1$ so that Q1 ON goes OFF.

$$V_{IN}1=\frac{(R1+R2)}{R2 \cdot (R3+R4//R5)}[1.25\ (V) \cdot (R3+R1//R2+R4//R5) - \frac{R1//R2}{R4+R5}(R4 \cdot V_{BE}+R5 \cdot V_{CC})]$$

Voltage $V_{IN}2$ so that Q1 OFF goes ON.

$$V_{IN}2=\frac{(R1+R2)}{R2 \cdot R3}[1.275\ (V) \cdot (R1//R2+R3) - V_{OL} \cdot (R1//R2)]$$

VOL: Low level output voltage
VBE: Base-emitter voltage of transistor Q1

$$R1//R2 \equiv \frac{R1 \cdot R2}{R1+R2} \qquad R4//R5 \equiv \frac{R4 \cdot R5}{R4+R5}$$