

System Reset (with built-in watchdog timer) Monolithic IC MM1096

Outline

This IC functions in a variety of CPU systems and other logic systems to generate a reset signal and reset the system accurately during momentary interruption or lowering of power supply voltage.

It also has a built-in watchdog timer for operation diagnosis. This prevents the system from running wild by generating an intermittent reset pulse during system mis-operation.

Features

1. Built-in watchdog timer
2. Low minimum operating voltage 130μA typ.
3. Low operating limit voltage $V_{CC}=0.8V$
4. Watchdog stop function (RCT pin)
5. Long clock monitoring time
 T_{PR} (POWER ON) : T_{WD} (clock monitoring)=1 : 5
6. Few external parts

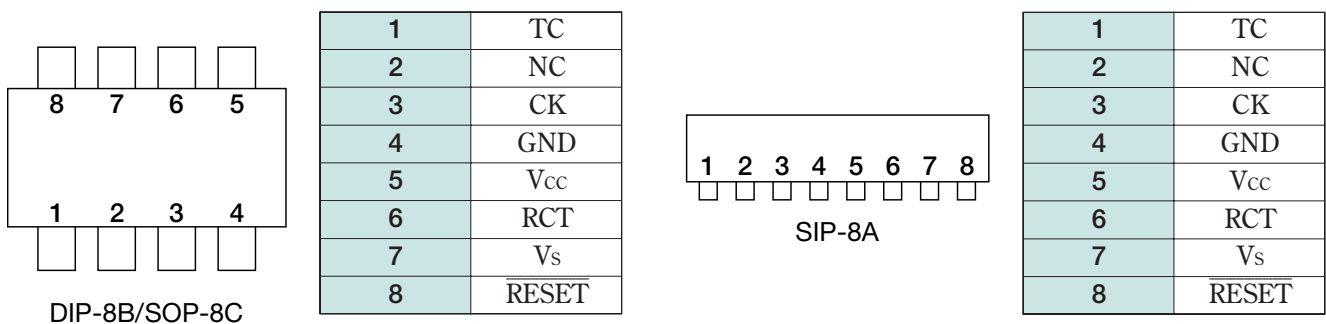
Package

- DIP-8B (MM1096AD, MM1096BD)
- SOP-8C (MM1096AF, MM1096BF)
- SIP-8A (MM1096AS, MM1096BS)

Applications

1. Reset circuits in microcomputers, CPUs and MPUs
2. Logic circuit reset circuits
3. Microcomputer system monitoring, etc.

Pin Assignment



Pin Description

Pin No.	Pin name	Function
1	TC	T _{WD} , T _{WR} , T _{PR} variable pins. (T _{WD} , T _{WR} and T _{PR} times are determined by the external capacitor.) T _{PR} (mS) = 500 × C _T (μF) T _{WD} (mS) = 2500 × C _T (μF) T _{WR} (mS) = 100 × C _T (μF)
2	N.C	
3	CK	Clock input pin, inputs clock from logic system
4	GND	GND pin
5	V _{CC}	Voltage detection MM1096A → 3.2V, MM1096B → 4.2V
6	RCT	Watchdog timer stop pin Operation modes : Operation → OPEN, Stop → connect to GND
7	V _S	Detection voltage variable pin
8	$\overline{\text{RESET}}$	Reset output pin (low output)




Absolute Maximum Ratings

Item	Symbol	Rating	Units
Power supply voltage	V _{CC} max.	-0.3~+10	V
CK pin input voltage	V _{CK}	-0.3~V _{CC} +0.3 (≤ +10)	V
V _S pin input voltage	V _{VS}	-0.3~V _{CC} +0.3 (≤ +10)	V
Voltage applied to RCT pin	V _{RCT}	-0.3~V _{CC} +0.3 (≤ +10)	V
Voltage applied to $\overline{\text{RESET}}$ pin	V _{OH}	-0.3~V _{CC} +0.3 (≤ +10)	V
Allowable loss	P _d	300	mW
Storage temperature	T _{STG}	-40~+125	°C


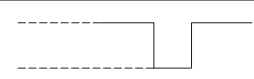
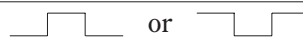

Recommended Operating Conditions

Item	Symbol	Rating	Units
Power supply voltage	V _{CC}	+2.2~+7.0	V
$\overline{\text{RESET}}$ sync current	I _{OL}	0~1.0	mA
Clock monitoring time setting	T _{WD}	0.1~1000	mS
Clock rise and fall times	t _{FC} , t _{FC}	<100	μS
TC pin capacitance	C _T	0.0002~2	μF
Operating temperature	T _{OP}	-25~+75	°C

Electrical Characteristics (DC) (Except where noted otherwise, MM1096A : $V_{CC}=3.6V$, $T_a=25^{\circ}C$, MM1096B : $V_{CC}=5.0V$)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Consumption current	MM1096A	I _{CC}	During watchdog timer operation		100	150	μA
	MM1096B				130	195	
Detection voltage	MM1096A	V _{SL}	V _S =OPEN, V _{CC} 	3.10	3.20	3.30	V
	MM1096B			4.05	4.20	4.35	
	MM1096A	V _{SH}	V _S =OPEN, V _{CC} 	3.15	3.25	3.35	
	MM1096B			4.15	4.30	4.45	
Detection voltage temperature coefficient		V _S /ΔT			±0.01		%/°C
Hysteresis voltage	MM1096A	V _{HYS}	V _{SH} -V _{SL} , V _{CC} 	25	50	100	mV
	MM1096B			50	100	150	
CK input threshold		V _{TH}		0.8	1.2	2	V
CK input current		I _{IH}	A : V _{CK} =3.6V, B : V _{CK} =5.0V		0	1	μA
		I _{IL}	V _{CK} =0V	-12	-6	-2	
Output voltage (High)	MM1096A	V _{OH}	I _{RESET} = 1μA V _S =OPEN	3.0	3.4		V
	MM1096B			4.0	4.5		
Output voltage (Low)		V _{OL1}	I _{RESET} = 0.5mA, V _S =0V		0.2	0.4	V
		V _{OL2}	I _{RESET} = 1.0mA, V _S =0V		0.3	0.5	
R output sync current		I _{OL}	V _{RESET} = 1.0V, V _S =0V	1	2		mA
C _T charge current		I _{CT1}	V _{TC} =1.0V during watchdog timer operation	-0.28	-0.48	-0.96	μA
		I _{CT2}	V _{TC} =1.0V during power ON reset operation	-1.60	-2.40	-4.80	μA
Minimum operating power supply voltage to ensure <u>RESET</u>		V _{CCL}	V _{RESET} = 0.4V I _{RESET} = 0.1mA		0.8	1.0	V

Electrical Characteristics (DC) (Except where noted otherwise, MM1096A : $V_{CC}=3.6V$, $T_a=25^{\circ}C$, MM1096B : $V_{CC}=5.0V$)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
V _{CC} input pulse width	T _{PI}	V _{CC} 3.6V 2.8V 	8			μS
		V _{CC} 5.0V 4.0V 	8			
CK input pulse width	T _{CKW}	CK 	3			μS
CK input cycle	T _{CK}		20			μS
Watchdog timer monitoring time *1	T _{WD}	C _T =0.02μF	25	50	75	mS
Reset time for watchdog timer *2	T _{WR}	C _T =0.02μF	1	2	3	mS
Reset hold time for power supply rise *3	T _{PR}	C _T =0.02μF, V _{CC} 	5	10	15	mS
Output delay time from V _{CC} *4	T _{PD}	$\overline{\text{RESET}}$ pin, R _L =10kΩ, C _L =20pF		2	10	μS
Output rise time *5	t _R	$\overline{\text{RESET}}$ pin, R _L =10kΩ, C _L =20pF		2.0	4.0	μS
Output fall time *5	t _F	$\overline{\text{RESET}}$ pin, R _L =10kΩ, C _L =20pF		0.2	1.0	μS

Notes:

- *1 Monitoring time is the time from the last pulse (negative edge) of the timer clear clock pulse until reset pulse output. In other words, reset output is output if a clock pulse is not input during this time.
- *2 Reset time means reset pulse width. However, this does not apply to power ON reset.
- *3 Reset hold time is the time from when V_{CC} exceeds detection voltage (V_{SH}) during power ON reset until reset release ($\overline{\text{RESET}}$ output high).
- *4 Output delay time is the time from when power supply voltage drops below detection voltage (V_{SL}) until reset ($\overline{\text{RESET}}$ output low).
- *5 Voltage range when measuring output rise and fall is 10~90%.
- *6 Watchdog timer monitoring time (T_{WD}), watchdog timer reset time (T_{WR}) and reset hold time (T_{PR}) during power supply rise can be changed by varying C_T capacitance. The times are expressed by the following formulae.

$$T_{PR} \text{ (mS)} \approx 500 \times C_T \text{ (}\mu\text{F)}$$

$$T_{WD} \text{ (mS)} \approx 2500 \times C_T \text{ (}\mu\text{F)}$$

$$T_{WR} \text{ (mS)} \approx 100 \times C_T \text{ (}\mu\text{F)}$$

Example : When C_T=0.02μF

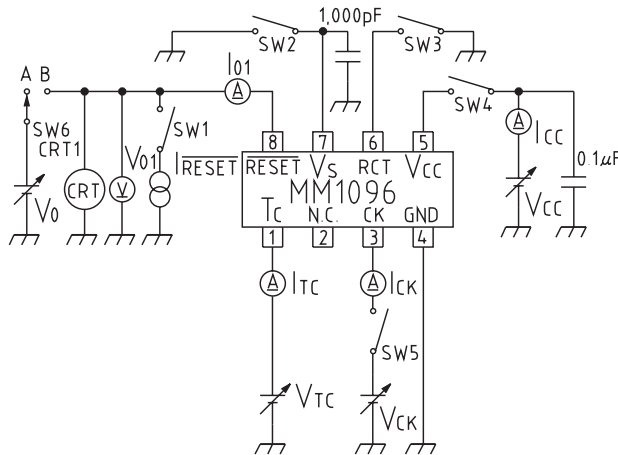
$$T_{PR} \approx 10\text{mS}$$

$$T_{WD} \approx 50\text{mS}$$

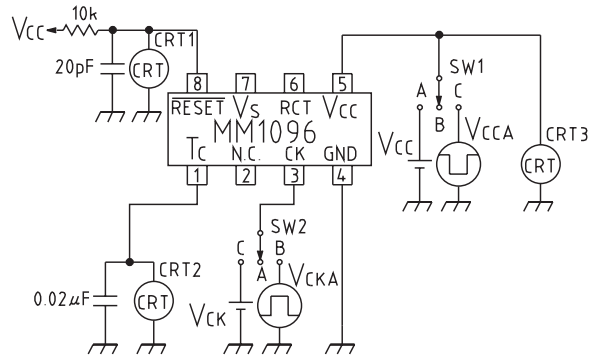
$$T_{WR} \approx 2\text{mS}$$

Measuring Circuits

Measuring Circuit 1 (DC)



Measuring Circuit 2 (AC)



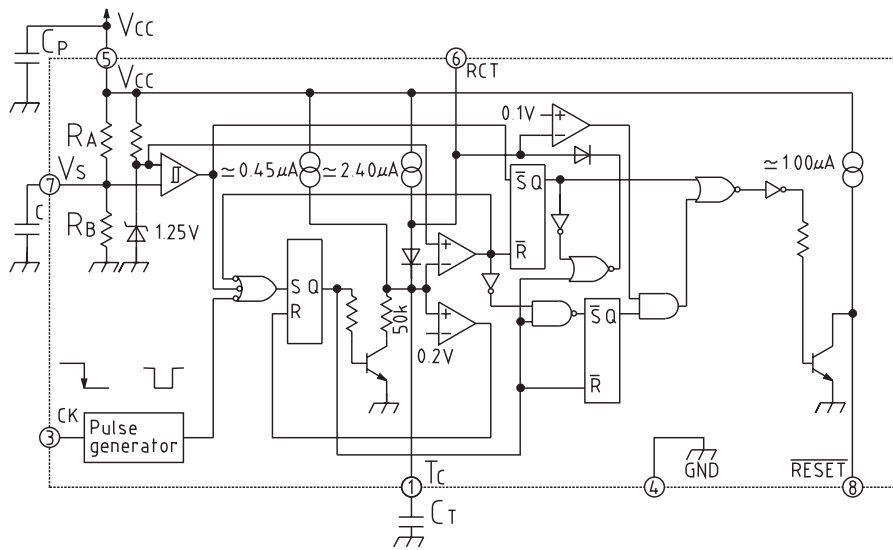
Measuring Circuit 1 SW & Power Supply Table

Item	Symbol	SW1	SW2	SW3	SW4	SW5	SW6	SW7	V _{CC}	V _{CK}	V _{CT}	I _{RESET}	VM, IM	Notes
Consumption current	I _{CC}	OFF	OFF	OFF	ON	ON	ON	A	3.6V	3.6V	0V	-	I _{CC}	
Detection voltage	V _{SL}	OFF	OFF	ON	ON	ON	ON	A	3.6V→3V	0V	2V	-	V _{O1} , CRT1	
	V _{SH}	OFF	OFF	ON	ON	ON	ON	A	3V→3.6V	0V	2V	-	V _{O1} , CRT1	
CK input threshold	V _{TH}	OFF	OFF	OFF	ON	ON	ON	A	3.6V	0V→3V	1V	-	I _{CK} , V _{CK}	
CK input current	I _{IH}	OFF	OFF	OFF	ON	ON	ON	A	3.6V	3.6V	0V	-	I _{CK}	
	I _{IL}	OFF	OFF	OFF	ON	ON	ON	A	3.6V	0V	0V	-	I _{CK}	
Output voltage (High)	V _{OH}	ON	OFF	ON	ON	ON	ON	A	3.6V	3.6V	2V	-1μA	V _{O1}	
Output voltage (Low)	V _{OL1}	ON	ON	ON	ON	ON	ON	A	3.6V	3.6V	2V	0.5mA	V _{O1}	
	V _{OL2}	ON	ON	ON	ON	ON	ON	A	3.6V	3.6V	2V	1.0mA	V _{O1}	
Output sink current	I _{OL1}	OFF	ON	ON	ON	ON	ON	B	3.6V	3.6V	2V	-	I _{O1}	V _O =1V
C _T charge current 1	I _{TC1}	OFF	OFF	OFF	ON	ON	OFF	A	3.6V	-	1V	-	I _{TC}	
C _T charge current 2	I _{TC2}	OFF	OFF	OFF	ON	ON	OFF	A	3.6V	-	IV	-	I _{TC}	
Minimum operating power supply voltage to ensure RESET	V _{CCL}	ON	OFF	ON	ON	ON	ON	A	0V→2V	0V	0V	-	V _{O1} , V _{CC}	

Measuring Circuit 2 SW & Power Supply Table

Item	Symbol	SW1	SW2	V _{C_{CA}}	V _{CC}	V _{C_{KA}}	V _{CK}	CRT	Notes
V _{CC} input pulse width	T _{P1}	C	B		-		-	CRT1 CRT2	T ₁ =8μS
CK input pulse width	T _{CKW}	A	B	-	3.6V		-	CRT1 CRT2	T ₂ =3μS
CK input cycle	T _{CK}	A	B	-	3.6V		-	CRT1 CRT2	T ₃ =20μS
Watchdog timer monitoring time	T _{WD}	A	A	-	3.6V	-	3.6V	CRT1 CRT2	
Reset time for watchdog timer	T _{WR}	A	A	-	3.6V	-	3.6V	CRT1 CRT2	
Reset hold time for power supply rise	T _{PR}	B→A	A	-	3.6V	-	3.6V	CRT1 CRT2	
Output delay time from V _{CC}	T _{PD}	C	A		-	-	0V	CRT1	
Output rise time	T _R	A	A	-	3.6V	-	3.6V	CRT1	
Output fall time	T _F	A	A	-	3.6V	-	3.6V	CRT1	

Block Diagram



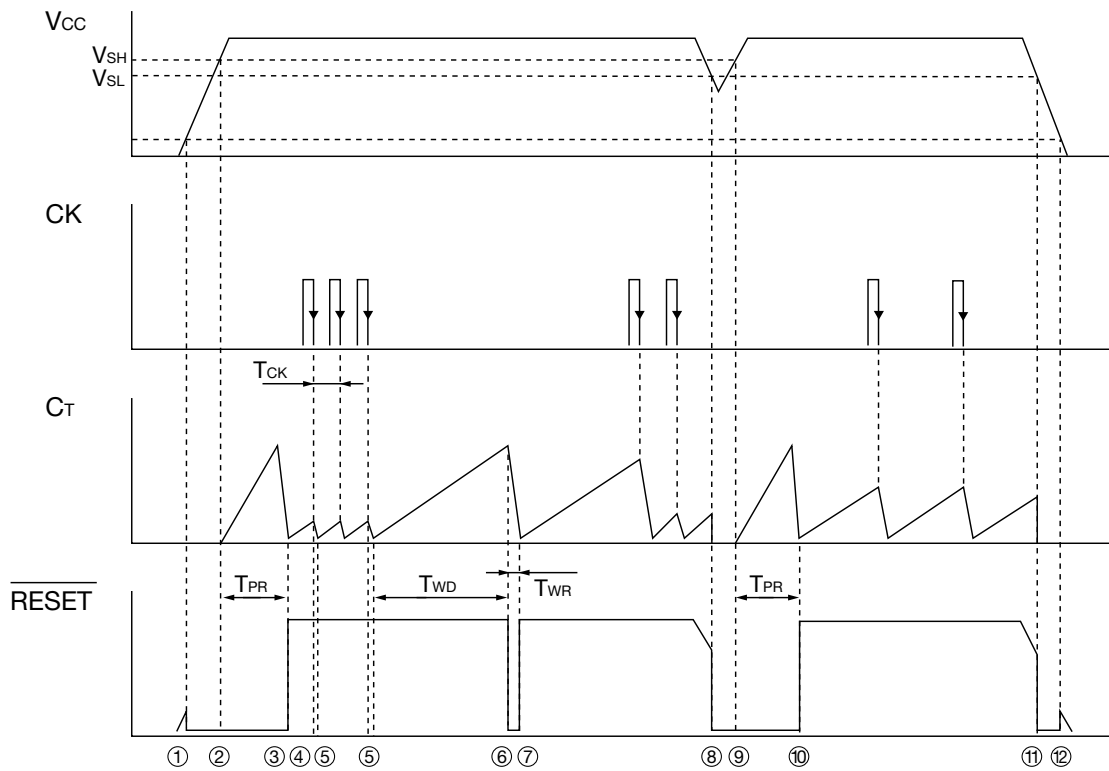
	RA	RB
MM1096A	≈ 305k	≈ 195k
MM1096B	≈ 350k	≈ 150k

Note 1: Cp=0.1µF approx.

Note 2: C=1000pF

Note 3: The watchdog timer can be stopped by connecting the RCT pin to GND. Then it functions as a voltage detection circuit.)

Timing Chart



Description of Operation

1. $\overline{\text{RESET}}$ goes low when V_{CC} rises to approximately 0.8V.
Approximately $1\mu\text{A}$ ($V_{CC}=0.8\text{V}$) of pull up current is output from $\overline{\text{RESET}}$
2. Capacitor C_T charging starts when V_{CC} rises to V_{SH} (MM1096A \approx 3.25V, MM1096B \approx 4.3V). Output is in reset state at this time.
3. Output reset is released ($\overline{\text{RESET}}$ goes high) after a certain time (T_{PR}), from when C_T starts charging until discharge (the time from when C_T voltage reaches a certain threshold value 1 (\approx 1.4V) until C_T voltage drops to a certain threshold value 2 (\approx 0.2V).
Reset hold time : T_{PR} is as follows.
 $T_{PR} \text{ (mS)} \approx 500 \times C_T \text{ (}\mu\text{F)}$
 C_T charging starts again after reset release, and watchdog timer operation begins.
Clock input to the CK pin during C_T charging will cause mis-operation.
4. If a clock is input (negative edge trigger) to the CK pin during C_T charging, C switches from charging to discharge.
5. Discharge switches to charging when C_T voltage drops to a certain threshold value (\approx 0.2V). Steps 4 and 5 are repeated while a normal clock is input from the logic system.
6. Output goes to reset state ($\overline{\text{RESET}}$ goes low) when the clock ceases and C_T voltage reaches reset ON threshold value (\approx 1.4V).
The formula for C_T charging time (T_{WD} : watchdog timer monitoring time) until reset is output is as follows.
 $T_{WD} \text{ (mS)} \approx 2500 \times C_T \text{ (}\mu\text{F)}$
7. Watchdog timer reset time T_{WR} is the discharge time until C_T voltage drops to reset OFF threshold value (\approx 0.2V). The formula is as follows.
 $T_{WR} \text{ (mS)} \approx 100 \times C_T \text{ (}\mu\text{F)}$
After reset OFF threshold value is reached, output reset is released and C_T starts charging. Thereafter, steps 4 and 5 are repeated if a normal clock is input, and when the clock ceases, 6 and 7 are repeated.
8. Reset is output when V_{CC} drops to V_{SL} (MM1096A \approx 3.2V, MM1096B \approx 4.2V). C_T is charged simultaneously.
9. C_T charging starts when V_{CC} rises to V_{SH} .
When V_{CC} drops momentarily, C_T charging begins after the charge is first discharged, if the time from V_{CC} dropping below V_{SL} until it rises to V_{SH} is longer than the V_{CC} input pulse width standard value T_{PI} .
10. Output reset is released after V_{CC} goes above V_{SH} and after T_{PR} , and the watchdog timer starts. Thereafter, 8~10 are repeated when V_{CC} goes below V_{SL} .
11. When power is OFF, reset is output if V_{CC} goes below V_{SL} .
12. When V_{CC} drops to 0V, reset output is held until V_{CC} reaches 0.8V.