

System Reset (with built-in watchdog timer) Monolithic IC MM1145

Outline

This IC has a built-in watchdog timer, with 2 channels for a clock monitoring function that monitors the microcomputer and outputs an intermittent reset signal if the microcomputer runs wild. Also, it has a power supply voltage monitoring function (system reset function) which generates a reset signal if power supply voltage is momentarily interrupted or drops, and performs power ON reset during normal power supply recovery and when power is turned on.

Features

1. Built-in edge trigger input watchdog timer
2. 2 clock pulse monitoring
3. Power ON reset time (T_{PR}) and watchdog timer monitoring time (T_{WD}) can be set individually with external elements (R, C)
4. Excellent watchdog timer monitoring time (T_{WD}) precision
 A type : $\pm 20\%$
 B type : $\pm 30\%$
5. Watchdog function stop pin allows use as system reset IC
6. Accurate power supply voltage drop detection
 4.2V $\pm 3.5\%$
7. Detection voltage has hysteresis
 100mV typ. $\pm 0.14\%/^{\circ}\text{C}$
8. Low reset minimum voltage
9. Low current consumption
 150 μA typ.

Package

SOP-8C (MM1145AF, MM1145BF)

Applications

Voltage detection for CPUs, microcomputers, etc. and clock pulse monitoring

Series Table

Model	V_{SL}	T_{PR}	T_{WA}	T_{WR}
MM1145A	4.2	100mS	50mS	10mS
MM1145B		40mS	110mS	10mS

* $C_T=0.02\mu\text{F}$, $R_{CT}=1\text{M}\Omega$

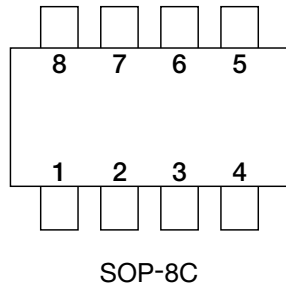
V_{SL} : Reset detection voltage

T_{PR} : Reset hold time during V_{CC} rise

T_{WD} : Watchdog timer monitoring time

T_{WR} : Reset time

Pin Assignment

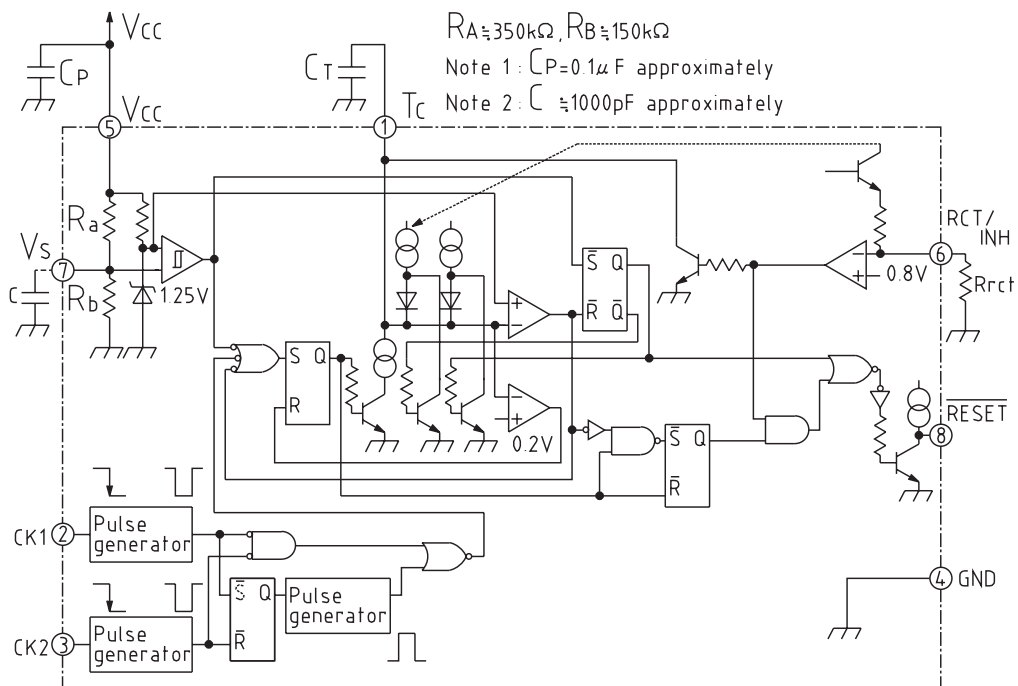


1	TC
2	CK1
3	CK2
4	GND
5	V _{CC}
6	RCT
7	V _S
8	$\overline{\text{RESET}}$

Pin Description

Pin No.	Pin name	Function
1	TC	T _{WD} , T _{WR} , T _{PR} time setting pins. Time determined by external capacitor.
2	CK1	Clock input pin 1 Clock input from logic system
3	CK2	Clock input pin 2 Clock input from logic system
4	GND	GND pin
5	V _{CC}	Power supply pin Detection voltage 4.2V
6	RCT	Watchdog timer stop pin and T _{WD} adjustment pin Operation modes : Operation → V _{CC} , Stop → GND T _{WD} time determined by external resistor R _{RCT} and C _T
7	V _S	Detection voltage adjustment pin
8	$\overline{\text{RESET}}$	Reset output pin (low output)

Block Diagram





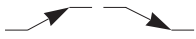
Absolute Maximum Ratings

Item	Symbol	Rating	Units
Power supply voltage	V _{CC max.}	-0.3~+7.5	V
CK pin input voltage	V _{CK}	-0.3~V _{CC} +0.3 (≤ +7.5)	V
VS pin input voltage	V _{VS}	-0.3~V _{CC} +0.3 (≤ +7.5)	V
Voltage applied to RCT pin	V _{RCT}	-0.3~V _{CC} +0.3 (≤ +7.5)	V
Voltage applied to RESET pin	V _{OH}	-0.3~V _{CC} +0.3 (≤ +7.5)	V
Allowable loss	P _d	300	mW
Storage temperature	T _{STG}	-40~+125	°C

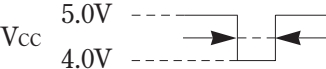
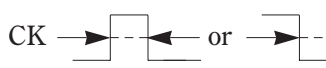
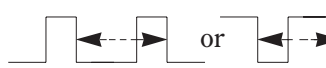
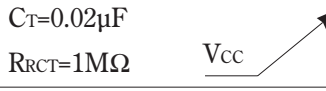
Recommended Operating Conditions

Item	Symbol	Rating	Units
Power supply voltage	V _{CC}	+2.2~+7.0	V
RESET sync current	I _{OL}	0~4.0	mA
Clock monitoring time setting	T _{WD}	1.95~10000	mS
Power supply voltage rise and fall times	t _{rv} , t _{rf}	<300	μS
Clock rise and fall times	t _{rc} , t _{fc}	<100	μS
C _T pin capacitance	C _T	0.002~2	μF
RCT pin resistance	R _{rct}	0.39~2	MΩ
Operating temperature	T _{OP}	-25~+75	°C

Electrical Characteristics (DC) (Except where noted otherwise, T_a=25°C, V_{CC}=5.0V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units		
Consumption current	I _{CC}	During watchdog timer operation		150	180	μA		
Detection voltage	V _{SL}	V _S =OPEN, V _{CC} 	4.05	4.20	4.35	V		
	V _{SH}	V _S =OPEN, V _{CC} 	4.15	4.30	4.45			
Detection voltage temperature coefficient	$\frac{V_S}{\Delta T}$	V _{SH} -V _{SL} , V _{CC} 		±0.01		%/°C		
Hysteresis voltage	V _{HYS}		50	100	150	mV		
CK input threshold	V _{TH}		0.8	1.2	2	V		
CK input current	I _{IH}	V _{CK} =5.0V		0	1	μA		
	I _{IL}	V _{CK} =0V	-14.5	-8.5	-4.5			
Output voltage (High)	V _{OH}	I _{RESET} = -1μA, V _S =OPEN	4.0	4.5		V		
Output voltage (Low)	V _{OL1}	I _{RESET} = 0.5mA, V _S =0V		0.10	0.20	V		
	V _{OL2}	I _{RESET} = 2.0mA, V _S =0V		0.15	0.35			
Output sync current	I _{OL}	V _{RESET} = 1.0V, V _S =0V	2	4		mA		
C _T charge current	MM1145A	I _{CT1}	During watchdog timer operation		-0.40	-0.48	-0.60	μA
					-0.17	-0.22	-0.30	
	MM1145B	I _{CT2}	During power ON reset operation		-0.21	-0.31	-0.62	μA
					-0.62	-0.93	-2.33	
Minimum operating power supply voltage to ensure RESET	V _{CCL}	V _{RESET} = 0.4V I _{RESET} = 0.1mA		0.8	1.0	V		

Electrical Characteristics (DC) (Except where noted otherwise, Ta=25°C, Vcc=5.0V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
V _{CC} input pulse width	T _{PI}	V _{CC} 	8			μS
CK input pulse width	T _{CKW1} T _{CKW2}	CK 	3			μS
CK input cycle *7	T _{CK1} T _{CK2}		200			μS
Watchdog timer monitoring time *1	MM1145A	C _T =0.02μF, R _{RCT} =1MΩ	40	50	60	mS
	MM1145B		80	110	140	
Watchdog timer reset time *2	MM1145A	C _T =0.02μF, R _{RCT} =1MΩ	5	10	15	mS
	MM1145B		5	10	15	
Reset hold time for power supply rise *3	MM1145A	C _T =0.02μF R _{RCT} =1MΩ 	50	100	150	mS
	MM1145B		20	40	60	
Output delay time from V _{CC} *4	T _{PD}	RESET pin, R _L =10kΩ, C _L =20pF		2	10	μS
Output rise time *5	t _r	RESET pin, R _L =10kΩ, C _L =20pF		2.0	4.0	μS
Output fall time *5	t _f	RESET pin, R _L =10kΩ, C _L =20pF		0.2	1.0	μS

Notes:

*1 Monitoring time is the time from the last pulse (negative edge) of the timer clear clock pulse until reset pulse output.

In other words, reset output is output if a clock pulse is not input during this time.

*2 Reset time means reset pulse width. However, this does not apply to power ON reset.

*3 Reset hold time is the time from when V_{CC} exceeds detection voltage (V_{SHR}) during power ON reset until reset release (RESET output high).

*4 Output delay time is the time from when power supply voltage drops below detection voltage (V_{SL}) until reset state occurs (RESET output low).

*5 The voltage range when measuring output rise and fall time is 10~90%.

*7 1 Set CK1 and CK2 input cycles within the following range.

$$T_{CK1} \leq nT_{CK2} < T_{WD} \text{ (mS)} \text{ (} n \leq 1 \text{)}$$

RESET output may go low even if CK1 and CK2 are input without these conditions being met.

(Recommended use is for T_{CK1} ≤ nT_{CK2})

2 T_{CK1}, T_{CK2} ≤ 200 μS results in the following operation.

Discharge switches to charging with the CK2 pulse (negative edge) that inputs 200μS after C_T switches from charging to discharge by the CK2 pulse (negative edge). RESET output stays high while this operation is being repeated. (However, T_{CK1}, T_{CK2} ≥ 20μS.)

Formula for C_T Pin External Constant

Watchdog timer monitoring time (T_{WD}), watchdog timer reset time (T_{WR}) and reset hold time (T_{PR}) during power supply rise can be changed by varying C_T capacitance. T_{WD} also can be changed with R_{RCT}.

The variable times are expressed by the following.

1. MM1145A

$$T_{PR} \text{ (mS)} \approx 5000 \times C_T \text{ (}\mu\text{F)}$$

$$T_{WD} \text{ (mS)} \approx 2500 \times C_T \text{ (}\mu\text{F)} \times R_{RCT} \text{ (M}\Omega\text{)}$$

$$T_{WR} \text{ (mS)} \approx 500 \times C_T \text{ (}\mu\text{F)}$$

Example : when C_T=0.02μF, R_{RCT}=1MΩ

$$T_{PR} \approx 100\text{mS}$$

$$T_{WD} \approx 50\text{mS}$$

$$T_{WR} \approx 10\text{mS}$$

2. MM1145B

$$T_{PR} \text{ (mS)} \approx 2000 \times C_T \text{ (}\mu\text{F)}$$

$$T_{WD} \text{ (mS)} \approx 5500 \times C_T \text{ (}\mu\text{F)} \times R_{RCT} \text{ (M}\Omega\text{)}$$

$$T_{WR} \text{ (mS)} \approx 500 \times C_T \text{ (}\mu\text{F)}$$

Example : when C_T=0.02μF, R_{RCT}=1MΩ

$$T_{PR} \approx 40\text{mS}$$

$$T_{WD} \approx 110\text{mS}$$

$$T_{WR} \approx 10\text{mS}$$

Formula for Watchdog Timer Monitoring Time (T_{WD}) Adjustment

The ratio between T_{PR} and T_{WD} can be changed within the range below by adjusting T_{WD} with R_{RCT}.

1. MM1145A

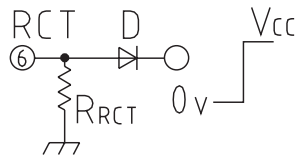
$$T_{WD}/T_{PR} \approx 2.0 \times R_{RCT} \text{ (}0.39 \text{ (M}\Omega\text{)} \leq R_{RCT} \leq 2 \text{ (M}\Omega\text{))}$$

2. MM1145B

$$T_{WD}/T_{PR} \approx 2.75 \times R_{RCT} \text{ (}0.39 \text{ (M}\Omega\text{)} \leq R_{RCT} \leq 2 \text{ (M}\Omega\text{))}$$

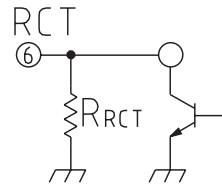
How to Use RCT Pin

Example 1



1. Watchdog timer operates when RCT pin is open.
2. Watchdog timer stops operating when RCT pin is connected to ground.

Example 2



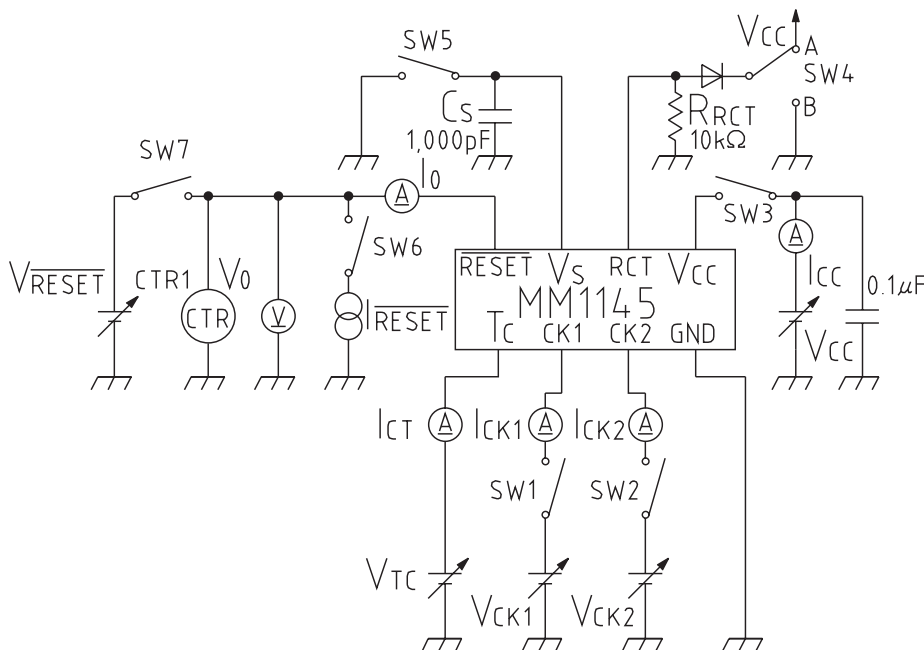
Description of Operation

1. $\overline{\text{RESET}}$ goes low when V_{CC} rises to approximately 0.8V.
Approximately 1μA (V_{CC}=0.8V) of pull up current is output from RESET.
2. Capacitor C_T charging starts when V_{CC} rises to V_{SH} (≈ 4.3V). Output is in reset state at this time.
3. Output reset is released ($\overline{\text{RESET}}$ goes high) after a certain time (T_{PR}), from when C_T starts charging until discharge (the time from when C_T voltage reaches a certain threshold value VT1 (≈ 1.4V) until C_T voltage drops to a certain threshold value VT2 (≈ 0.2V).
Reset hold time : T_{PR} is as follows.
T_{PR} (mS) ≈ 5000 × C_T (μF)
C_T charging starts again after reset release, and watchdog timer operation begins.
Clock input during power ON reset time (T_{PR}) will cause mis-operation.
4. If CK1 and CK2 are input in that order (or simultaneously) during C_T charging, CK2 negative edge trigger causes the TC pin to switch from charging to discharge.
5. Discharge switches to charging when C_T voltage drops to threshold value VT2 (≈ 0.2V). Steps 4 and 5 are repeated while a normal clock is input from the logic system.

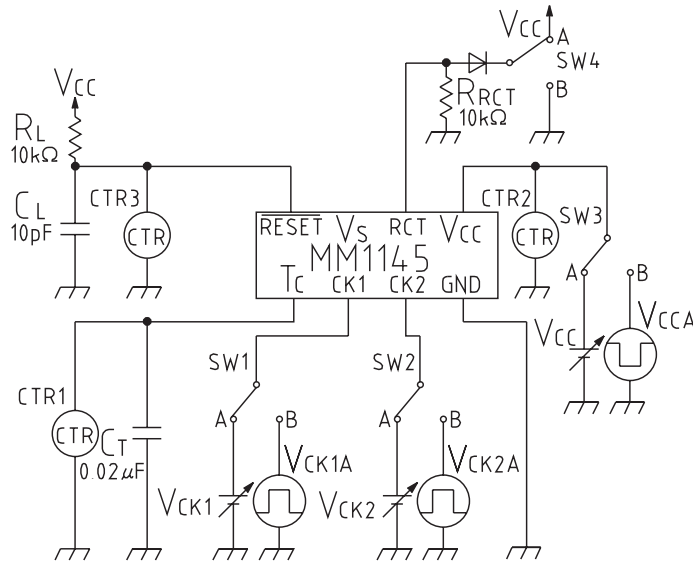
6. Operation is as follows if either clock CK1 or CK2 ceases (the figure shows CK1).
 Output goes to reset state ($\overline{\text{RESET}}$ goes low) when C_T voltage reaches reset ON threshold value V_{T1} ($\approx 1.4V$).
 The formula for C_T charging time (T_{WD} : watchdog timer monitoring time) until reset is output is as follows.
 $T_{WD} \text{ (mS)} \approx 2500 \times C_T \text{ (\mu F)}$
7. Watchdog timer reset time T_{WR} is the discharge time until C_T voltage drops to reset OFF threshold value V_{T2} from reset ON threshold value V_{T1} . The formula is as follows.
 $T_{WR} \text{ (mS)} \approx 500 \times C_T \text{ (\mu F)}$
 After reset OFF threshold value is reached, output reset is released and C_T starts charging. Thereafter, steps 4 and 5 are repeated if a normal clock is input, and when one of the clocks ceases, 6 and 7 are repeated.
 In the same way, 6 and 7 are repeated if both clocks CK1 and CK2 cease.
8. Reset is output when V_{CC} drops to V_{SL} ($\approx 4.2V$). C_T is charged simultaneously.
9. C_T charging starts when V_{CC} rises to V_{SH} .
 When V_{CC} drops momentarily, C_T charging begins after the charge is first discharged, if the time from V_{CC} dropping below V_{SL} until it rises to V_{SH} is longer than the V_{CC} input pulse width standard value T_{PI} .
10. Output reset is released after V_{CC} goes above V_{SH} and after T_{PR} , and the watchdog timer starts.
11. Watchdog timer operation can be stopped by switching R_{CT} voltage from high to low. (Clocks CK1 and CK2 are invalid. Regardless of status, TC pin voltage discharges quickly and goes to 0V.) This operation can be applied from any timing. In this state the IC functions as a reset IC with power ON reset.
12. Watchdog timer operation re-starts when R_{CT} voltage switches to high.
13. When power is OFF, reset is output if V_{CC} goes below V_{SL} .
14. When V_{CC} drops to 0V, reset output is held until V_{CC} reaches 0.8V.

Measuring Circuit

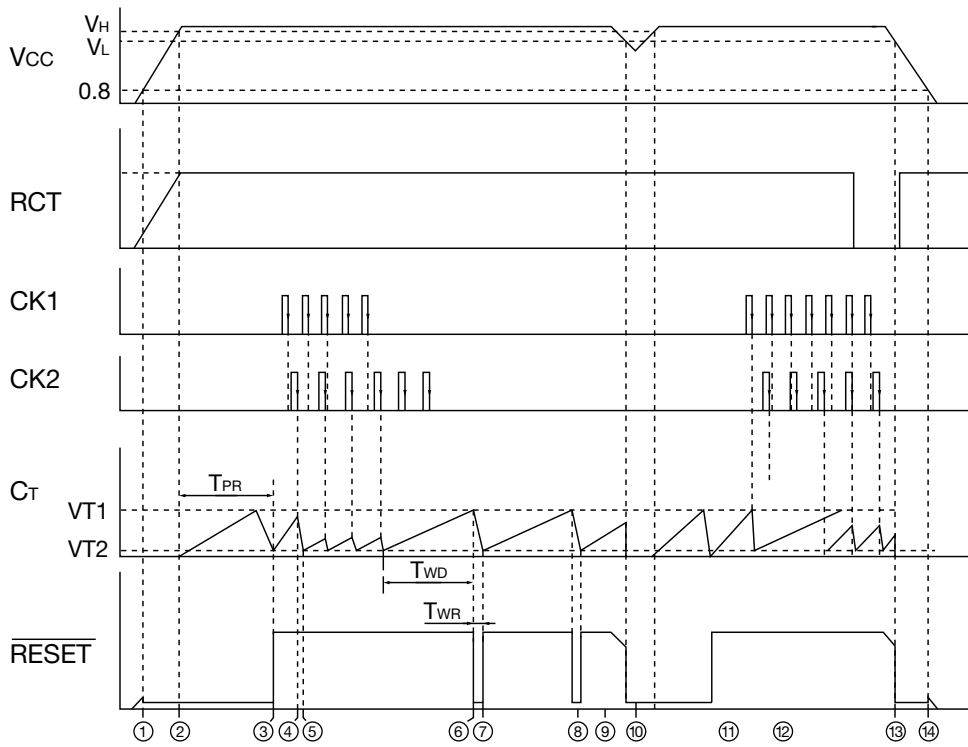
Measuring Circuit 1



Measuring Circuit 2



Timing Chart



Basic Circuit Diagram

