I^{2}C Bus Video Switch
Monolithic IC MM1250

Outline

This IC is an audio/video switch that supports an I^{2}C bus for television.

Features

1. Utilizes serial control by I^{2}C bus
2. 3 video input systems for 3 outputs, V$_{OUT}$, Y$_{OUT}$ and C$_{OUT}$
3. V$_{OUT}$ has built-in 6dB amp
4. V$_{OUT}$ has built-in output clamp circuit
5. Audio system has built-in mute function
6. 1 output port built-in
7. Operating power supply voltage range   8~13V
8. Video frequency response   10MHz
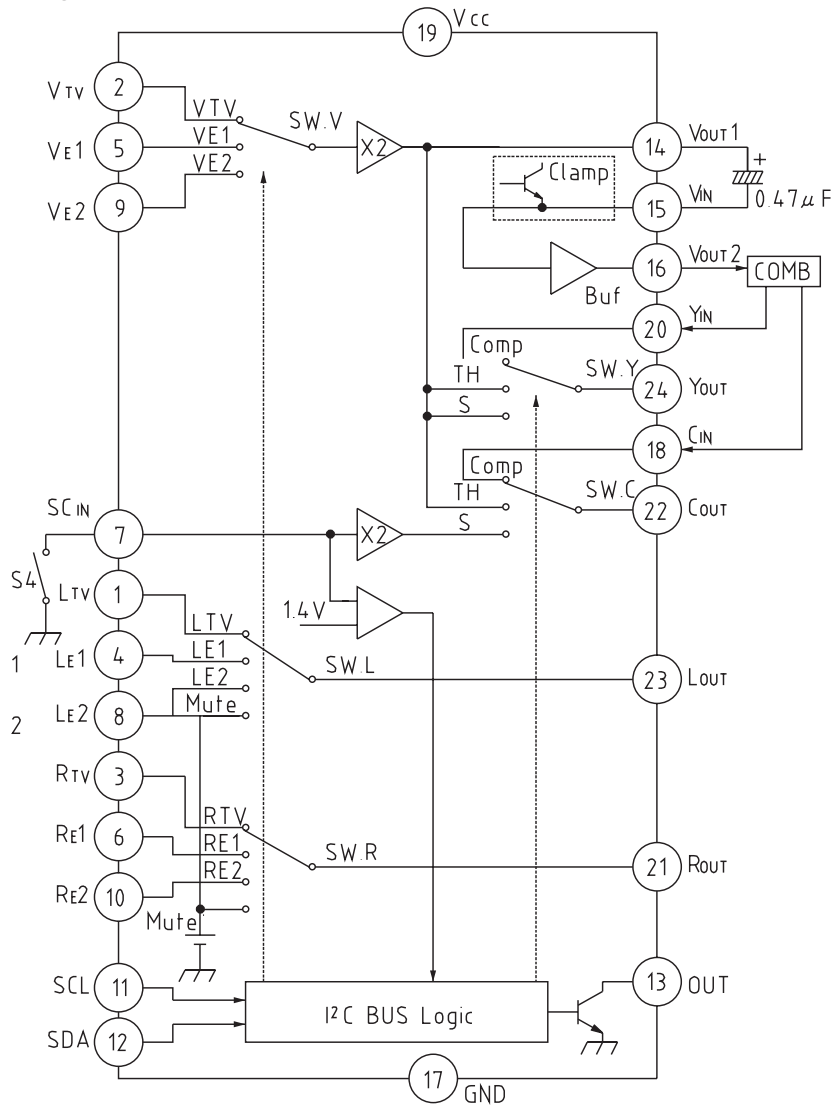9. Slave address   92H (fixed)

Package

SDIP-24A (MM1250XD)

Applications

I^{2}C bus televisions, etc.

Block Diagram

■ Fig. 1   Block Diagram

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	−40~+125	°C
Operating temperature	T_{OPR}	−20~+75	°C
Power supply voltage	V_{CC}	15	V
Allowable loss	Pd	1000	mW

Electrical Characteristics (Except where noted otherwise, Ta=25°C, Vcc=8V~13V)

Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units
Operating power supply voltage	V_{CC}	V_{CC}		8.0		13.0	V
Consumption current	I_{CC}		$V_{CC}=9V$	17	25	33	mA
V_{OUT} output							
Voltage gain	G_V1	TP9	SG1 : sine wave 1V_{P-P}, 0.1MHz	5.5	6.0	6.5	dB
	G_V2	TP7					
Frequency characteristic	F_V1	TP9	SG1 : sweep signal, 1V_{P-P} 10MHz/0.1MHz	−1.0	0	1.0	dB
	F_V2	TP7					
Differential gain	DG_V1	TP9	SG1 : staircase wave, 1V_{P-P} APL=10, 50, 90%	−3	0	3	%
	DG_V2	TP8					
Differential phase	DP_V1	TP9	SG1 : staircase wave, 1V_{P-P} APL=10, 50, 90%	−3	0	3	deg
	DP_V2	TP8					
Input dynamic	D_V1	TP9	SG1 : range sine wave, 1kHz	2.1			V_{P-P}
	D_V2	TP8					
Output offset voltage	V_{OFFV}	TP9	$V_{OUT}1$ pin DC level difference during switching		0	±30	mV
Input impedance	Z_{IV}		V_{TV}, V_E1, V_E2	10	15	20	kΩ
Output impedance	$Z_{OV}2$			10	20	30	Ω
Y_{OUT} output							
Voltage gain	G_Y1	TP1	SG1 : sine wave, 1V_{P-P}, 0.1MHz	5.5	6.0	6.5	dB
	G_Y2	TP1	SG6 : sine wave, 2V_{P-P}, 0.1MHz	−0.5	0	0.5	dB
Frequency characteristic	F_Y1	TP1	SG1 : sweep signal, 1V_{P-P} 10MHz/0.1MHz	−1.0	0	1.0	dB
	F_Y2	TP1	SG6 : sweep signal, 2V_{P-P} 10MHz/0.1MHz	−1.0	0	1.0	dB
Differential gain	DG_Y	TP2	SG1 : staircase wave, 1V_{P-P} APL=10, 50, 90%	−3	0	3	%
Differential phase	DP_Y	TP2	SG1 : staircase wave, 1V_{P-P} APL=10, 50, 90%	−3	0	3	deg
Input dynamic range	D_Y1	TP1	SG6 : sine wave, 1kHz, Comp mode	4.2			V_{P-P}
	D_Y2	TP1	SG1 : sine wave, 1kHz, TH·S mode	2.1			
Output offset voltage	V_{OFFY}	TP1	$Y_{OUT}1$ pin DC level difference during switching		0	±30	mV
Input impedance	Z_{IY}		Y_{IN}	10	15	20	kΩ
Output impedance	Z_{OY}			8	15	22	Ω
C_{OUT} output							
Voltage gain	G_C1	TP4	SG1 : sine wave, 1V_{P-P}, 0.1MHz	5.5	6.0	6.5	dB
	G_C2	TP4	SG2 : sine wave, 1V_{P-P}, 0.1MHz	5.5	6.0	6.5	dB
	G_C3	TP4	SG5 : sine wave, 2V_{P-P}, 0.1MHz	−0.5	0	0.5	dB
Frequency characteristic	F_C1	TP4	SG1 : sweep signal, 1V_{P-P}, 10MHz/0.1MHz	−1.0	0	1.0	dB
	F_C2	TP4	SG2 : sweep signal, 1V_{P-P}, 10MHz/0.1MHz	−1.0	0	1.0	dB
	F_C3	TP4	SG5 : sweep signal, 2V_{P-P}, 10MHz/0.1MHz	−1.0	0	1.0	dB
Differential gain	DG_C	TP5	SG1 : staircase wave, 1V_{P-P} APL=10, 50, 90%	−3	0	3	%
Differential phase	DP_C	TP5	SG1 : staircase wave, 1V_{P-P} APL=10, 50, 90%	−3	0	3	deg
Input dynamic range	D_C1	TP4	SG5 : sine wave, 1kHz, COMP mode	4.2			V_{P-P}
	D_C2	TP4	SG1 : sine wave, 1kHz, TH mode	2.1			
	D_C3	TP4	SG2 : sine wave, 1kHz, S mode	2.1			
Output offset voltage	V_{OFFC}	TP4	$C_{OUT}1$ pin DC level difference during switching		0	±30	mV
Input impedance	Z_{IC}		C_{IN}	10	15	20	kΩ
Output impedance	Z_{OC}			8	15	22	Ω

Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units
R_{OUT} output							
Voltage gain	G_R	TP6	sine wave, 2.5V_{P-P}, 1kHz	−0.5	0	0.5	dB
Total harmonic distortion	THD_R	TP6	sine wave, 2.5V_{P-P}, 1kHz		0.01	0.1	%
Output noise voltage	V_{NR}	TP6	band 15kHz (except during mute)		3	30	μVrms
Mute noise	V_{M1}	TP6	during mute		200	600	μVrms
Input dynamic range	D_R	TP6	SG3 : sine wave, 1kHz, total higher harmonic distortion rate=0.5%	2.0			Vrms
Output offset voltage	V_{OFFR}	TP6	R_{OUT} pin DC level difference during switching		0	±15	mV
Input impedance	$Z_{IR}1$		R_{TV}	22	30	38	kΩ
	$Z_{IR}2$		R_E1, R_E2	50	68	86	kΩ
Output impedance	Z_{OR}			60	80	100	Ω
L_{OUT} output							
Voltage gain	G_L	TP3	sine wave, 2.5V_{P-P}, 1kHz	−0.5	0	0.5	dB
Total harmonic distortion	THD_L	TP3	sine wave, 2.5V_{P-P}, 1kHz		0.01	0.1	%
Output noise voltage	V_{NL}	TP3	band 15kHz (except during mute)		3	50	μVrms
Mute noise	V_{M2}	TP3	during mute		200	600	μVrms
Input dynamic range	D_L	TP3	SG3 : sine wave, 1kHz, total higher harmonic distortion rate=0.5%	2.0			Vrms
Output offset voltage	V_{OFFL}	TP3	Lout pin DC level difference during switching		0	±15	mV
Input impedance	$Z_{IL}1$		L_{TV}	22	30	38	kΩ
	$Z_{IL}2$		L_E1, L_E2	50	68	86	kΩ
Output impedance	Z_{OL}			60	80	100	Ω
OUT output							
Output voltage L	V_{OL}	TP10	Bit4=0			0.4	V
Crosstalk							
V_{OUT}2	CT_V	TP7	4.43MHz ＊1		−70	−60	dB
Y_{OUT}	CT_Y	TP1	4.43MHz ＊2		−70	−60	dB
C_{OUT}	CT_C	TP4	4.43MHz ＊3		−70	−60	dB
R_{OUT}	CT_R	TP6	2.5V_{P-P}, 1kHz		−80	−70	dB
L_{OUT}	CT_L	TP3	2.5V_{P-P}, 1kHz		−80	−70	dB
Pin DC voltage							
1 pin voltage	Vt1		Vcc=9.0V, SG1~6=no signal	4.8	5.3	5.8	V
2 pin voltage	Vt2		Vcc=9.0V, SG1~6=no signal	4.1	4.6	5.1	V
3 pin voltage	Vt3		Vcc=9.0V, SG1~6=no signal	4.8	5.3	5.8	V
4 pin voltage	Vt4		Vcc=9.0V, SG1~6=no signal	4.8	5.3	5.8	V
5 pin voltage	Vt5		Vcc=9.0V, SG1~6=no signal	4.1	4.6	5.1	V
6 pin voltage	Vt6		Vcc=9.0V, SG1~6=no signal	4.8	5.3	5.8	V
7 pin voltage	Vt7		Vcc=9.0V, SG1~6=no signal, S4=B	4.1	4.6	5.1	V
8 pin voltage	Vt8		Vcc=9.0V, SG1~6=no signal	4.8	5.3	5.8	V
9 pin voltage	Vt9		Vcc=9.0V, SG1~6=no signal	4.1	4.6	5.1	V
10 pin voltage	Vt10		Vcc=9.0V, SG1~6=no signal	4.8	5.3	5.8	V
11 pin voltage	Vt13		Vcc=9.0V, SG1~6=no signal, BIT4=0		0.2	0.4	V
12 pin voltage	Vt14		Vcc=9.0V, SG1~6=no signal	4.1	4.6	5.1	V
13 pin voltage	Vt15		Vcc=9.0V, SG1~6=no signal	3.5	4.0	4.5	V
14 pin voltage	Vt16		Vcc=9.0V, SG1~6=no signal	2.1	2.6	3.1	V
15 pin voltage	Vt17		Vcc=9.0V, SG1~6=no signal		0		V
16 pin voltage	Vt18		Vcc=9.0V, SG1~6=no signal	4.1	4.6	5.1	V
17 pin voltage	Vt19		Vcc=9.0V, SG1~6=no signal		9		V
18 pin voltage	Vt20		Vcc=9.0V, SG1~6=no signal	4.1	4.6	5.1	V
19 pin voltage	Vt21		Vcc=9.0V, SG1~6=no signal	4.1	4.6	5.1	V
20 pin voltage	Vt22		Vcc=9.0V, SG1~6=no signal	3.4	3.9	4.4	V
21 pin voltage	Vt23		Vcc=9.0V, SG1~6=no signal	4.1	4.6	5.1	V
22 pin voltage	Vt24		Vcc=9.0V, SG1~6=no signal	3.4	3.9	4.4	V

I²C Bus Recommended Operating Conditions (Refer to diagram below)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Input voltage L	V_{IL}	I²C logic low level discrimination value			0.7	V
Input voltage H	V_{IH}	I²C logic high level discrimination value	2.1		5.0	V
Clock frequency	f_{SCL}				100	kHz
Data transfer wait time	t_{BUF}		4.7			µS
SCL start hold time	$t_{HD:STA}$		4.0			µS
SCL low level hold time	t_{LOW}		4.7			µS
SCL high level hold time	t_{HIGH}		4.0			µS
SCL start setup time	$t_{SU:STA}$		4.7			µS
SDA data hold time	$t_{HD:DAT}$		5.0			µS
SDA data setup time	$t_{SU:DAT}$		250			µS
SCL rise time	t_R				1000	nS
SCL fall time	t_F				300	nS
SCL stop setup time	$t_{SU:STO}$		4.0			µS

Notes :
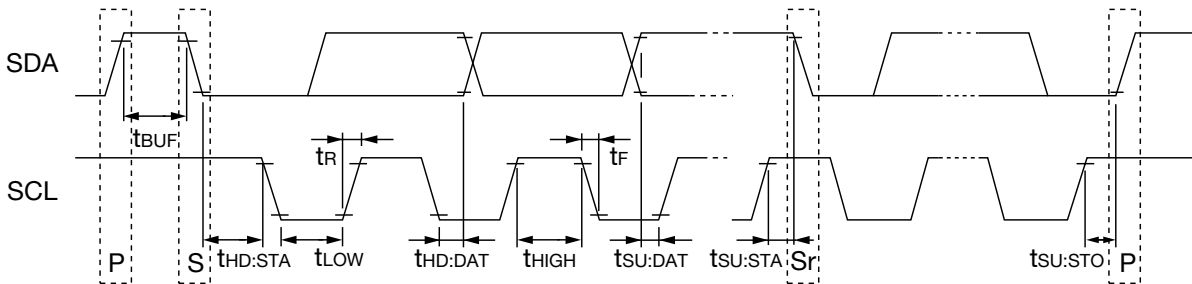
*1   Crosstalk $V_{OUT}2$

Input a $1V_{P-P}$, 4.43MHz sine wave to SG1.

Given S1=A, S5=A, S6~S10= B, Bit=011 and TP7 amplitude V01,

Combinations below : V02, then C_{TV} is obtained as follows:

$$C_{TV}=20\log (V02/V01) \text{ dB}$$

I²C Bus control signals

Signal input	Input amplitude	Switch status								Control bit		
		S1	S4	S5	S6	S7	S8	S9	S10	Bit2	Bit1	Bit0
SG1	$1V_{P-P}$	A	A	A	B	B	B	B	B	–	0	1
			B	A	B	B	B	B	B			
			–	A	B	B	B	B	B	–	1	0
		B	–	B	A	B	B	B	B	–	1	1
			–	B	A	B	B	B	B	–	1	0
			–	B	B	B	A	B	B	–	1	1
		C	A	B	B	B	A	B	B	–	0	1
			B	B	B	B	A	B	B			
SG6	$2V_{P-P}$	–	–	B	B	B	B	B	A	–	1	1
SG5	$2V_{P-P}$	–	–	B	B	B	B	A	B	–	1	1
SG2	$1V_{P-P}$	–	B	B	B	A	B	B	B	–	0	1

*2   Crosstalk Y$_{OUT}$

Input a 1V$_{P–P}$, 4.43MHz sine wave to SG1.

Given S1=A, S5=A, S6~S10=B, Bit=111 and TP1 amplitude V03,

Combinations below : V04, then Cty is obtained as follows:

$$C_{TY} = 20\log (V04/V03) \text{ dB}$$

Signal input	Input amplitude	Switch status								Control bit		
		S1	S4	S5	S6	S7	S8	S9	S10	Bit2	Bit1	Bit0
SG1	1V$_{P-P}$	A	–	A	B	B	B	B	B	0	1	1
SG6	2V$_{P-P}$	–	B	B	B	B	B	B	A	0	0	1
			–	B	B	B	B	B	A	1	1	1
SG5	2V$_{P-P}$	–	–	B	B	B	B	A	B	–	1	1
SG2	1V$_{P-P}$	–	–	B	B	A	B	B	B	–	1	1

*3   Crosstalk C$_{OUT}$

Input a 1V$_{P–P}$, 4.43MHz sine wave to SG1.

Given S1=A, S5=A, S6~S10=B, Bit=111 and TP5 amplitude V05,

Combinations below : V06, then C$_{TC}$ is obtained as follows:

$$C_{TC} = 20\log (V06/V05) \text{ dB}$$

Signal input	Input amplitude	Switch status								Control bit		
		S1	S4	S5	S6	S7	S8	S9	S10	Bit2	Bit1	Bit0
SG1	1V$_{P-P}$	A	–	A	B	B	B	B	B	0	1	1
		B	B	B	A	B	B	B	B	–	0	1
SG6	2V$_{P-P}$	–	–	B	B	B	B	B	A	–	1	1
			B	B	B	B	B	B	A	–	0	1
SG5	2V$_{P-P}$	–	B	B	B	B	B	A	B	–	0	1
			–	B	B	B	B	A	B	1	1	1
SG2	1V$_{P-P}$	–	–	B	B	A	B	B	B	–	1	1

I²C Bus

S:Start Condition
P:Stop Condition
ACK:Acknowledge
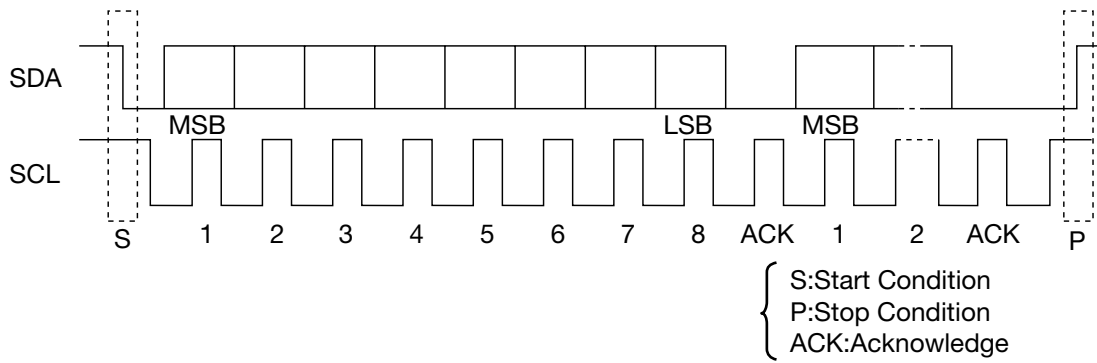
The I²C bus (Inter IC Bus) is a bus system developed by Philips.
Data is transferred on two lines, SDA and SCL.
Data is transferred in byte units, and MSB is first from start condition.

1. Data format

S	Slave address							R/W	A	Control bits								A	P
	1	0	0	1	0	0	1	0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		

Address byte — Control byte

The first 7 bits of the address byte is the salve address, and the last bit is allocated as R/W bit. On
MM1250XD, 92_H is used for the slave address and 0 (write only) for the R/W bit.
The A at the 9th bit is an acknowledge signal added for verification from slave.

2. Control byte format

Control byte configuration on MM1250XD is allocated as shown in the table below.
Each bit is set at "0" when power is turned on.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
×	×	×	OUT	Mute	SW2	SW1	SW0

×: Don't Care

SW V, L, R control

Control		Control results			
SW1	SW0	MODE1	V_{OUT}	L_{OUT}	R_{OUT}
0	0	TV	V_{TV}	L_{TV}	R_{TV}
0	1	E1	V_{E1}	L_{E1}	R_{E1}
1	0	E2	V_{E2}	L_{E2}	R_{E2}
1	1	TV	V_{TV}	L_{TV}	R_{TV}

SW Y, C control

Control			Control results		
MODE1	S4	SW2	Mode2	SW·Y	SW·C
TV	–	0	Comp	Y_{IN}	C_{IN}
E1	A	0	Comp	Y_{IN}	C_{IN}
	B	0	S	V_{E1}	S_{CIN}
E2	–	0	Comp	Y_{IN}	C_{IN}
TV	–	1	TH	V_{TV}	V_{TV}
E1	A	1	TH	V_{E1}	V_{E1}
	B	1	S	V_{E1}	S_{CIN}
E2	–	1	TH	V_{E2}	V_{E2}

Audio Mute control

Mute	L_{OUT}	R_{OUT}
0	SW·L	SW·R
1	Mute	Mute

Out Port control

OUT	Pin 13 status
0	Low
1	Open

Pin Description

Pin no.	Pin name	Internal equivalent circuit diagram	Pin no.	Pin name	Internal equivalent circuit diagram
1 3	L_{TV} R_{TV}	Vcc 30k　220	14	$V_{OUT}1$	Vcc 220 7.5k 4.4k　200
2 5 7 9 18 20	V_{TV} V_E1 SC_{IN} V_E2 C_{IN} Y_{IN}	Vcc 15k　220	15	V_{IN}	Vcc 33k　　220
4 6 8 10	L_E1 R_E1 L_E2 R_E2	Vcc 68k　220	16	$V_{OUT}2$	Vcc 220 3.3k　200
11	SCL		17	GND	
			19	V_{CC}	
			21 23	R_{OUT} L_{OUT}	Vcc 2.2k　280
12	SDA				
13	OUT		22 24	C_{OUT} Y_{OUT}	Vcc 220 5.5k　200

Measuring Circuit