May 1997

Micro Linear

ML2111*

Universal Dual High Frequency Filter

GENERAL DESCRIPTION

The ML2111 consists of two independent switched capacitor filters that operate at up to 150kHz and perform second order filter functions such as lowpass, bandpass, highpass, notch and allpass. All filter configurations, including Butterworth, Bessel, Cauer, and Chebyshev can be formed.

The center frequency of these filters is tuned by an external clock or the external clock and resistor ratio.

The ML2111 frequency range is specified up to 150kHz with ±5.0V ±10% power supplies. Using a single 5.0V ±10% power supply the frequency range is up to 100kHz. These filters are ideal where center frequency accuracy and high Qs are needed.

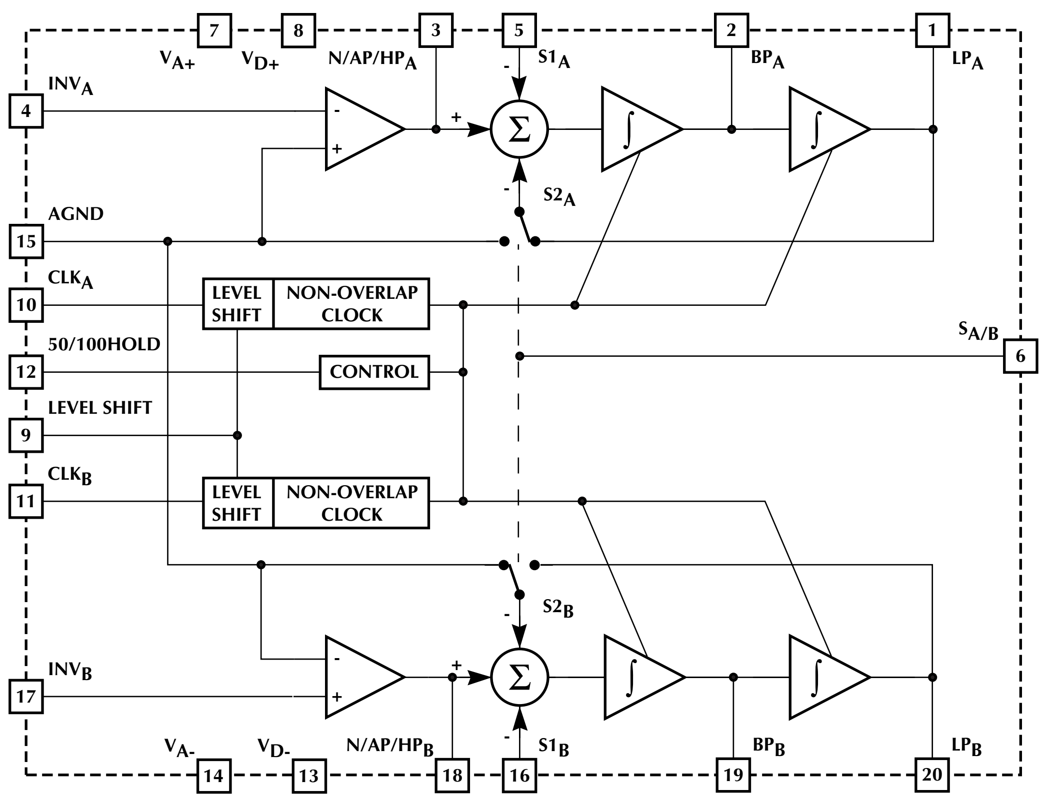
The ML2111 is a pin compatible superior replacement for MF10, LMF100, and LTC1060 filters.

FEATURES

- Specified for operation up to 150kHz
- Center frequency x Q product ≤ 5MHz
- Separate highpass, notch, allpass, bandpass, and lowpass outputs
- Center frequency accuracy of ±0.4% or ±0.8% max.
- Q accuracy of ±4% or ±8% max.
- Clock inputs are TTL or CMOS compatible
- Single 5V (±2.25V) or ±5V supply operation

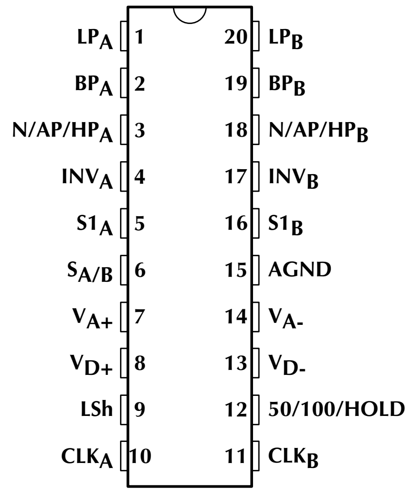
* Some Packages Are End Of Life and Obsolete

BLOCK DIAGRAM



PIN CONFIGURATION

ML2111
20-Pin PDIP (P20)
20-Pin SOIC (S20)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	LP_A	Lowpass output for biquad A.
2	BP_A	Bandpass output for biquad A.
3	$N/AP/HP_A$	Notch/allpass/highpass output for biquad A.
4	INV_A	Inverting input of the summing op amp for biquad A.
5	$S1_A$	Auxiliary signal input pin used in modes 1a, 1d, 4, 5, and 6b.
6	$S_{A/B}$	Controls S2 input function.
7	V_{A+}	Positive analog supply.
8	V_{D+}	Positive digital supply.
9	LSh	Reference point for clock input levels. Logic threshold typically 1.4V above LSh voltage.
10	CLK_A	Clock input for biquad A.
11	CLK_B	Clock input for biquad B.
12	50/100/HOLD	Input pin to control the clock-to-center-frequency ratio of 50:1 or 100:1, or to stop the clock to hold the last sample of the bandpass or lowpass outputs.
13	V_{D-}	Negative digital supply.
14	V_{A-}	Negative analog supply.
15	AGND	Analog ground.
16	$S1_B$	Auxiliary signal input pin used in modes 1a, 1d, 4, 5, and 6b.
17	INV_B	Inverting input of the summing op amp for biquad B.
18	$N/AP/HP_B$	Notch/allpass/highpass output for biquad B.
19	BP_B	Bandpass output for biquad B.
20	LP_B	Lowpass output for biquad B.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage
- $|V_{A+}|$, $|V_{D+}|$ - $|V_{A-}|$, $|V_{D-}|$ 13V
- V_{A+}, V_{D+} to LSh 13V

Inputs .... $|V_{A+}, V_{D+}|$ +0.3V to $|V_{A-}, V_{D-}|$ -0.3V
Outputs .... $|V_{A+}, V_{D+}|$ +0.3V to $|V_{A-}, V_{D-}|$ -0.3V
$|V_{A+}|$ to $|V_{D+}|$ .... ±0.3V
Junction Temperature 150ºC
Storage Temperature Range .... –65ºC to 150ºC

Lead Temperature (Soldering, 10 sec) 300ºC
Thermal Resistance (θ_{JA})
- 20-Pin PDIP 67ºC/W
- 20-Pin SOIC 95ºC/W

OPERATING CONDITIONS

Temperature Range
- ML2111CCX .... 0ºC to 70ºC
- ML2111CIP .... -40ºC to 85ºC

Supply Range .... ±2.25V to ±6.0V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{A+} = V_{D+} = 5V \pm 10\%$, $V_{A-} = V_{D-} = -5V \pm 10\%$, $C_L = 25pF$, $V_{IN} = 1.41V_{PK}$ ($1.000V_{RMS}$), Clock Duty Cycle = 50%, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER							
$f_{0(MAX)}$	Maximum Center Frequency (Note 2) $V_{IN}=1V_{PK}$ ($0.707V_{RMS}$)	Figure 15 (Mode 1), Q ≤ 50, Q Accuracy ≤ ± 25%				100	kHz
		Figure 15 (Mode 1), Q ≤ 20, Q Accuracy ≤ ± 15%				150	kHz
$f_{0(MIN)}$	Minimum Center Frequency (Note 2) $V_{IN}=1V_{PK}$ ($0.707V_{RMS}$)	Figure 15 (Mode 1), Q ≤ 50, Q Accuracy ≤ ± 30%		25			Hz
		Figure 15 (Mode 1), Q ≤ 20, Q Accuracy ≤ ± 15%		25			Hz
	f_0 Temperature Coefficient	f_{CLK} < 5MHz			-10		ppm/ºC
	Clock to Center Frequency Ratio	50:1, f_{CLK} = 5MHz	B Suffix	49.65	49.85	50.05	
	Q = 10, Figure 15 (Mode 1)		C Suffix	49.45	49.85	50.25	
		100:1, f_{CLK} = 5MHz	B Suffix	99.6	100.0	100.4	
			C Suffix	99.2	100.0	100.8	
f_{CLK}	Clock Frequency	Q ≤ 20, Q Accuracy ≤ ±15%		2.5		7500	kHz
	Clock Feedthrough	f_{CLK} ≤ 5MHz			10	20	$mV_{(P-P)}$
	Q Accuracy	f_{CLK} = 5MHz, Q = 10,	B Suffix			±3	%
		50:1, Figure 15 (Mode 1)	C Suffix			±5	%
		f_{CLK} = 5MHz, Q = 10,	B Suffix			±4	%
		100:1, Figure 15 (Mode 1)	C Suffix			±8	%
	Q Temperature Coefficient	f_{CLK} < 5MHz, Q = 10			20		ppm/ºC
$V_{OS2,3}$	DC Offset	50:1, f_{CLK} = 5MHz	B Suffix		7	40	mV
		$S_{A/B}$ = High or Low	C Suffix		7	60	mV
		100:1, f_{CLK} = 5MHz	B Suffix		14	60	mV
		$S_{A/B}$ =High or Low	C Suffix		14	100	mV

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER (Continued)							
	Gain Accuracy, DC Lowpass	R1,R3 = 20kΩ, R2 = 2kΩ, 100:1, f_0 = 50kHz, Q = 10			0.01	2	%
	Gain Accuracy, Bandpass at f_0	R1,R3 = 20kΩ, R2 = 2kΩ,	B Suffix		1	4	%
		100:1, f_0 = 50kHz, Q = 10	C Suffix		1	6	%
	Gain Accuracy, DC Notch Output	R1,R3 = 20kΩ, R2 = 2kΩ, 100:1, f_0 = 50kHz, Q = 10			0.02	2	%
	Noise (Note 3)	Bandpass	100kHz, 50:1		103		μV_{RMS}
	Figure 15 (Mode 1),		50kHz, 100:1		121		μV_{RMS}
	Q = 1, R1 = R2 = R3 = 2kΩ	Lowpass	100kHz, 50:1		120		μV_{RMS}
			50kHz, 100:1		150		μV_{RMS}
		Notch	100kHz, 50:1		115		μV_{RMS}
			50kHz, 100:1		135		μV_{RMS}
	Noise (Note 3)	Bandpass,	100kHz, 50:1		262		μV_{RMS}
	Figure 15 (Mode 1),	R1 = 20kΩ	50kHz, 100:1		333		μV_{RMS}
	Q = 10, R3 = 20kΩ, R2 = 2kΩ	Lowpass,	100kHz, 50:1		268		μV_{RMS}
		R1 = 2kΩ	50kHz, 100:1		342		μV_{RMS}
		Notch,	100kHz, 50:1		64		μV_{RMS}
		R1 = 2kΩ	50kHz, 100:1		72		μV_{RMS}
	Crosstalk	f_{CLK} = 5MHz, f_0= 100kHz			-50		dB
FILTER, $V_A+ = V_D+ = 2.25V$, $V_A- = V_D- = -2.25V$, $V_{IN} = 0.707 \times V_{PK}$ ($0.5 \times V_{RMS}$)							
$f_{0(MAX)}$	Maximum Center Frequency	Figure 15 (Mode 1), Q ≤ 50, Q Accuracy ≤ ± 30%				75	kHz
		Figure 15 (Mode 1), Q ≤ 20, Q Accuracy ≤ ± 15%				100	kHz
$f_{0(MIN)}$	Minimum Center Frequency	Figure 15 (Mode 1), Q ≤ 50, Q Accuracy ≤ ± 30%		25			Hz
		Figure 15 (Mode 1), Q ≤ 20, Q Accuracy ≤ ± 15%		25			Hz
	Clock to Center Frequency Ratio	50:1, f_{CLK} = 2.5MHz	B Suffix	49.65	49.85	50.05	
	Q = 10, Figure 15 (Mode 1)		C Suffix	49.45	49.85	50.25	
		100:1, f_{CLK} = 2.5MHz	B Suffix	99.60	100.0	100.4	
			C Suffix	99.20	100.0	100.8	
f_{CLK}	Clock Frequency	Q ≤ 20, Q Accuracy ≤ ±15%		2.5		5000	kHz
	Q Accuracy	f_{CLK} = 2.5MHz, Q = 10,	B Suffix			±4	%
		50:1, Figure 15 (Mode 1)	C Suffix			±8	%
		f_{CLK} = 2.5MHz, Q = 10,	B Suffix		±3		%
		100:1, Figure 15 (Mode 1)	C Suffix		±6		%

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER, $V_A+ = V_D+ = 2.25V$, $V_A- = V_D- = -2.25V$, $V_{IN} = 0.707 \times V_{PK}$ (0.5 x V_{RMS}) (Continued)							
	Noise (Note 3) Figure 15 (Mode 1), Q = 1, R1 = R2 = R3 = 2kΩ	Bandpass	100kHz, 50:1		105		μV_{RMS}
			50kHz, 100:1		123		μV_{RMS}
		Lowpass	100kHz, 50:1		122		μV_{RMS}
			50kHz, 100:1		152		μV_{RMS}
		Notch	100kHz, 50:1		117		μV_{RMS}
			50kHz, 100:1		138		μV_{RMS}
	Noise (Note 3) Figure 15 (Mode 1), Q = 10, R3 = 20kΩ, R2 = 2kΩ	Bandpass, R1 = 20kΩ	100kHz, 50:1		265		μV_{RMS}
			50kHz, 100:1		335		μV_{RMS}
		Lowpass, R1 = 2kΩ	100kHz, 50:1		270		μV_{RMS}
			50kHz, 100:1		245		μV_{RMS}
		Notch, R1 = 2kΩ	100kHz, 50:1		65		μV_{RMS}
			50kHz, 100:1		73		μV_{RMS}
OPERATIONAL AMPLIFIERS							
V_{OS1}	DC Offset Voltage				2	15	mV
A_{VOL}	DC Open Loop Gain	$R_L = 1k\Omega$			95		dB
	Gain Bandwidth Product				2.4		MHz
	Slew Rate				2.0		V/µs
	Output Voltage Swing (Clipping Level)	$R_L = 2k\Omega$, |V| from V_{A+} or V_{A-}			0.5	1.2	V
	Output Short Circuit Current	Source			50		mA
		Sink			25		mA
CLOCK							
	V_{CLK} Input Low Voltage					0.6	V
	V_{CLK} Input High Voltage			3.0			V
	CLK_A, CLK_B Pulse Width	$\|V_{D+}\| - \|V_{D-}\| \geq 4.5V$		100			ns
	CLK_A, CLK_B Pulse Width	$\|V_{D+}\| - \|V_{D-}\| \geq .90V$		66			ns
SUPPLY							
$(I_{A+})+(I_{D+})$	Supply Current, $(V_{A+}) + (V_{D+})$	$f_{CLK} = 5MHz$			13	22	mA
$(I_{A-})+(I_{D-})$	Supply Current, $(V_{A-}) + (V_{D-})$	$f_{CLK} = 5MHz$			12	21	mA
I_{LSh}	Supply Current, LSh	$f_{CLK} = 5MHz$			0.5	1	mA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

Note 2: The center frequency is defined as the peak of the bandpass output.

Note 3: The noise is meassured with an HP8903A audio analyzer with a bandwidth of 700kHz, which is 7.5 times the f_0 at 50:1 and 15 times the f_0 at 100:1.

TYPICAL PERFORMANCE CURVES

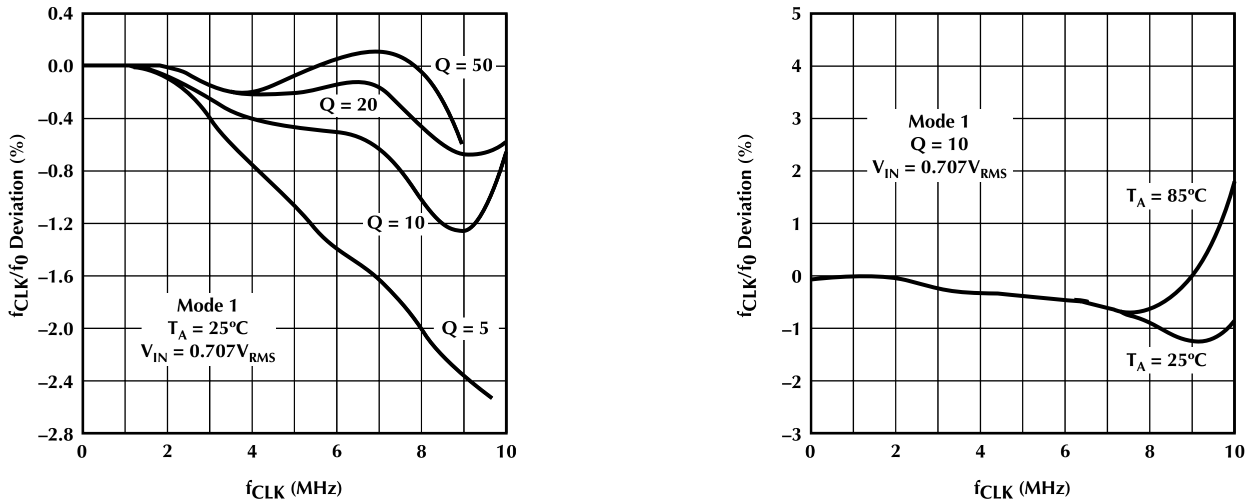


Figure 1A. f_{CLK}/f_0 vs. f_{CLK} (50:1, V_S = ±5V)

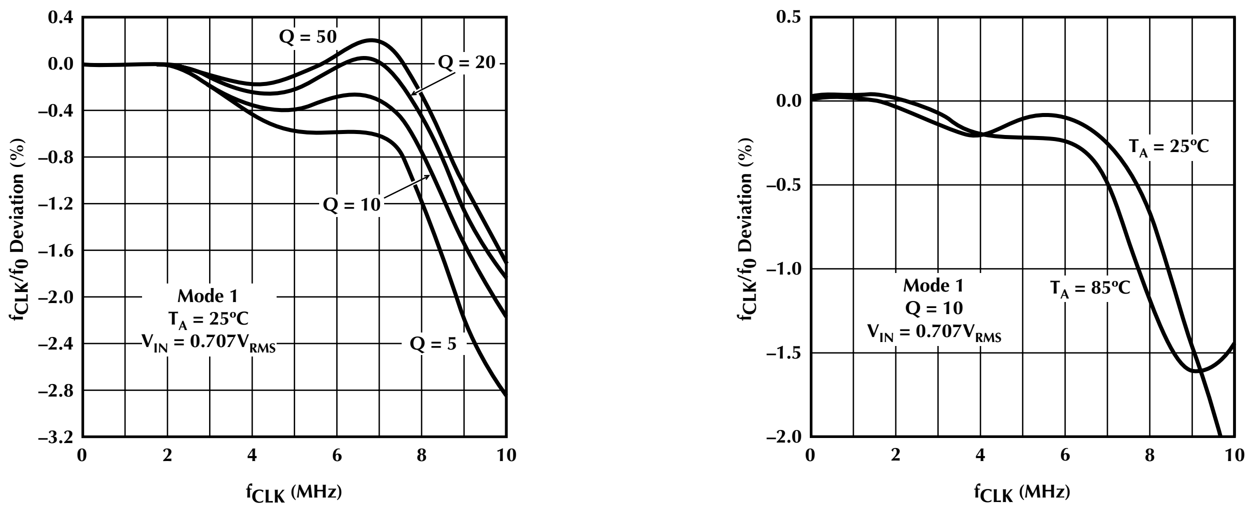


Figure 1B. f_{CLK}/f_0 vs. f_{CLK} (100:1, V_S = ±5V)

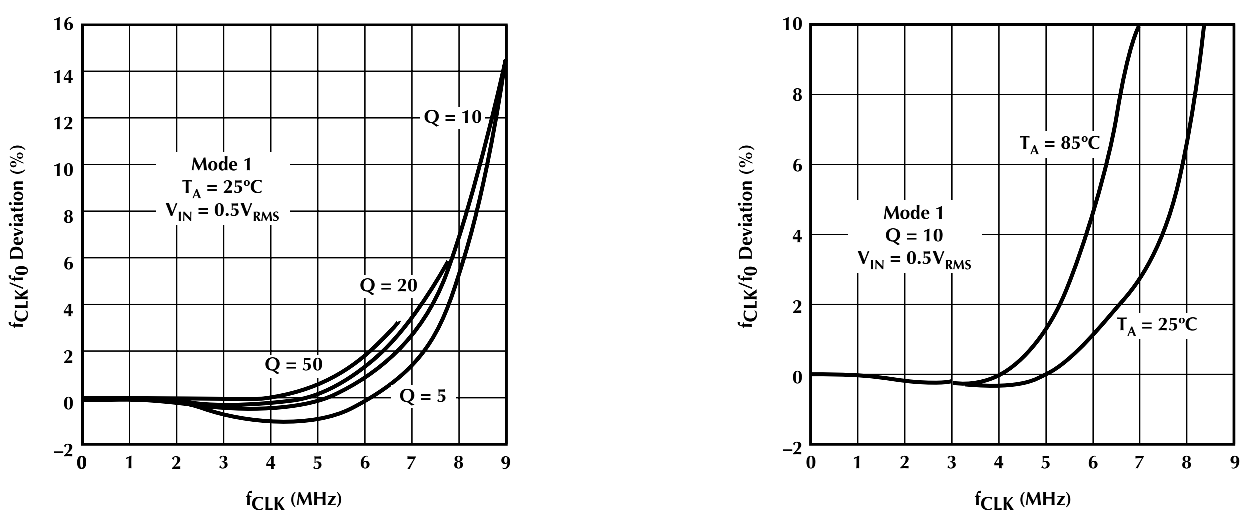


Figure 1C. f_{CLK}/f_0 vs. f_{CLK} (50:1, V_S = ±2.5V)

TYPICAL PERFORMANCE CURVES (Continued)

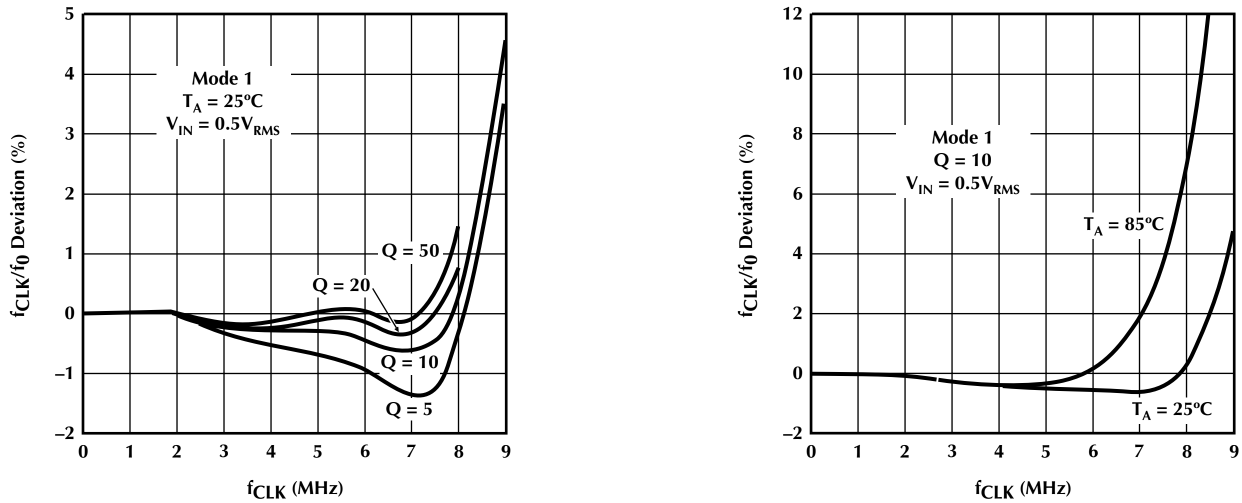


Figure 1D. f_{CLK}/f_0 vs. f_{CLK} (100:1, V_S = ±2.5V)

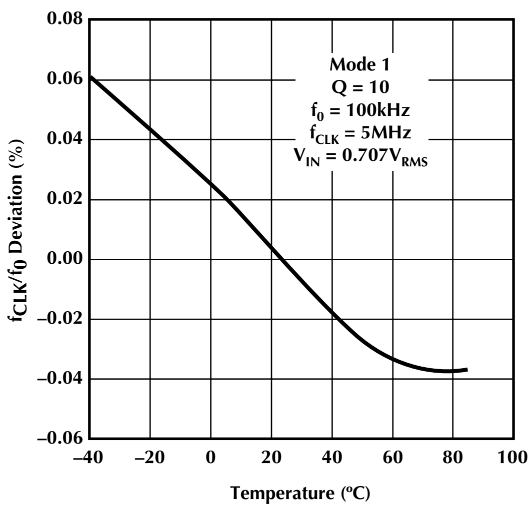


Figure 2A. f_{CLK}/f_0 Deviation vs. Temperature (50:1, V_S = ±5V)

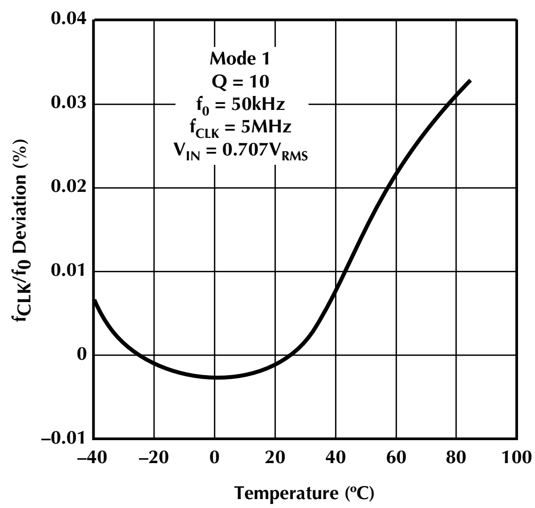


Figure 2B. f_{CLK}/f_0 Deviation vs. Temperature (100:1, V_S = ±5V)

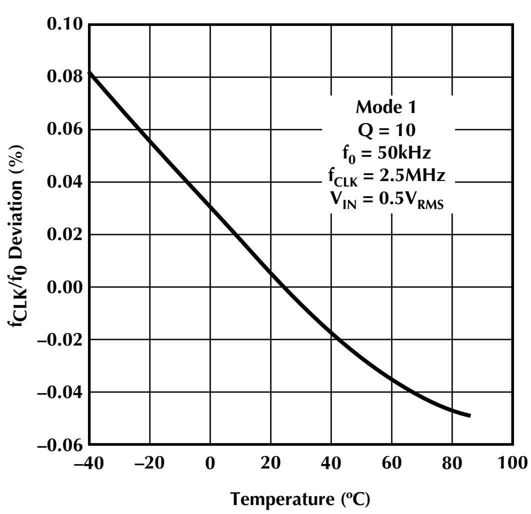


Figure 2C. f_{CLK}/f_0 Deviation vs. Temperature (50:1, V_S = ±2.5V)

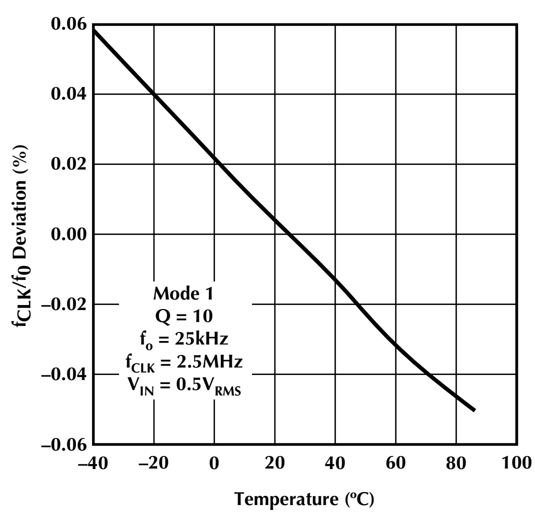


Figure 2D. f_{CLK}/f_0 Deviation vs. Temperature (100:1, V_S = ±2.5V)

TYPICAL PERFORMANCE CURVES (Continued)

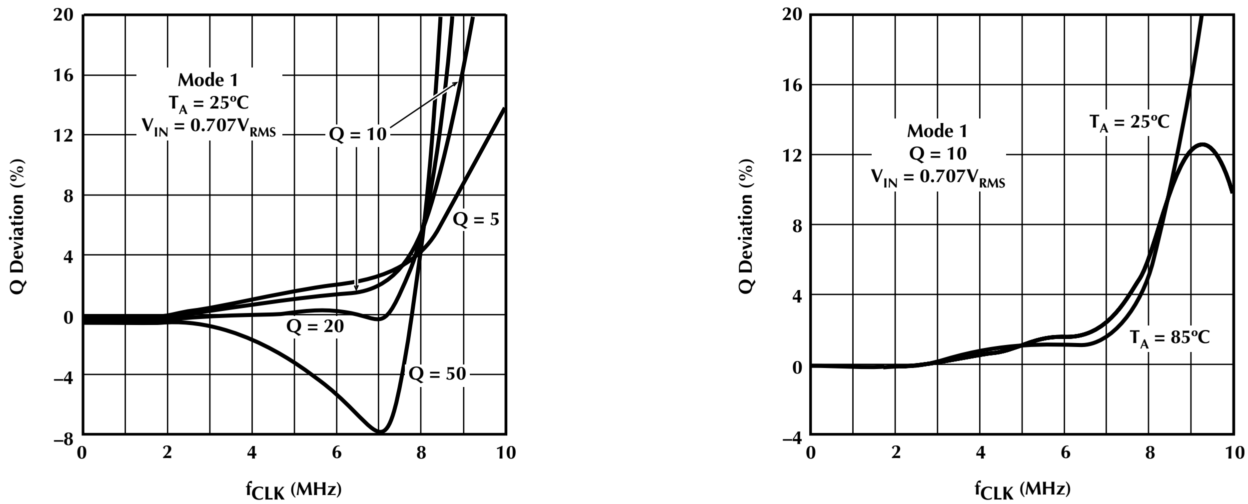


Figure 2E. Q Error vs. f_{CLK} (50:1, V_S = ±5V)

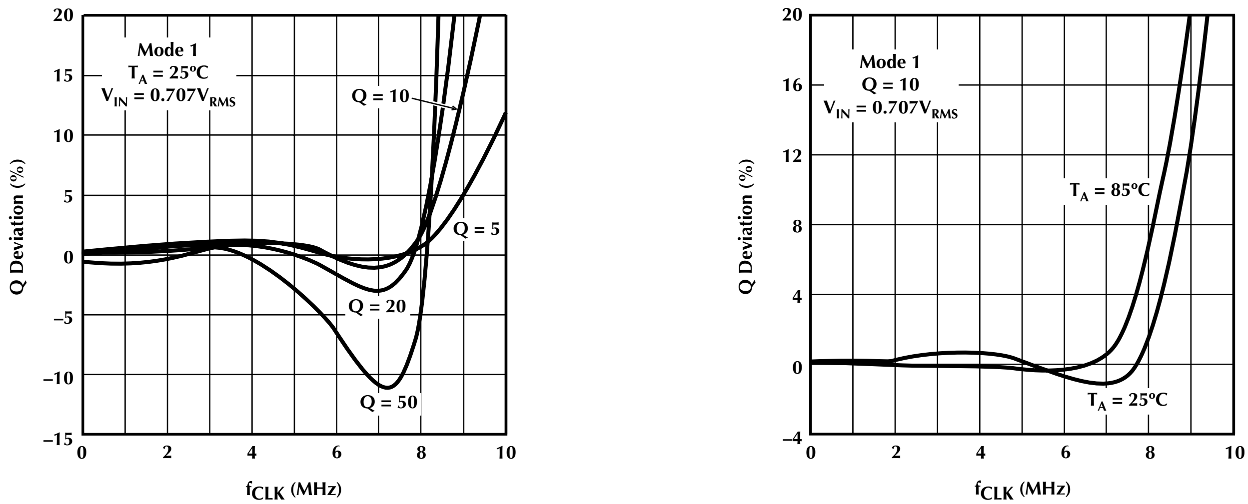


Figure 2F. Q Error vs. f_{CLK} (100:1, V_S = ±5V)

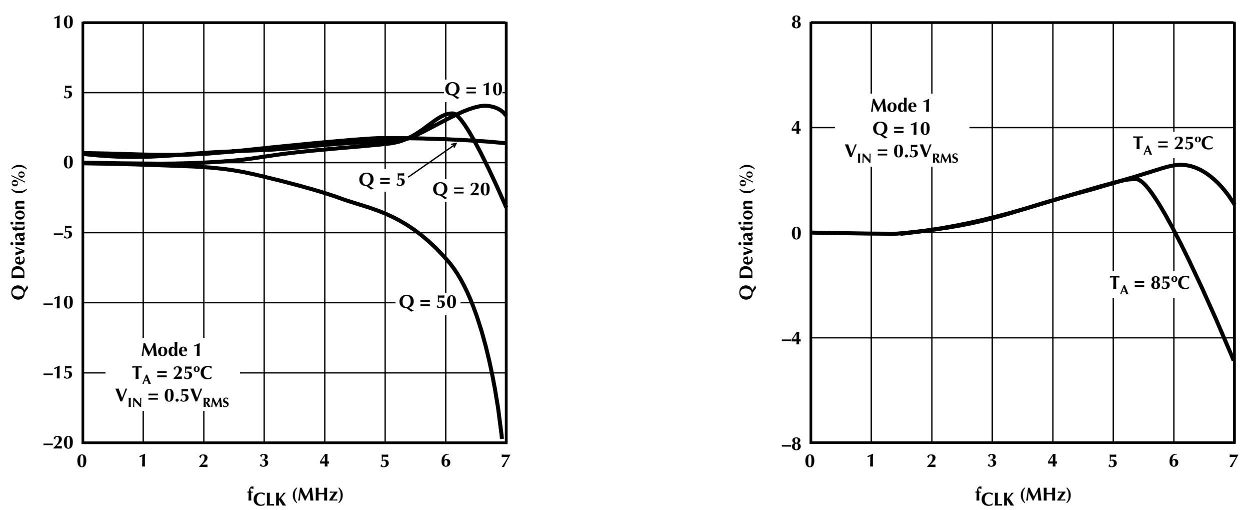


Figure 2G. Q Error vs. f_{CLK} (50:1, V_S = ±2.5V)

TYPICAL PERFORMANCE CURVES (Continued)

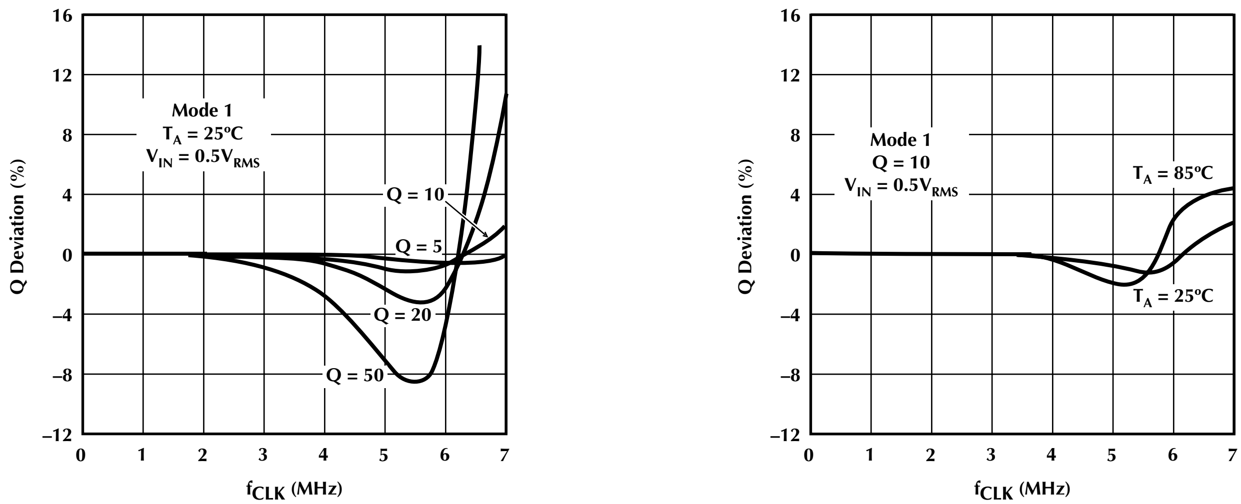


Figure 2H. Q Error vs. f_{CLK} (100:1, V_S = ±2.5V)

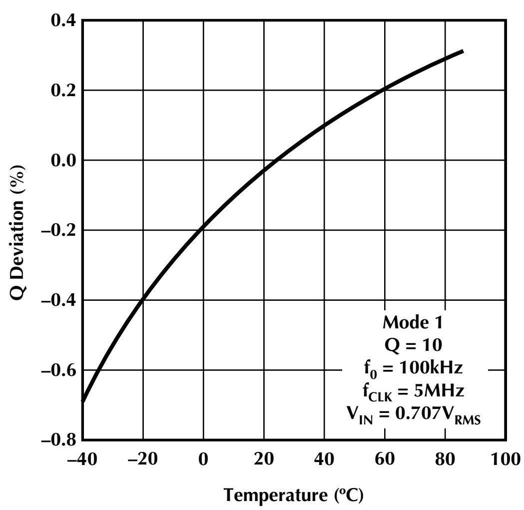


Figure 3A. Q Deviation vs. Temperature (50:1, V_S = ±5V)

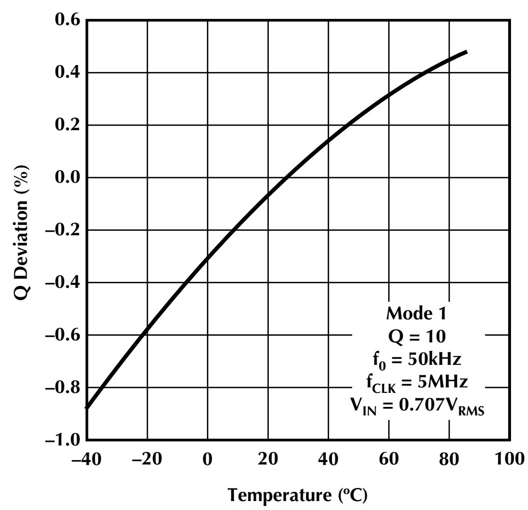


Figure 3B. Q Deviation vs. Temperature (100:1, V_S = ±5V)

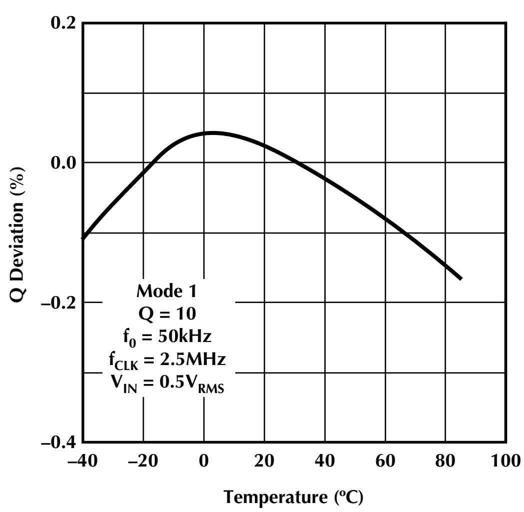


Figure 3C. Q Deviation vs. Temperature (50:1, V_S = ±2.5V)

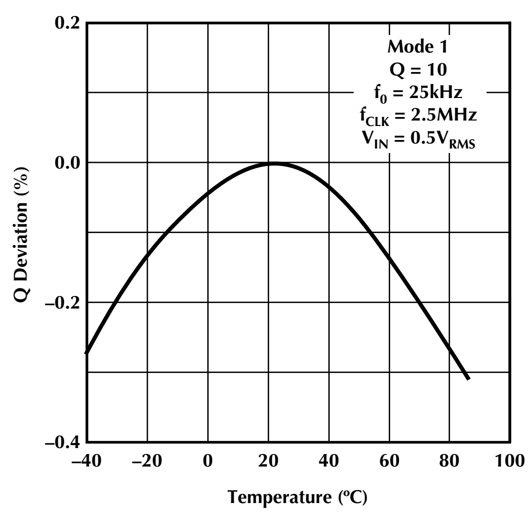


Figure 3D. Q Deviation vs. Temperature (100:1, V_S = ±2.5V)

TYPICAL PERFORMANCE CURVES (Continued)

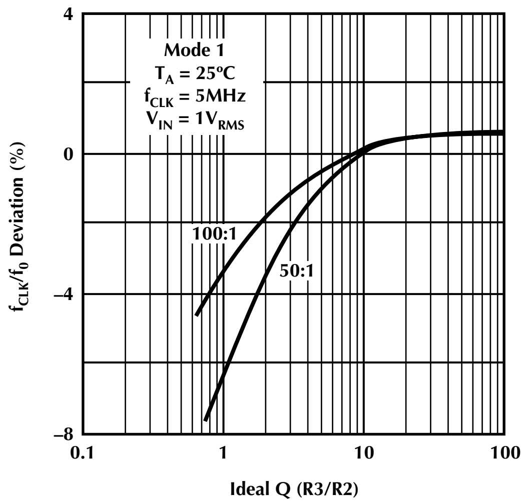


Figure 4A. f_{CLK}/f_0 Deviation vs. Q (V_S = ±5V)

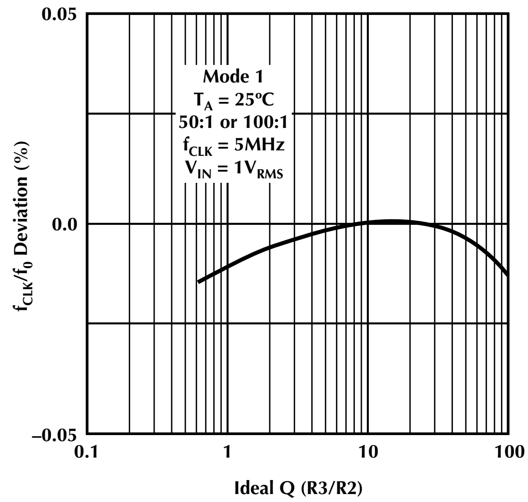


Figure 4A. f_{CLK}/f_{NOTCH} Deviation vs. Q (V_S = ±5V)

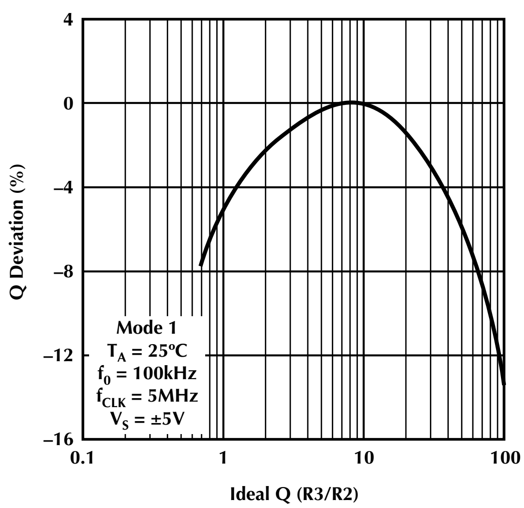


Figure 5A. Q Deviation vs. Q (50:1, V_S = ±5V)

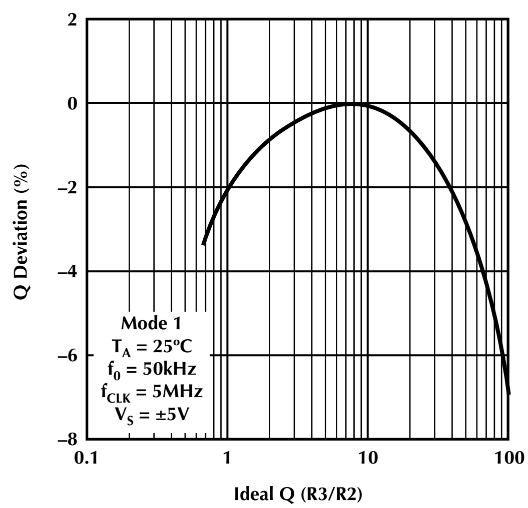


Figure 5B. Q Deviation vs. Q (100:1, V_S = ±5V)

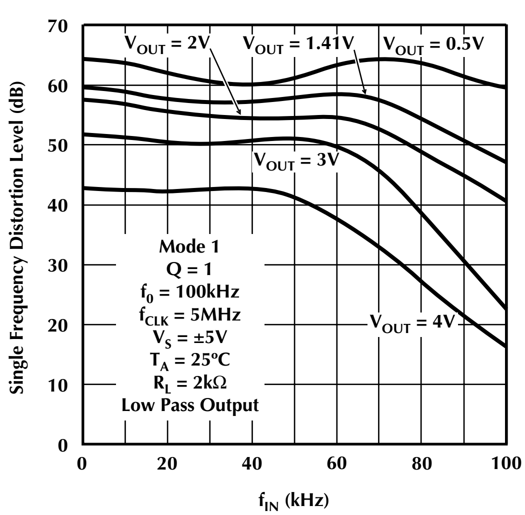


Figure 6A. Distortion vs. f_{IN} (50:1, V_S = ±5V)

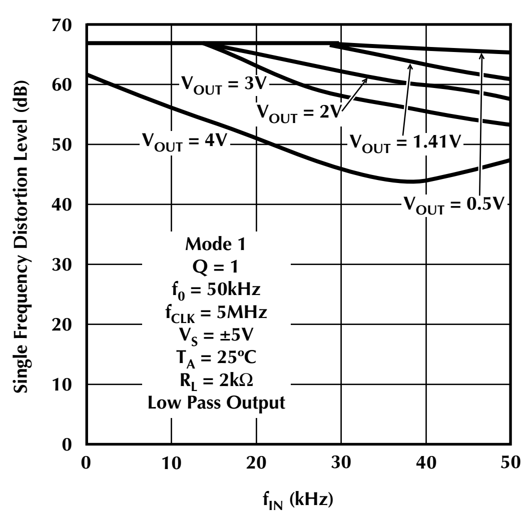


Figure 6B. Distortion vs. f_{IN} (100:1, V_S = ±5V)

TYPICAL PERFORMANCE CURVES (Continued)

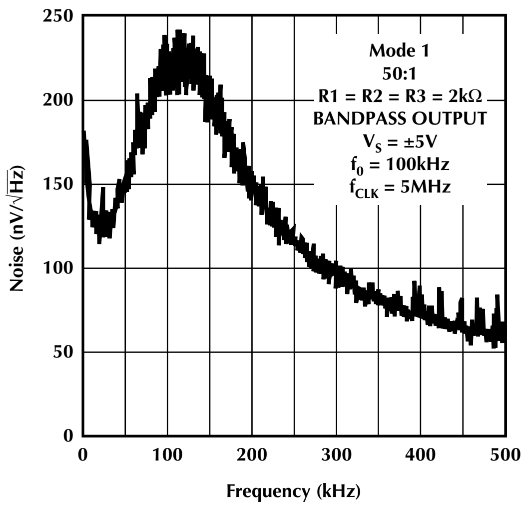


Figure 7A. Noise Spectrum Density (Q = 1)

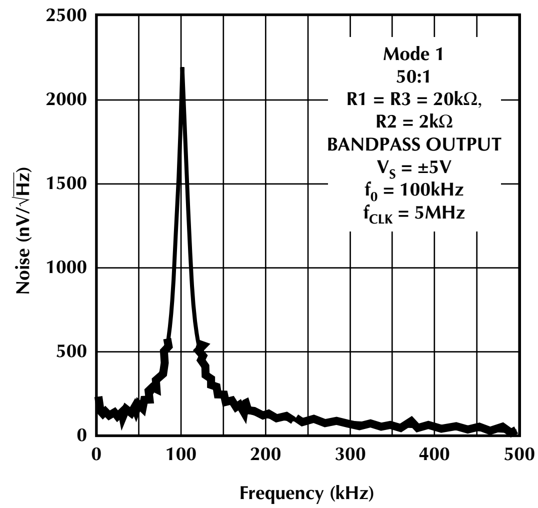


Figure 7B. Noise Spectrum Density (Q = 10)

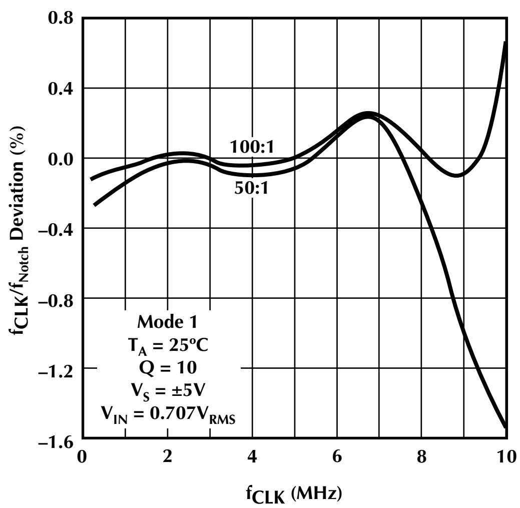


Figure 8. f_{CLK}/f_{NOTCH} vs. f_{CLK}

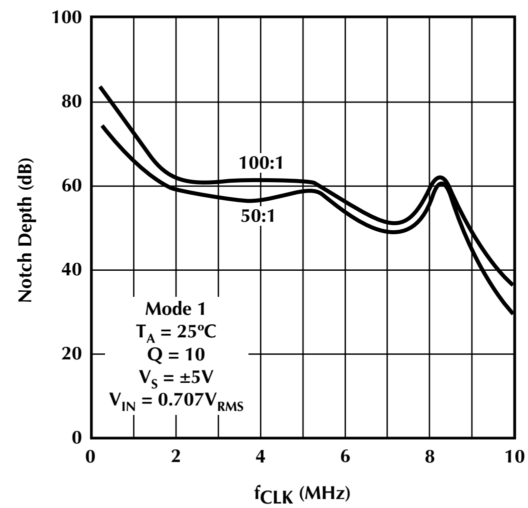


Figure 9. Notch Depth vs. f_{CLK}

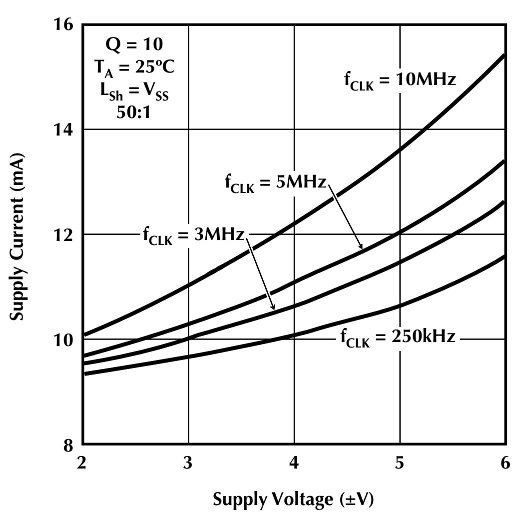


Figure 10. Supply Current vs. Supply Voltage

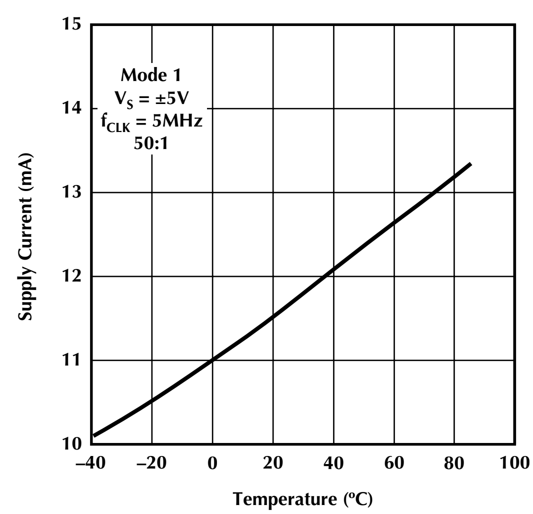


Figure 11. Supply Current vs. Temperature

FUNCTIONAL DESCRIPTION

POWER SUPPLIES

The analog (V_{A+}) and digital (V_{D+}) supply pins, in most cases, are tied together and bypassed to AGND with 100nF and 10nF disk ceramic capacitors. The supply pins can be bypassed separately if a high level of digital noise exists. These pins are internally connected by the IC substrate and should be biased from the same DC source. The ML2111 operates from either a single supply from 4V to 12V, or with dual supplies at ±2V to ±6V.

CLOCK INPUT PINS AND LEVEL SHIFT

With dual supplies equal to or higher than ±4.0V, the LSh pin can be connected to the same potential as either the AGND or the V_{A-} pin. With single supply operation the negative supply pins and LSh pin should be tied to the system ground. The AGND pin should be biased half way between V_{A+} and V_{A-}. Under these conditions the clock levels are TTL or CMOS compatible. Both input clock pins share the same level shift pin.

50/100/HOLD

Tying the 50/100/HOLD pin to the V_{A+} and V_{D+} pins makes the filter operate in the 50:1 mode. Tying the pin half way between V_{A+} and V_{A-} makes the filter operate in the 100:1 mode. The input range for 50/100/HOLD is either 2.5V ±0.5V with a total power supply range of 5V, or 5V ±0.5V with a total power supply range of 10V. When 50/100/HOLD is tied to the negative power supply input, the filter operation is stopped and the bandpass and lowpass outputs act as a sample/hold circuit which holds the last sample.

$S1_A$ & $S1_B$

These voltage signal input pins should be driven by a source impedance of less than 5kΩ. The S_{1A} and S_{1B} pins can be used to feedforward the input signal for allpass filter configurations (see modes 4 & 5) or to alter the clock-to-center-frequency ratio (f_{CLK}/f_0) of the filter (see modes 1b, 1c, 2a, & 2b). When these pins are not used they should be tied to the AGND pin.

$S_{A/B}$

When $S_{A/B}$ is high, the S2 negative input of the voltage summing device is tied to the lowpass output. When the $S_{A/B}$ pin is connected to the negative supply, the S2 input switches to ground.

AGND

AGND is connected to the system ground for dual supply operation. When operating with a single positive supply the analog ground pin should be biased half way between V_{A+} and V_{A-}, and bypassed with a 100nF capacitor. The positive inputs of the internal op amps and the reference point of the internal switches are connected to the AGND pin.

f_{CLK}/f_0 RATIO

The ML2111 is a sampled data filter and approximates continuous time filters. The filter deviates from its ideal continuous filter model when the (f_{CLK}/f_0) ratio decreases and when the Qs are low.

$f_0 \times$ Q PRODUCT RATIO

The $f_0 \times Q$ product of the ML2111 depends on the clock frequency and the mode of operation. The $f_0 \times Q$ product is mainly limited by the desired f_0 and Q accuracy for clock frequencies below 1MHz in mode 1 and its derivatives. If the clock to center frequency ratio is lowered below 50:1, the $f_0 \times Q$ product can be further increased for the same clock frequency and for the same Q value.

Mode 3, (Figure 23) and the modes of operation where R4 is finite, are "slower" than the basic mode 1. The resistor R4 places the input op amp inside the resonant loop. The finite GBW of this op amp creates an additional phase shift and enhances the Q value at high clock frequencies.

OUTPUT NOISE

The wideband RMS noise on the outputs of the ML2111 is nearly independent of the clock frequency, provided that the clock itself does not become part of the noise. Noise at the BP and LP outputs increases for high values of Q.

FILTER FUNCTION DEFINITIONS

Each filter of the ML2111, along with external resistors and a clock, approximates second order filter functions. These are tabulated below in the frequency domain.

1. **Bandpass function:** available at the bandpass output pins (BP_A, BP_B), Figure 12.

$$G(s) = H_{OBP} \times \frac{\frac{s \times \omega_0}{Q}}{s^2 + \left(\frac{s \times \omega_0}{Q}\right) + \omega_0^{\,2}} \qquad (1)$$

where:

H_{OBP} = Gain at $\omega = \omega_0$

$f_0 = \omega_0/2\pi$. The center frequency of the complex pole pair is f_0. It is measured as the peak frequency of the bandpass output.

Q = the Quality factor of the complex pole pair. It is the ratio of f_0 to the -3dB bandwidth of the 2nd order bandpass function. The Q is always measured at the filter BP output.

FILTER FUNCTION DEFINITIONS (Continued)

2. **Lowpass function:** available at the LP output pins, Figure 13.

$$G(s) = H_{OLP} \times \frac{\omega_0^2}{s^2 + \left(\frac{s \times \omega_0}{Q}\right) + \omega_0^2} \qquad (2)$$

where:

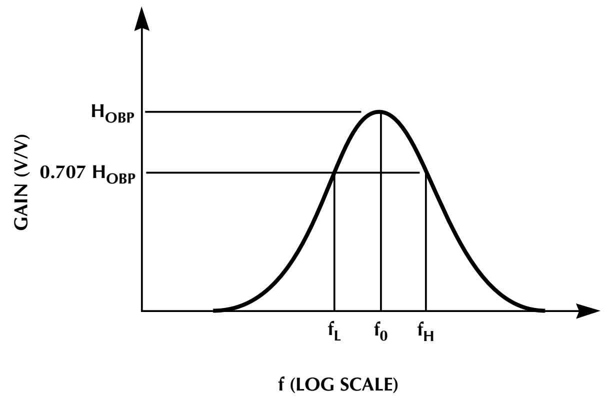
H_{OLP} = DC gain of the LP output

3. **Highpass function:** available only in mode 3 at $N/AP/HP_A$ and $N/AP/HP_B$, Figure 14.

$$G(s) = H_{OHP} \times \frac{s^2}{s^2 + \left(\frac{s \times \omega_0}{Q}\right) + \omega_0^2} \qquad (3)$$

H_{OHP} = Gain of the HP output for $f \rightarrow f_{CLK}/2$.

BANDPASS OUTPUT



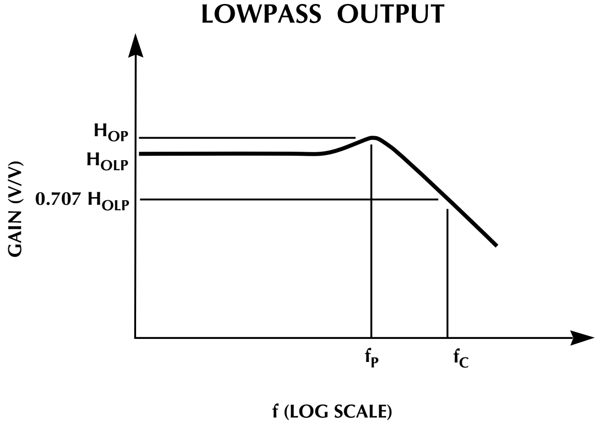
$$Q = \frac{f_0}{f_H - f_L}; f_0 = \sqrt{f_L \times f_H}$$

$$f_L = f_0 \times \left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_0 \times \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

Figure 12.

LOWPASS OUTPUT



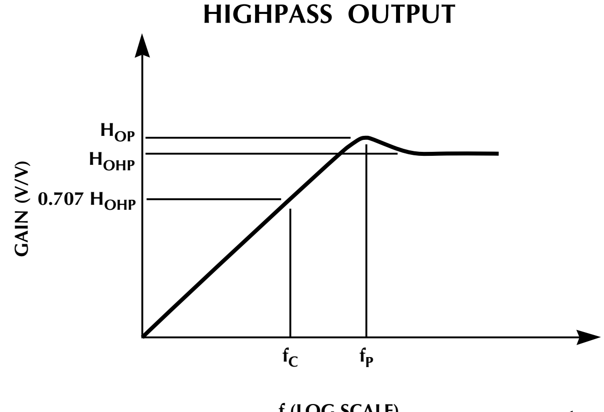
$$f_C = f_0 \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_P = f_0 \times \sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q} \times \sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 13.

HIGHPASS OUTPUT



$$f_C = f_0 \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

$$f_P = f_0 \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q} \times \sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 14.

FILTER FUNCTION DEFINITIONS

4. **Notch function:** available at N/AP/HP_A and N/AP/HP_B for several modes of operation.

$$G(s) = H_{ON2} \times \frac{\left(s^2 + \omega_n{}^2\right)}{s^2 + \left(\frac{s \times \omega_0}{Q}\right) + \omega_0{}^2} \qquad (4)$$

H_{ON2} = Gain of the notch output for $f \rightarrow f_{CLK}/2$.

H_{ON1} = Gain of the HP output for $f \rightarrow 0$

$f_n = \omega_n/2\pi$. The frequency of the notch occurrence is f_n.

5. **Allpass function:** available at N/AP/HP_A and N/AP/HP_B for modes 4 and 4a.

$$G(s) = H_{OAP} \times \frac{s^2 - \frac{s \times \omega_0}{Q} + \omega_0{}^2}{s^2 + \frac{s \times \omega_0}{Q} + \omega_0{}^2} \qquad (5)$$

H_{OAP} = Gain of the allpass output for $0 < f < f_{CLK}/2$

For allpass functions, the center frequency and the Q of the numerator complex zero pair is the same as the denominator. Under these conditions the magnitude response is a straight line. In mode 5, the center frequency f_Z of the numerator complex zero pair is different than f_0. For high numerator Q's, the magnitude response will have a notch at f_Z.

OPERATION MODES

There are three basic modes of operation — Modes 1, 2, and 3 , each of which has derivatives; and four secondary modes of operation — Modes 4, 5, 6, and 7, each of which also has derivatives.

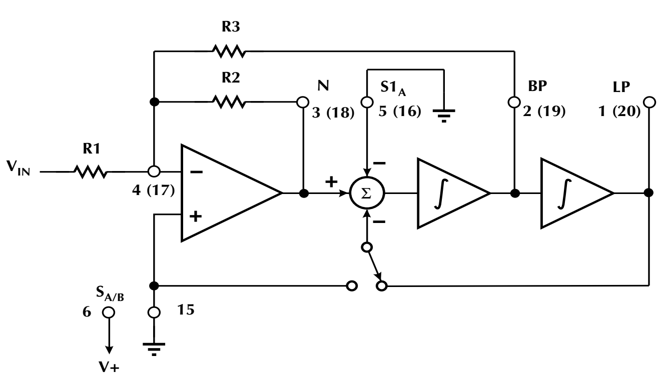
In Figure 15, the input amplifier is outside the resonant loop. Because of this, mode 1 and its derivatives (modes 1a, 1b, 1c, and 1d) are faster than modes 2 and 3.

Mode 1 provides a clock tunable notch. It is a practical configuration for second order clock tunable bandpass/notch filters. In mode 1, a band pass output with a very high Q, together with unity gain can be obtained with the dynamics of the remaining notch and lowpass outputs.

Mode 1a (Figure 16) represents the simplest hookup of the ML2111. It is useful when voltage gain at the bandpass output is required. However, the bandpass voltage gain is equal to the value of Q, and second order, clock tunable, BP resonator can be achieved with only 2 resistors. The filter center frequency directly depends on the external clock frequency. Mode 1a is not practical for high order filters as it requires several clock frequencies to tune the overall filter response.

Modes 1b and 1c, Figures 17 and 18, are similar. They both produce a notch with a frequency which is always equal to the filter center frequency. The notch and the center frequency can be adjusted with an external resistor ratio.

½ ML2111

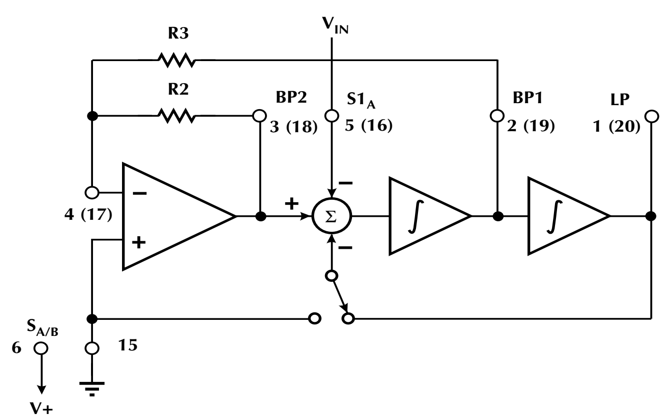


$$f_0 = \frac{f_{CLK}}{100(50)}; f_n = f_0; H_{OLP} = -\frac{R2}{R1}; H_{OBP} = -\frac{R3}{R1};$$

$$H_{ON1} = -\frac{R2}{R1}; Q = \frac{R3}{R2}$$

Figure 15. Mode 1: 2nd Order Filter Providing Notch, Bandpass, Lowpass

½ ML2111



$$f_0 = \frac{f_{CLK}}{100(50)}; Q = \frac{R3}{R2}; H_{OBP1} = -\frac{R3}{R2};$$

$$H_{OBP2} = 1 (\text{non-inverting}); H_{OLP} = -1$$

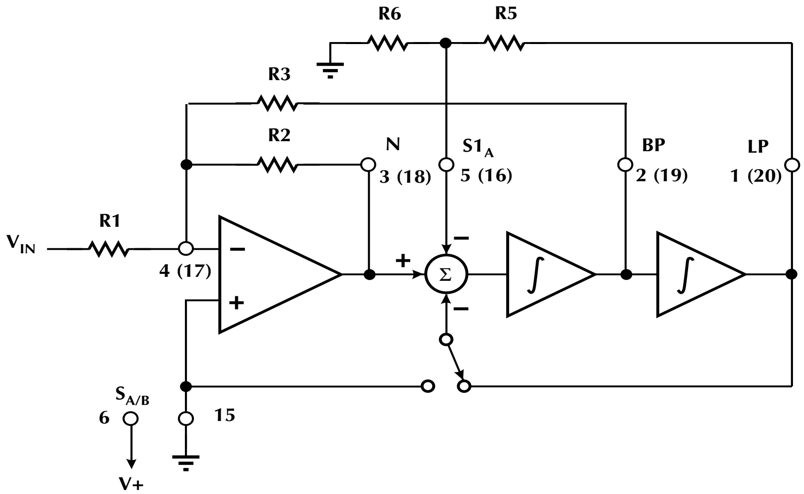
Figure 16. Mode 1a: 2nd Order Filter Providing Bandpass, Lowpass

MODE	BP_A, BP_B	$N/AP/HP_A, N/AP/HP_B$	f_C	f_Z
6a	LP	HP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	
6b	LP	LP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	
7	LP	AP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$

Table 1. First Order Functions.

MODE	LP_A, LP_B	BP_A, BP_B	$N/AP/HP_{A\&B}$	f_0	f_N
1	LP	BP	Notch	$\frac{f_{CLK}}{100(50)}$	f_0
1a	LP	BP	BP	$\frac{f_{CLK}}{100(50)}$	
1b	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1+\frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1+\frac{R6}{R5+R6}}$
1c	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$
1d	LP	BP		$\frac{f_{CLK}}{100(50)}$	
2	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1+\frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)}$
2a	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1+\frac{R2}{R4}+\frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1+\frac{R6}{R5+R6}}$
2b	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}+\frac{R6}{R5+R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}$
3	LP	BP	HP	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	
3a	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R_h}{R_l}}$
4	LP	BP	AP	$\frac{f_{CLK}}{100(50)}$	
4a	LP	BP	AP	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	
5	LP	BP	CZ	$\frac{f_{CLK}}{100(50)} \times \sqrt{1+\frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1-\frac{R2}{R4}}$

Table 2. Second Order Functions



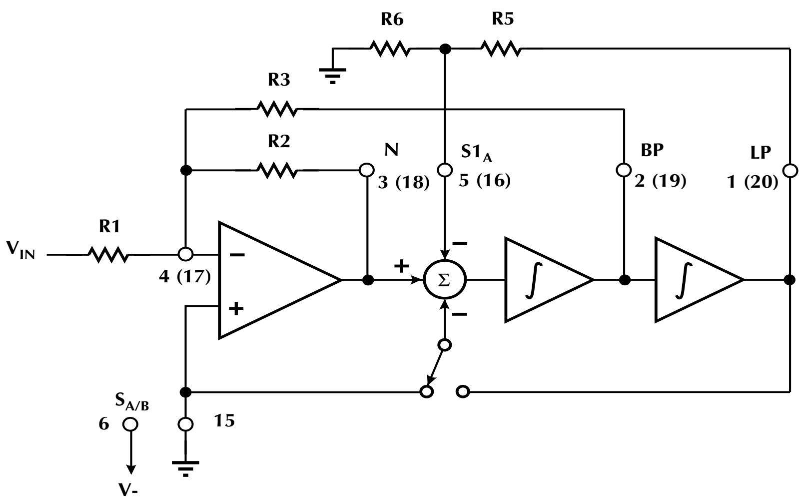
$$f_0 = \frac{f_{CLK}}{100(50)} \times \sqrt{1+\frac{R6}{R5+R6}}; f_n = f_0$$

$$Q = \frac{R3}{R2} \times \sqrt{1+\frac{R6}{R5+R6}}; R5 < 5k\Omega$$

$$H_{ON1}(f \to 0) = H_{ON2}\left(f \to \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}; H_{OLP} = \frac{-R2/R1}{1+R6/(R5+R6)}$$

Figure 17. Mode 1b: 2nd Order Filter Providing Notch, Bandpass, Lowpass



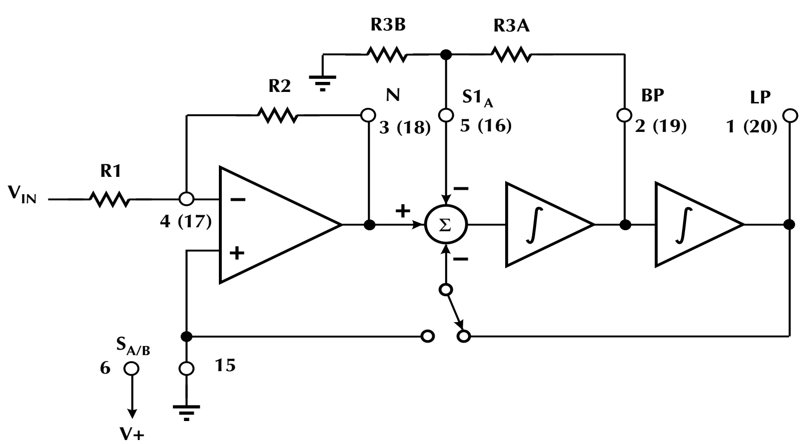
$$f_0 = \frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5+R6}}; f_n = f_0$$

$$Q = \frac{R3}{R2} \times \sqrt{\frac{R6}{R5+R6}};$$

$$H_{ON1}(f \to 0) = H_{ON2}\left(f \to \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1};$$

$$H_{OBP} = -\frac{R3}{R1}; H_{OLP} = \frac{-R2/R1}{R6/(R5+R6)}; R5 < 5k\Omega$$

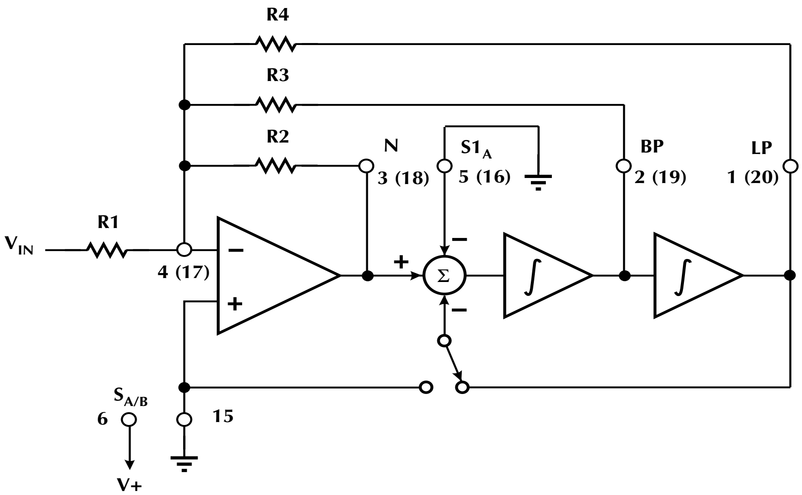
Figure 18. Mode 1c: 2nd Order Filter Providing Notch, Bandpass, Lowpass



$$f_0 = \frac{f_{CLK}}{100(50)}; Q = 1 + \frac{R3_A}{R3_B}; H_{OBP} = -\frac{R2}{R1} \times Q;$$

$$H_{OLP} = -\frac{R2}{R1}; V_N - \frac{R2}{R1} \times V_{IN}$$

Figure 19. Mode 1d: 2nd Order Filter Providing Bandpass and Lowpass for Qs Greater Than or Equal To 1.



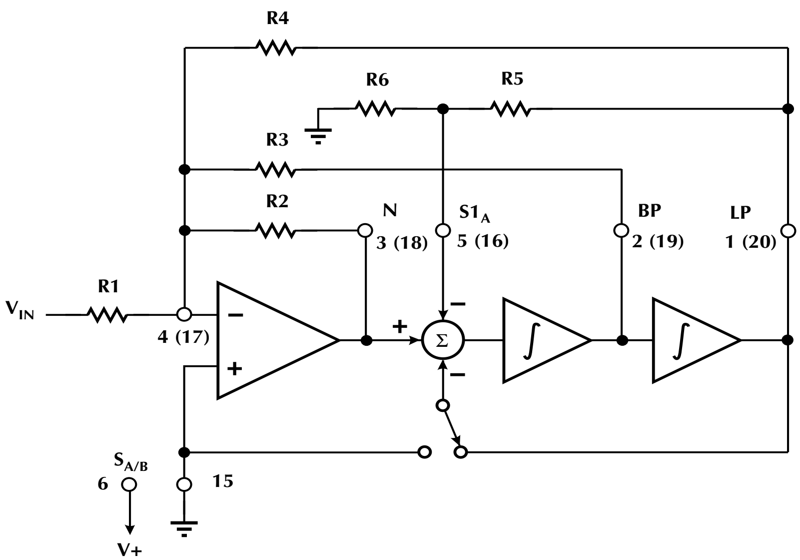
$$f_0 = \frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4}}; f_n = \frac{f_{CLK}}{100(50)};$$

$$Q = \frac{R3}{R2} \times \sqrt{1 + \frac{R2}{R4}}; H_{OLP} = \frac{-R2/R1}{1 + (R2/R4)};$$

$$H_{OBP} = \frac{-R3}{R1}; H_{ON1}(f \to 0) = \frac{-R2/R1}{1 + (R2/R4)};$$

$$H_{ON2}\left(f \to \frac{f_{CLK}}{2}\right) = \frac{-R2}{R1}$$

Figure 20. Mode 2: 2nd Order Filter Providing Notch, Bandpass, Lowpass



$$f_0 = \frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4} + \frac{R6}{R5 + R6}}; H_{OBP} = -\frac{R3}{R1};$$

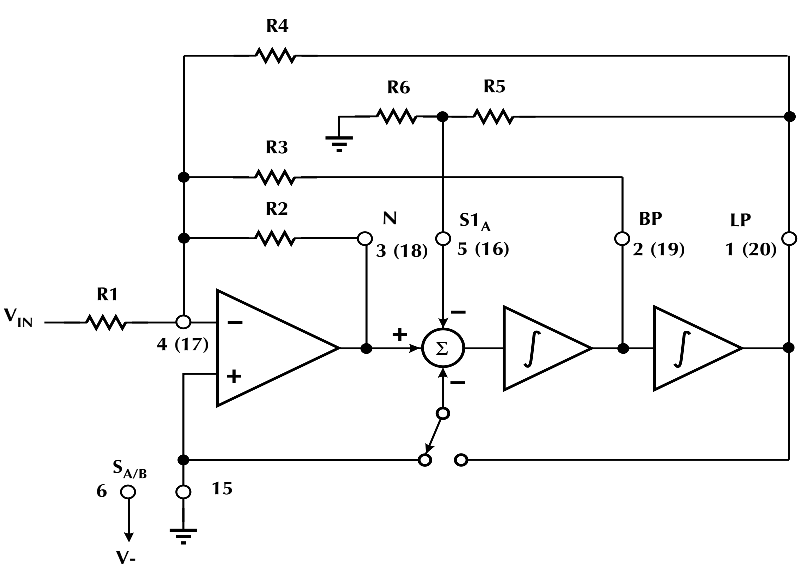
$$f_n = \frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5 + R6}}; H_{ON2}\left(f \to \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1};$$

$$Q = \frac{R3}{R2} \times \sqrt{1 + \frac{R2}{R4} + \frac{R6}{R5 + R6}};$$

$$H_{ON1}(f \to 0) = -\frac{R2}{R1}\left\{\frac{1 + R6/(R5 + R6)}{1 + (R2/R4) + [R6/R5 + R6]}\right\};$$

$$H_{OLP} = \frac{-R2/R1}{1 + (R2/R4) + [R6/(R5 + R6)]}$$

Figure 21. Mode 2a: 2nd Order Filter Providing Notch, Bandpass, Lowpass



$$f_0 = \frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4} + \frac{R6}{R5 + R6}};$$

$$f_n = \frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5 + R6}}; Q = \frac{R3}{R2} \times \sqrt{\frac{R2}{R4} + \frac{R6}{R5 + R6}};$$

$$H_{ON1}(f \to 0) = -\frac{R2}{R1}\left\{\frac{R6/(R5 + R6)}{(R2/R4) + [R6/R5 + R6]}\right\};$$

$$H_{ON2}\left(f \to \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}; H_{OBP} = -\frac{R3}{R1};$$

$$H_{OLP} = \frac{-R2/R1}{(R2/R4) + [R6/(R5 + R6)]}$$

Figure 22. Mode 2b: 2nd Order Filter Providing Notch, Bandpass, Lowpass

OPERATION MODES (Continued)

The clock to center frequency ratio range is:

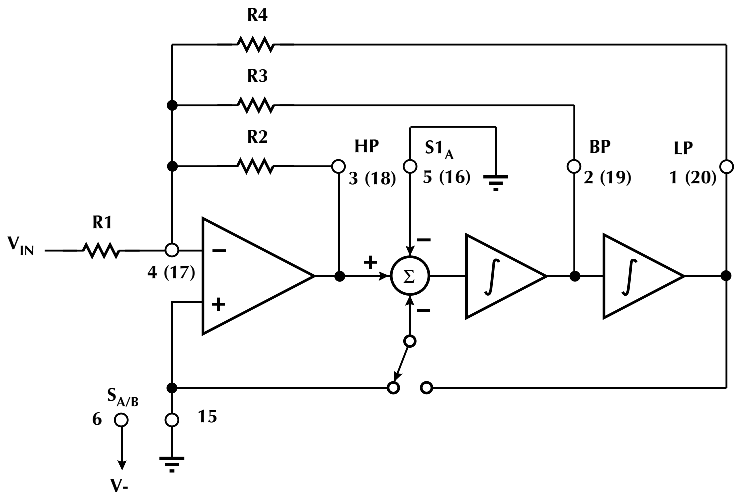
$$\frac{500}{1} \geq \frac{f_{CLK}}{f_0} \geq \frac{100}{1} \text{ or } \frac{50}{1} \quad \text{(mode 1c)} \qquad (6)$$

$$\frac{100}{1} \text{ or } \frac{50}{1} \geq \frac{f_{CLK}}{f_0} \geq \frac{100}{\sqrt{2}} \text{ or } \frac{50}{\sqrt{2}} \quad \text{(mode 1b)} \qquad (7)$$

The input impedance of the S1 pin is clock dependent, and in general R5 should not be larger than 5kΩ for f_{CLK} < 2.5MHz and 2kΩ for f_{CLK} > 2.5MHz. Mode 1c can be used to increase the clock-to-center-frequency ratio beyond 100:1. The limit for the (f_{CLK}/f_0) ratio is 500:1 for this mode. The filter will exhibit large output offsets with larger ratios. Mode 1d (Figure 19) is the fastest mode of operation: center frequencies beyond 20kHz can easily be achieved at a 50:1 ratio.

Modes 2, 2a, and 2b (Figures 20, 21, and 22) have notch outputs whose frequency, f_n, can be tuned independently from the center frequency, f_0. However, for all cases $f_n < f_0$. These modes are useful when cascading second order functions to create an overall elliptic highpass, bandpass or notch response. The input amplifier and its feedback resistors R2 and R4 are now part of the resonant loop. Because of this, mode 2 and its derivatives are slower than mode 1 and its derivatives.

In Mode 3 (Figure 23) a single resistor ratio, R2/R4, can tune the center frequency below or above the f_{CLK}/100 (or f_{CLK}/50) ratio. Mode 3 is a state variable configuration since it provides a highpass, bandpass, lowpass output through progressive integration. Notches are acquired by summing the highpass and lowpass outputs (mode 3a, Figure 24). The notch frequency can be tuned below or



$$f_0 = \frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}; Q = \frac{R3}{R2} \times \sqrt{\frac{R2}{R4}};$$

$$H_{OHP} = -\frac{R2}{R1}; H_{OLP} = -\frac{R4}{R1}; H_{OBP} = -\frac{R3}{R1}$$

Figure 23. Mode 3: 2nd Order Filter Providing Highpass, Bandpass, Lowpass — ½ ML2111

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$f_0 = \frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}; f_n = \frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R_h}{R_l}};$$

$$H_{OHP} = -\frac{R2}{R1}; H_{OBP} = -\frac{R3}{R1}; H_{OLP} = -\frac{R4}{R1};$$

$$H_{ON}(f = f_0) = Q \times \left(\frac{R_g}{R_l} \times H_{OLP} - \frac{R_g}{R_h} \times H_{OHP}\right);$$

$$H_{ON2}\left(f \to \frac{f_{CLK}}{2}\right) = \frac{R_g}{R_h} \times \frac{R2}{R1};$$

$$H_{ON1}(f \to 0) = \frac{R_g}{R_l} \times \frac{R4}{R1}$$

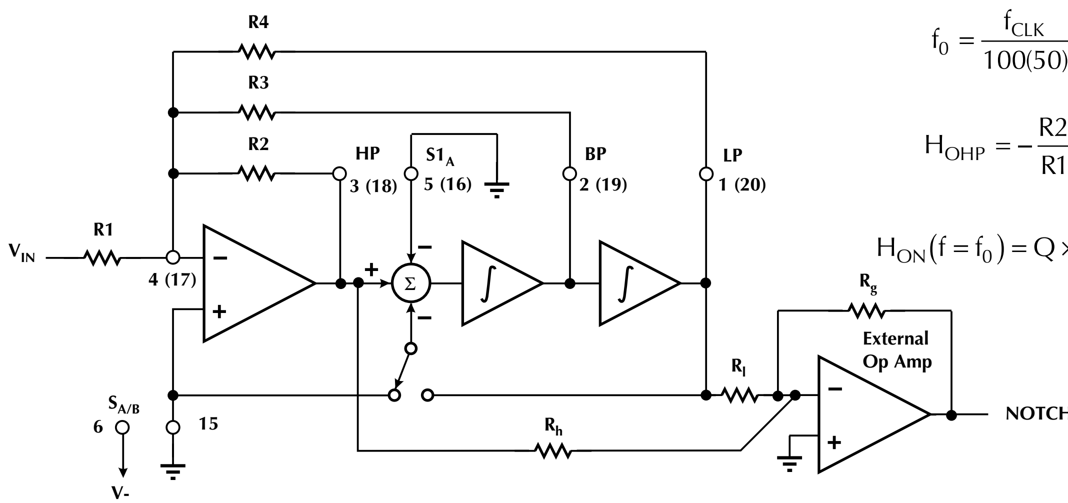


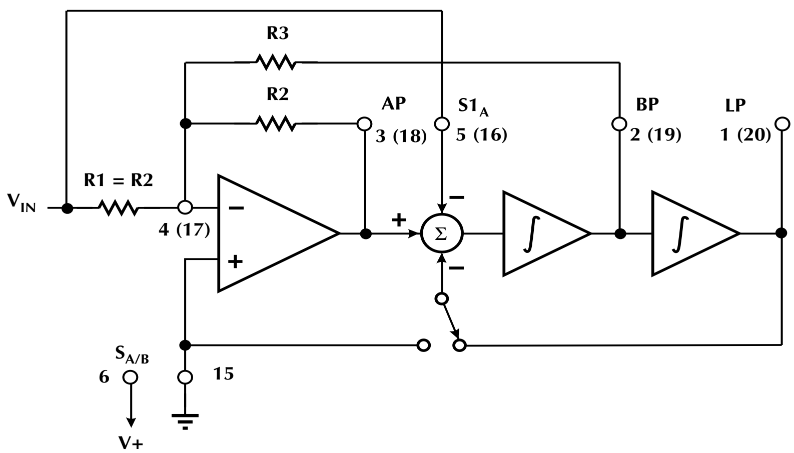
Figure 24. Mode 3a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Notch — ½ ML2111

OPERATION MODES (Continued)

above the center frequency through the resistor ratio R_h/R_l. Because of this, modes 3 and 3a are the most versatile and useful modes for cascading second order sections to obtain high order elliptic filters. For very selective bandpass/bandreject filters the mode 3a approach , as in Figure 24, yields better dynamic range since the external op amp helps to optimize the dynamics of the output nodes of the ML2111.

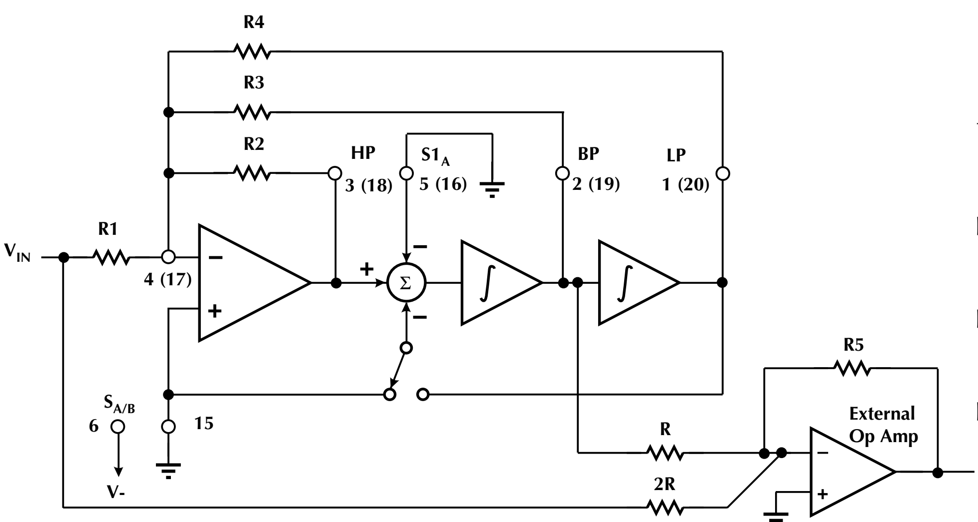
Modes 4 and 5 are useful for constructing allpass response filters. Mode 4, Figure 25, gives an allpass response, but due to the sampled nature of the filter, a slight 0.5 dB peaking can occur around the center frequency. Mode 4a (Figure 26) gives a non-inverting output, but requires an external op amp. Mode 5 is recommended if this response is unacceptable. Mode 5 (Figure 27) gives a flatter response than mode 4 if R1 = R2 = 0.02 × R4.

Modes 6 and 7 are used to construct 1st order filters. Mode 6a (Figure 28) gives a lowpass and a highpass single pole response. Mode 6b (Figure 29) gives an inverting and non-inverting lowpass single pole filter response. Mode 7 (Figure 30) gives an allpass and lowpass single pole response.



$$f_o = \frac{f_{CLK}}{100(50)};\ Q = \frac{R3}{R2};\ H_{OAP} = -\frac{R2}{R1};\ H_{OLP} = -2;\ H_{OBP} = -2\left(\frac{R3}{R2}\right)$$

Figure 25. Mode 4: 2nd Order Filter Providing Allpass, Bandpass, Lowpass — ½ ML2111



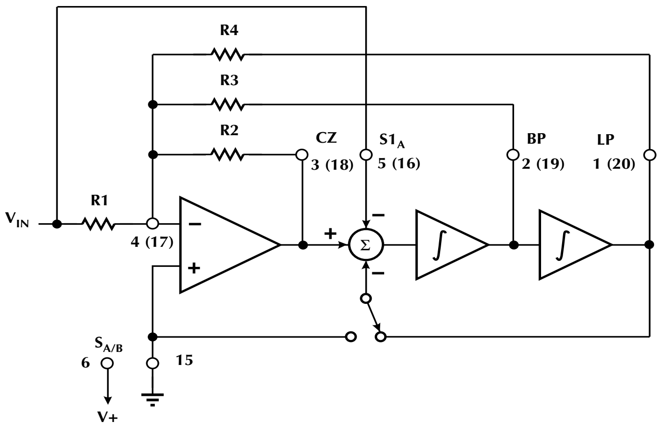
$$f_0 = \frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}};Q = \frac{R3}{R2} \times \sqrt{\frac{R2}{R4}};$$

$$H_{OAP} = \frac{R5}{2R};H_{OHP} = -\frac{R2}{R1};$$

$$H_{OLP} = -\frac{R4}{R1};$$

$$H_{OBP} = -\frac{R3}{R1}$$

Figure 26. Mode 4a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Allpass — ½ ML2111



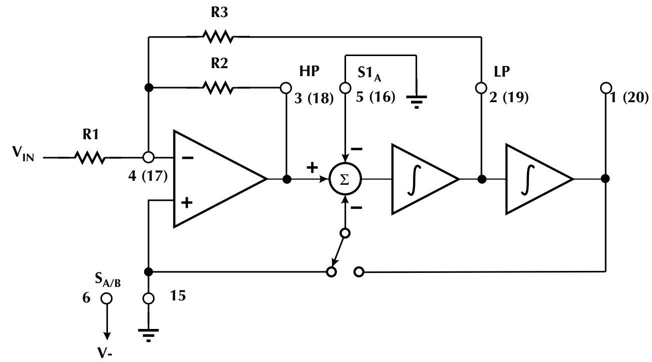
$$f_0 = \frac{f_{CLK}}{100(50)} \times \sqrt{1+\frac{R2}{R4}}; f_Z = \frac{f_{CLK}}{100(50)} \times \sqrt{1-\frac{R1}{R4}};$$

$$Q = \frac{R3}{R2} \times \sqrt{1+\frac{R2}{R4}}; Q_Z = \frac{R3}{R1} \times \sqrt{1-\frac{R1}{R4}};$$

$$H_{OBP} = \frac{R3}{R2} \times \left(1+\frac{R2}{R1}\right); H_{OZ}(f \to 0) = \frac{(R4/R1)-1}{(R4/R2)+1};$$

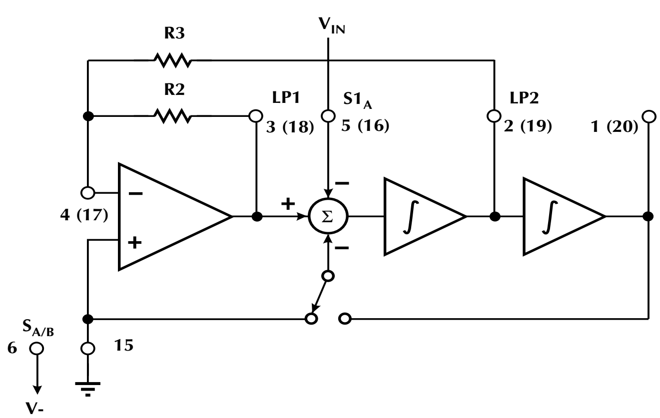
$$H_{OZ}\left(f \to \frac{f_{CLK}}{2}\right) = \frac{R2}{R1}; H_{OLP} = \frac{1+(R2/R1)}{1+(R2/R4)}$$

Figure 27. Mode 5: 2nd Order Filter Providing Numerator Complex Zeroes, Bandpass, Lowpass — ½ ML2111



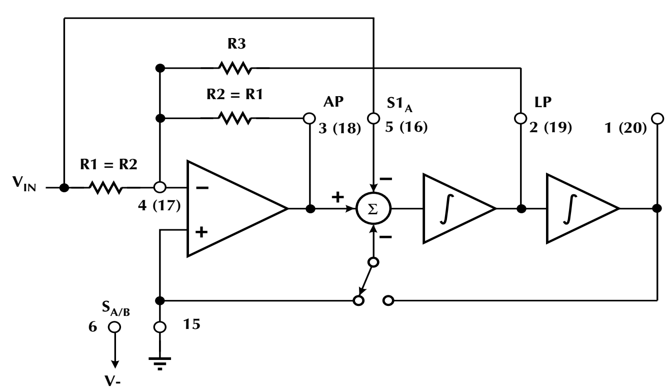
$$f_C = \frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}; H_{OLP} = -\frac{R3}{R1}; H_{OHP} = -\frac{R2}{R1}$$

Figure 28. Mode 6a: 1st Order Filter Providing Highpass, Lowpass — ½ ML2111



$$f_C = \frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}; H_{OLP1} = 1; H_{OLP2} = -\frac{R3}{R2}$$

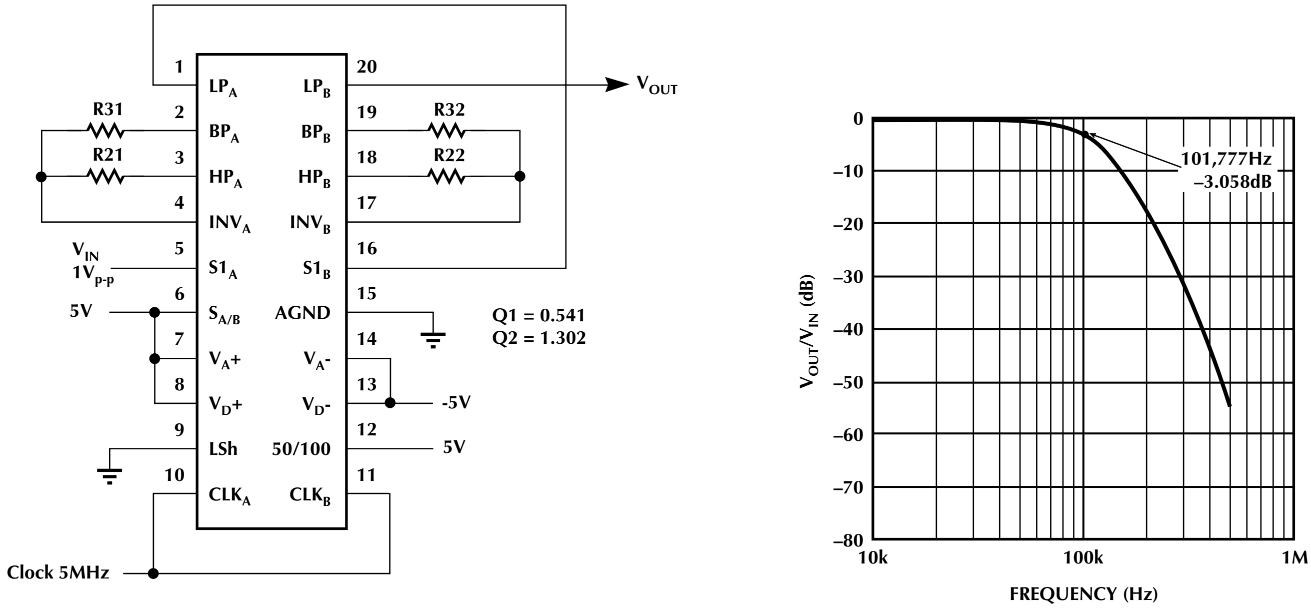
Figure 29. Mode 6b: 1st Order Filter Providing Lowpass — ½ ML2111



$$f_P = f_Z = \frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}; H_{OLP} = 2 \times -\frac{R2}{R3}$$

$$|\text{GAIN AT OUTPUT}| = 1 \text{ FOR } 0 \le f \le \frac{f_{CLK}}{2}$$

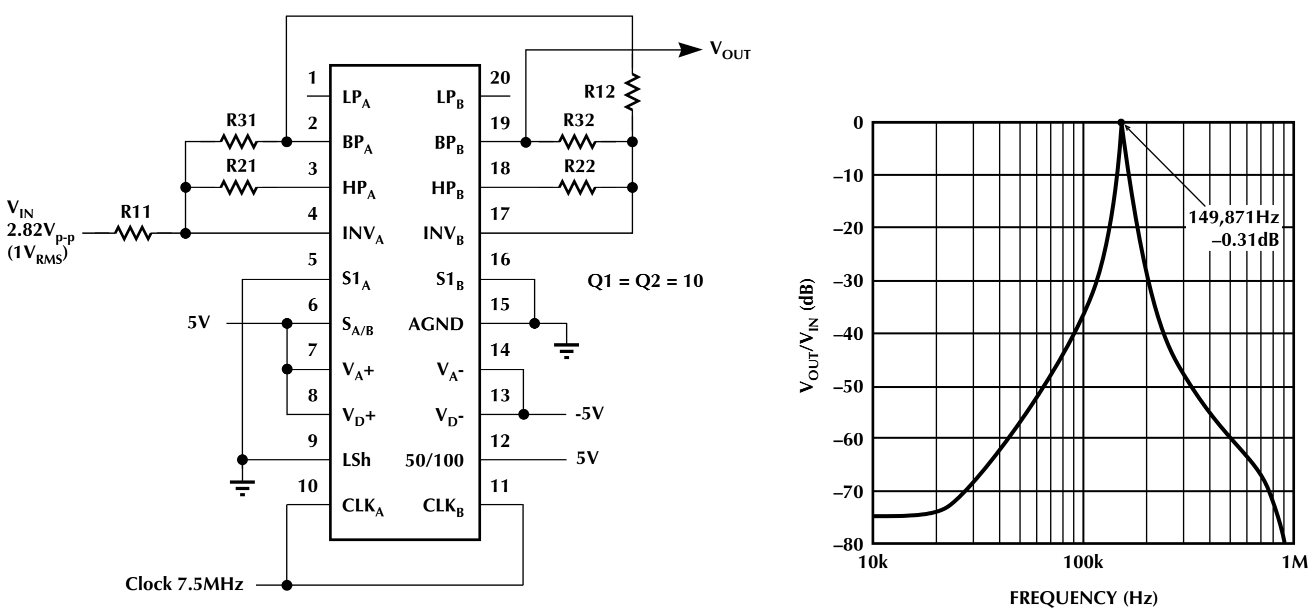
Figure 30. Mode 7: 1st Order Filter Providing Allpass, Lowpass — ½ ML2111



1% RESISTOR VALUES

R21 = 3746Ω R22 = 1996Ω
R31 = 2003Ω R32 = 2604Ω

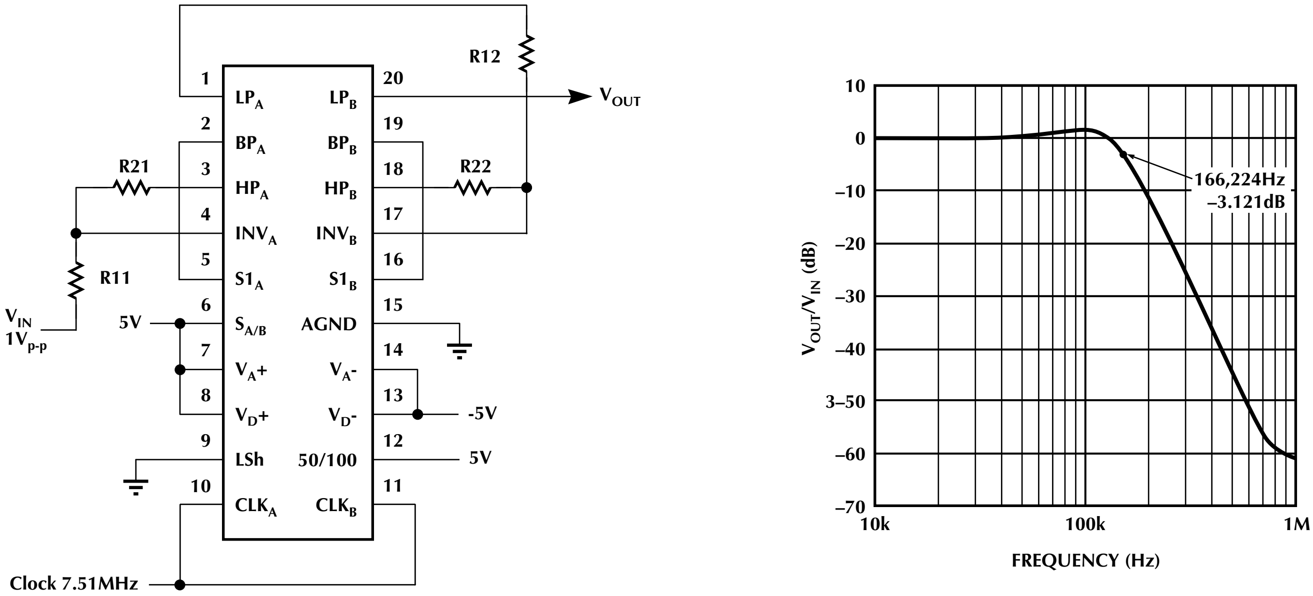
Figure 31. 4th Order, 100kHz Lowpass Butterworth Filter Obtained by Cascading Two Sections in Mode 1a.



RESISTOR VALUES

R11 = 20kΩ R12 = 20kΩ
R21 = 2kΩ R22 = 2kΩ
R31 = 20kΩ R32 = 20kΩ

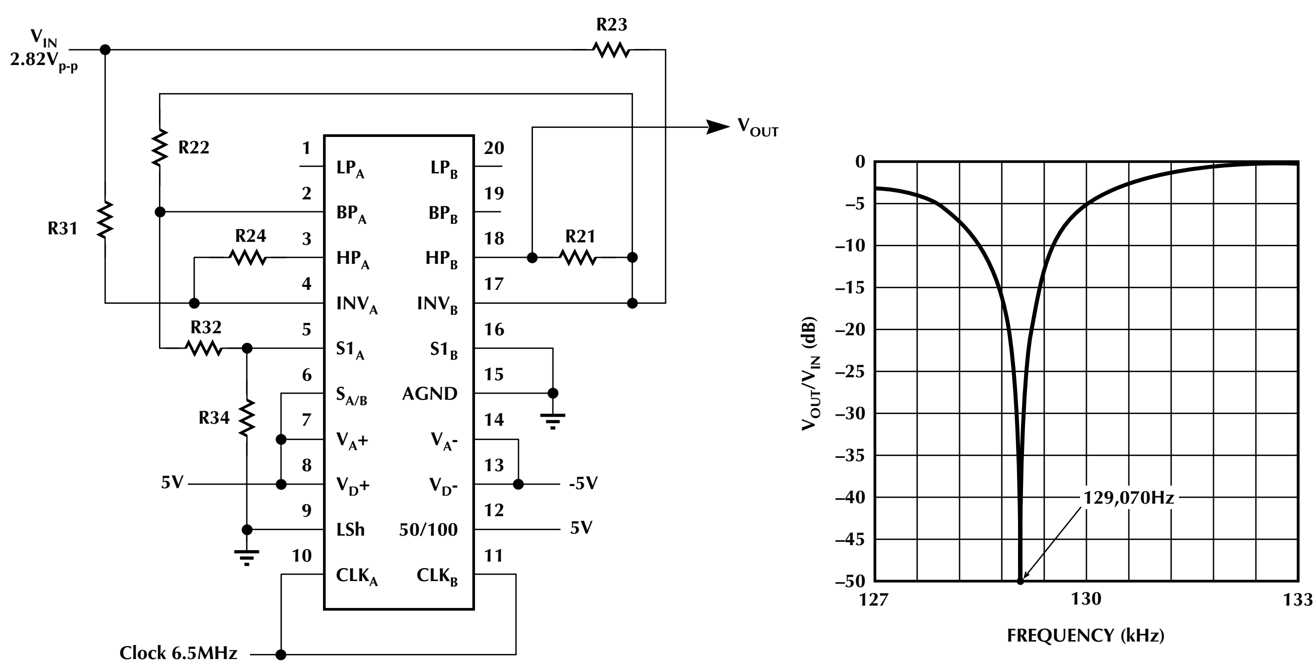
Figure 32. Cascasding 2 Sections Connected in Mode 1, each with Q = 10, to obtain a Bandpass Filter with Q = 15.5, and f_0 = 150kHz (f_{CLK} = 7.5MHz).



RESISTOR VALUES

R11 = R21 = R12 = R22 = 2.0kΩ

Figure 33. Cascading Two Sections in Mode 1d, Each with Q =1, (Independent of Resistor Ratios) to Create a Sharper 4th Order Lowpass Filter.



1% RESISTOR VALUES

R21 = R22 = R23 = R24 = 2kΩ

R31 = 80kΩ R32 = 4.9kΩ

R34 = 100Ω

Figure 34. Notch Filter with Q = 50 and f_0 = 130kHz. This Circuit Uses Side A in Mode 1d and the Side B Op Amp to Create a Notch Whose Depth is Controlled by R31. The Notch is Created by Subtracting the Bandpass from V_{IN}. The Bandpass of Side A is Subtracted Using the Op Amp of Side B.

OPERATION MODES (Continued)

Mode 1a is a good choice when Butterworth filters are desired since they have poles in a circle with the same f_0. Figure 31 shows an example of a 4th order, 100kHz lowpass Butterworth filter clocked at 5MHz.

A monotonic passband response with a smooth transition band results, showing the circuit's low sensitivity, even though 1% resistors are used which results in an approximate value of Q.

Figure 32 gives an example of a 4th order bandpass filter implemented by cascading 2 sections, each with a Q of 10. This figure shows the amplitude response when f_{CLK} = 7.5MHz, resulting in a center frequency of 150kHz and a Q of 15.5.

Figure 33 uses mode 1d of a 4th order flter where each section has a Q of 1, independent of resistor ratios. In this mode, the input amplifier is outside the damping (Q) loop. Therefore, its finite bandwidth does not degrade the response at high frequency. This allows the amplifier to be used as an anti-aliasing and continuous smoothing fliter by placing a capacitor across R2.

OFFSETS

Switched capacitor integrators generally exhibit higher input offsets than discrete RC integrators.

These offsets are mainly the charge injection of the CMOS switchers into the integrating capacitors. The internal op amp offsets also add to the overall offset budget.Figure 35 shows half of the ML2111 filter with its equivalent input offsets V_{OS1}, V_{OS2}, & V_{OS3}.

The DC offset at the filter bandpass output is always equal to V_{OS3}. The DC offsets at the remaining two outputs (Notch and LP) depend on the mode of operation and external resistor ratios. Table 3 illustrates this.

It is important to know the value of the DC output offsets, especially when the filter handles input signals with large dynamic range. As a rule of thumb, the output DC offsets increase when:

1. The Qs decrease
2. The ratio (f_{CLK}/f_o) increases beyond 100:1. This is done by decreasing either the (R2/R4) or the R6/(R5 + R6) resistor ratios.

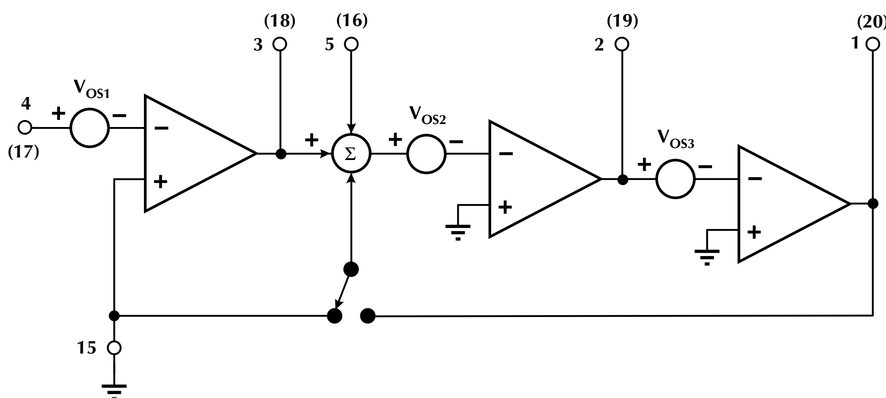


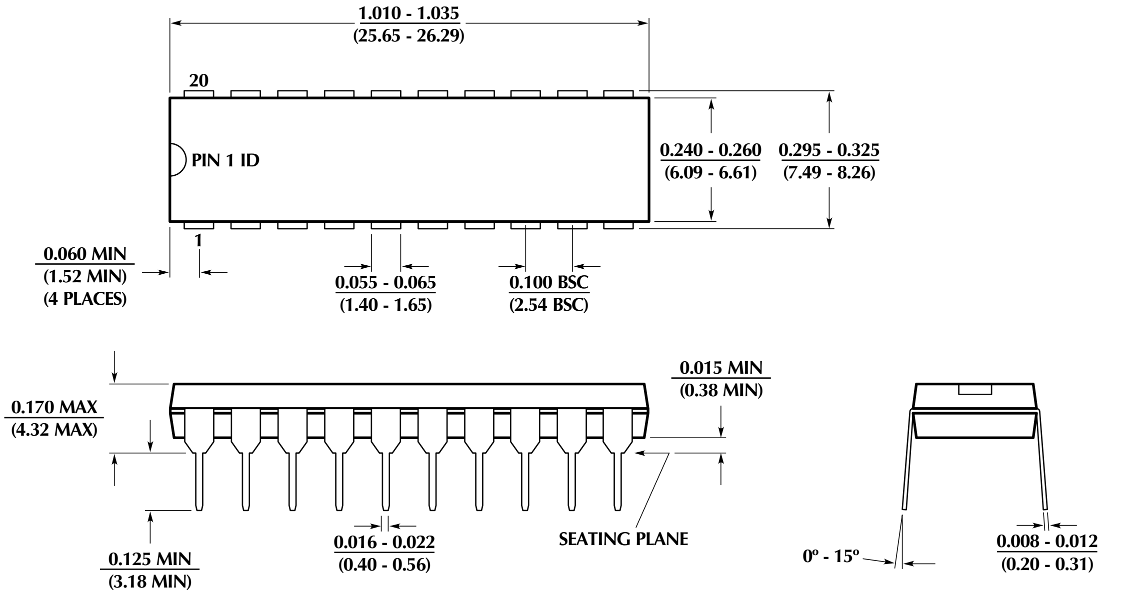
Figure 35. Equivalent Input Offsets of ½ of an ML2111 Filter.

MODE	V_{OSN} N/AP/HP_A, N/AP/HP_B	V_{OSBP} BP_A, BP_B	V_{OSLP} LP_A, LP_B
1, 4	V_{OS1} [(1/Q) + 1 + ||H_{OLP}||] – V_{OS3}/Q	V_{OS3}	$V_{OSN} - V_{OS2}$
1a	V_{OS1} [1 + (1/Q)] – V_{OS3}/Q	V_{OS3}	$V_{OSN} - V_{OS2}$
1b	V_{OS1} [(1/Q)] + 1 + R2/R1] – V_{OS3}/Q	V_{OS3}	~($V_{OSN} - V_{OS2}$) (1 + R5/R6)
1c	V_{OS1} [(1/Q)] + 1 + R2/R1] – V_{OS3}/Q	V_{OS3}	$\sim\left(V_{OSN} - V_{OS2}\right)\frac{R5+R6}{R5+2R6}$
1d	V_{OS1} [1 + R2/R1]	V_{OS3}	$V_{OSN} - V_{OS2} - V_{OS3}/Q$
2, 5	[V_{OS1} (1 + R2/R1 + R2/R3 + R2/R4) – V_{OS3}(R2/R3)] × [R4/(R2 + R4)] + V_{OS2}[R2/(R2 + R4)]	V_{OS3}	$V_{OSN} - V_{OS2}$
2a	[V_{OS1} (1 + R2/R1 + R2/R3 + R2/R4) – V_{OS3}(R2/R3)] × $\left[\frac{R4(1+k)}{R2+R4(1+k)}\right] + V_{OS2}\left[\frac{R2}{R2+R4(1+k)}\right]; k = \frac{R6}{R5+R6}$	V_{OS3}	$\sim\left(V_{OSN} - V_{OS2}\right)\frac{R5+R6}{R5+2R6}$
2b	[V_{OS1} (1 + R2/R1 + R2/R3 + R2/R4) – V_{OS3}(R2/R3)] × $\left[\frac{R4(k)}{R2+R4(k)}\right] + V_{OS2}\left[\frac{R2}{R2+R4(k)}\right]; k = \frac{R6}{R5+R6}$	V_{OS3}	$\sim\left(V_{OSN} - V_{OS2}\right)\left(1+\frac{R5}{R6}\right)$
3, 4a	V_{OS2}	V_{OS3}	$V_{OS1}\left[1+\frac{R4}{R1}+\frac{R4}{R2}+\frac{R4}{R3}\right] - V_{OS2}\left(\frac{R4}{R2}\right) - V_{OS3}\left(\frac{R4}{R3}\right)$

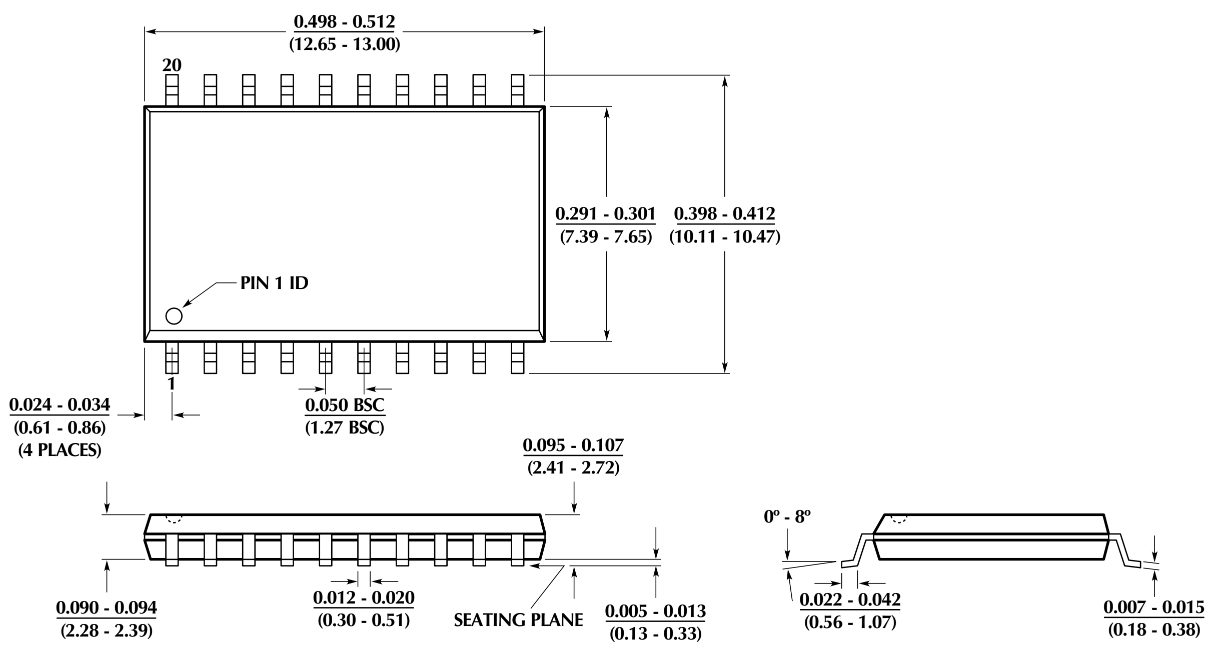
Table 3.

PHYSICAL DIMENSIONS inches (millimeters)

Package: P20
20-Pin PDIP



Package: S20
20-Pin SOIC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML2111CCP (EOL)	0°C to 70°C	20-Pin PDIP (P20)
ML2111CCS	0°C to 70°C	20-Pin SOIC (S20)
ML2111CIP (OBS)	-40°C to 85°C	20-Pin PDIP (P20)

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