Micro Linear

ML4665

Low Cost Single Chip 10BASE-FL Transceiver

GENERAL DESCRIPTION

The ML4665 is a low power, low cost, single chip 10BASE-FL transceiver. The ML4665 contains a fiber optic data quantizer and an LED output driver for direct connection to an optical module(s). The ML4665 offers a standard IEEE 802.3 AU interface that allows it to be directly connected to industry standard manchester encoder/decoder chips or an AUI connector.

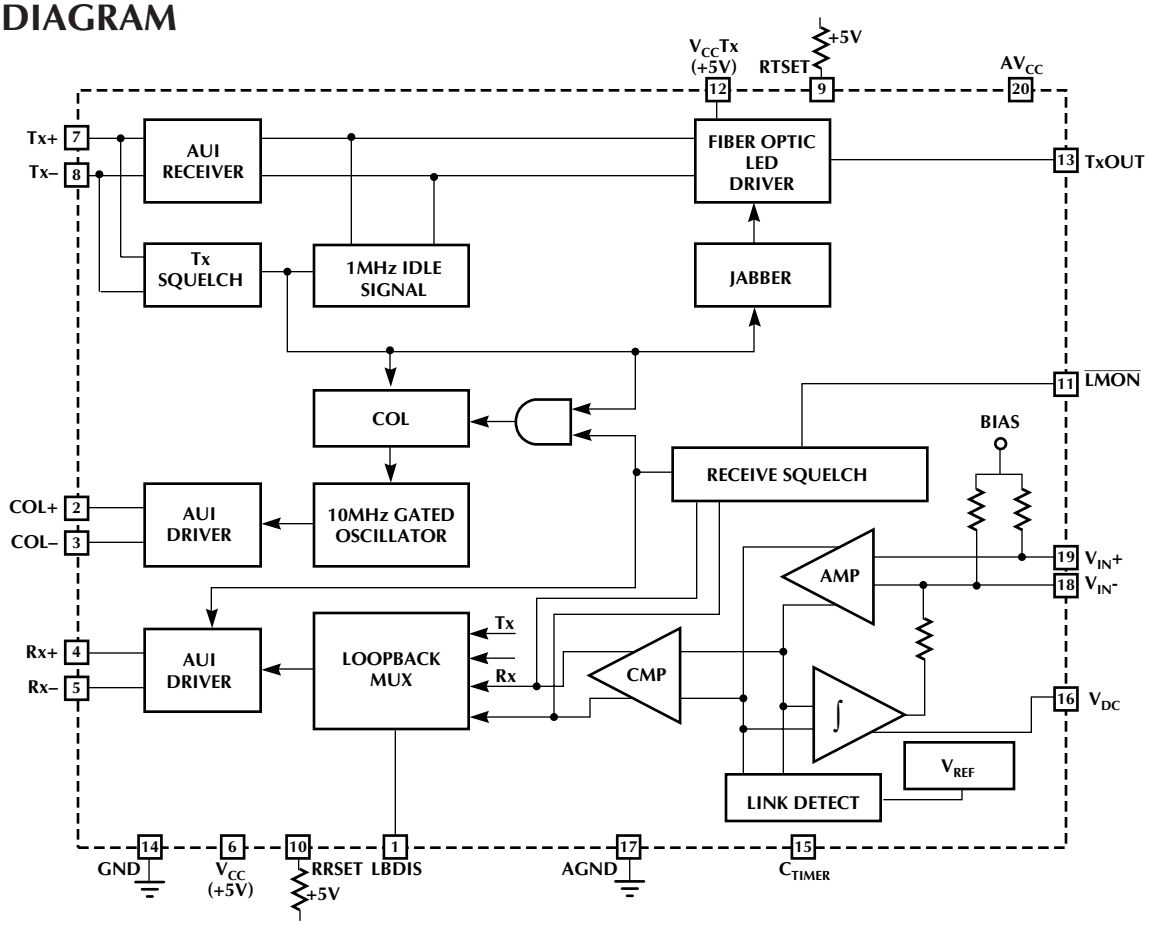
The ML4665 provides a highly integrated solution that requires a minimal number of external components. The transmitter offers a 100mA maximum current drive output that directly drives a fiber optic LED transmitter. The receiver offers a highly stable fiber optic data quantizer capable of accepting input signals as low as $2mV_{P-P}$ with a 55dB dynamic range.

The ML4665 is a lower cost version of the industry standard ML4663. To achieve lower cost, the ML4665 eliminates some functionality (as described below) and is packaged in a 20-lead PLCC package.

FEATURES

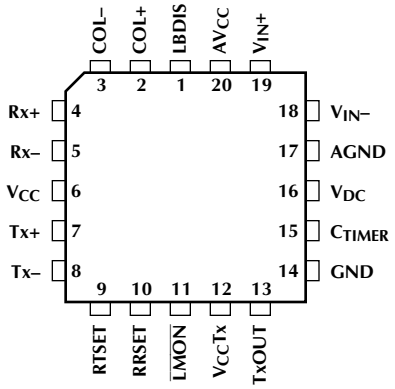
- Lower cost single chip solution for 10BASE-FL internal or external Medium Attachment Units (MAUs)
- Incorporates an AU interface
- Highly stable data quantizer with 55dB input dynamic range
- Input sensitivity as low as $2mV_{P-P}$
- 100mA maximum current driven fiber optic LED driver for accurate launch power
- Single +5 volt supply
- No crystal or clock required
- Link monitor LED indicator

BLOCK DIAGRAM



PIN CONNECTION

ML4665
20-Pin PLCC (Q20)



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	LBDIS	Loopback disable. When this pin is tied to V_{CC}, the AUI transmit pair data is not looped back to the AUI receive pair. The ML4665 will now operate in the full duplex mode. When tied to GND or left floating, the AUI transmit pair data is looped back to the AUI receive pair, except during collision. The ML4665 will now operate in the half duplex mode.
2	COL+	Gated 10MHz oscillation used to indicate a collision or jabber. Balanced differential line driver outputs that meet AUI specifications.
3	COL–	
4	Rx+	Manchester encoded receive data output to the local device. Balanced differential line driver outputs that meet AUI specifications.
5	Rx–	
6	V_{CC}	+5 volt power input.
7	Tx+	Balanced differential line receiver inputs that meet AUI specifications. These inputs may be transformer or capacitively coupled. The Tx input pins are internally DC biased for AC coupling.
8	Tx–	
9	RTSET	Sets the current driven output of the transmitter.
10	RRSET	A 1% 61.9kΩ resistor tied from this pin to V_{CC} sets the biasing currents for internal nodes.
11	$\overline{LMON}$	Link Monitor "Low Light" LED status output. This pin is pulled low when the voltage on the V_{IN}+, V_{IN}– inputs exceed the minimum threshold and there are transitions on V_{IN}+, V_{IN}– indicating an idle signal or active data. If either the voltage on the V_{IN}+, V_{IN}– inputs fall below the minimum threshold or transitions cease on V_{IN}+, V_{IN}–, $\overline{LMON}$ will go high. Active low LED driver, open collector.
12	V_{CC}Tx	+5 volt supply for fiber optic LED driver.
13	TxOUT	Fiber optic LED driver output.
14	GND	Ground Reference.
15	C_{TIMER}	A capacitor from this pin to V_{CC} determines the Link Monitor response time.
16	V_{DC}	An external capacitor on this pin integrates an error signal which nulls the offset of the input amplifier. If the DC feedback loop is not being used, this pin should be connected to V_{REF}.
17	AGND	Analog Filtered Ground.
18	V_{IN}–	This input pin should be capacitively coupled to the input source or to filtered AV_{CC}. (The input resistance is approximately 1.3kΩ.)
19	V_{IN}+	This input pin should be capacitively coupled to the input source or to filtered AV_{CC}. (The input resistance is approximately 1.3kΩ.)
20	AV_{CC}	Analog Filtered +5 volts.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Power Supply Voltage Range
  V_{CC} ..... GND –0.3 to 6V
Input Voltage Range
  Digital Inputs
    (SQEN, LBDIS) ..... GND –0.3 to V_{CC} +0.3V
  Tx+, Tx–, V_{IN}+, V_{IN}– ..... GND –0.3 to V_{CC} +0.3V
Input Current
  RRSET, RTSET, $\overline{LMON}$ 60mA
Output Current
  TxOUT 120mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering) ..... 260°C
Thermal Resistance (θ_{JA}) ..... 78°C/W

OPERATING CONDITIONS

Supply Voltage (V_{CC}) ..... 5V ± 5%
LED on Current 10mA
RRSET ..... 61.9kΩ ± 1%
RTSET ..... 115Ω ± 1%

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = Operating Temperature Range, V_{CC} = V_{CC}Tx = 5V ± 5% (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Power Supply Current I_{CC}: While Transmitting	V_{CC} = 5V, RTSET = 115Ω (Note 2)			140	mA
V_{OL}	LED Driver: V_{OL}	I_{OL} = 10mA (Note 3)			0.8	V
I_{OUT}	Transmit Peak Output Current	RTSET = 115Ω (Note 4)	44	52	57	mA
V_{SQ}	Transmit Squelch Voltage Level (Tx+, Tx–)		–300	–250	–200	mV
V_{DO}	Differential Output Voltage (Rx±, COL±)		±550		±1200	mV
V_{CM}	Common Mode Output Voltage (Rx±, COL±)			4.0		V
V_{DOO}	Differential Output Voltage Imbalance (Rx±, COL±)				±40	mV
V_{LBTH}	LBDIS Threshold	Loopback disabled	V_{CC} – 0.1			V
		Loopback enabled			1.0	V
V_{TXCM}	Common Mode Voltage (Tx+, Tx–)			3.5		V
V_{INCM}	Common Mode Voltage (V_{IN}+, V_{IN}–)			1.65		V
A_V	Amplifier Gain			100		V/V
V_{ISR}	Input Signal Range		2		1600	mV_{P-P}
V_N	Input Referred Noise	50MHz BW		25		µV
R_{IN}	Input Resistance	V_{IN}+ = V_{IN}–	0.8	1.3	2.0	kΩ
V_{TH}	Input Threshold Voltage		5	6	7	mV
H	Hysteresis			20		%

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Transmit					
F_{TXIDF}	Transmit Idle Frequency	0.85		1.25	MHz
t_{TXDC}	Transmit Idle duty Cycle	45		55	%
t_{TXNPW}	Transmit Turn-On Pulse Width		20		ns
t_{TXODY}	Transmit Turn-On Delay			200	ns
t_{TXLP}	Transmit loopback Start-up Delay			500	ns
t_{TXFPW}	Transmit Turn-Off Pulse Width		180		ns
t_{TXSOI}	Transmit Start of Idle	400		2100	ns
t_{TXSDY}	Transmit Steady State Propagation Delay		15	50	ns
t_{TXJ}	Transmit Jitter into 31Ω Load			±1.5	ns
Receive					
F_{RXSFT}	Receive Squelch Frequency Threshold	2.51		4.5	MHz
t_{RXODY}	Receive Turn-On Delay			285	ns
t_{RXFX}	Last Bit Received to Slow Decay Output	230	300		ns
t_{RXSDY}	Receive Steady State Propagation Delay		15	50	ns
t_{RXJ}	Receive Jitter			±1.5	ns
t_{AR}	Differential Output Rise Time 20% to 80% (Rx±, COL±)		4		ns
t_{AF}	Differential Output Fall Time 20% to 80% (Rx±, COL±)		4		ns
Collision					
t_{CPSQE}	Collision Present to SQE Assert	0		350	ns
t_{SQEXR}	Time for SQE to Deactivate After Collision	0		700	ns
F_{CLF}	Collision Frequency	8.5		11.5	MHz
P_{CLPDC}	Collision Pulse Duty Cycle	40	50	60	%
Jabber and $\overline{\text{LMON}}$ Timing					
t_{JAD}	Jabber Activation Delay	20	70	150	ms
t_{JRT}	Jabber Reset Unjab Time	250	450	750	ms
t_{JSQE}	Delay from Outputs Disabled to Collision Oscillator On		100		ns
t_{LLPH}	Low Light Present to $\overline{\text{LMON}}$ High	3	5	10	µs
t_{LLCL}	Low Light Present to $\overline{\text{LMON}}$ Low	250		750	ms

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 2: This dose not include the current from the AUI pull-down resistors, or LED status outputs.
Note 3: LED drivercan sink up to 20mA, but V_{OL} will be higher.
Note 4: Does not include pre-bias current for fiber optic LED which would typically be 3mA.

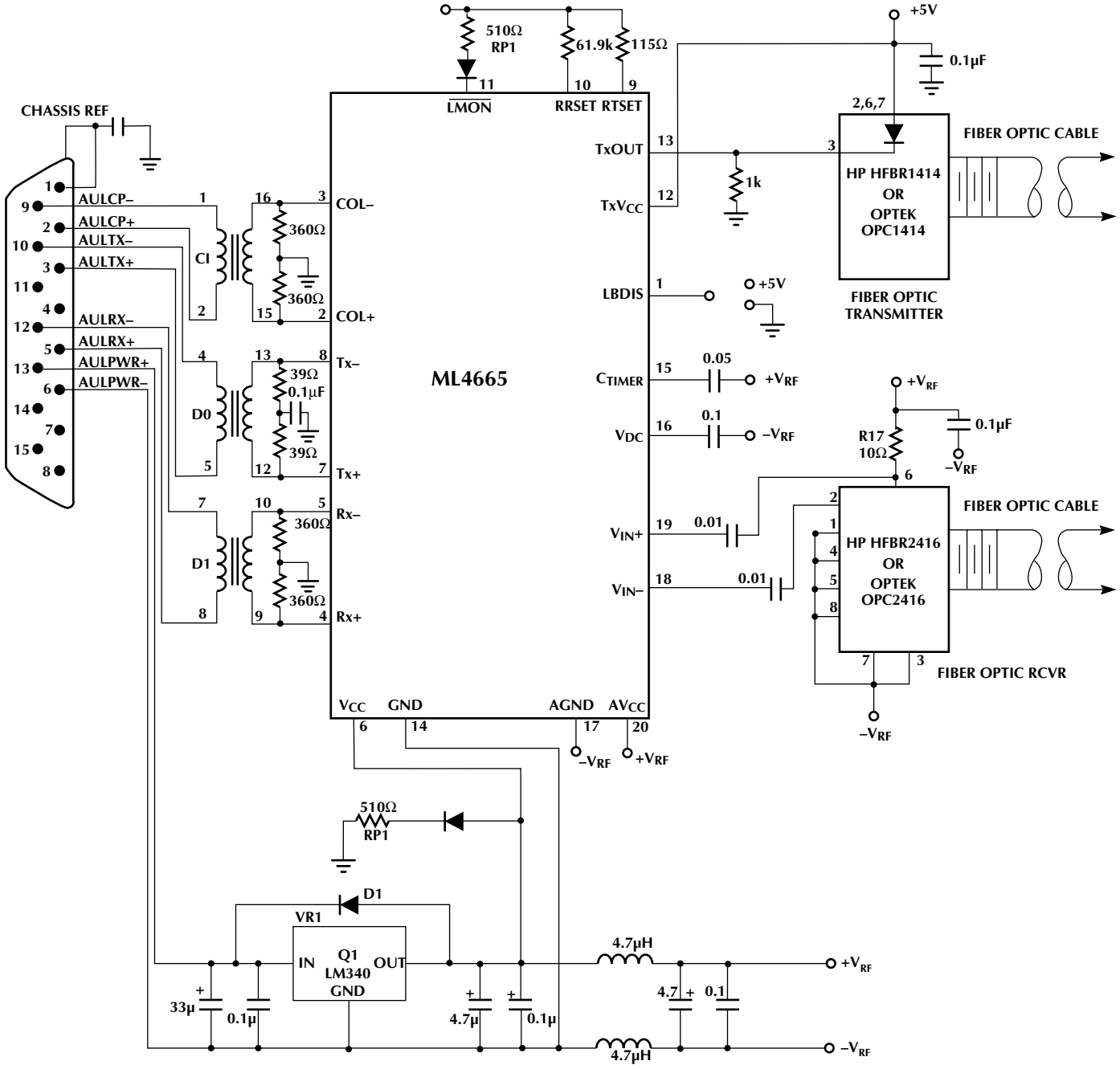


Figure 1. ML4665 Schematic Diagram

SYSTEM DESCRIPTION

Figure 1 shows a schematic diagram of the ML4665 in an internal or external 10BASE-FL MAU. On one side of the transceiver is the AU interface and the other is the fiber optic interface. The AU interface is AC coupled when used in an external transceiver or an internal transceiver. The AU interface for an external transceiver includes isolation transformers, some biasing resistors, and a voltage regulator for power.

The fiber optic side of the transceiver requires an external fiber optic transmitter and fiber optic receiver. The transmitter uses a current driven output that directly drives the fiber optic transmitter. The receive side of the transceiver accepts the data after passing through a fiber optic receiver, which consists of a module containing a pin diode and a transimpedance amplifier.

AU INTERFACE

The AU interface consists of 3 pairs of signals: DO, CI and DI (Figure 1). The DO pair contains transmit data from the DTE which is received by the transceiver and sent out onto the fiber optic cable. The DI pair contains valid data that has been either received from the fiber optic cable or looped back from the DO, and output through the DI pair to the DTE. The CI pair indicates whether a collision has occurred. It is an output that oscillates at 10MHz if a collision or Jabber has taken place, otherwise it remains idle.

When the transceiver is external, these three pairs are AC coupled through isolation transformers, while an internal transceiver may be capacitively coupled. Tx+, Tx– is internally DC biased (shifted up in voltage) for the proper common mode input voltage.

The two 39Ω 1% resistors (or one 78Ω 1% resistor) tied to the Tx+ and Tx– pins will provide the proper termination. The CI and DI pair, which are output from the transceiver to the AUI cable, require 360Ω pull down resistors when terminated with a 78Ω load. However, on a DTE card, CI and DI do not need 78Ω terminating resistors. This also means that the pull down resistors on CI and DI can be 1kΩ or greater depending upon the particular Manchester encoder/decoder chip used. Using higher value pull down resistors as in a DTE card will save power. Refer to Application Note 13 for a more detailed explanation of the AUI pull-down resistors.

The AUI drivers are capable of driving the full 50 meters of cable length and have a rise and fall time of typically 4ns. In the idle state, the outputs go to the same voltage to prevent DC standing current in the isolation transformers.

TRANSMISSION

The transmit function consists of detecting the presence of data from the AUI DO input (Tx+, Tx–) and driving that data onto the fiber optic LED transmitter. A positive signal on the Tx+ lead relative to the Tx– lead of the DO circuit will result in no current, hence the fiber optic LED is in a low light condition. When Tx+ is more negative than Tx–, the ML4665 will sink current into the chip and the fiber optic LED will light up.

Before data will be transmitted onto the fiber optic cable from the AUI interface, it must exceed the squelch requirements for the DO pair. The Tx squelch circuit serves the function of preventing any noise from being transmitted onto the fiber. This circuit rejects signals with pulse widths less than typically 20ns (negative going), or with levels less than –250mV. Once Tx squelch circuit has unsquelched, it looks for the start of idle signal to turn on the squelch circuit again. The transmitter turns on the squelch again when it receives an input signal at Tx+, Tx– that is more positive than –250mV for more than approximately 180ns.

At the start of a packet transmission, no more than 2 bits are received from the DO circuit, and are not transmitted onto the fiber optic cable. The difference between start-up delays (bit loss plus steady-state propagation delay) for any two packets that are separated by 9.6µs or less will not exceed 200ns.

FIBER OPTIC LED DRIVER

The output stage of the transmitter is a current mode switch which develops the output light by sinking current through the LED into the TxOUT pin. Once the current requirement for the LED is determined, the RTSET resistor is selected. The following equation is used to select the correct RTSET resistor:

$$RTSET = \left(\frac{52mA}{I_{OUT}}\right)115\Omega$$

The ML4665 transmitter output will drive up to 100mA, which requires RTSET to equal 60Ω. The transmitter enters the idle state when it detects start of idle on Tx+ and Tx– input pins. After detecting the start of idle the transmitter switches to a 1MHz output idle signal.

The output current is switched through the TxOUT pin during the on cycle and the V_{CC}Tx pin during the off cycle as shown in figure 2. Since the sum of the current in these two pins is constant, V_{CC}Tx should be connected as close as possible to the V_{CC} connection for the LED.

If not driving an optical LED directly, a differential output can be generated by tying resistors from V_{CC}Tx and TxOUT to V_{CC} as shown in figure 3. The minimum voltage on these two pins should not be less than V_{CC} – 2V.

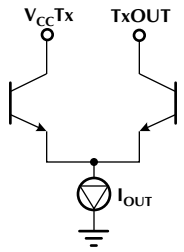


Figure 2. Fiber Optic LED Driver Structure.

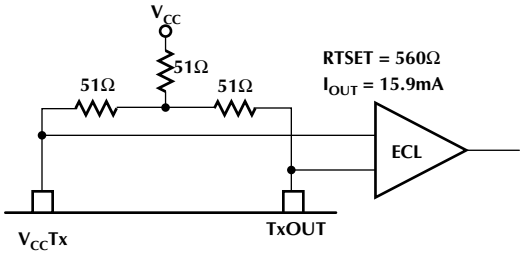


Figure 3. Converting Optical LED Driver Output to Differential ECL.

RECEPTION

The input to the transceiver comes from a fiber optic receiver as shown in figure 1. At the start of packet reception no more than 2.7 bits are received from the fiber cable, and are not transmitted onto the DI circuit. The receive squelch will reject frequencies lower than 2.51MHz.

While in the unsquelch state, the receive squelch circuit looks for the start of idle signal at the end of the packet. Start of idle occurs when the input signal remains idle for more than 160ns. When start of idle is detected, the receive squelch circuit returns to the squelch state and the start of idle signal is output on the DI circuit (Rx+, Rx–).

COLLISION

Whenever the receiver and the transmitter are active at the same time the chip will activate the collision output. The collision output is a differential square wave matching the AUI specifications and capable of driving a 78Ω load. The frequency of the square wave is 10MHz ± 15% with a 60/40 to 40/60 duty cycle. The collision oscillator also is activated Jabber.

LOOPBACK

The loopback function emulates a 10BASE-T transceiver whereby the transmit data sent by the DTE is looped back over the AUI receive pair. Some LAN controllers use this loopback information to determine whether a MAU is connected by monitoring the carrier sense while transmitting. The software can use this loopback information to determine whether a MAU is connected to the DTE by checking the status of carrier sense after each packet transmission.

When data is received by the chip while transmitting, a collision condition exits. This will cause the collision oscillator to turn on and the data on the DI pair will follow V_{IN}+, V_{IN}–. After a collision is detected, the collision oscillator will remain on until either DO or V_{IN}+, V_{IN}– go idle.

Loopback can be disabled by strapping LBDIS to V_{CC}. In this mode the chip operates as a full duplex transmitter and receiver, and collision detection is disabled. A loopback through the transceiver can be accomplished by tying the fiber transmitter to the receiver.

JABBER FUNCTION REQUIREMENTS

The Jabber function prevents a babbling transmitter from bringing down the network. Within the transceiver is a Jabber timer that starts at the beginning of each transmission and resets at the end of each transmission. If the transmission last longer than 20ms the jabber logic disables the transmitter, and turns on the collision signal COL+, COL–. When Tx+ and Tx– finally go idle, a second timer measures 0.5 seconds of idle time before the transmitter is enabled and collision is turned off. Even though the transmitter is disabled during jabber, the 1MHz idle signal is still transmitted.

LOW LIGHT CONDITION

The $\overline{\text{LMON}}$ LED output is used to indicate a low light condition. $\overline{\text{LMON}}$ is activated low when both the receive power exceeds the Link Monitor threshold and there are transitions on V_{IN}+, V_{IN}– less than 3µs apart. If either one of these conditions do not exist, $\overline{\text{LMON}}$ will go high.

INPUT AMPLIFIER

The V_{IN}+, V_{IN}– input signal is fed into a limiting amplifier with a gain of about 100 and input resistance of 1.3kΩ. Maximum sensitivity is achieved through the use of a DC restoration feedback loop and AC coupling the input. When AC coupled, the input DC bias voltage is set by an on-chip network at about 1.7V. These coupling capacitors, in conjunction with the input impedance of the amplifier, establish a high pass filter with 3dB corner frequency, f_L, at

$$f_L = \frac{1}{2\pi 1300 C} \quad (1)$$

Since the amplifier has a differential input, two capacitors of equal value are required. If the signal driving the input is single ended, one of the coupling capacitors can be tied to AV_{CC} as shown in figure 1.

The internal amplifier has a lowpass filter built-in to band limit the input signal which in turn will improve the signal to noise ratio.

Although the input is AC coupled, the offset voltage *within* the amplifier will be present at the amplifier's output. This is represented by V_{OS} in figure 4. Inorder to reduce this error a DC feedback loop is incorporated. This negative feedback loop nulls the offset voltage, forcing V_{OS} to be zero. Although the capacitor on V_{DC} is non-critical, the pole it creates can effect the stability of the feedback loop. To avoid stability problems, the value of this capacitor should be at least 10 times larger than the input coupling capacitors.

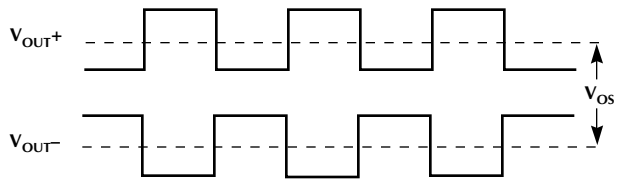


Figure 4.

The comparator is a high-speed differential zero crossing detector that slices and accurately digitizes the receive signal. The output of the comparator is fed in parallel into both the receive squelch circuit and the loopback MUX.

LINK DETECT CIRCUIT AND LOW LIGHT

The link detect circuit monitors the input signal and determines when the input falls below a preset voltage level. When the input falls below a preset voltage, the ML4665 goes into the Low Light state. In the Low Light state the transmitter is disabled, but continues sending the 1MHz idle signal, the loopback is disabled, the receiver is disabled, and the $\overline{LMON}$ LED pin goes to high shutting off the $\overline{LMON}$ LED. To return to the Link Pass state, the optical receiver power must be 20% higher than the shut-off state. This built-in hysteresis adds stability to the Link Monitor circuit. Once the receiver power threshold is exceeded, the ML4665 waits 250ms to 750ms, then checks to see that Tx+. Tx– is idle and no data is being received before re-enabling the transmitter, receiver, loopback circuit, and lighting up the $\overline{LMON}$ LED.

The V_{THADJ} pin is used to adjust the sensitivity of the receiver. The ML4665 is capable of exceeding the 10BASE-FL specifications for sensitivity. The sensitivity is dependent on the layout of the PC board. A good low noise layout will exceed the 10BASE-FL specifications, while a poor layout will fail to meet the sensitivity and BER spec.

The response time of the Link Detect circuit is set by the C_{TIMER} pin. Starting from the link off state the link can be switched on if the input exceeds the set threshold for a time given by:

$$T = \frac{C_{TIMER} \times 0.7V}{700\mu A} \quad (3)$$

To switch the link from on to off, the above time will be doubled. A value of 0.05µF will meet to 10BASE-FL specifications.

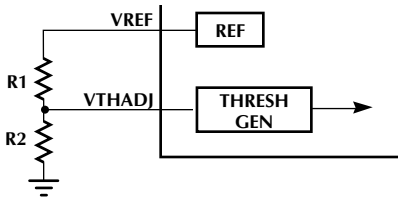


Figure 5.

DIFFERENCES BETWEEN ML4665 AND ML4663/ML4668

The ML4665 is a low cost, reduced pin count alternative to the industry standard ML4663/ML4668. The following itemizes the differences between the devices.

1. The SQEN pin found in the ML4663/ML4668, has been removed. In the ML4665, jabber is always enabled and SQE pulses are not sent on the AUI collision pair following a transmission.
2. The $\overline{JAB}$, $\overline{CLSN}$, $\overline{RCV}$ and $\overline{XMT}$ LED pins on the ML4663/ML4668 have been removed. LEDs showing transmit, receive and collision activity can be added externally. See Figure 6.
3. The V_{REF} and V_{THADJ} pins available on the ML4663/ML4668, have been removed. In the ML4665, these pins are tied together internally, and the threshold is set at 6mV_{P-P} typical. This threshold cannot be externally modified.

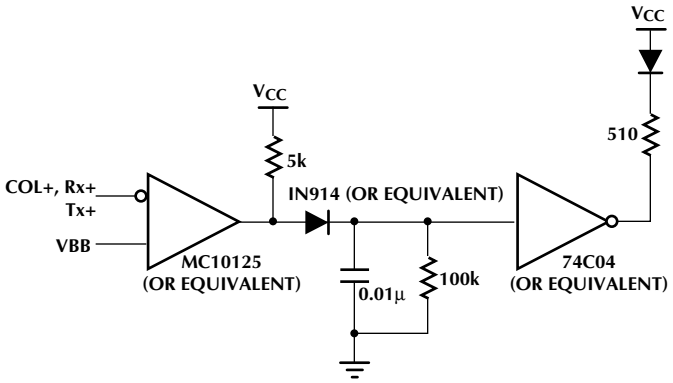


Figure 6.

TIMING DIAGRAMS

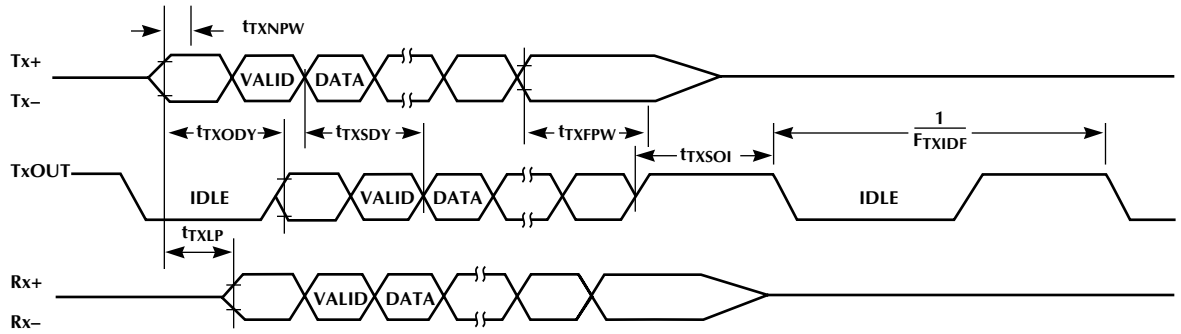


Figure 7. Transmit and Loopback Timing

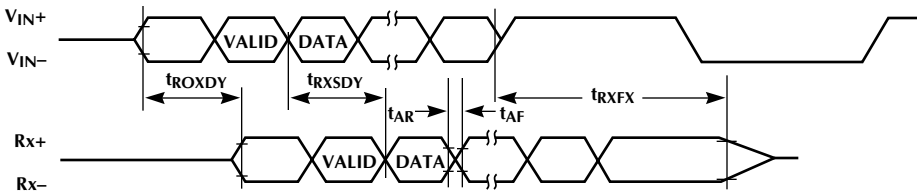


Figure 8. Receive Timing

TIMING DIAGRAMS

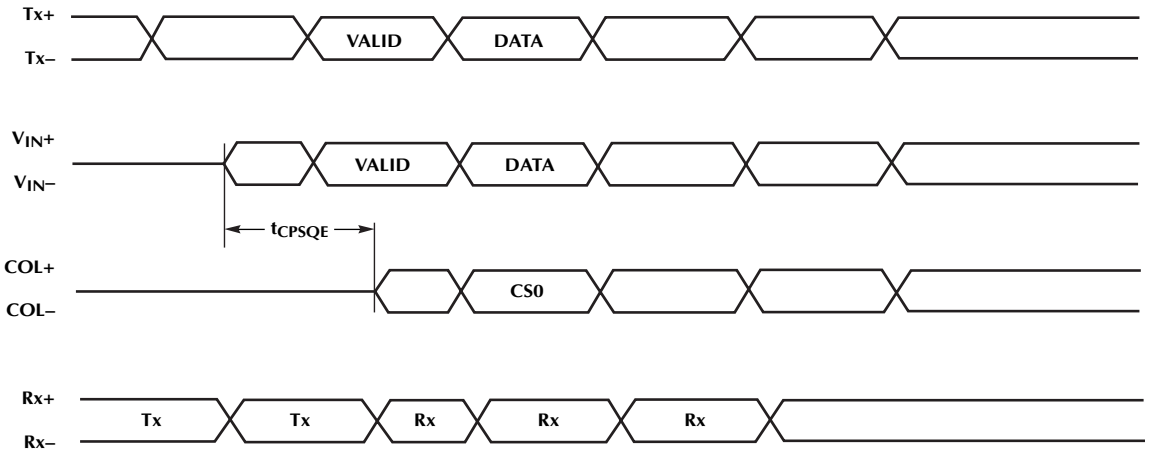


Figure 9. Collision Timing

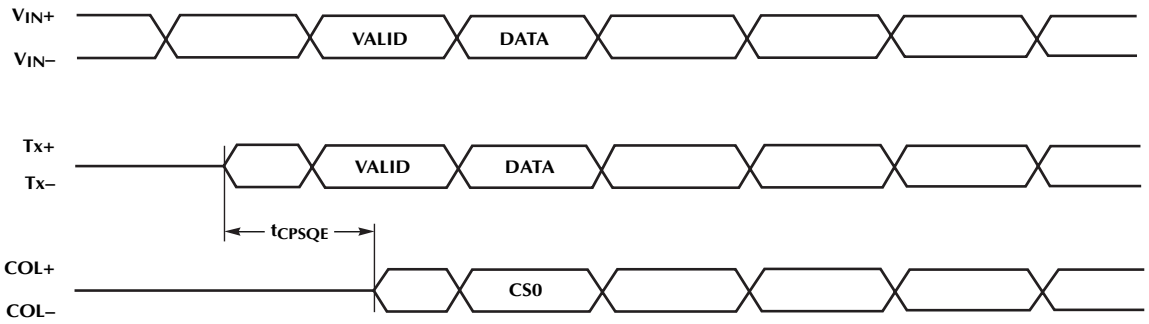


Figure 10. Collision Timing

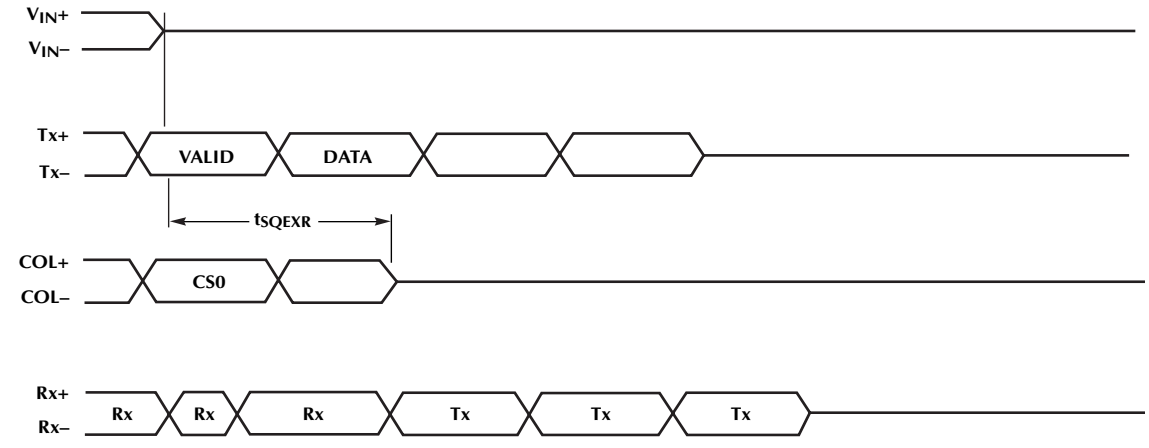


Figure 11. Collision Timing

TIMING DIAGRAMS

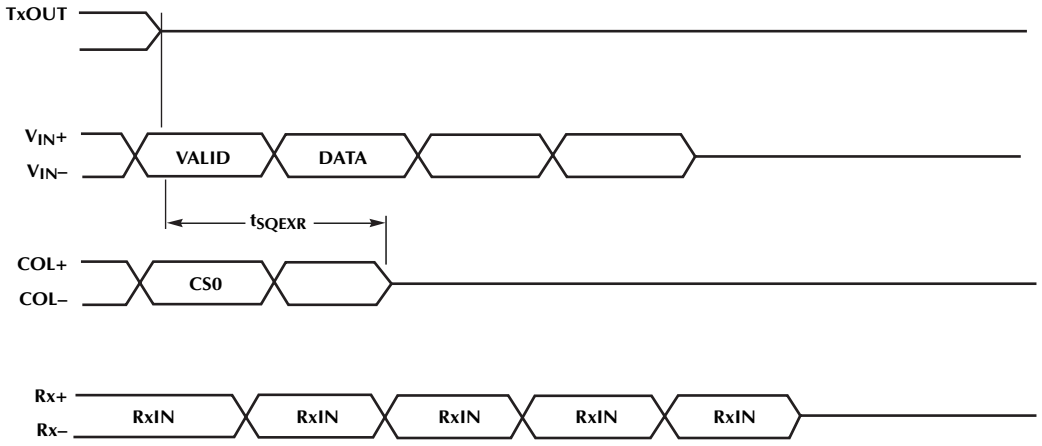


Figure 12. Collision Timing

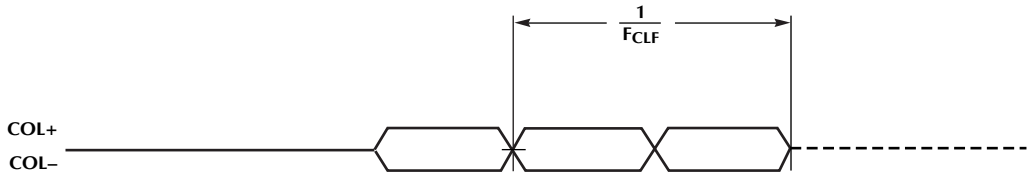


Figure 13. Collision Timing

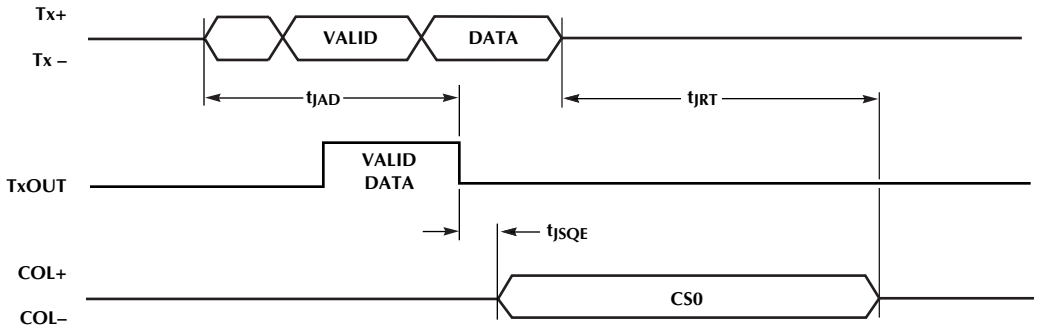


Figure 14. Jabber Timing

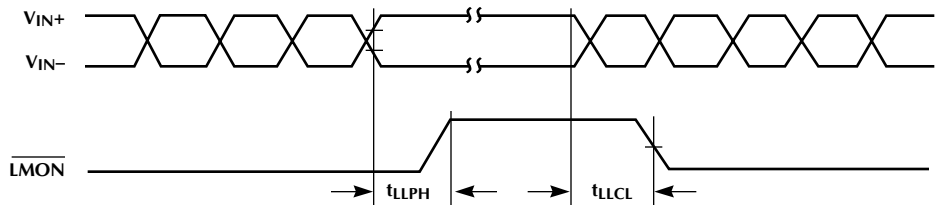
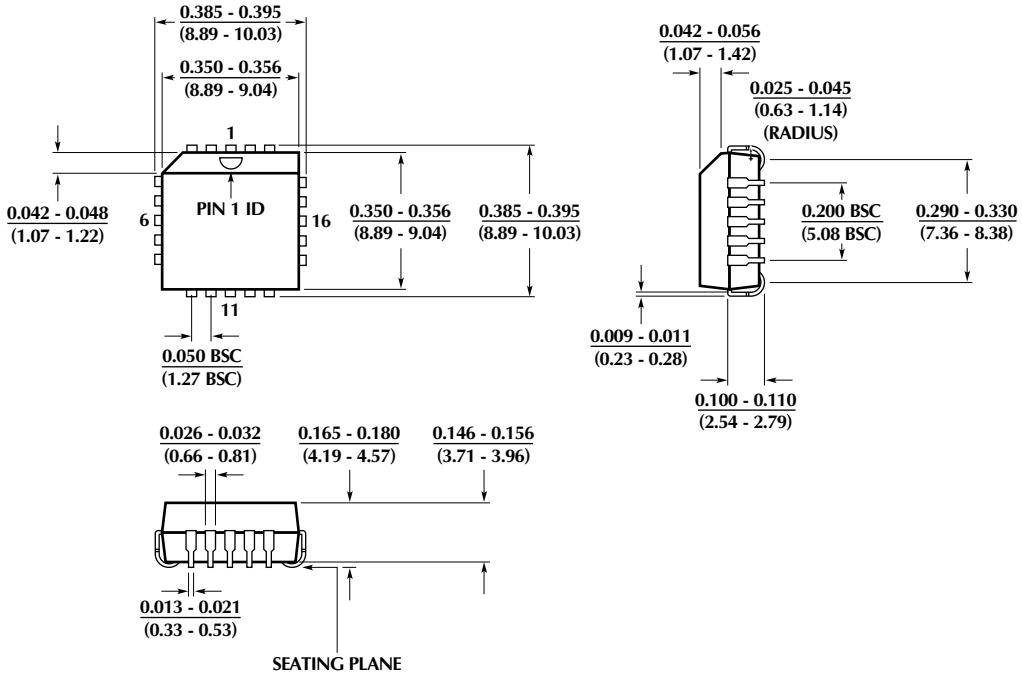


Figure 15. $\overline{\text{LMON}}$ Timing

PHYSICAL DIMENSIONS inches (millimeters)

Package: Q20
20-Pin PLCC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE	PACKAGE
ML4665CQ	0°C TO 70°C	20-pin PLCC (Q20)

2092 Concourse Drive
San Jose, CA 95131
Tel: 408/433-5200
Fax: 408/432-0295