

# 2 Cell, Adjustable Output Boost Regulator with Load Disconnect

## GENERAL DESCRIPTION

The ML4769 is a continuous conduction boost regulator designed for DC to DC conversion in multiple cell battery power systems. Continuous conduction allows the regulator to maximize output current for a given inductor. The maximum switching frequency can exceed 200kHz, allowing the use of small, low cost inductors. The ML4769 is capable of start-up with input voltages as low as 1.8V. The output voltage can be set anywhere between 3.0V and 5.5V by an external resistor divider connected to the SENSE pin.

An integrated synchronous rectifier eliminates the need for an external Schottky diode and provides a lower forward voltage drop, resulting in higher conversion efficiency. In addition, low quiescent current and variable frequency operation result in high efficiency even at light loads. The ML4769 requires only a few external components to build a very small regulator capable of achieving conversion efficiencies approaching 85%.

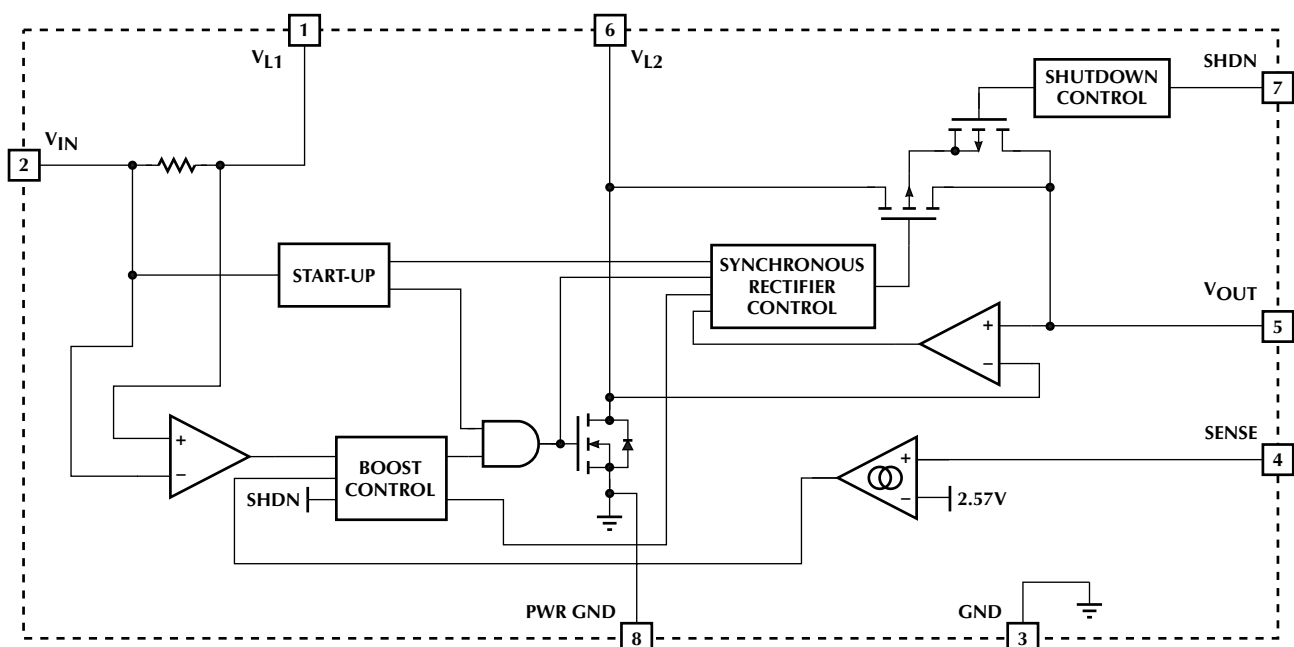
The SHDN input allows the user to stop the regulator from switching, and provides complete isolation of the load from the battery.

## FEATURES

- Guaranteed full load start-up and operation at 1.8V input
- Continuous conduction mode for high output current
- Pulse Frequency Modulation and internal synchronous rectification for high efficiency
- Isolates the load from the input during shutdown
- Minimum external components
- Low ON resistance internal switching FETs
- Low supply current
- Adjustable output voltage (3V to 5.5V)

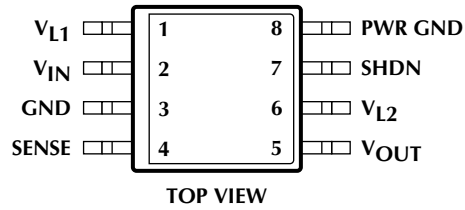
\* Some Packages Are Obsolete

## BLOCK DIAGRAM



## PIN CONFIGURATION

**ML4769**  
**8-Pin SOIC (S08)**



## PIN DESCRIPTION

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	V <sub>L1</sub>	Boost inductor connection	5	V <sub>OUT</sub>	Boost regulator output
2	V <sub>IN</sub>	Battery input voltage	6	V <sub>L2</sub>	Boost inductor connection
3	GND	Ground	7	SHDN	Pulling this pin to V <sub>IN</sub> shuts down the regulator, isolating the load from the input
4	SENSE	Programming pin for setting the output voltage	8	PWR GND	Return for the NMOS output transistor

**ABSOLUTE MAXIMUM RATINGS**

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

$V_{OUT}$ .....	7V
Voltage on any other pin .....	GND - 0.3V to $V_{OUT} + 0.3V$
Peak Switch Current ( $I_{PEAK}$ ) .....	2A
Average Switch Current ( $I_{AVG}$ ) .....	1A
Junction Temperature .....	150°C
Storage Temperature Range .....	-65°C to 150°C
Lead Temperature (Soldering, 10 sec) .....	260°C
Thermal Resistance ( $\theta_{JA}$ ) .....	160°C/W

**OPERATING CONDITIONS**

Temperature Range	
ML4769CS-X .....	0°C to 70°C
ML4769ES-X .....	-20°C to 70°C
$V_{IN}$ Operating Range .....	1.8V to $V_{OUT} - 0.2V$
$V_{OUT}$ Operating Range .....	3.0V to 5.5V

**ELECTRICAL CHARACTERISTICS**

Unless otherwise specified,  $V_{IN}$  = Operating Voltage Range,  $T_A$  = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SUPPLY</b>						
$I_{IN}$	$V_{IN}$ Current	$V_{IN} = V_{OUT} - 0.2V$ , SHDN = 0V		3	6	$\mu A$
		$V_{IN} = SHDN = 2.4V$ , $V_{OUT} = 0V$		0.3	1	$\mu A$
$I_{OUT(Q)}$	$V_{OUT}$ Quiescent Current	SHDN = 0V		25	35	$\mu A$
		$V_{IN} = SHDN = 2.4V$ , $V_{OUT} = V_{OUT(NOM)}$		14	20	$\mu A$
<b>PFM REGULATOR</b>						
$I_{PEAK}$	$I_L$ Peak Current		750	850	950	mA
$V_{SENSE}$	SENSE Comparator Threshold Voltage		2.52	2.57	2.62	V
	Line Regulation	$I_{OUT} = 0$ , See Figure 1	4.95	5.05	5.15	V
	Load Regulation	$V_{IN} = 2.4V$ , $I_{OUT} \leq 180mA$ See Figure 1	4.85	4.95	5.15	V
<b>SHUTDOWN</b>						
$V_{IL}$	Input Low Voltage				0.5	V
$V_{IH}$	Input High Voltage		$V_{IN} - 0.5$			V
	Input Bias Current		-100		100	nA

**Note 1:** Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

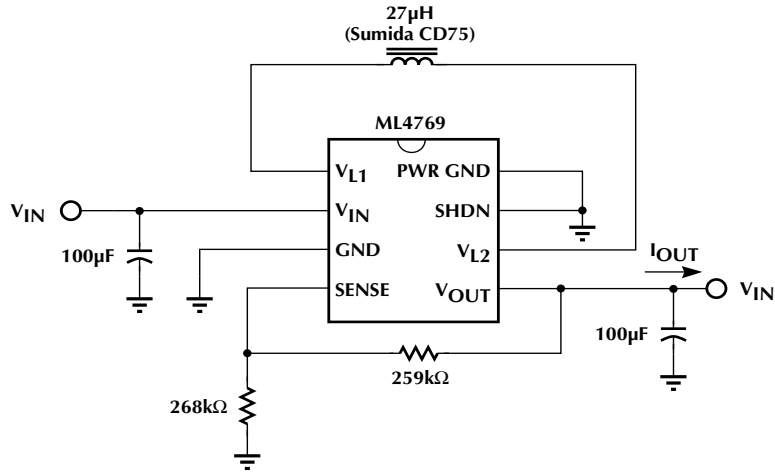


Figure 1. Application Test Circuit

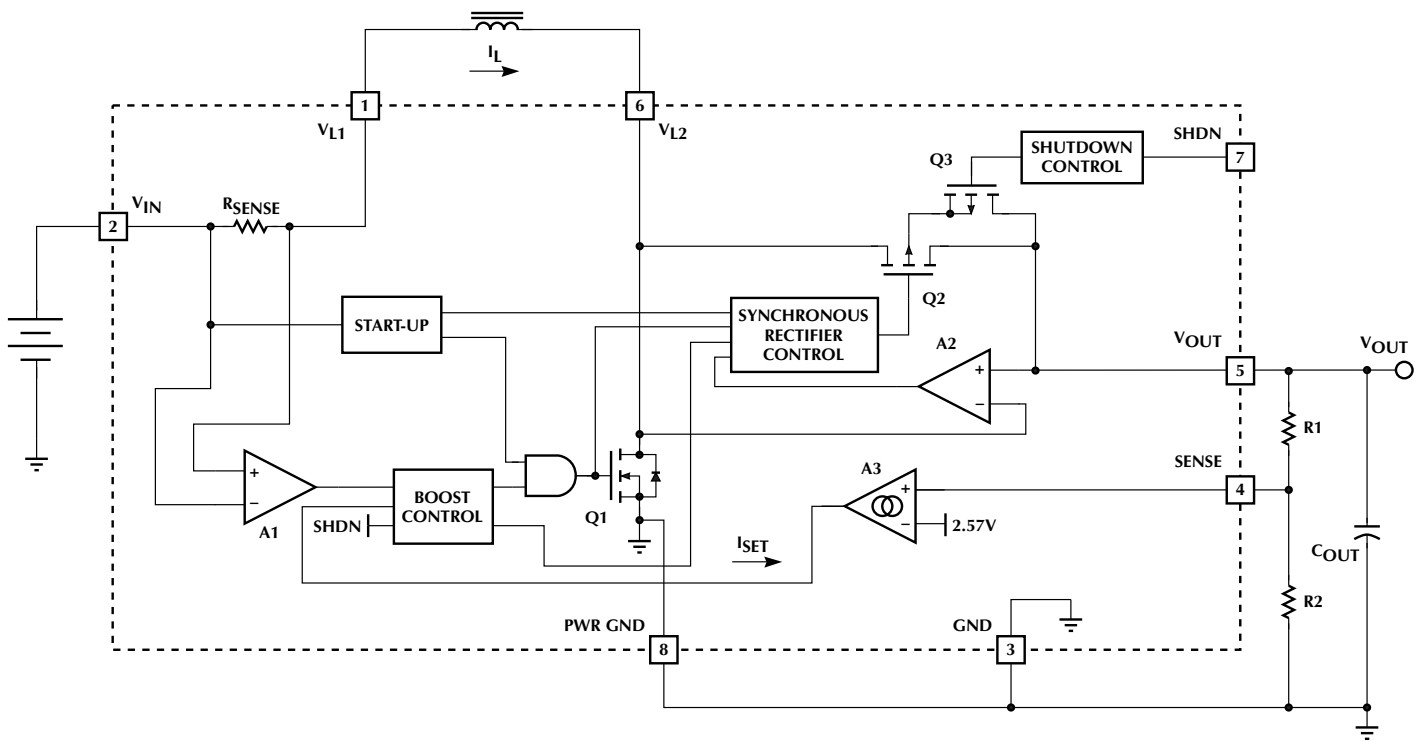


Figure 2. PFM Regulator Block Diagram

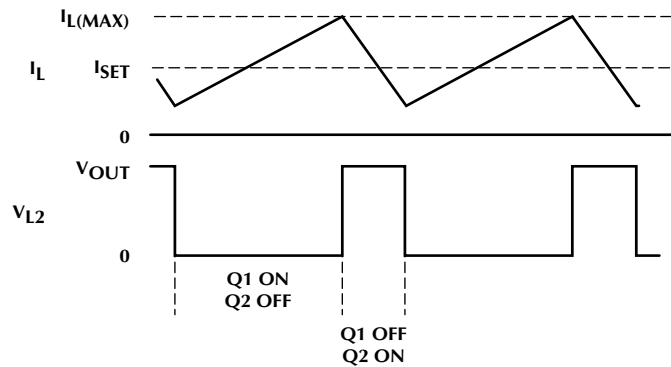


Figure 3. Inductor Current and Voltage Waveforms

## FUNCTIONAL DESCRIPTION

The ML4769 combines a unique form of current mode control with a synchronous rectifier to create a boost converter that can deliver high currents while maintaining high efficiency. Current mode control allows the use of a very small high frequency inductor and output capacitor. Synchronous rectification replaces the conventional external Schottky diode with an on-chip P-channel MOSFET to reduce losses, eliminate an external component, and provide the means for load disconnect. Also included on-chip are an N-channel MOSFET main switch and current sense resistor.

### REGULATOR OPERATION

The ML4769 is a variable frequency, current mode switching regulator. Its unique control scheme converts efficiently over more than three decades of load current. A block diagram of the boost converter including the key external components is shown in Figure 2.

Error amp A3 converts deviations in the desired output voltage to a small current,  $I_{SET}$ . The inductor current is measured through a current sense resistor ( $R_{SENSE}$ ) which is amplified by A1. The boost control block matches the average inductor current to a multiple of the  $I_{SET}$  current by switching Q1 on and off. The peak inductor current is limited by the controller to about 900mA.

At light loads,  $I_{SET}$  will momentarily reach zero after an inductor discharge cycle, causing Q1 to stop switching. Depending on the load, this idle time can extend to tenths of a second. When the circuit is not switching, only 25 $\mu$ A of supply current is drawn from the output. This allows the part to remain efficient even when the load current drops below 250 $\mu$ A.

Amplifier A2 and the PMOS transistor Q2 work together to form a low drop diode. When transistor Q1 turns off, the current flowing in the inductor causes  $V_{L2}$  to go high. As the voltage on  $V_{L2}$  rises above  $V_{OUT}$ , amplifier A2 allows the PMOS transistor Q2 to turn on. In discontinuous operation, (where  $I_L$  always returns to zero), A2 uses the resistive drop across the PMOS switch Q2 to sense zero inductor current and turns the PMOS switch off. In continuous operation, the PMOS turn off point is independent of A2 and is determined by the boost control circuitry.

Typical inductor current and voltage waveforms are shown in Figure 3.

### SHUTDOWN

The ML4769 output can be shut down by pulling the SHDN pin high (to  $V_{IN}$ ). When SHDN is high, the regulator stops switching, the control circuitry is powered down, and the body diode of the PMOS synchronous rectifier is disconnected from the output. By switching Q1, Q2, and Q3 off, the load is isolated from the input. This allows the output voltage to be independent of the input while in shutdown.

## DESIGN CONSIDERATIONS

### OUTPUT CURRENT CAPABILITY

The maximum current available at the output of the regulator is related to the maximum inductor current by the ratio of the input to output voltage and the conversion efficiency. The maximum inductor current is limited by the boost controller to about 600mA. The conversion efficiency is determined mainly by the internal switches as well as the external components, but can be estimated at about 80%. The maximum output current can be determined by using the typical performance curves shown in Figures 4 and 5, or by calculation using the following equation:

$$I_{OUT(MAX)} = \left[ \left( \frac{V_{IN(MIN)}}{V_{OUT}} \right) \times ((0.0392 \times V_{OUT}) + 0.488) \right] - 0.144A \quad (1)$$

Since the maximum output current is based on when the inductor current goes into current limit, it is not recommended to operate the ML4769 at the maximum output current continuously. Applications that have high transient load currents should be evaluated under worst case conditions to determine suitability.

### INDUCTOR SELECTION

The ML4769 is able to operate over a wide range of inductor values. A value of 10 $\mu$ H is a good choice, but any value between 5 $\mu$ H and 33 $\mu$ H is acceptable. As the inductor value changes, the control circuitry will automatically adjust to keep the inductor current under control. Choosing an inductance value of less than 10 $\mu$ H will reduce the component's footprint, but the efficiency and maximum output current may drop.

It is important to use an inductor that is rated to handle 1.0A peak currents without saturating. Also look for an inductor with low winding resistance. A good rule of thumb is to allow 5 to 10m $\Omega$  of resistance for each 1 $\mu$ H of inductance.

The final selection of the inductor will be based on trade-offs between size, cost and efficiency. Inductor tolerance, core and copper loss will vary with the type of inductor selected and should be evaluated with a ML4769 under worst case conditions to determine its suitability.

Several manufacturers supply standard inductance values in surface mount packages:

Coilcraft	(847) 639-6400
Coiltronics	(561) 241-7876
Dale	(605) 665-9301
Sumida	(847) 956-0666

## DESIGN CONSIDERATIONS (Continued)

### OUTPUT CAPACITOR

The output capacitor filters the pulses of current from the switching regulator. Since the switching frequency will vary with inductance, the minimum output capacitance required to reduce the output ripple to an acceptable level will be a function of the inductor used. Therefore, to maintain an output voltage with less than 100mV of ripple at full load current, use the following equation:

$$C_{OUT} = \frac{44 \times L}{V_{OUT}} \quad (2)$$

The output capacitor's Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL), also contribute to the ripple. Just after the Q1 turns off, the current in the output capacitor ramps quickly to between 0.3A and

0.9A. This fast change in current through the capacitor's ESL causes a high frequency (5ns) spike to appear on the output. After the ESL spike settles, the output still has a ripple component equal to the inductor discharge current times the ESR. To minimize these effects, choose an output capacitor with less than 10nH of ESL and less than 100mΩ of ESR.

Suitable tantalum capacitors can be obtained from the following vendors:

AVX	(207) 282-5111
Kemet	(846) 963-6300
Sprague	(207) 324-4140

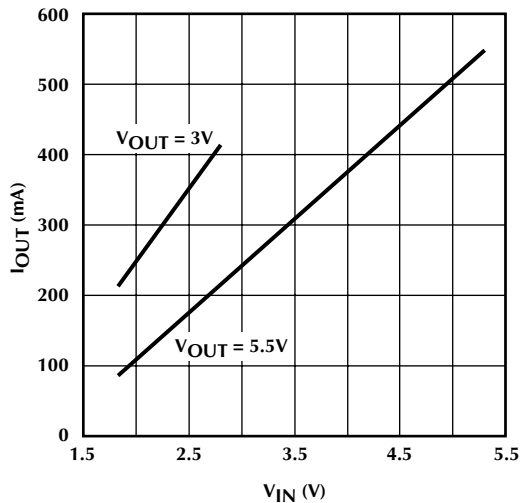


Figure 4.  $I_{OUT}$  vs.  $V_{IN}$  Using the Circuit of Figure 8

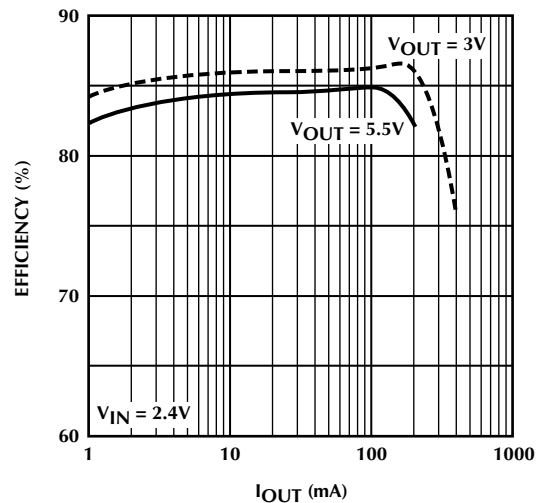


Figure 5. Efficiency vs.  $I_{OUT}$  Using the Circuit of Figure 8

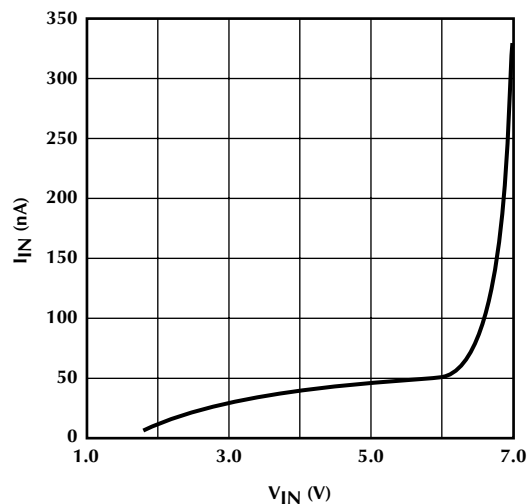


Figure 6. Input Leakage vs.  $V_{IN}$  in Shutdown

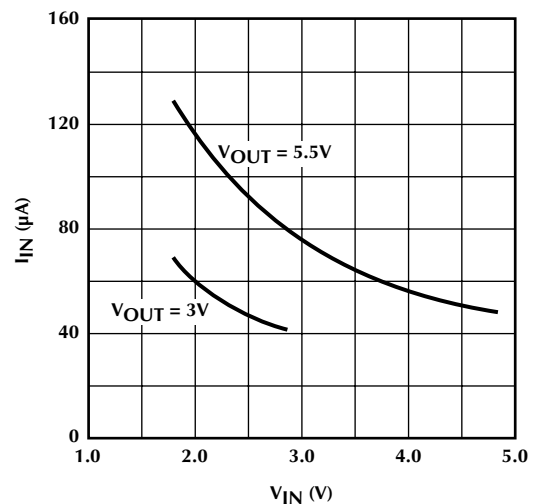


Figure 7. No Load Input Current vs.  $V_{IN}$

## DESIGN CONSIDERATIONS (Continued)

In applications where the ML4769 is operated at or near the maximum output current, it is recommended to add a 10nF to 100nF ceramic capacitor from  $V_{OUT}$  to GND. The optimum value of the high frequency bypass capacitor is dependent on the layout and the value of the bulk output capacitor selected.

### INPUT CAPACITOR

Due to the high input current drawn at startup and possibly during operation, it is recommended to decouple the input with a capacitor with a value of 47 $\mu$ F to 100 $\mu$ F. This filtering prevents the input ripple from affecting the ML4769 control circuitry, and also improves the efficiency by reducing the  $I^2R$  losses during the charge cycle of the inductor. Again, a low ESR capacitor (such as tantalum) is recommended.

It is also recommended that low source impedance batteries be used. Otherwise, the voltage drop across the source impedance during high input current situations will cause the ML4769 to fail to start up or to operate unreliably. In general, for two cell applications the source impedance should be less than 400m $\Omega$ , which means that small alkaline cells should be avoided.

### SHUTDOWN

The input levels of the SHDN pin are CMOS compatible. To guarantee proper operation, SHDN must be pulled to within 0.5V of GND or  $V_{IN}$  to prevent excessive power dissipation and possible oscillations.

### SETTING THE OUTPUT VOLTAGE

The adjustable output of the ML4769 requires an external feedback resistor divider to set  $V_{OUT}$ . The output voltage can be determined from the following equation:

$$V_{OUT} = 2.57 \times \frac{(R1 + R2)}{R2} \quad (3)$$

where R1 and R2 are connected as shown in Figure 2. The value of R2 should be 250k $\Omega$  or less to minimize bias current errors. Choose an appropriate value for R2 and calculate R1.

## LAYOUT

Good layout practices will ensure proper operation of the ML4769. Some layout guidelines follow:

- Use adequate ground and power traces or planes
- Keep components as close as possible to the ML4769
- Use short trace lengths from the inductor to the  $V_{L1}$  and  $V_{L2}$  pins and from the output capacitor to the  $V_{OUT}$  pin

## LAYOUT (Continued)

- Use a single point ground for the ML4769 PWR GND pin and the input and output capacitors, and connect the GND pin to PWR GND using a separate trace
- Separate the ground for the converter circuitry from the ground of the load circuitry and connect at a single point
- Route the feedback trace away from the  $V_{L2}$  trace to avoid noise pickup
- Route the high frequency bypass capacitor from a  $V_{OUT}$  location near the output voltage setting resistor to the GND pin

## DESIGN EXAMPLE

In order to design a boost converter using the ML4769, it is necessary to define the values of a few parameters. For this example, assume that  $V_{IN} = 3.0V$  to 3.6V,  $V_{OUT} = 5.0V$ , and  $I_{OUT(MAX)} = 250mA$ .

First, it must be determined whether the ML4769 is capable of delivering the output current. This is done using Equation 1:

$$I_{OUT(MAX)} = \left[ \left( \frac{3}{5} \right) \times ((0.0392 \times 5) + 0.488) \right] - 0.144A = 266mA$$

The next step is to select an inductor. As previously mentioned, the recommended inductance is 10 $\mu$ H. Make sure that the peak current rating of the inductor is at least 1.0A, and that the DC resistance of the inductor is between 50m $\Omega$  and 100m $\Omega$ .

Finally, the value of the output capacitor is determined using Equation 2:

$$C_{OUT} = \frac{44 \times 10\mu H}{5.0V} = 88\mu F$$

The closest standard value would be a 100 $\mu$ F capacitor with an ESR rating of 100m $\Omega$ . If such a low ESR value cannot be found, two 47 $\mu$ F capacitors in parallel could also be used. Since the 250mA output current requirement is close to the 266mA maximum, a 10nF capacitor from  $V_{OUT}$  to GND is recommended.

Finally, the values of R1 and R2 are calculated using equation 3. Assuming R2 = 250k $\Omega$ :

$$R1 = \left( \frac{5.0V}{2.57} \times 250k\Omega \right) - 250k\Omega = 236k\Omega$$

The complete circuit is shown in Figure 8. As mentioned previously, the use of an input supply bypass capacitor is strongly recommended.

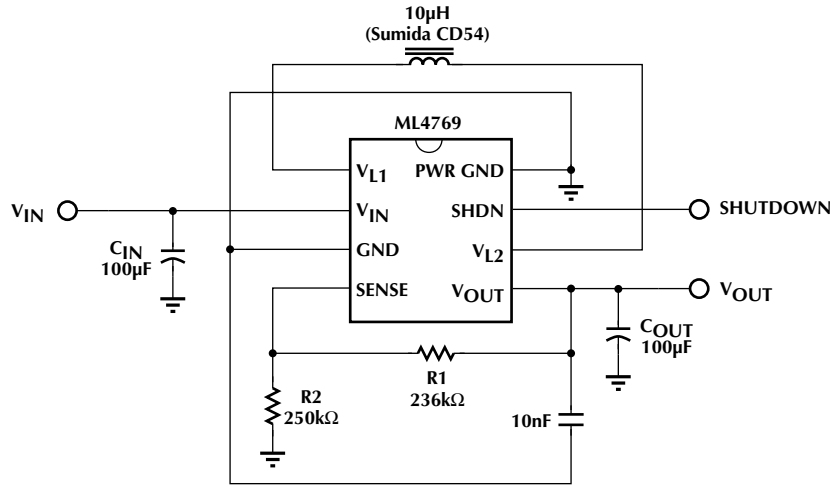
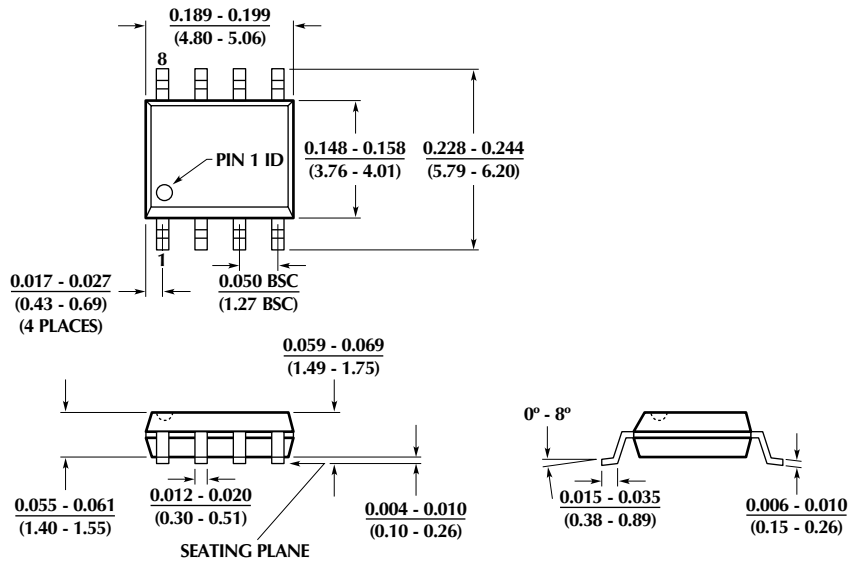


Figure 8. Design Example Schematic Diagram

## PHYSICAL DIMENSIONS inches (millimeters)

Package: S08  
8-Pin SOIC



## ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4769CS (Obsolete)	0°C to 70°C	8-Pin SOIC (S08)
ML4769ES	-20°C to 70°C	8-Pin SOIC (S08)

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