Dual S-Video Lowpass Filter with Phase and Sinx/x Equalization

GENERAL DESCRIPTION

The ML6423 monolithic BiCMOS 6th-order filter provides a two-channel fixed frequency lowpass filtering for video applications. This dual phase equalized filter with sinx/x correction is designed for reconstruction filtering at the output of a Video DAC. A composite sum output eliminates the need for a third DAC.

Cutoff frequencies are either 5.5MHz or 9.6MHz. Each channel incorporates a 6th-order lowpass filter, a first order allpass filter, a gain boost circuit, and a 75Ω coax cable driver. A control pin (RANGE) is provided to allow the inputs to swing from 0 to 1V, or 0.5 to 1.5V, by providing a 0.5V offset to the input.

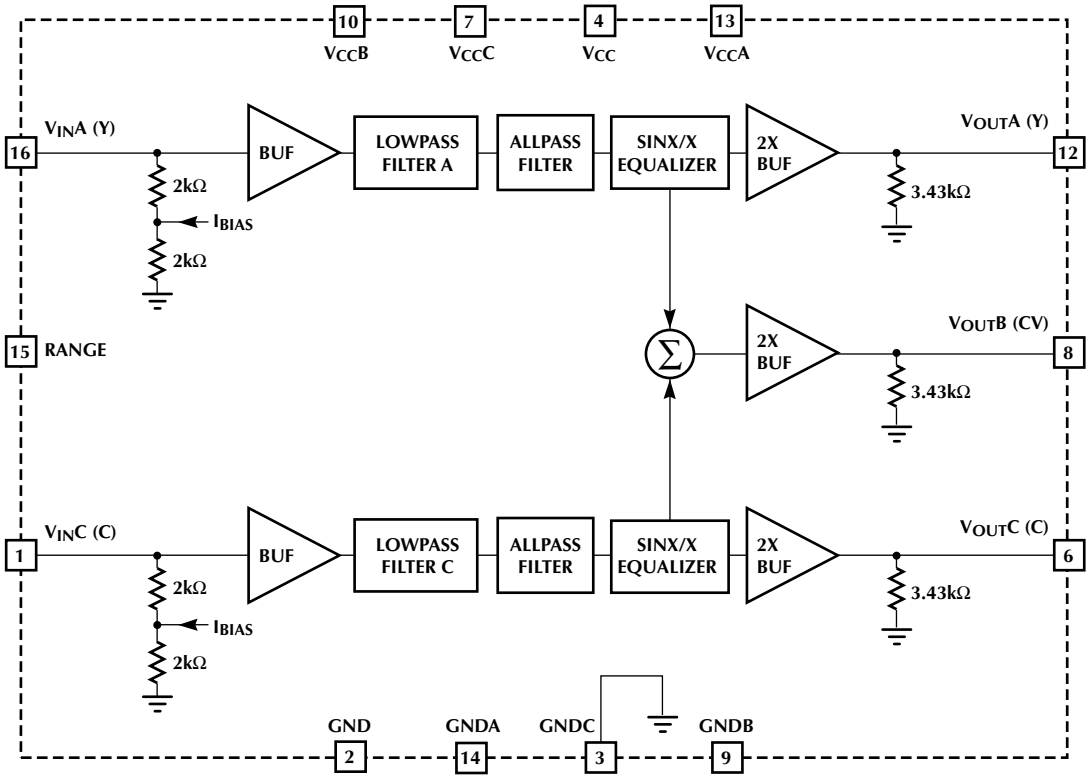
The 2X gain filters are powered from a single 5V supply, and can drive $1V_{P-P}$ into 75Ω (0.5V to 1.5V), or $2V_{P-P}$ into 150Ω (0.5V to 2.5V) with the internal coax drivers.

FEATURES

- 5.5 or 9.6MHz bandwidth with 6dB gain
- >40dB stopband rejection
- No external components or clocks
- ±10% frequency accuracy over maximum supply and temperature variation
- <2% differential gain, <2° differential phase
- <20ns group delay variation
- 5V ±10% operation
- Composite (sum) output
- High sink current for AC coupled loads, ML6423-5

*** This Product Is End Of Life As Of August 1, 2000**

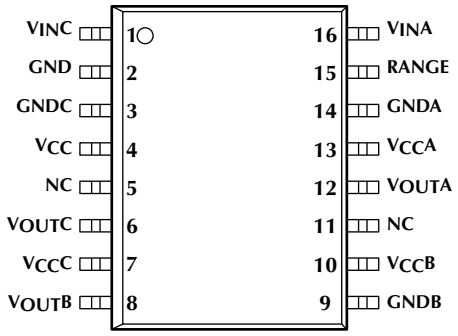
BLOCK DIAGRAM



	ML6423-1	ML6423-2	ML6423-5
Filter A	5.50MHz	9.6MHz	9.6MHz
Filter C	5.50MHz	9.6MHz	9.6MHz

PIN CONFIGURATION

ML6423
16-Pin Wide SOIC (S16W)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	$V_{IN}C$	Signal input to filter C. Input impedance is 4kΩ.
2	GND	Power and logic ground.
3	GNDC	Ground pin for filter C.
4	V_{CC}	Positive supply: 4.5V to 5.5V.
5	NC	No Connect
6	$V_{OUT}C$	Output of filter C. Drive is $1V_{P-P}$ into 75Ω (0.5V to 1.5V) or $2V_{P-P}$ into 150Ω (0.5V to 2.5V).
7	$V_{CC}C$	Power supply voltage for filter C.
8	$V_{OUT}B$	Sum of Filter A and Filter C. Drive is $1V_{P-P}$ into 75Ω (0.5V to 1.5V) or $2V_{P-P}$ into 150Ω (0.5V to 2.5V).
9	GNDB	Ground pin for output B.
10	$V_{CC}B$	Power supply voltage for output B.
11	NC	No Connect
12	$V_{OUT}A$	Output of filter A. Drive is $1V_{P-P}$ into 75Ω (0.5V to 1.5V) or $2V_{P-P}$ into 150Ω (0.5V to 2.5V).
13	$V_{CC}A$	Power supply voltage for filter A.
14	GNDA	Ground pin for filter A.
15	RANGE	Input signal range select. When RANGE is low (0), the input signal range is 0.5V to 1.5V, with an output range of 0.5V to 2.5V. When RANGE is high (1) the input signal range is 0V to 1V, while the output range is 0.5V to 2.5V.
16	$V_{IN}A$	Signal input to filter A. Input impedance is 4kΩ.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (V_{CC}) ..... –0.3 to 7V
GND ..... –0.3 to V_{CC} +0.3V
Logic Inputs ..... –0.3 to V_{CC} +0.3V
Input Current per Pin ..... ±25mA

Storage Temperature ..... –65° to 150°C
Lead Temperature (Soldering 10 sec) ..... 150°C
Thermal Resistance (θ_{JA}) ..... 65°C/W

OPERATING CONDITIONS

Supply Voltage ..... 5V ±10%
Temperature Range ..... 0°C to 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified V_{CC} = 5V ± 10%, R_L =75Ω or 150Ω, V_{OUT} = $2V_{P-P}$ for 150Ω Load and V_{OUT} = $1V_{P-P}$ for 75Ω Load, T_A = Operating Temperature Range (Notes 1, 2, 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
R_{IN}	Input Impedance		3k	4	5	kΩ
DR/R_{IN}	Input R Matching				±2	%
I_{BIAS}	Input Current	V_{IN} = 0.5V, RANGE = low		45		µA
		V_{IN} = 0.0V, RANGE = high	–210		µA	
	Differential Gain	V_{IN} = 0.8V to 1.5V at 3.58 & 4.43 MHz		1		%
	Differential Phase	V_{IN} = 0.8V to 1.5V at 3.58 & 4.43 MHz		1		deg
V_{IN}	Input Range	RANGE = Low	0.5		1.5	V
		RANGE = High	0.0		1.0	V
	Peak Overshoot	2T, $0.7V_{P-P}$ pulse		2.0		%
	Crosstalk Rejection	f_{IN} = 3.58, f_{IN} = 4.43MHz	45			dB
	Channel to Channel Group Delay Matching (f_C = 5.5MHz)	f_{IN} = 100kHz		±3		ns
	Channel to Channel Gain Matching	f_{IN} = 100kHz		±1.5		%
	Output Current	R_L = 0 (short circuit)		75		mA
C_L	Load Capacitance				35	pF
	Composite Chroma/Luma delay	f_C = 5.5MHz		±15		ns
		f_C = 9.6MHz		±8		ns
5.50MHz FILTER						
	Bandwidth (monotonic passband)	–0.55dB (Note 4)	4.95	5.50	6.05	MHz
	Subcarrier Frequency Gain	f_{IN} = 3.58MHz	0.9	1.4	2.3	dB
	ML6423-1	f_{IN} = 4.43MHz	1.1	1.6	2.5	dB
	Attenuation	f_{IN} = 10MHz	20	25		dB
		f_{IN} = 50MHz	45	55		dB
	Output Noise	BW = 30MHz			1	mV_{RMS}
	Group Delay			180		ns

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
5.50MHz FILTER (Continued)						
	Small Signal Gain	V_{IN} = 100mV$_{P-P}$ at 100kHz, Filter A or C	5.5	6	6.5	dB
	Composite (CV) Small Signal Gain	V_{IN}A, C = 100mV$_{P-P}$ at 100kHz	11	12	13	dB
9.6MHz FILTER						
	Bandwidth (monotonic passband)	–2dB (Note 4)	8.6	9.6	10.6	MHz
	Subcarrier Frequency Gain	f_{IN} = 3.58MHz	–0.1	0.4	1.1	dB
	ML6423-2	f_{IN} = 4.43MHz	–0.1	0.6	1.3	dB
	Subcarrier Frequncy Gain	f_{IN} = 3.58MHz	–0.1	0.4	1.9	dB
	ML6423-5	f_{IN} = 4.43MHz	–0.1	0.6	1.1	dB
	Attenuation	f_{IN} = 17MHz	20	25		dB
		f_{IN} = 85MHz	45	55		dB
	Output Noise	BW = 30MHz			1	mV_{RMS}
	Group Delay				100	ns
	Composite (CV) Small Signal Gain	V_{IN}A, C = 100mV$_{P-P}$ at 100kHz	11	12	13	dB
I_{CC}	ML6423-5 Supply Current R_L = 150Ω	V_{IN} = 0.5V (Note 5)		140	175	mA
		V_{IN} = 1.5V		170	215	mA
	ML6423-5 V_{OUT}A, V_{OUT}B sink current	V_{IN} = 0.5V	8.3	11.5		mA
	ML6423-5 V_{OUT}C sink current	V_{IN} = 0.5V	4.3	6.5		mA
	ML6423-5 Output DC Level	V_{IN} = 0.5V, Range = Low		0.5		V
DIGITAL AND DC						
V_{IL}	Logic Input Low	Range			0.8	V
V_{IH}	Logic Input High	Range	V_{CC} – 0.8			V
I_{IL}	Logic Input Low	V_{IN} = GND	–1			µA
I_{IL}	Logic Input High	V_{IN} = V_{CC}			1	µA
I_{CC}	Supply Current R_L = 150Ω	V_{IN} = 0.5V (Note 5)		110	135	mA
		V_{IN} = 1.5V		140	175	mA

Note 1: Limits are guaranteed by 100% testing, sampling or correlation with worst case test conditions.

Note 2: Maximum resistance on the outputs is 500Ω in order to improve step response.

Note 3: Connect all ground pins to the ground plane via the shortest path.

Note 4: The bandwidth is the –3dB frequency of the unboosted filter. This represents the attenuation that results from boosting the gain from the –3dB point at the specified frequency.

Note 5: Power dissipation: $P_D = (I_{CC} \times V_{CC}) - [3(V_{OUT}^2/RL)]$

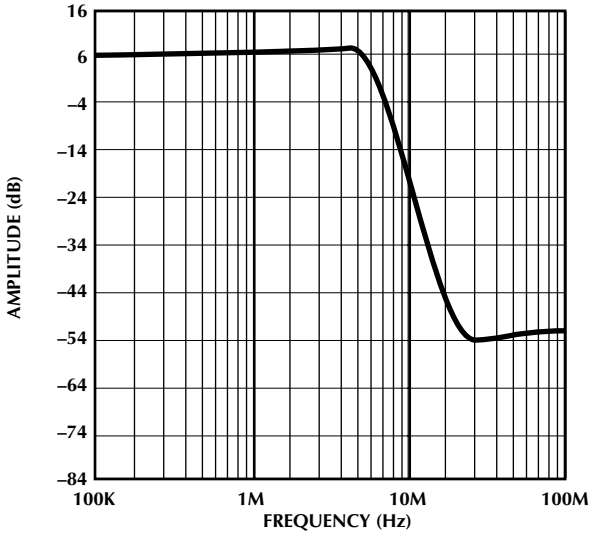


Figure 1a. Stop-Band Amplitude vs. Frequency (f_C = 5.5MHz)

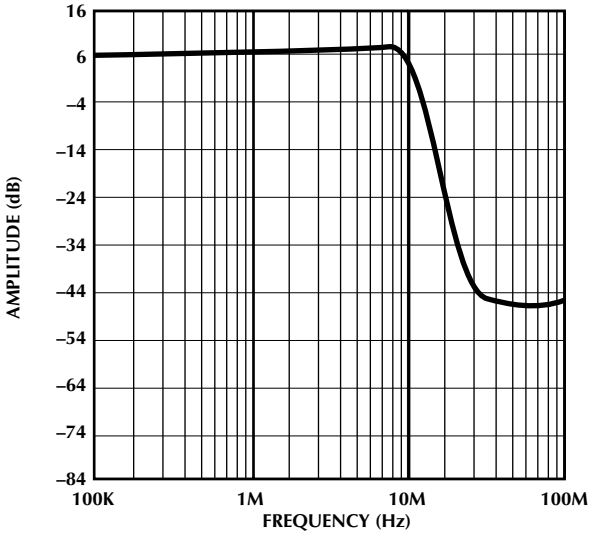


Figure 1b. Stop-Band Amplitude vs. Frequency (f_C = 9.6MHz)

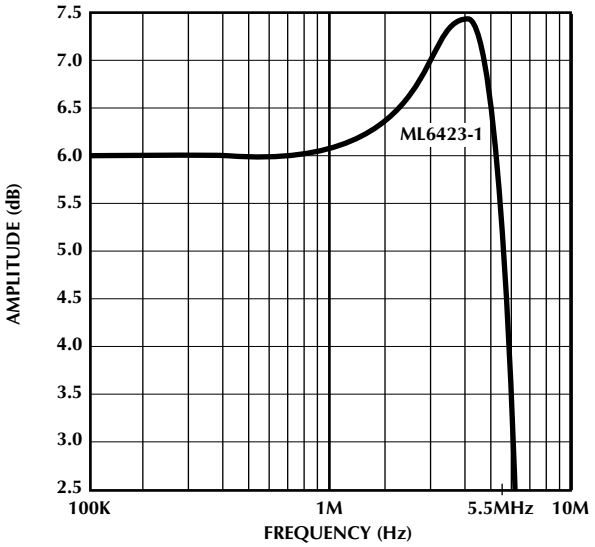


Figure 2a. Pass-Band Amplitude vs. Frequency (f_C = 5.5MHz)

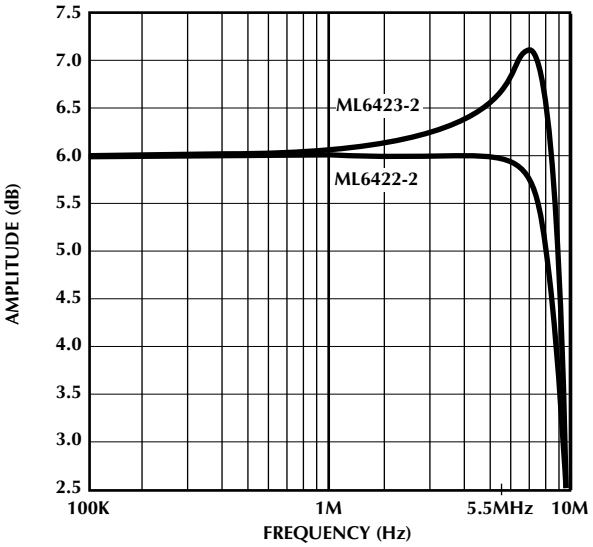


Figure 2b. Pass-Band Amplitude vs. Frequency (f_C = 9.6MHz)

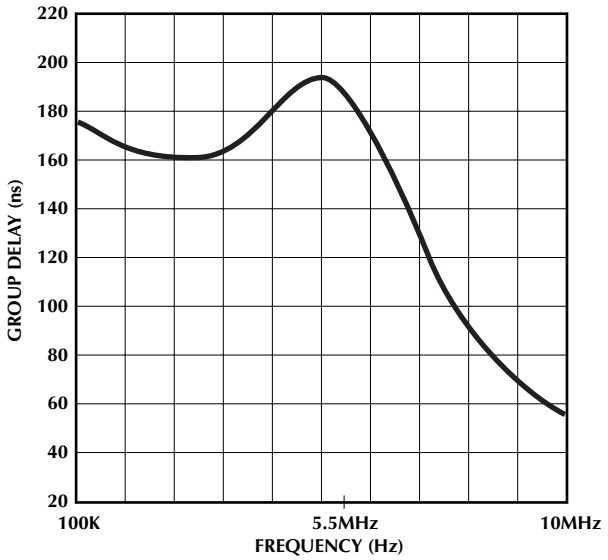


Figure 3a. Group Delay vs. Frequency (f_C = 5.5MHz)

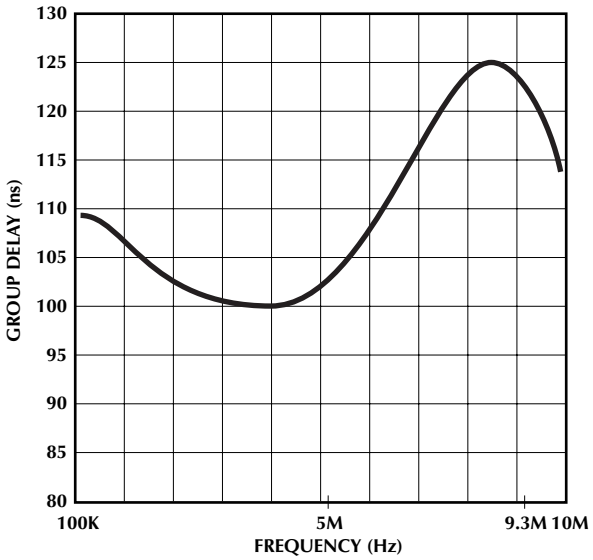


Figure 3b. Group Delay vs. Frequency (f_C = 9.6MHz)

FUNCTIONAL DESCRIPTION

The ML6423 single-chip dual video filter is intended for low cost professional and consumer video applications. Each of the two channels incorporates an input buffer amplifier, a 6th-order lowpass filter, a 1st-order allpass equalizer, sinx/x equalizer and an output 2X gain amplifier capable of driving 75Ω to ground. A third output (B) is the sum of the A and C inputs and have the identical output amplifier as the A and C channels.

The ML6423 can be driven by a DAC with RANGE down to 0V. When RANGE is low the input range is 0.5V to 1.5V. When the input signal range is 0V to 0.1V, RANGE should be tied high. In this case, an offset is added to the input so that the output swing is kept between 0.5V to 2.5V. The output amplifier is capable of driving up to 24mA of peak current; therefore the output voltage should not exceed 1.8V when driving 75Ω to ground.

APPLICATION GUIDELINES

OUTPUT & INPUT CONSIDERATIONS

The dual filters have 2X gain. The circuit has 2X gain (6dB) when connected to a 150W load, and 0dB gain when driving a 75Ω load via a 75Ω series output resistor. The output may be either AC or DC coupled. For AC coupling, the –3dB point should be 5Hz or less. There must also be a DC path of ≤500Ω to ground for output biasing. The ML6423-5 provides higher sink current to better drive AC coupled loads.

The input resistance is 4kΩ. The input may be either DC or AC coupled. (Note that each input sources 80 to 125µA of bias current). The ML6423 is designed to be directly driven by a DAC. For current output video DACs, a 75Ω or 150Ω resistor to ground may need to be added to the DAC output (filter input).

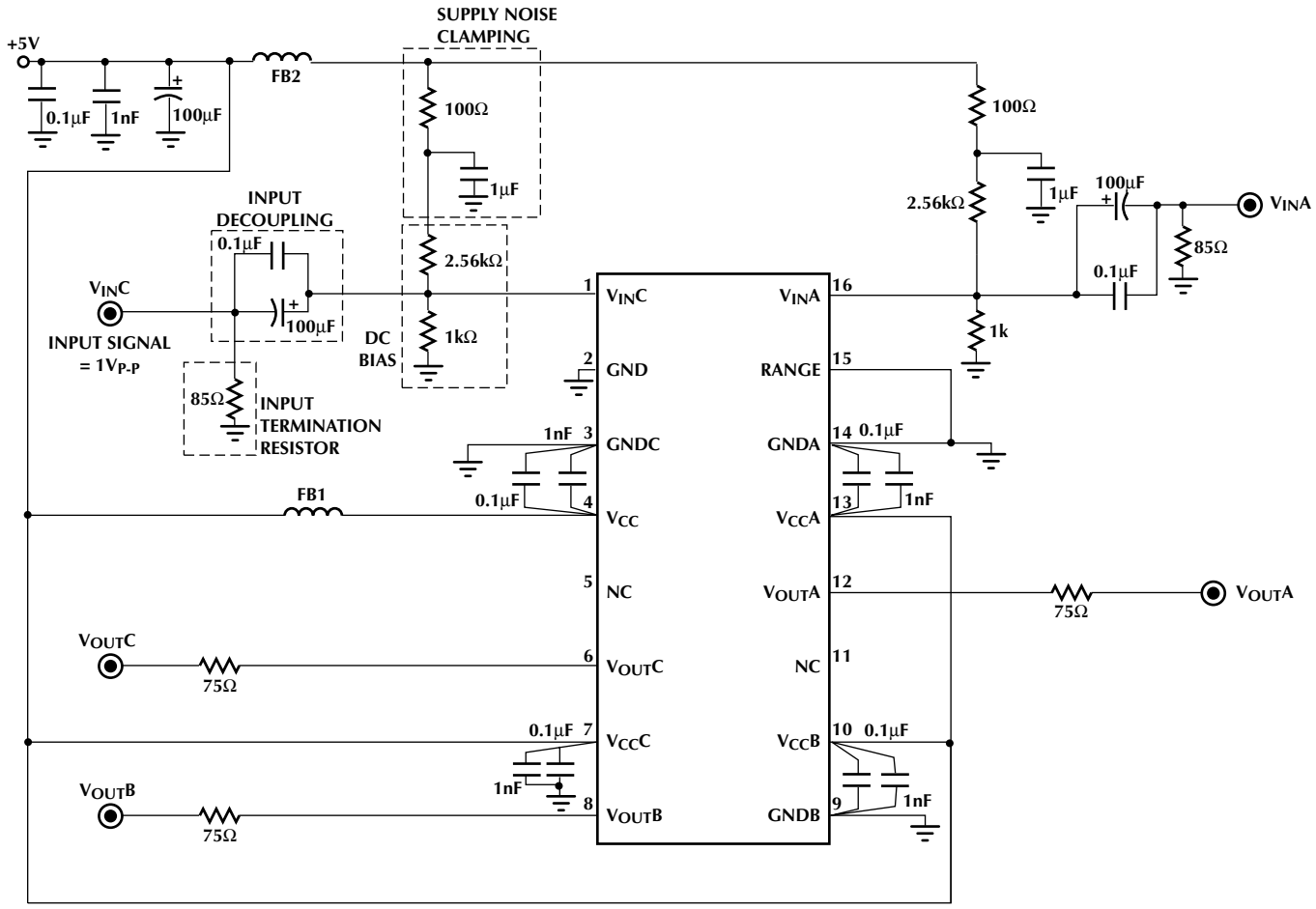


Figure 4. ML6423 AC Coupled DC Bias Test Circuit

APPLICATION GUIDELINES (Continued)

LAYOUT CONSIDERATIONS

In order to obtain full performance from these dual filters, layout is very important. Good high frequency decoupling is required between each power supply and ground. Otherwise, oscillations and/or excessive crosstalk may occur. A ground plane is recommended.

Each filter has its own supply and ground pins. In the test circuit, 0.1µF capacitors are connected in parallel with 1nF capacitors on all V_{CC} pins for maximum noise rejection (Figure 4).

Further noise reduction is achieved by using series ferrite beads. In typical applications, this degree of bypassing may not be necessary.

Since there are two filters and a sum output driver in one package, space the signal leads away from each other as much as possible.

POWER CONSIDERATIONS

The ML6423 power dissipation follows the formula:

$$P_D = (I_{CC} \times V_{CC}) - \left[\left(\frac{{V_{OUT}}^2}{RL} \times 3\right)\right]$$

This is a measure of the amount of current the part sinks (current in – current out to the load).

Under worst case conditions:

$$P_D = (0.175 \times 5.5) - \left[\left(\frac{1.5^2}{75} \times 3\right)\right] = 872.5\text{mW}$$

FILTER SELECTION

The ML6423 provides several choices in filter cutoff frequencies depending on the application.

S-Video: For Y/C (S-video) and Y/C + CV (Composite Video) systems the 5.5MHz or 9.6MHz filters are appropriate. In NTSC the C signal occupies the bandwidth from about 2.6MHz to about 4.6MHz, while in PAL the C signal occupies the bandwidth from about 3.4MHz to about 5.4MHz. In both cases, a 5.5MHz lowpass filter provides adequate rejection for both sampling and reconstruction. In addition, using the same filter for both Y/C and CV maintains identical signal timing without adjustments.

Composite: When one or more composite signals need to be filtered, then the 5.5MHz and 9.6MHz filters permit filtering of one, two, or three composite signals.

Over Sampling: While the ML6423 filters can eliminate the need for over sampling combined with digital filtering, there are times when over sampling is used. For these situations, 9.3MHz could be used in place of 5.5MHz.

NTSC/PAL: A 5.5MHz cutoff frequency provides good filtering for 4.2MHz, 5.0MHz and 5.5MHz signals without the need to change filters on a production basis.

Sinx/x: For digital video system with output D/A converters, there is a fall off in response with frequency due to discrete sampling. The fall off follows a sinx/x response (Figure 5a). The ML6423 filters have a complementary boost to provide a flatter overall response. The boost is designed for 13.5MHz Y/C and CV sampling and 6.75MHz U/V sampling.

In a typical application (Figure 5b) the ML6423 is used as the final output device in a video processing chain. In this case, inputs to the ML6423 are supplied by DAC outputs with their associated load resistors (typically 75Ω or 150Ω). Resistance values should be adjusted to provide $1V_{P-P}$ at the input of the ML6423. The ML6423 will drive 75Ω source termination resistors (making the total load 150Ω) so that no external drivers or amplifiers are required.

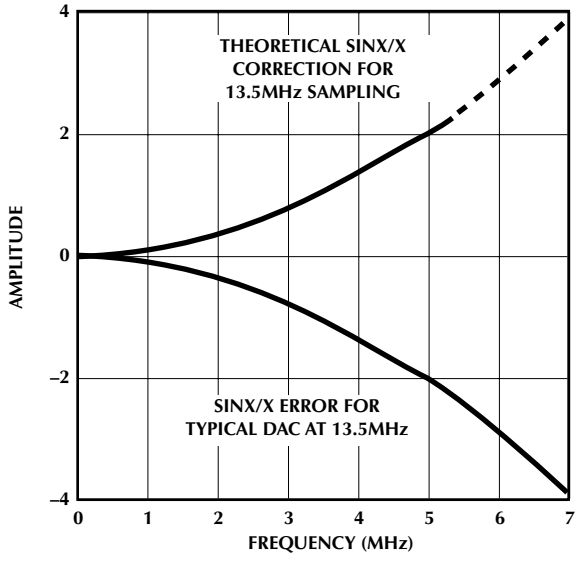


Figure 5a. Sinx/x Frequency Response

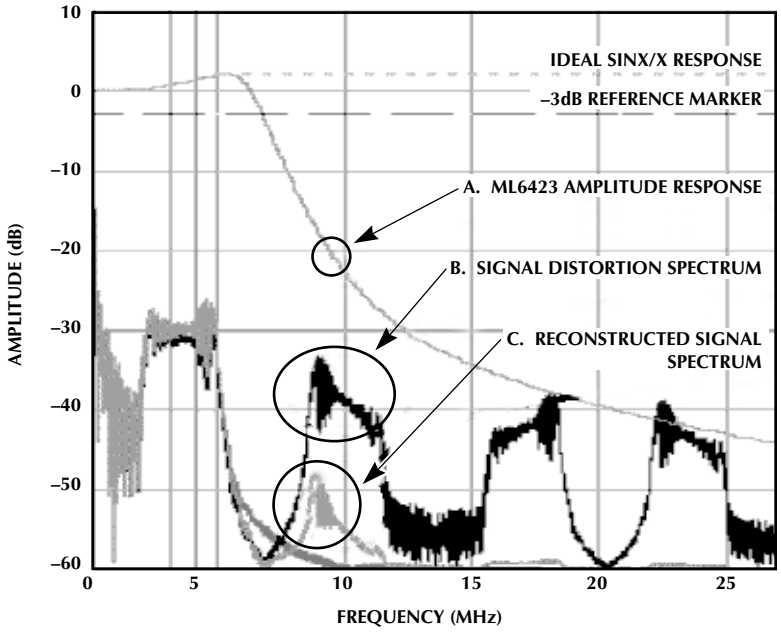


Figure 6. ML6423 Reconstruction Performance in the Frequency Domain

FILTER PERFORMANCE

The reconstruction performance of a filter is based on its ability to remove the high band spectral artifacts that result from the sampling process without distorting the valid signal spectral contents within the passband. For video signals, the effect of these artifacts is a variation of the amplitude of small detail elements in the picture (such as highlights or fine pattern details) as the elements move relative to the sampling clock. The result is similar to the aliasing problem and causes a "winking" of details as they move in the picture.

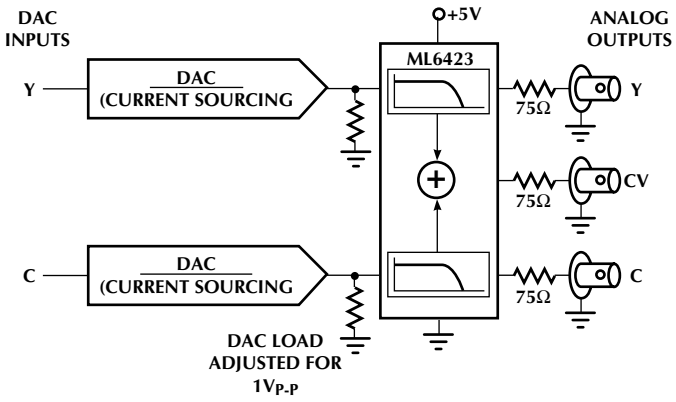


Figure 5b. Typical ML6423 Reconstruction Application

Figure 6 shows the problem in the frequency domain. Curve A shows the amplitude response of the ML6423 filter, while curve B shows the signal spectrum as it is distorted by the sampling process. Curve C shows the composite of the two curves which is the result of passing the sampled waveform through the ML6423. It is clear that the distortion artifacts are reduced significantly.

Ultimately it is the time domain signal that is viewed on a TV monitor, so the effect of the reconstruction filter on the time domain signal is important. Figure 7 shows the sampling artifacts in the time domain. Curve A is the original signal, curve B is the result of CCIR601 sampling, and curve C is the same signal filtered through the ML6423. Again the distortions in the signal are essentially removed by the filter.

In an effort to measure the time domain effectiveness of a reconstruction filter, Figure 8 was generated from a swept frequency waveform. Curves A, B, and C are generated as in Figure 7, but additional curves D and E help quantify the effect of filtering in the time domain. Curves D and E represent the envelopes (instantaneous amplitudes) of curves B and C. Again, it is evident in curve D that the envelope varies significantly due to the sampling process. In curve E, filtering with the ML6423 removes these artifacts and generates an analog output signal that rivals the oversampled (and more ideal) signal waveforms. The ML6423 reduces the amplitude variation from over 6% to less than 1%.

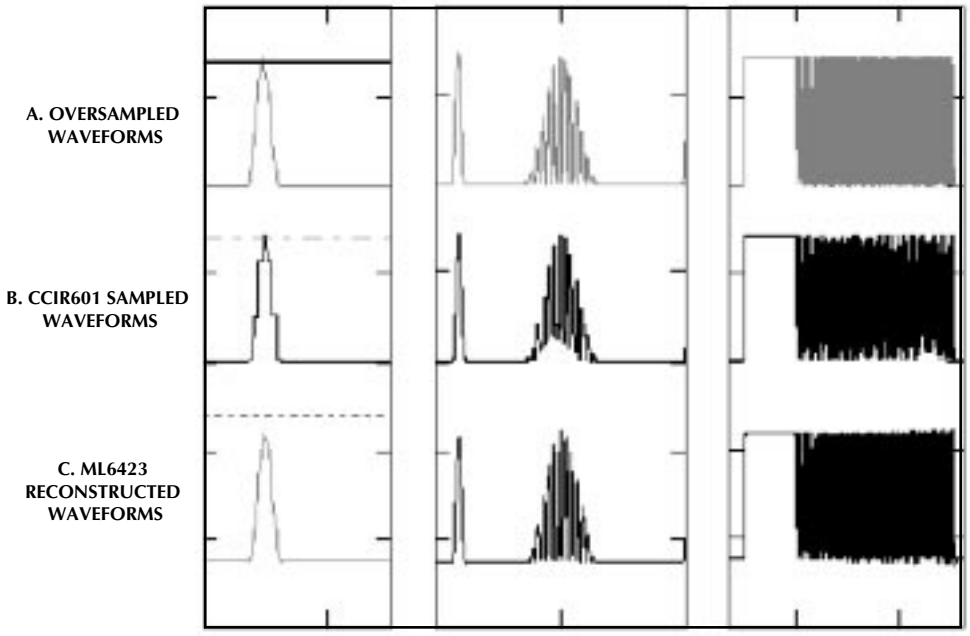


Figure 7. ML6423 Reconstruction Performance in the Time Domain

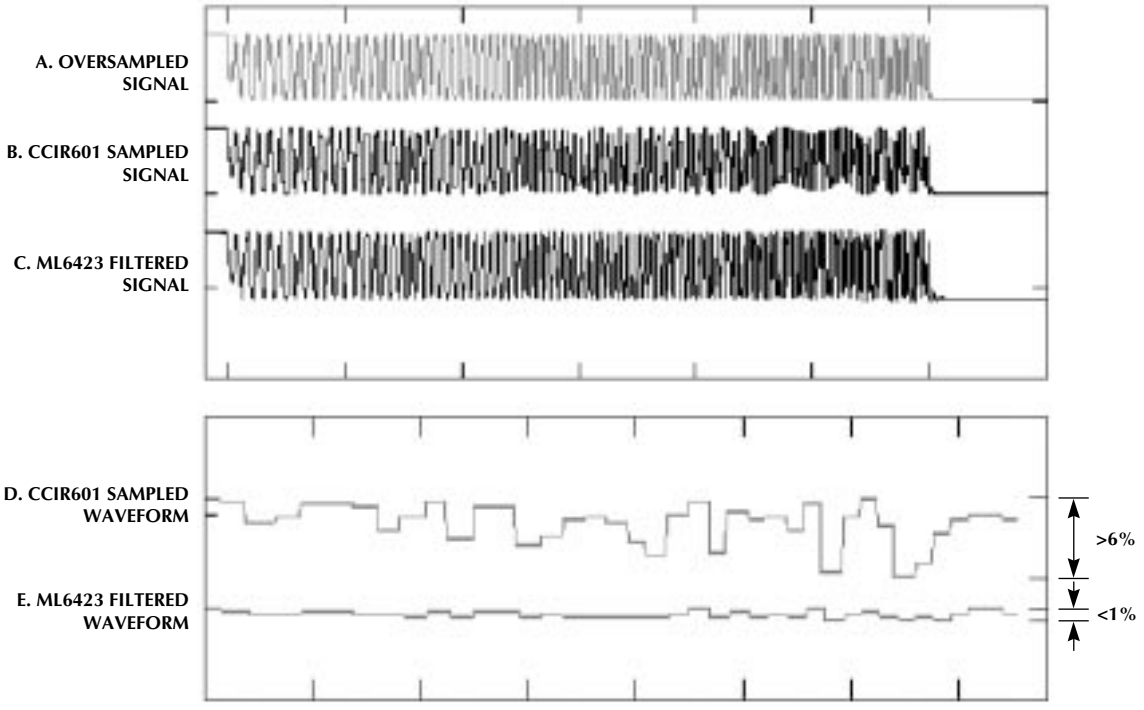
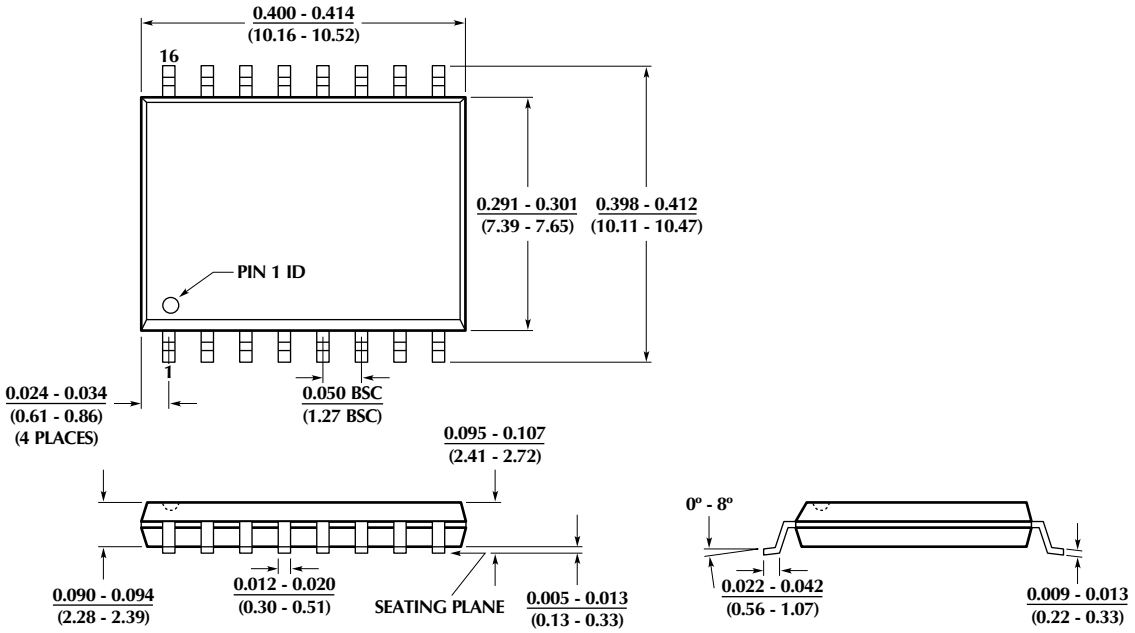


Figure 8. Amplitude Ripple of Reconstructed Swept Pulses

PHYSICAL DIMENSIONS inches (millimeters)

Package: S16W
16-Pin Wide SOIC



ORDERING INFORMATION

PART NUMBER	BW (MHz)	TEMPERATURE RANGE	PACKAGE
ML6423CS-1 (EOL)	5.5/5.5	0°C to 70°C	16-pin Wide SOIC (S16W)
ML6423CS-2 (EOL)	9.6/9.6	0°C to 70°C	16-pin Wide SOIC (S16W)
ML6423CS-5 (Obsolete)	9.6/9.6	0°C to 70°C	16-pin Wide SOIC (S16W)

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