Micro Linear

ADVANCED
Information

ML6651 Auto-Negotiating Media Converter

GENERAL DESCRIPTION

The ML6651 converts signals transmitted between twisted pair and fiber optic Ethernet technologies. It supports conversion between 10BASE-T and 10BASE-FL, between 100BASE-TX and 100BASE-FX/SX, and between FLP (fast link pulse) bursts and FLNP (fiber link negotiation pulse) bursts. Either 850nm or 1300nm laser optics can be used for both 10 and 100 Mb/second operating data rates while fully auto-negotiating for speed and duplex mode communication. One or both of the fiber optic and twisted pair interfaces can be set to interface with industry standard 1x9 fiber optic PMD modules, using PECL or LVPECL compatible modes.

FEATURES

- Complete implementation of fiber optic and twisted pair media interface
- ISO/IEC 8802.3, IEEE 802.3 and TIA/EIA-785 compliance, including full auto-negotiation for twisted pair and fiber optic media
- 850nm, 1300nm and 1x9 PMD modules
- Supports 1:1 receiver/transmitter transformer ratio for twisted pair
- Low latency 10Mb/s path
- Integrated voltage and current references
- Integrated twisted pair output wave shaping eliminate external filtering
- Integrated twisted pair 10BASE-T input filter and 100BASE-TX equalizer with baseline wander correction circuit

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WARRANTY

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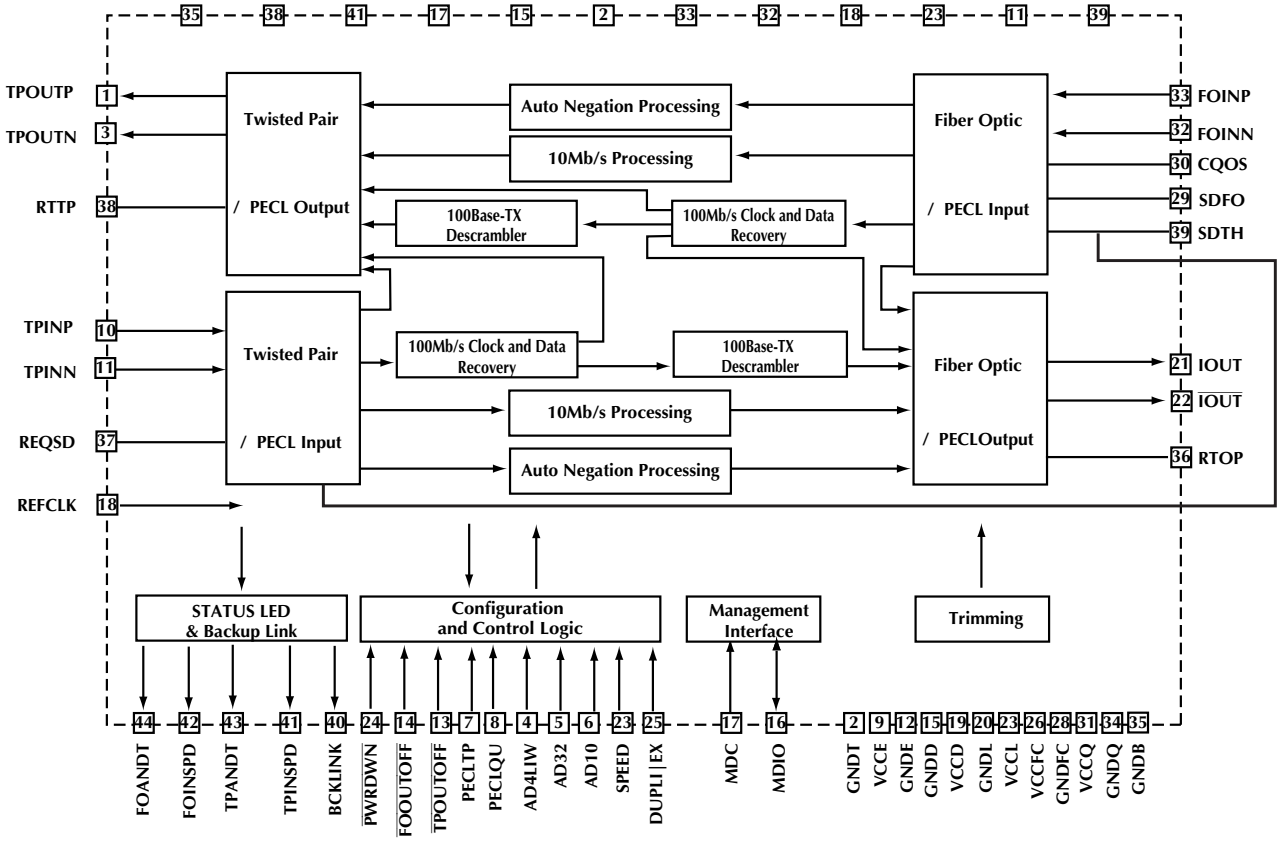
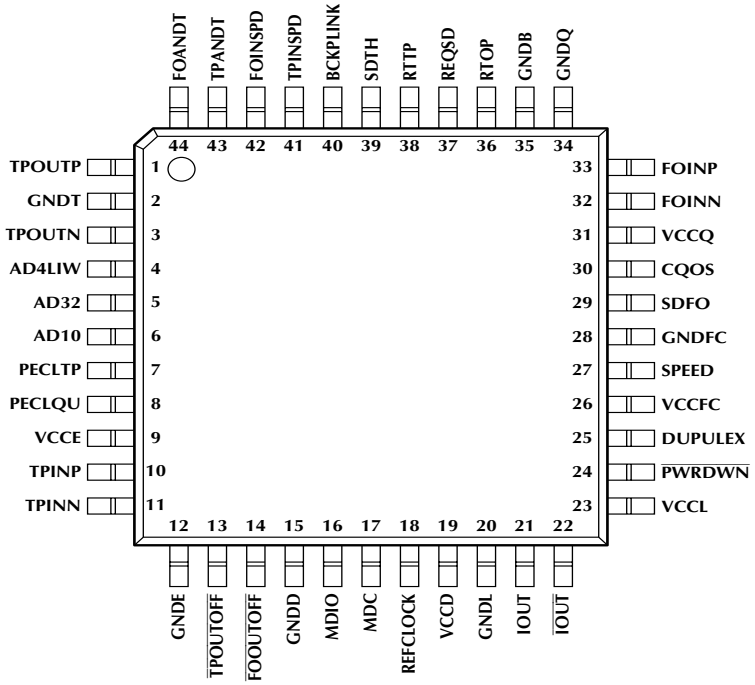
BLOCK DIAGRAM



PIN CONFIGURATION

ML6651
44-Pin TQFP (H44-10)



TOP VIEW

PIN DESCRIPTIONS

Pin #	Signal Name	Description
1	TPOUTP	Two operating modes are available for these pins and are selected with the configuration pin PECLTP (pin 7) or the configuration bit LVPECLTP (bit 30.3)
3	TPOUTN	**Twisted Pair Interface Mode:** Transmit twisted pair positive and complementary outputs. These outputs form a differential current output pair that drives MLT-3 waveforms into the network coupling transformer during 100 Mb/s mode, Manchester encoded 10BASE-T data or NLPs during 10 Mb/s mode, and FLP Bursts during Auto-Negotiation. The polarity of TPOUTP/N is such that during the transmission of a linkpulse, all the current goes into TPOUTN than it into TPOUTP. Since there is a resistor to VCC from each of the 2 pins, the differential voltage V(TPOUTP)-V(TPOUTN) is positive during the linkpulse. **LVPECL/PECL Compatible Interface Mode:** LVPECL or PECL interface positive and complementary outputs. These outputs form a differential current output pair that drives NRZI encoded 100BASE-FX or 100BASE-SX symbols during 100 Mb/s mode, Manchester encoded 10BASE-FL data or OPT_IDL during 10 Mb/s mode, and FLNP Bursts during Auto-Negotiation. TPOUTP and TPOUTN are loaded with external resistors to VCC and AC coupled to the inputs of a 1x9 fiber optic PMD module. A resistor network may be needed to setup the common mode voltage at the input pins of the PMD module.

PIN DESCRIPTIONS (continued)

Pin #	Signal Name	Description
38	RTTP	Twisted pair or LVPECL/PECL compatible driver bias resistor. An external resistor connected between RTTP and ground sets a constant bias current for the differential output driver circuitry. These output currents depend on the operating mode. The recommended external component values are: **Twisted pair mode:** 2KΩ, 1 %, between RTTP and ground. 50Ω, 1 %, between TPOUTP and VCC 50Ω, 1 %, between TPOUTN and VCC **LVPECL/PECL compatible mode:** 2KΩ, 1 %, between RTTP and ground. 62Ω, 1 %, between TPOUTP and VCC 62Ω, 1 %, between TPOUTN and VCC Also AC couple to the PMD inputs
10	TPINP	Two operating modes are available for these pins and are selected with the configuration pin PECLTP or the configuration bit LVPECLTP (bit 30.3).
11	TPINN	**Twisted Pair Interface Mode:** Receive twisted pair positive and complementary inputs. These inputs form a differential input pair that receives 100BASE-TX, FLP Burst, or 10BASE-T signal from the network. The common mode voltage is set internally and the input impedance is about 10KΩ. **LVPECL/PECL Compatible Interface Mode:** LVPECL or PECL compatible interface positive and complementary inputs. These inputs form a differential input pair that receives 100BASE-FX, 100BASE-SX, FLNP Bursts, or 10BASE-FL signal from a fiber optic PMD. The PMD outputs are AC coupled to these inputs with .1mF capacitors. The common mode voltage is set internally with resistors of about 1KΩ from each input pin to an on-chip voltage reference. The positive output of the PMD (high during the high-light state) must connect to TPINP and the complementary output of the PMD must connect to TPIN
37	REQSD	**Twisted Pair Interface Mode:** Equalizer bias resistor pin. An external resistor connected between this pin and ground sets internal currents that control the receiver's adaptive equalizer transfer function. The voltage at this pin is PTAT. It's nominal value is 1.2V and it's range is .9V to 1.5V. The recommended resistor value is 5KΩ, 1 % **LVPECL/PECL Compatible Interface Mode:** This input pin is connected to the Signal Detect (SD) output of a fiber optic PMD module. The voltage level at this pin is compared to the voltage level at pin SDTH to determine the logic value. If it is lower, then the input at TPINP/TPINN is rejected. If it is higher, then the input at TPINP/TPINN is passed to the internal circuits.
39	SDTH	The voltage at this pin is a single ended LVPECL/PECL reference. Refer to description of SDFO and REQSD pins. This pin is not used if neither the TPINP/TPINN interface, nor the FOINP/FOINN are setup for LVPECL/PECL compatible mode. In such a case, the SDTH pin must be connected to any potential between VCC and Ground.
21	IOUT	2 operating modes are available for these pins and are selected with the configuration pin "PECL_QU" or the configuration bit "LVPECLQU" (bit 30.7).

PIN DESCRIPTIONS (continued)

Pin #	Signal Name	Description
22	$\overline{\text{IOUT}}$	**Fiber Optic Interface Mode:** IOUT (pin 21) is the Fiber optic LED driver output while pin $\overline{\text{IOUT}}$ (pin 22) is optionally used to provide current peaking. IOUT connects to the cathode of an external LED. It drives NRZI encoded 100BASE-FX or 100BASE-SX symbols during 100Mb/s mode, Manchester encoded 10BASE-FL data or OPTIDL during 10Mb/s mode, and FLNP Bursts during Auto-Negotiation. When peaking is not used, $\overline{\text{IOUT}}$ should connect to VCC. When peaking is used, an off-chip resistor from this pin to ground and an off-chip capacitor from this pin to IOUT determine the peaking current waveform. (Typical values are 1KΩ and 1nF) **LVPECL / PECL Compatible Interface Mode:** LVPECL or PECL interface positive and complementary outputs. These outputs form a differential current output pair that drives NRZI encoded 100BASE-SX or 100BASE-FX symbols during 100Mb/s mode, Manchester encoded 10BASE-FL data or OPTIDL during 10Mb/s mode, and FLNP Bursts during Auto-Negotiation. IOUT and $\overline{\text{IOUT}}$ are loaded with external resistors to VCC and AC coupled to the inputs of a 1x9 fiber optic PMD module. A resistor network may be needed to setup the common mode voltage at the input pins of the PMD module.
36	RTOP	Fiber optic LED or LVPECL/PECL driver bias resistor. An external resistor connected between RTOP and ground sets a constant bias current for the single ended LED driver or differential LVPECL/PECL driver circuitry. These output currents depend on the operating mode. The recommended external component values are: Fiber Optic Interface mode: (1% resistors, +/- 10% currents) Indicated is the current into pin IOUT during the High-Light state. 2.8KΩ between RTOP and ground for 50mA. 2KΩ between RTOP and ground for 70mA. 1.4KΩ between RTOP and ground for 100mA. LVPECL Interface mode: 1.4KΩ, 1 %, between RTOP and ground for 10mA tail current. 62Ω , 1 %, between IOUT and VCC. 62Ω 1 %, between $\overline{\text{IOUT}}$ and VCC. Also AC couple to PMD inputs.
33	FOINP	2 operating modes are available for these pins and are selected with the configuration pin PECLQU or the configuration bit LVPECLQU (bit 30.7).
32	FOINN	**Fiber Optic Interface Mode:** Fiber optic quantizer positive and complementary inputs. FOINP is capacitively coupled to the output of a fiber optic receiver, while FOINN is capacitively coupled to the VCC of the fiber optic receiver. Recommended capacitor values: 10nF, 5%. FOINP voltage must be higher during the “high light” state than during the low-light state. LVPECL/PECL Compatible Interface Mode: LVPECL/PECL interface positive and complementary inputs. These inputs form a differential input pair that receives 100BASE-FX, 100BASE-SX, FLNP Bursts, or 10BASE-FL signal from a fiber optic PMD. The PMD outputs are AC coupled to these inputs with .1mF capacitors. The common mode voltage is set internally with resistors of about 500Ω from each input pin to an on-chip voltage reference. FOINP voltage must be higher during the “high light” state than during the low-light state.
30	CQOS	**Fiber Optic Interface Mode:** Data quantizer offset cancellation loop capacitor. An external capacitor between this pin and VCC determines the dominant pole of the offset cancellation feedback look. The recommended value is .1mF, 10 %. **LVPECL/PECL Compatible Interface Mode:** This pin is not used and should be left unconnected.

PIN DESCRIPTIONS (continued)

Pin #	Signal Name	Description
29	SDFO	**Fiber Optic Interface Mode:** This pin is not used and should be connected to any potential between VCC and Ground. **LVPECL/PECL Compatible Interface Mode:** This input pin is connected to the Signal Detect (SD) output of a fiber optic PMD. The voltage level at this pin is compared to the voltage level at pin SDTH to determine the logic value.
39	SDTH	The voltage at this pin is a single ended LVPECL/PECL reference. Refer to description of SDFO and REQSD pins. This pin is not used if either the TPINP/TPINN interface, or the FOINP/FOINN are setup for LVPECL/PECL compatible mode. In such a case, the SDTH pin must be connected to any potential between VCC and Ground.
41	TPINSPD	This output pulls up to indicate that 100Mb/s signal is present at the TPINP/TPINN interface, and it pulls down to indicates that 10Mb/s signal is present at the TPINP/TPINN interface. The signal can be idle or packets. This pin is set to high impedance otherwise. This pin can also be configured as a test output (see Test Outputs).
42	FOINSPD	This output pulls up to indicate that 100Mb/s signal is present at the FOINP/FOINN interface, and it pulls down to indicates that 10Mb/s signal is present at the FOINP/FOINN interface. The signal can be idle or packets. This pin is set to high impedance otherwise. This pin can also be configured as a test output (see Test Outputs).
43	TPANDT	When TPINSPD is in the high impedance state, no 10 or 100Mbs signal at TPINP/TPINN, the TPANDT LED pulls low while receiving Auto-Negotiation signal at the TPINP/TPINN interface. When TPINSPD is not in the high impedance state, the TPANDTpin pulls low to indicate that a data packet is being detected at the TPINP/TPINN interface. When a data packet is indicated, the pulse width at TPANDT is stretch to a minimum of 1.3 to 2.7ms to improve visibility (or 163ms to 328ms, when the TestFast bit 28.0 is 1). This pin can also be configured as a test output (see Test Outputs). In any other case this pin is in high impedance state.
44	FOANDT	When FOINSPD is in the high impedance state, no 10 or 100 Mb/s signal at FOINP/FOINN, the FOANDT LED pulls low while receiving Auto-Negotiation signal at the FOINP/FOINN interface. When FOINSPD is not in the high impedance state, the FOANDT pin pulls low to indicate that a data packet is being detected at the FOINP/FOINN interface. When a data packet is indicated, the pulse width at FOANDT is stretch to a minimum of 1.3 to 2.7ms to improve visibility (or 163ms to 328ms, when the TestFast bit 28.0 is 1). This pin can also be configured as a test output (see Test Outputs). In any other case this pin is in high impedance state.
40	BCKPLINK	When the Backup Link function is enabled, this pin is the enabler of a secondary link. Connect to VCC to disable this function. Pull down to ground to enable this function. Recommended pull down resistor value: 10KΩ.
7	PECLTP	This pin sets the Media Converter to interface at pins TPINP/TPINN and TPOUTP/TPOUTN, to an external PECL or LVPECL PMD, or to twisted pair interface magnetics. When PECL or LVPECL interface is selected, the 100Mb/s scrambler and descrambler functions are disabled by default and can be enabled with a management register bit. When twisted pair interface is selected, the scrambler and descrambler are enabled by default and can be disabled with a management register bit. When using twisted pair interface, this pin also indicates the maximum supported link distance. When the 10m maximum link length is selected, the input is not equalized before being sliced.

PIN DESCRIPTIONS (continued)

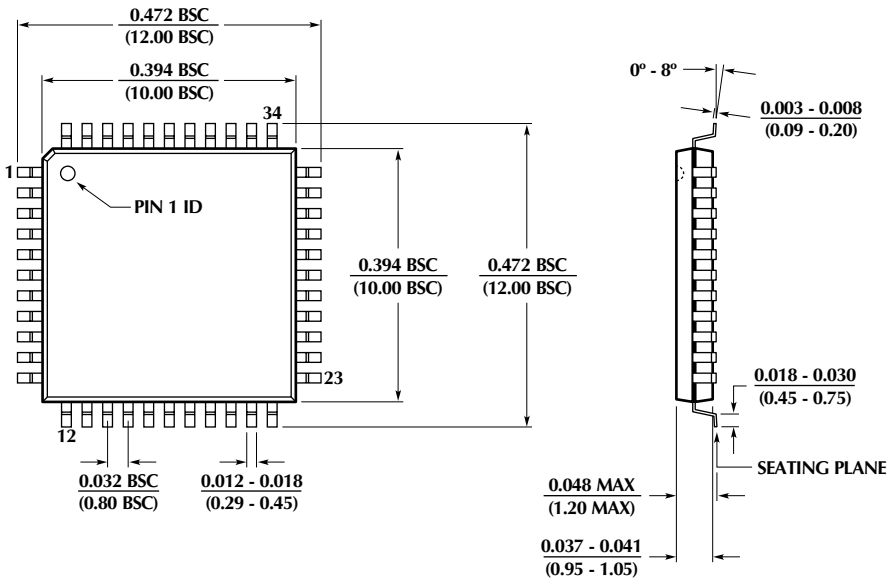
Pin #	Signal Name	Description
8	PECLQU	This pin sets the Media Converter to interface at pins FOINP/FOINN and IOUT /$\overline{\text{IOUT}}$, to an external PECL or LVPECL PMD, or to an LED and a fiber optic receiver. When using an LED and fiber optic receiver, this pin also indicates the maximum supported link distance. When the 300m maximum link length is selected, the voltage thresholds for Signal Detect are increased.
4	AD4LIW	Determines the value of the PHY address bit 4 for accessing the Serial Management Interface, and determines if the Link Integrity Warning (LIW) function is enabled or disabled. The Link Integrity Warning (LIW) function can only be enabled when only one SPEED is available through setting of pin SPEED and/or management registers. When LIW is enabled and the input link is down at one interface to the Media Converter, the transmitter output on that interface is turned off for about 425ms every 3.8 seconds (or 104ms every 934ms, when the TestFast bit 28.0 is 1). It applies to both network interfaces and both data rates. Notice that if the link at the other interface to the Media Converter is also down, there is never an output. The LIW function causes the Link Up indicator of the link partner to blink.
5	AD32	Determines the value of the PHY address bits 3 and 2 for accessing the Serial Management Interface.
6	AD10	Determines the value of the PHY address bits 1 and 0 for accessing the Serial Management Interface.
25	DUPLEX	This DUPLEX input can have one of three (3) levels. VCC, VCC/2 and 0Volt. DUPLEX input has 80KW resistors to VCC and Ground. With the input floating the input voltage is VCC/2. Left open the Transparent mode of operation is enabled. VCC or 0Volt at the DUPLEX input enables the Non-Transparent mode of operation
27	SPEED	This SPEED input can have one of three (3) levels: VCC, VCC/2, and 0Volt. VCC input enables only 100Mb/s operation. 10Mb/s and Auto-Negotiation are disabled. Duplex operation is also disabled. SPEED input has 80KΩ resistor to VCC and Ground. With the input floating the input voltage is VCC/2. Left open, this mode enables 100Mb/s and 10Mb/s operation. The Duplex mode enables Transparent or Non-Transparent mode operation. Link Integrity Warning (LIW) can be enabled. 0Volt input on SPEED enables only 10Mb/s operation. 100Mb/s and Auto-Negotiation are disabled. Duplex operation is also disabled
13	$\overline{\text{TPOUTOFF}}$	When this input is low, the output stage of the twisted pair output is turned off. CMOS input.
14	$\overline{\text{FOOUTOFF}}$	When this input is low, the output stage of the fiber optic output is turned off. CMOS input.
24	$\overline{\text{PWRDWN}}$	When this input is low, all the circuits are powered down. Configuration pins are read and register bits are initialized, 3 to 8ms after a rising edge of PWRDWN. CMOS input.
18	REFCLOCK	25MHz Reference clock CMOS input. This clock is used for internal digital logic, and as a reference for the PLLs.
2	GNDT	Ground for the twisted pair driver output stage.
12	GNDE	Ground for the equalizer, one PLL and part of the descrambler and twisted pair driver.
15	GNDD	Ground for CMOS noisy circuits.
20	GNDL	Ground for the fiber optic LED driver output stage.

PIN DESCRIPTIONS (continued)

Pin #	Signal Name	Description
28	GNDFC	Ground for one PLL, part of the scrambler, fiber optic LED driver, and quantizer.
34	GNDQ	Ground for the data quantizer and central bias.
35	GNDB	Ground for part of the central biasing.
9	VCCE	Power supply for the equalizer, one PLL and part of the descrambler and twisted pair driver.
19	VCCD	Power supply for CMOS noisy circuits.
23	VCCL	Power supply for the fiber optic LED driver output stage.
26	VCCFC	Power supply for one PLL, part of the scrambler, fiber optic LED driver, and quantizer.
31	VCCQ	Power supply for the data quantizer and central bias.
16	MDIO	Management data TTL input/output pin.
17	MDC	Management clock TTL input. The maximum frequency can be 12.5MHz instead of the 2.5MHz limit of IEEE 802.3.

PHYSICAL DIMENSIONS (inches/millimeters)

Package: H44-10
44-Pin (10 x 10 x 1mm) TQFP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6651CH	0^0C to 70^0C	44 Pin TQFP (10 x 10 x 1.4mm body)

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