Micro Linear

ML6673

Fast Ethernet/FDDI TP-PMD Transceiver

GENERAL DESCRIPTION

The ML6673 is a complete monolithic transceiver for 125 Mbaud MLT-3 encoded data transmission over Category 5 unshielded twisted pair and shielded twisted pair cables. The ML6673 integrates the baseline restoration function defined in the TP-PMD standard. The adaptive equalizer in the ML6673 will accurately compensate for line losses exceeding the IEEE 802.3u limit of 100m of UTP.

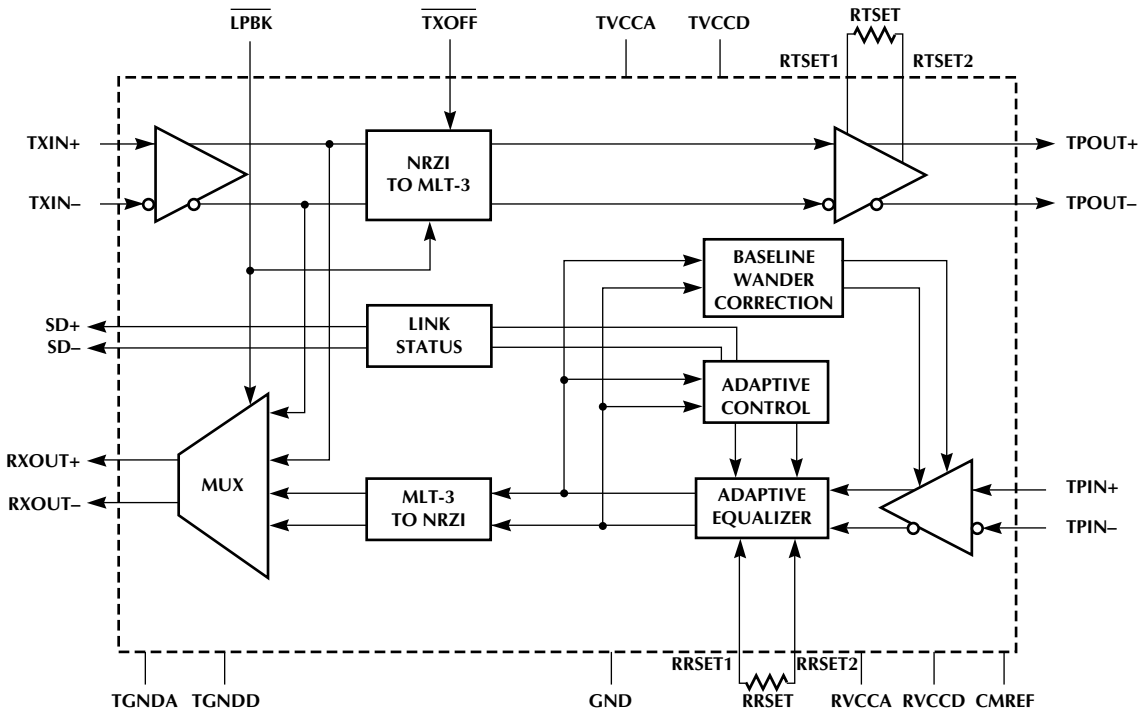
The ML6673 receive section consists of an equalizing filter with a feedback loop for controlling effective line compensation. The feedback loop contains a filter and detection block for determining the proper control signal. The ML6673 also contains data comparators with precisely controlled slicing thresholds and an MLT-3 to NRZI translator.

The ML6673 transmit section accepts ECL 100K compatible NRZ inputs and converts them to differential current mode MLT-3 signals. Transmit amplitude is controlled by a single external resistor.

FEATURES

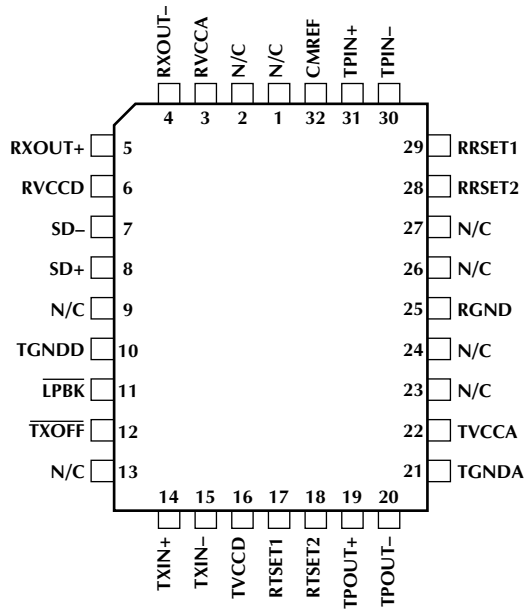
- Compliant with IEEE 802.3u Fast Ethernet (100BASE-TX) standard
- Compliant with ANSI X3T12 FDDI over copper (TP-PMD) standard
- Integrated baseline wander correction circuit
- Transmitter converts NRZI ECL signals to MLT-3 current driven outputs
- Transmitter can be externally turned off (high impedence) for true quiet line
- Receiver includes adaptive equalizer and MLT-3 to NRZI decoder
- Operates over 100 meters of STP or category 5 UTP Twisted Pair Cable set by the IEEE 802.3u standards
- 32-pin PLCC and TQFP

BLOCK DIAGRAM

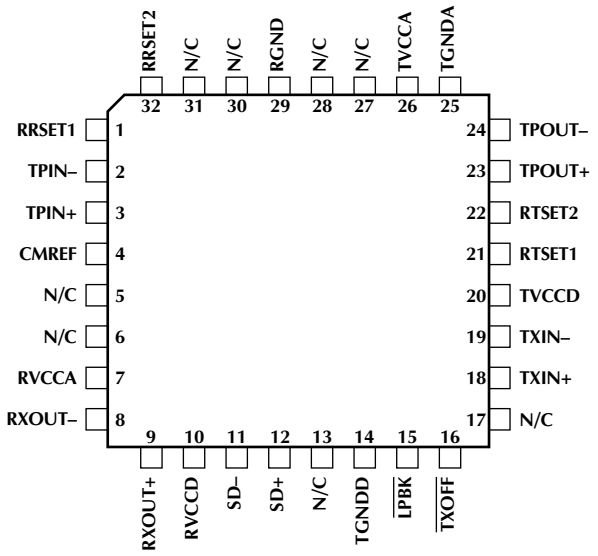


PIN CONFIGURATION

ML6673
32-Pin PCC (Q32)



ML6673
32-Pin TQFP (H32-7)



PIN DESCRIPTION

NAME	FUNCTION
TXIN+, TXIN–	These differential ECL100K compatible inputs receive NRZI data from the PHY for transmission.
TPOUT+, TPOUT–	Outputs from the NRZI-MLT3 state machine drive these differential current outputs. The transmitter filter/transformer module connects the media to these pins.
$\overline{\text{LPBK}}$	This TTL input enables transmitter-receiver loopback internally when asserted low. When LPBK is asserted, signal detect is asserted.
$\overline{\text{TXOFF}}$	This TTL input forces the NRZI-MLT3 state machine to a high impedence state when asserted low and shuts off transmit bias current.
RTSET1, RTSET2	An external 1% resistor connected between these pins controls the transmitter output current amplitude. I_{OUT} = 64 x 1.25V/RTSET
TVCCA, TVCCD	Separate analog and digital transmitter power supply pins help to isolate sensitive circuitry from noise generating digital functions. Both supplies are nominally +5 volts.
TGNDA, TGNDD	Analog and digital transmitter grounds provide separate return paths for clean and noisy signals.
SD+, SD–	These differential ECL100K compatible outputs indicate the presence of a data signal with an amplitude exceeding a preset threshold.
TPIN+, TPIN–	MLT-3 encoded data from the receiver filter/transformer module enters the receiver through these pins.
RXOUT+, RXOUT–	Differential ECL100K compatible outputs provide NRZI encoded data to the PHY.
RRSET1, RRSET2	Internal time constants controlling the equalizer's transfer function are set by an external resistor connected across these pins.
CMREF	This pin provides a DC common mode reference point for the receiver inputs.
RVCCA, RVCCD	Analog and digital supply pins are separated to isolate clean and noisy circuit functions. Both supplies are nominally +5 volts.
RGND	Receiver ground.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} Supply Voltage Range ..... GND –0.3V to 6V
Input Voltage Range
  Digital Inputs ..... GND –0.3V to V_{CC} +0.3V
Output Current
  TPOUT±, SD±, RXOUT± 50mA
  All other outputs 10mA
Junction Temperature ..... 150°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C
Thermal Resistance (θ_{JA})
  PLCC ..... 60°C/W
  TQFP ..... 80°C/W

OPERATING CONDITIONS

V_{CC} Supply Voltage ..... 5V ± 5%
T_A, Ambient Temperature ..... 0°C to 70°C
RTSET ..... 2kΩ ±1%
RRSET ..... 9.53kΩ ±1%
Receive Transformer Insertion Loss ..... < –0.5dB

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ±5%, RTSET = 2kΩ. (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics					
Supply Current					
RVCCD			74		mA
RVCCA			65		mA
TVCCD			24		mA
TVCCA			6		mA
RVCCD + RVCCA + TVCCD + TVCCA				195	mA
TTL Inputs ($\overline{TXOFF}$, $\overline{LPBK}$)					
V_{IL} Input Low Voltage				0.8	V
V_{IH} Input High Voltage		2.0			V
Differential Inputs (TPIN±, TXIN±)					
TPIN+, TPIN– Common Mode Input Voltage		2.2		V_{CC}	V
TPIN+, TPIN– Differential Input Voltage				1.5	V
TPIN+, TPIN– Differential Input Resistance		10.0K			Ω
TPIN+, TPIN– Common Mode Input Current				+10	µA
TXIN+, TXIN– Input Voltage HIGH (V_{IH})		V_{CC}–1.165		V_{CC}–0.88	V
TXIN+, TXIN– Input Voltage LOW (V_{IL})		V_{CC}–1.810		V_{CC}–1.475	V
TXIN+, TXIN– Input Current LOW (I_{IL})		0.5			µA
TXIN+, TXIN– Input Current HIGH (I_{IH})				50	µA
Differential Outputs (SD±, RXOUT±, TPOUT±)					
SD+, SD–, RXOUT+, RXOUT– Output Voltage HIGH (V_{OH})	Note 3	V_{CC}–1.025		V_{CC}–0.88	V
SD+, SD–, RXOUT+, RXOUT– Output Voltage LOW (V_{OL})	Note 3	V_{CC}–1.81		V_{CC}–1.62	V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Outputs (SD±, RXOUT±, TPOUT±) (Continued)					
TPOUT+, TPOUT– Output Current HIGH	$V_{OUT} = V_{CC} \pm 0.5$, Note 2	38.0		42.0	mA
TPOUT+, TPOUT– Output Current LOW	$V_{OUT} = V_{CC} \pm 0.5$, Note 2	0		0.5	mA
TPOUT+, TPOUT– Output Current Offset				0.5	mA
TPOUT+, TPOUT–$V_{OUT} = V_{CC}$ Output Amplitude Error	Note 2	–5.0		5.0	%
TPOUT+, TPOUT–$V_{OUT} = V_{CC} \pm 1.1V$ Output Voltage Compliance		–2.0		+2.0	%
AC Characteristics					
TPOUT+, TPOUT– Rise/Fall Time			2.0		ns
TPOUT+, TPOUT– Output Jitter			0.8		ns
RXOUT+, RXOUT– Rise/Fall Time			2.0		ns
RXOUT+, RXOUT– Output Jitter			2.0		ns

Note 1. Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 2. Output current amplitude is determined by $I_{OUT} = 64 \times 1.25V/RTSET$.
Note 3. Output voltage levels are specified when terminated by 50Ω to $V_{CC} - 2V$ or equivalent load.

FUNCTIONAL DESCRIPTION

The ML6673 MLT-3 transceiver is a physical media dependent transceiver that allows the transmission and reception of 125 Mbaud data over shielded twisted pair cable or category 5 unshielded twisted pair cable. It provides a standard Physical Media Dependent (PMD) interface compatible with many FDDI chip sets.

The transmit section accepts NRZI data, converting it to a three level MLT-3 code and sending the information on a two pin current driven transmitter. The transmitted output passes through an external low pass filter and transformer before entering the connectors to the STP or UTP cable. The output amplitude of the transmitted signal is programmable through the external RTSET resistor.

$$I_{OUT} = \frac{64 \times 1.25V}{RTSET}$$

For 100BASE-TX UTP application, the transmit amplitude is 2VP-P differential achieved by setting RTSET = 2kΩ (1%).

The receive section accepts MLT-3 coded data after passing through an isolation transformer and band limiting filter. Before the data can be converted from MLT-3 back to NRZI, the adaptive equalizer is used to compensate for the amplitude and phase distortion incurred from the cable. The adaptive control section determines the signal amplitude (and therefore the cable length) and adjusts the equalizer accordingly.

The receiver also includes the Baseline Wander correction circuitry. The circuit will compensate and track the DC baseline wander caused by DC imbalance of the received data. It will tolerate the test pattern as specified in the ANSI X3T12 TP-PMD specification. A parallel 10pF capacitor can be connected between TPIN+ and TPIN– to improve Bit Error Rate.

The adaptive control block governs both the equalization level as well as the signal detection status. Signal detect is asserted when the equalizer control loop settles or when loop back is asserted. When the input signal is small, the equalization will be at its maximum.

After the signal has been equalized, it passes into the MLT-3 to NRZI converter where it is converted back to NRZI and fed through the loopback multiplexer onto the RXOUT± pins.

Figure 1 shows a timing diagram of NRZI data and the equivalent MLT-3 data. The MLT-3 data shows the output current I_{OUT} for one side of the transmitter, either TPOUT+ or TPOUT–. The other transmit output pin will be the complement. Whenever there is a change in level in NRZI, MLT-3 will change levels too. The maximum fundamental frequency of MLT-3 is half of the maximum fundamental of NRZI.

Figure 2 shows a typical gain vs frequency plot of the adaptive equalizer for 0, 25, 50, 75 and 100 meter category 5 cable lengths.

ML6671 COMPATIBILITY

The ML6673 implements the Baseline Wander correction circuit, in addition to providing the functionality of the existing ML6671 device. The ML6673 is plug-compatible with the ML6671 with the following note:

- In the ML6673 design, the following passive components may be eliminated
  - — RSET resistor
  - — RTH resistor
  - — CAP1 capacitor
  - — CAP2 capacitor

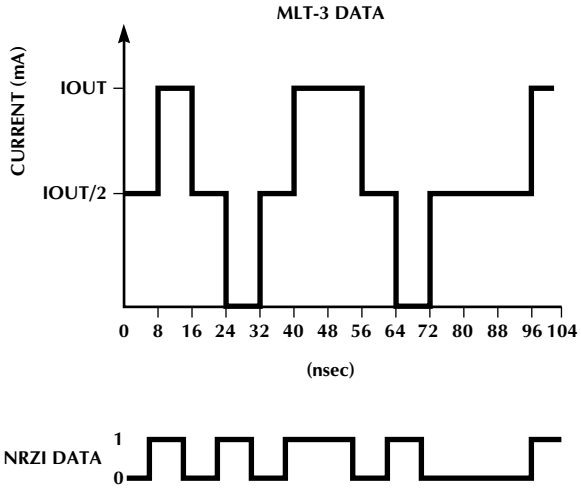


Figure 1. MLT-3 Encoding

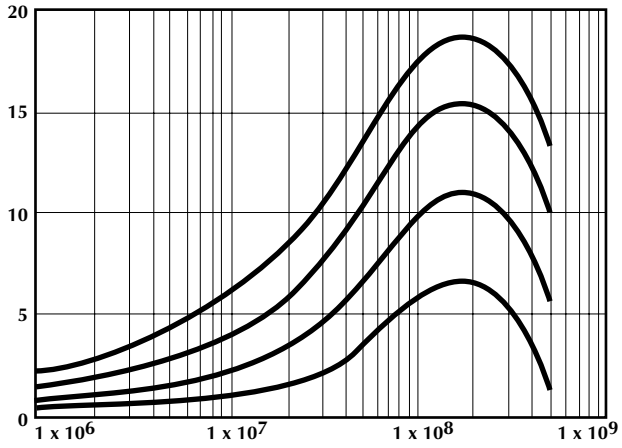
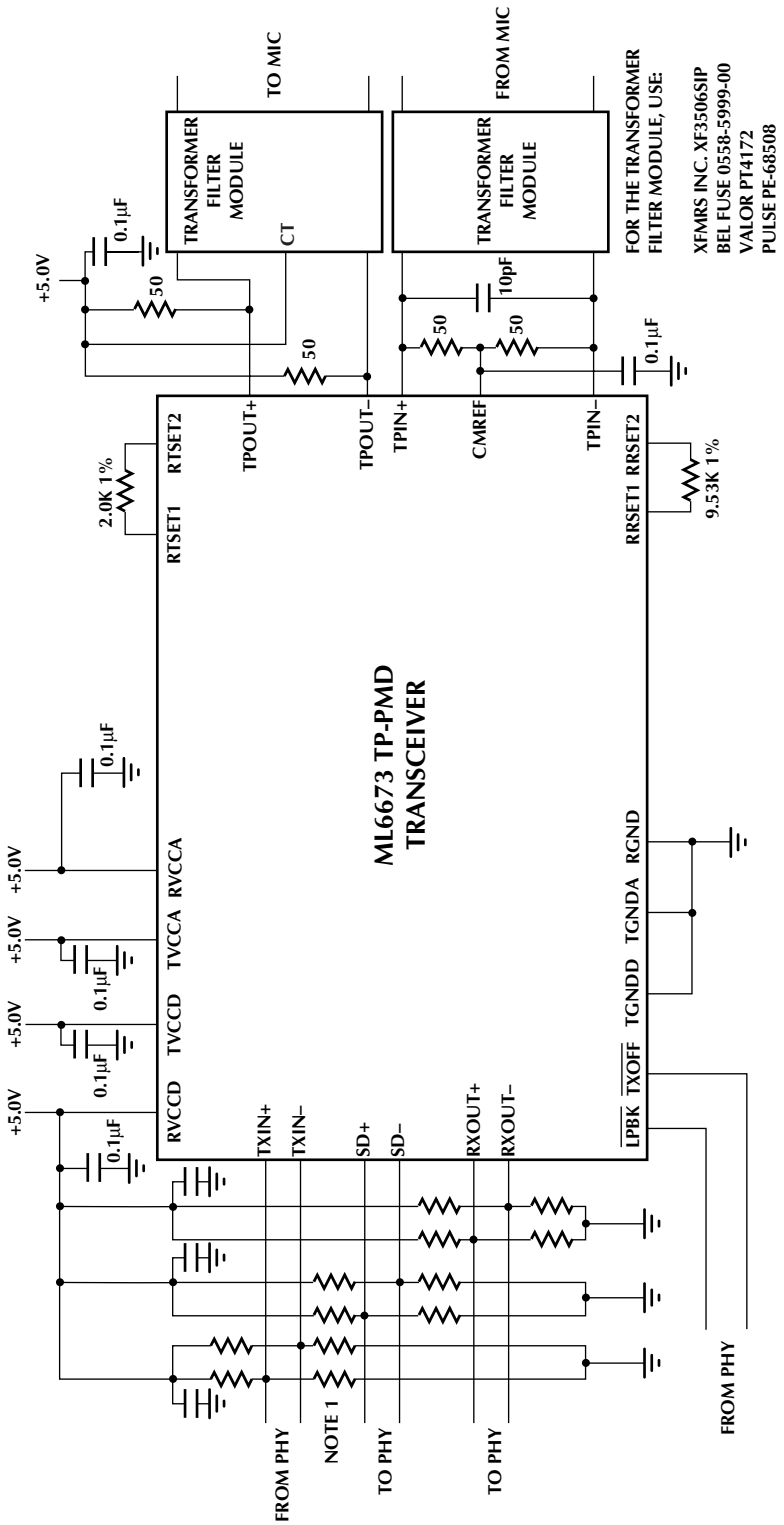


Figure 2. Equalization Range

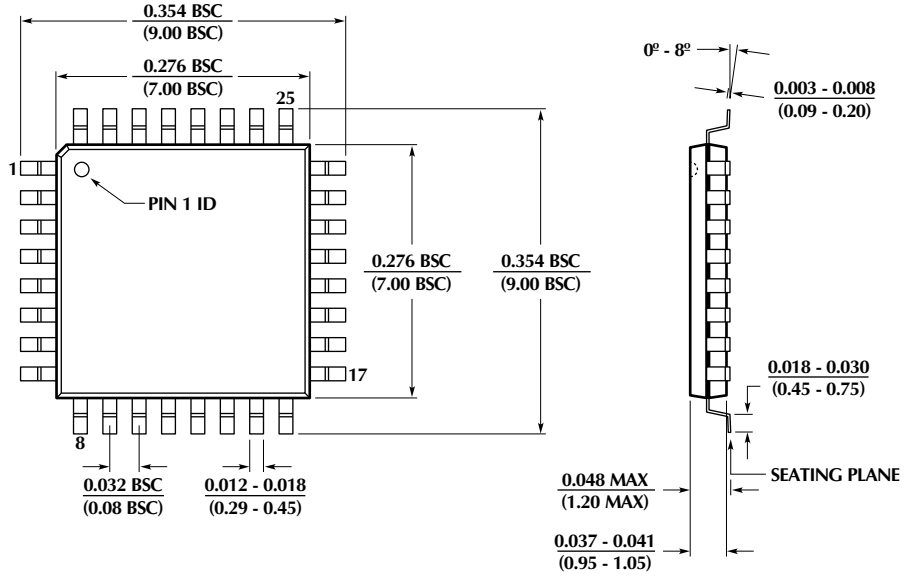


Application Example of ML6673 Configured for 2.0V_{P-P} Transmit Amplitude on C5 UTP.

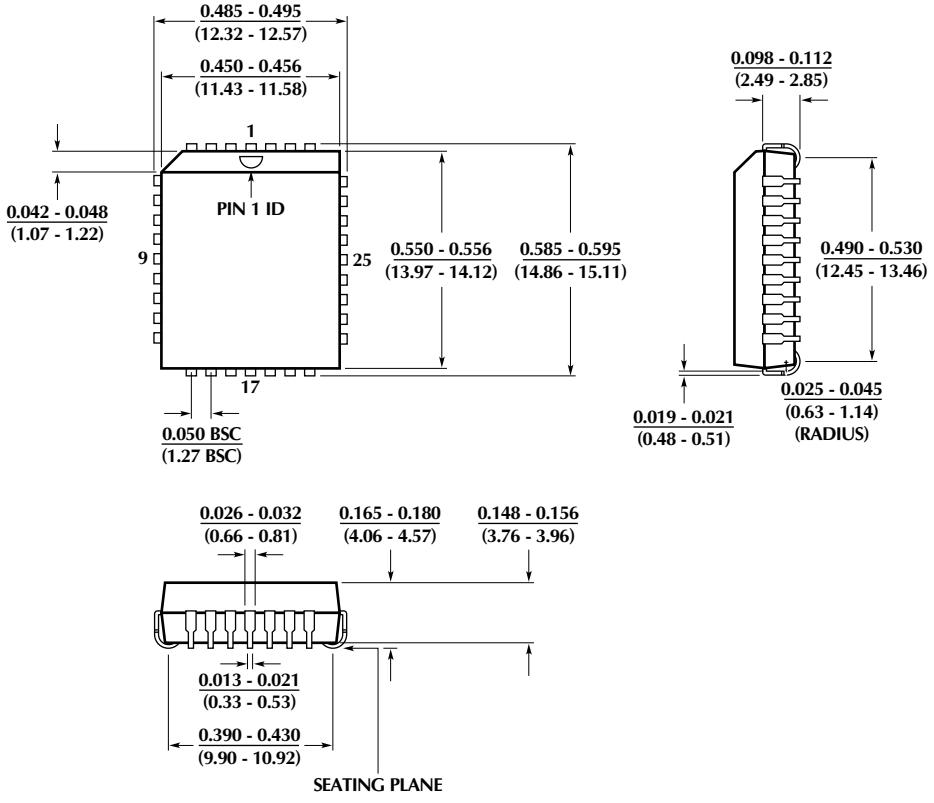
Note 1. Split 100K ECL terminations are 82ý and 130ý to VCC and GND respectively.
Note 2. Recommended power supply bypass capacitors are 0.1µF with optional 10µF tantalum in parallel.
Note 3. Transformer turns ratio is 1:1.
Note 4. LPBK and TXOFF inputs are active LOW.

PHYSICAL DIMENSIONS inches (millimeters)

Package: H32-7
32-Pin (7 x 7 x 1mm) TQFP



Package: Q32
32-Pin PLCC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6673CQ	0°C to 70°C	32-Pin PLCC (Q32)
ML6673CH	0°C to 70°C	32-Pin TQFP (H32-7)

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Products described in this document may be covered by one or more of the following patents, U.S.: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; Japan: 2598946; 2619299. Other patents are pending.

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