

100BASE-X Fiber Physical Layer With 5-bit Interface

GENERAL DESCRIPTION

The ML6695 implements the physical layer of the Fast Ethernet 100BASE-X standard for fiber media. The device provides the 5-bit (or symbol) interface for interface to upper-layer silicon. The ML6695 integrates the data quantizer and the LED driver, allowing the use of low cost optical PMD components.

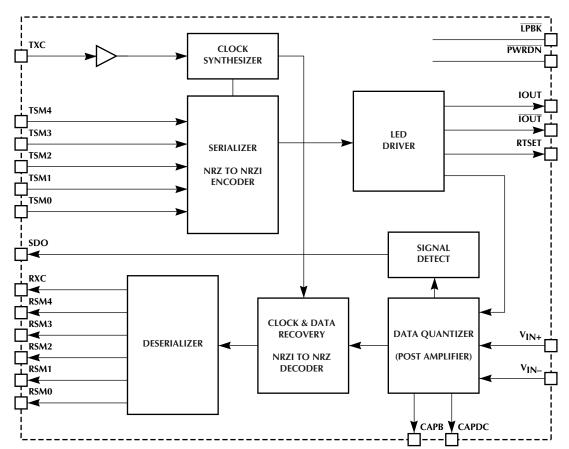
The ML6695 includes 125MHz clock recovery/clock generation, an LED driver, and a data quantizer (post amplifier). The device also offers a power down mode which results in total power consumption of less than 20mA.

The ML6695 is suitable for the current 100BASE-FX IEEE 803.2u standard defined using 1300nm optics, as well as for the *proposed* 100BASE-SX standard defined using lower cost 820nm optics.

FEATURES

- 100BASE-FX physical layer with 5-bit interface
- Optimal 100BASE-SX solution (draft standard)
- Integrated data quantizer (post-amplifier)
- Integrated LED driver
- 125MHz clock generation and recovery
- Power-down mode

BLOCK DIAGRAM

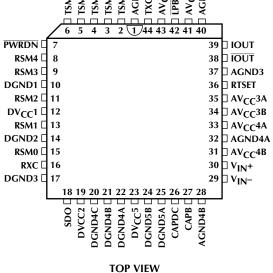




PIN CONFIGURATION

44-Pin PLCC (Q44) 7 8 9

ML6695



PIN DESCRIPTION

PIN		FUNCTION	PIN	NAME	FUNCTION
FIN	INAME	FUNCTION	FIIN	INAME	FUNCTION
1	A _{GND} 1	Analog ground	5	TSM1	Transmit data TTL inputs. TSM 0-4 inputs accept TX data symbols
2	TSM4	Transmit data TTL inputs. TSM 0-4 inputs accept TX data symbols from the MII. Data appearing at TSM 0-4 are clocked into the ML6695 on the rising edge of			from the MII. Data appearing at TSM 0-4 are clocked into the ML6695 on the rising edge of TXC.
		TXCLK .	6	TSM0	Transmit data TTL inputs. TSM 0-4 inputs accept TX data symbols
3	TSM3	Transmit data TTL inputs. TSM 0-4 inputs accept TX data symbols from the MII. Data appearing at TSM 0-4 are clocked into the ML6695 on the rising edge of			from the MII. Data appearing at TSM 0-4 are clocked into the ML6695 on the rising edge of TXC.
		TXC.	7	PWRDN	Powerdown TTL input. Driving this pin low, or floating the pin, powers
4	TSM2	Transmit data TTL inputs. TSM 0-4 inputs accept TX data symbols from the MII. Data appearing at TSM 0-4 are clocked into the ML6695 on the rising edge of			the ML6695 down to a low- current, inoperative state. Driving PWRDN high enables the ML6695.
		TXC.	8	RSM4	Receive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising edge.



PIN DESCRIPTION (Continued)

NAME	FUNCTION	PIN	NAME	FUNCTION
RSM3	Receive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising edge.	26	CAPDC	Data quantizer offset-correction loop, offset-storage capacitor input pin. The capacitor tied between this pin and AV _{CC} stores the amplified data quantizer offset
DGND1	Digital ground			amplified data quantizer offset voltage and also sets the dominant
RSM2	Receive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising	27	CARR	pole in the offset-correction loop. A 0.1µF surface mount is recommended.
	0	27	САРВ	Data quantizer input bias bypass capacitor input. The capacitor tied
				between this pin and AV _{CC} filters the quantizer's internal input bias
RSM1	4 output may be sampled			reference. A 0.1µF surface-mount capacitor is recommended.
	edge.	28	AGND4B	Analog ground
DGND2	Digital ground	29	V_{IN} -	Receive quantizer input. This differential input pair receives
RSM0	Receive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising			100BASE-FX NRZI signals from the network opto-coupler.
RXC	edge. Recovered receive symbol clock TTL output. This 25MHz clock is	30	V _{IN} +	Receive quantizer input. This differential input pair receives 100BASE-FX NRZI signals from the network opto-coupler.
	125MHz bit clock recovered from	31	AV _{CC} 4B	Analog positive power supply
	Receive data are clocked out at	32	AGND4A	Analog ground
	this clock.	33	AV _{CC} 4A	Analog positive power supply
DGND3	Digital ground	34	AV _{CC} 3B	Analog positive power supply
SDO	Signal Detect TTL output. This	35	AV _{CC} 3A	Analog positive power supply
	at VIN+/- exceeds the preset amplitude threshold.	36	RTSET	Transmit level bias resistor. For 100BASE-FX, an external 2.32kΩ, 1% resistor connected between
DV _{CC} 2	Digital positive power supply			RTSET and AGND3 sets a
DGND4C	Digital ground			precision constant bias current that gives a nominal output "on" current of 75mA at I _{OUT} .
DGND4B	Digital ground	27		Analog ground
DGND4	Digital ground			
DV _{CC} 5	Digital positive power supply	30	1001	Transmit LED output. This pin connects through an external 15Ω
DGND5B	Digital ground			resistor to AV _{CC} when the part is used to drive a network LED.
DGND5A	Digital ground			
	RSM3 DGND1 RSM2 DV _{CC} 1 RSM1 DGND2 RSM0 RXC RXC DGND3 SDO DV _{CC} 2 DGND4C DGND4B DGND4B DGND4B DGND4B	RSM3Receive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising edge.DGND1Digital groundRSM2Receive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising edge.DV _{CC} 1Digital positive power supplyRSM1Receive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising edge.DV _{CC} 1Digital positive power supplyRSM1Receive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising edge.DGND2Digital groundRSM0Receive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising edge.DGND2Digital groundRSM0Receive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising edge.DGND2Digital groundRXCRecovered receive symbol clock TTL output. This 25MHz clock is phase-aligned with the internal 125MHz bit clock recovered from the signal received at VIN+/ Receive data are clocked out at RSM 0-4 on the falling edges of this clock.DGND3Digital groundSDOSignal Detect TTL output. This output goes high when the signal at VIN+/- exceeds the preset amplitude threshold.DV _{CC} 2Digital groundDGND4EDigital groundDGND4Digital groundDV _{CC} 5Digital groundDV _{CC} 5Digital ground	RSM3Receive data TTL outputs. RSM 0-4 doutput may be sampled synchronously with RXC's rising edge.26DGND1Digital ground27RSM2Receive data TTL outputs. RSM 0-4 doutput may be sampled synchronously with RXC's rising edge.27DV _{CC} 1Digital positive power supply27RSM1Receive data TTL outputs. RSM 0-4 doutput may be sampled synchronously with RXC's rising edge.28DGND2Digital ground29RSM0Receive data TTL outputs. RSM 0-4 doutput may be sampled synchronously with RXC's rising edge.28DGND2Digital ground29RSM0Receive data TTL outputs. RSM 0-4 doutput may be sampled synchronously with RXC's rising edge.30RXCReceive data TTL outputs. RSM 0-4 doutput may be sampled synchronously with RXC's rising edge.30RXCReceive data TTL output. This 25MHz clock is phase-aligned with the internal 125MHz bit clock recovered from the signal received at VIN+/ Receive data are clocked out at RSM 0-4 on the falling edges of this clock.33DGND3Digital ground34SDOSignal Detect TTL output. This output goes high when the signal at VIN+/- exceeds the preset amplitude threshold.37DV _{CC} 2Digital ground37DGND4Digital ground37DGND4Digital ground38DV _{CC5} Digital ground38	RSM3Receive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising edge.26CAPDCDGND1Digital groundRSM2Receive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising edge.27CAPBDVcc1Digital positive power supply27CAPBDVcc1Digital positive power supply28AGND4BDGND2Digital ground29VIN-RSM0Receive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising edge.28AGND4BDGND2Digital ground29VIN-RSM0Receive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising edge.30VIN+RXCReceive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising edge.30VIN+RXCReceive data TTL outputs. RSM 0- 4 output may be sampled synchronously with RXC's rising edge.30VIN+RXCReceive data TTL outputs. RSM 0-4 4 output may be sampled synchronously with RXC's rising edge.30VIN+RXCReceive data TTL outputs. RSM 0-4 4 output may be sampled synchronously with RXC's rising edge.30VIN+RXCReceive data TTL outputs. RSM 0-4 4 output may be sampled synchronously with RXC's rising edge.31AVcc4ADGND3Digital ground34AVcc3BSDOSignal Detect TTL output. This output goes high when the signal at VIN+/- excected the preset amplitude th



PIN DESCRIPTION (Continued)

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
39	IOUT	Transmit LED output. This open- collector current output drives NRZI waveforms into an LED.	43	AV _{CC} 1	Analog positive power supply
		Output current can be set externally by choosing RTSET value.	44	TXC	Transmit clock TTL input. This 25MHz clock is phase-aligned with the internal 125MHz TX bit clock. Data appaging at
40	AGND2	Analog ground			clock. Data appearing at Tsm<4:0> are clocked into the ML6695 on the rising edge of this
41	$AV_{CC}2$	Analog positive power supply			clock.
42	LPBK	Loopback TTL input pin. Tying this pin to ground places the part in loopback mode; data at TSM0 0-4 are serialized, then sent to the quantizer, followed by the receive PLL for clock recovery, and finally to the RSM<4:07> outputs. Floating this pin or tying it to V _{CC} places the part in its normal mode of operation.			

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V _{CC} Supply Voltage Range–0.3V to 6V
Input Voltage Range
Digital Inputs
VIN+, VIN-, TXC, CAPDC, CAPB –0.3V to V _{CC}
Output Current
IOUT, IOUT 90mA
All Other Outputs 10mA

Junction Temperature	0°C to 125°C
Storage Temperature	
Lead Temperature (Soldering,	
Thermal Resistance (θ_{IA})	

OPERATING CONDITIONS

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{CC} = 5V \pm 5\%$, $T_A = Operating Temperature Range (Note 1)$ SYMBOL **CONDITIONS** MIN ТҮР UNITS PARAMETER MAX TTL INPUTS (TSM<4:0>, LPBK, TXC, PWRDN) Input Low Voltage $I_{II} = -400 \mu A$ V V_{IL} -0.3 0.8 V_{IH} Input High Voltage $I_{IH} = 100 \mu A$ 2.0 V_{CC}+0.3 V μΑ Ι_{ΙL} Input Low Current $V_{IN} = 0.4V$ -200Input High Current $V_{IN} = 2.4V$ 100 μΑ $I_{\rm H}$ TTL OUTPUTS (RSM<4:0>, RXC, SDO) V VOL Output Low Voltage $I_{OL} = 4mA$ 0.4 Output High Voltage VOH $I_{OH} = -4mA$ 2.4 RECEIVER -V $V_{CC} = 5V$ 2.5 VICM V_{IN+/-} input common-mode voltage VID V_{IN+/-} differential input voltage range 3.5 1700 mV_{P-P} RIDR V_{IN}+/- differential input resistance 500 1k Ω Signal detect assertion threshold peak-to-peak non-idle 8 V_{SDA} 12 mV_{P-P} signal level at V_{IN}+/- for SDO assertion Input hysteresis 1.5 2 dB A_{HYST}

TRANSMITTER

IRT

RTSET input current

I _{LEDH}	I _{OUT} high output current (Note 2)	$RTSET = 2.32k\Omega \pm 1\%$	67.5	75	82.5	mA		
I _{LEDL}	I _{OUT} /I _{OUT} low output current	$RTSET = 2.32k\Omega \pm 1\%$			0.1	mA		
POWER SU	POWER SUPPLY CURRENT							

 $RTSET = 2.32k\Omega \pm 1\%$

I _{CC}	Supply Current, 100BASE-FX operation, transmitting	Current into all V _{CC} pins, V _{CC} = $5.25V$	200	295	mA
I _{PD}	Supply Current, Powerdown Mode			20	mA



594

μΑ

540

486

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	ТҮР	MAX	UNITS
TRANSMIT	ITER (NOTE 8)					
t _{TR/F}	I _{OUT} rise/fall time	Note 3			2	ns
t _{TDC}	I _{OUT} output duty cycle distortion	Note 3	-0.5		0.5	ns
SIGNAL D	ETECT					_
t _{AS}	SDO assert time (SDO low to high)	VIN>8mV _{P-P}			100	μs
t _{ANS}	SDO deassert time (SDO high to low)	VIN<8mV _{P-P}	350			μs
DATA INT	ERFACE					
X _{NTOL}	TX input clock frequency tolerance	25MHz frequency	-50		50	ppm
t _{TPWH}	TXC pulse width HIGH		14		ns	
t _{TPWL}	TXC pulse width LOW		14		ns	
t _{RPWH}	RXC pulse width HIGH		14		ns	
t _{RPWL}	RXC pulse width LOW		14		ns	
t _{TPS}	Setup time, TSM 0-4 data valid to TXC rising edge (1.4V point)		13			ns
t _{TPH}	Hold time, TSM 0-4 data valid after TXC rising edge (1.4V point)		3			ns
t _{RCS}	Time that RSM0-4 data are valid before RXC falling edge (1.4V point)		10			ns
t _{RCH}	Time that RSM0-4 data are valid after RXC falling edge (1.4V point)		10			ns
t _{RPCR}	RXC 10%-90% rise time				6	ns
t _{RPCF}	RXC 90%-10% fall time				6	ns

Unless otherwise specified, $V_{CC} = 5V \pm 5\%$, $T_A = Operating Temperature Range (Note 1)$

Note 1. Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

Note 2. Output current amplitude is $I_{OUT} = 207V/RTSET$.

Note 3. Using the test load shown in Figure 1, transmitting $"H"\ symbols.$



FUNCTIONAL DESCRIPTION

TRANSMIT SECTION

The ML6695 transmit section accepts parallel NRZ data nibbles, creates a serial NRZI data stream using the internal 125MHz clock multiplier, and provides an open-collector output IOUT to directly drive an LED. IOUT must be connected to V_{CC} through a 15 Ω resistor. The internal clock multiplier accepts an external 25MHz clock input.

The LED driver at IOUT is a current mode switch which develops the output light by sinking current through the network LED into IOUT. RTSET'S value determines the output current:

$$\mathsf{RTSET} = \left(\frac{1.25\mathsf{V}}{\mathsf{IOUT}}\right) \times 140\Omega \tag{1}$$

where IOUT is the desired output current.

RECEIVE SECTION

The ML6695 receive section includes a fiber optic quantizer and a 125MHz receive clock recovery circuit. The quantizer is a wide-bandwidth limiting amplifier with DC offset correction. The quantizer output drives a data comparator with a controlled slicing threshold. The comparator provides a large-amplitude receive signal. The clock recovery circuit extracts 125MHz receive clock from the large-amplitude signal, and provides the clock for the parallel data output registers. Received NRZ data nibbles appear at the RSM outputs synchronously with RXC falling edges. Received signals exceeding the preset signal detect amplitude threshold for more than 5µs cause the SDO output to go high. Received signals that fall below the preset threshold for more than 5µs cause SDO to go low.

OTHER MODES

The ML6695 will enter a power down mode when the \overline{PWRDN} pin is tied low. In this state the ML6695 powers down to a low-current (less than 20mA), inoperative state. Driving it high enables normal operation of the ML6695.

Loopback mode is entered when the \overline{LPBK} is tied to ground. In this mode, the data at TSM0-4 are serialized, then sent to the quantizer, followed by the receive PLL for clock recovery, and finally to the RSM0-4 outputs. Tying \overline{LPBK} to V_{CC} places the ML6695 in its normal mode of operation.

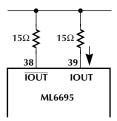
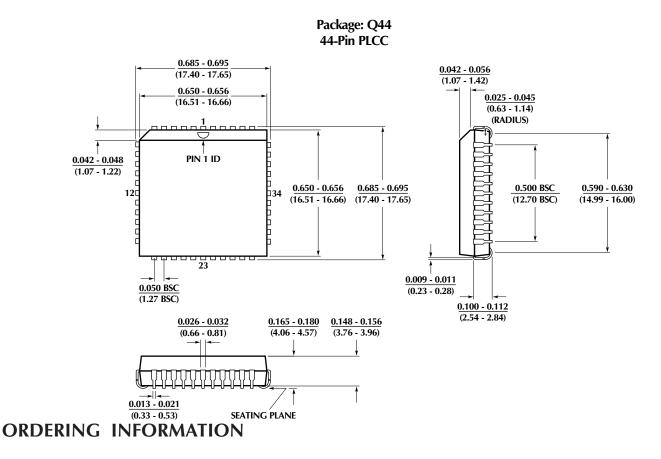


Figure 1. Test Load



PHYSICAL DIMENSIONS inches (millimeters)



PART NUMBER	TEMPERATURE RANGE	PACKAGE		
ML6695CQ	0°C to 70°C	44-Pin PLCC (Q44)		

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Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; 5,652,479; 5,661,427; 5,663,874; 5,672,959; 5,689,167; 5,714,897; 5,717,798; 5,742,151; 5,747,977; 5,754,012; 5,757,174; 5,767,653; 5,777,514; 5,793,168; 5,798,635; 5,804,950; 5,808,455; 5,811,999; 5,818,207; 5,818,669; 5,825,165; 5,825,223; 5,838,723; 5,844,378; 5,844,941. Japan: 2,598,946; 2,619,299; 2,704,176; 2,821,714. Other patents are pending.

2092 Concourse Drive San Jose, CA 95131 Tel: (408) 433-5200 Fax: (408) 432-0295 www.microlinear.com

