ML6697

100BASE-TX Physical Layer with MII

GENERAL DESCRIPTION

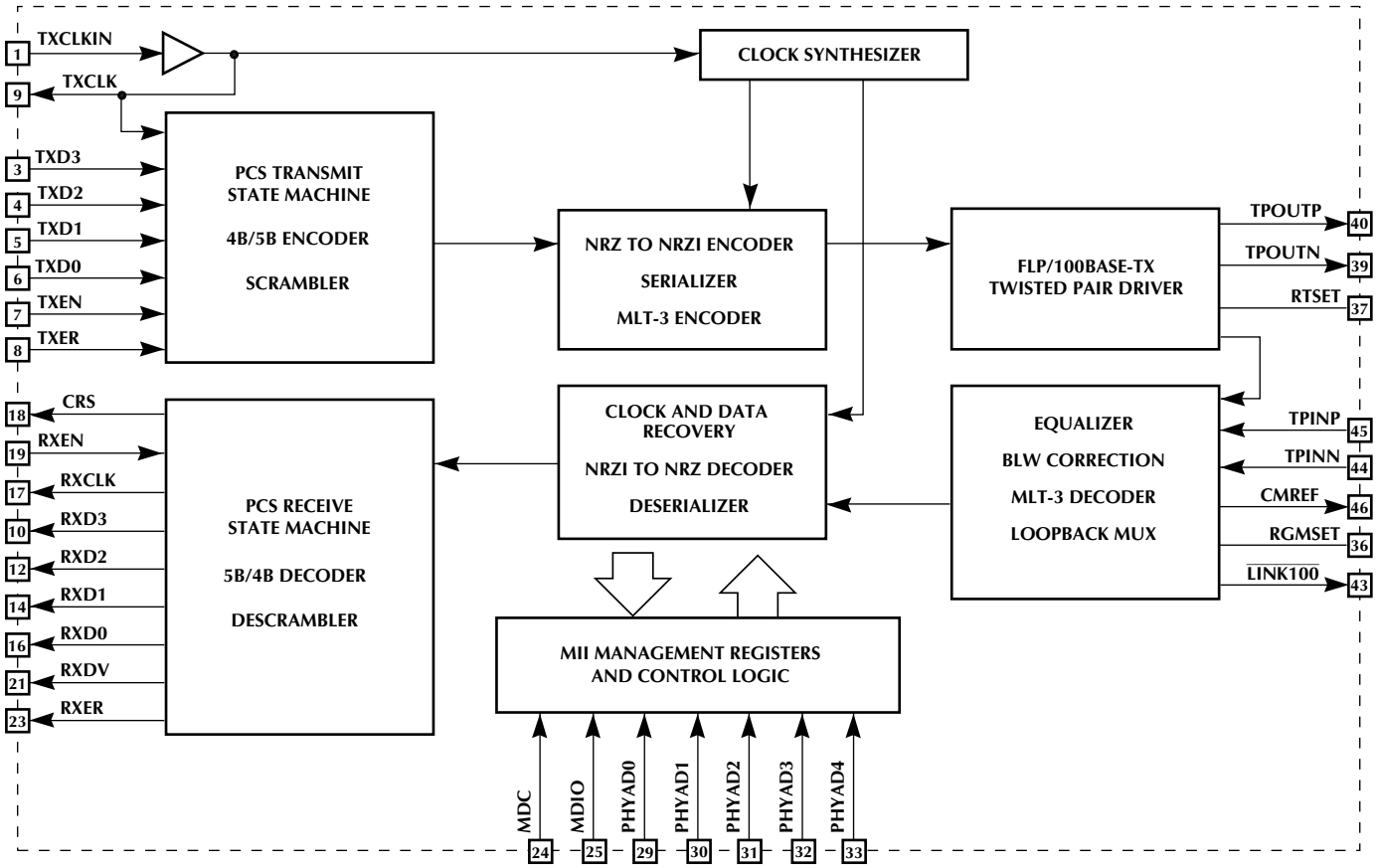
The ML6697 implements the complete physical layer of the Fast Ethernet 100BASE-TX standard. The ML6697 offers a single-chip per-port solution for MII-based repeater applications. The ML6697 interfaces to the controller through the Media Independent Interface (MII).

The ML6697 functionality includes 4B/5B encoding/decoding, Stream Cipher scrambling/descrambling, 125MHz clock recovery/generation, receive adaptive equalization, baseline wander correction, and MLT-3 transmitter.

FEATURES

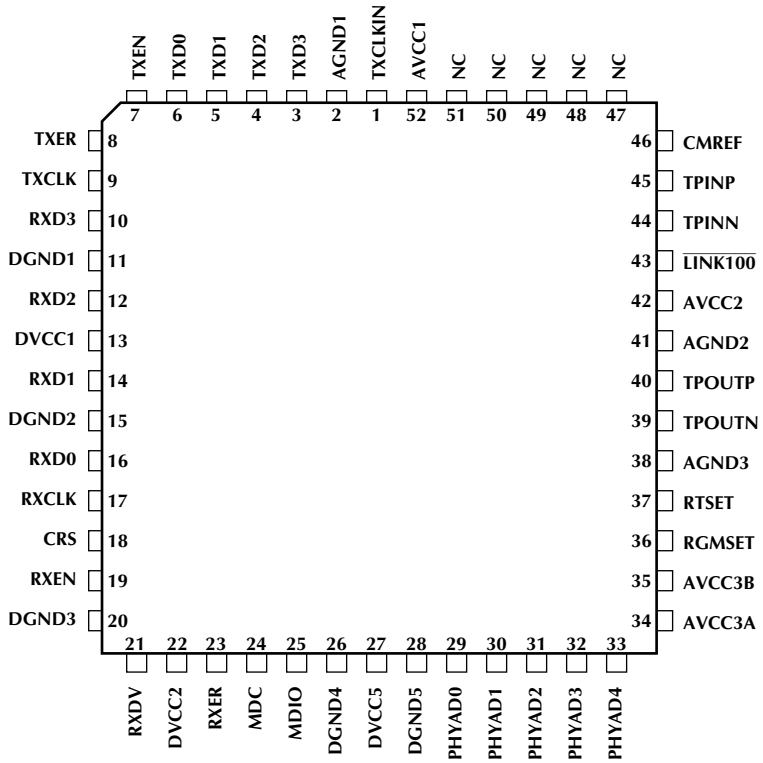
- Single-chip 100BASE-TX physical layer
- Compliant to IEEE 802.3u 100BASE-TX standard
- Supports MII-based repeater applications
- Compliant MII (Media Indendent Interface)
- 4B/5B encoder/decoder
- Stream Cipher scrambler/descrambler
- 125MHz clock recovery/generation
- Baseline wander correction
- Adaptive equalization and MLT-3 encoding/decoding

BLOCK DIAGRAM (PLCC Package)



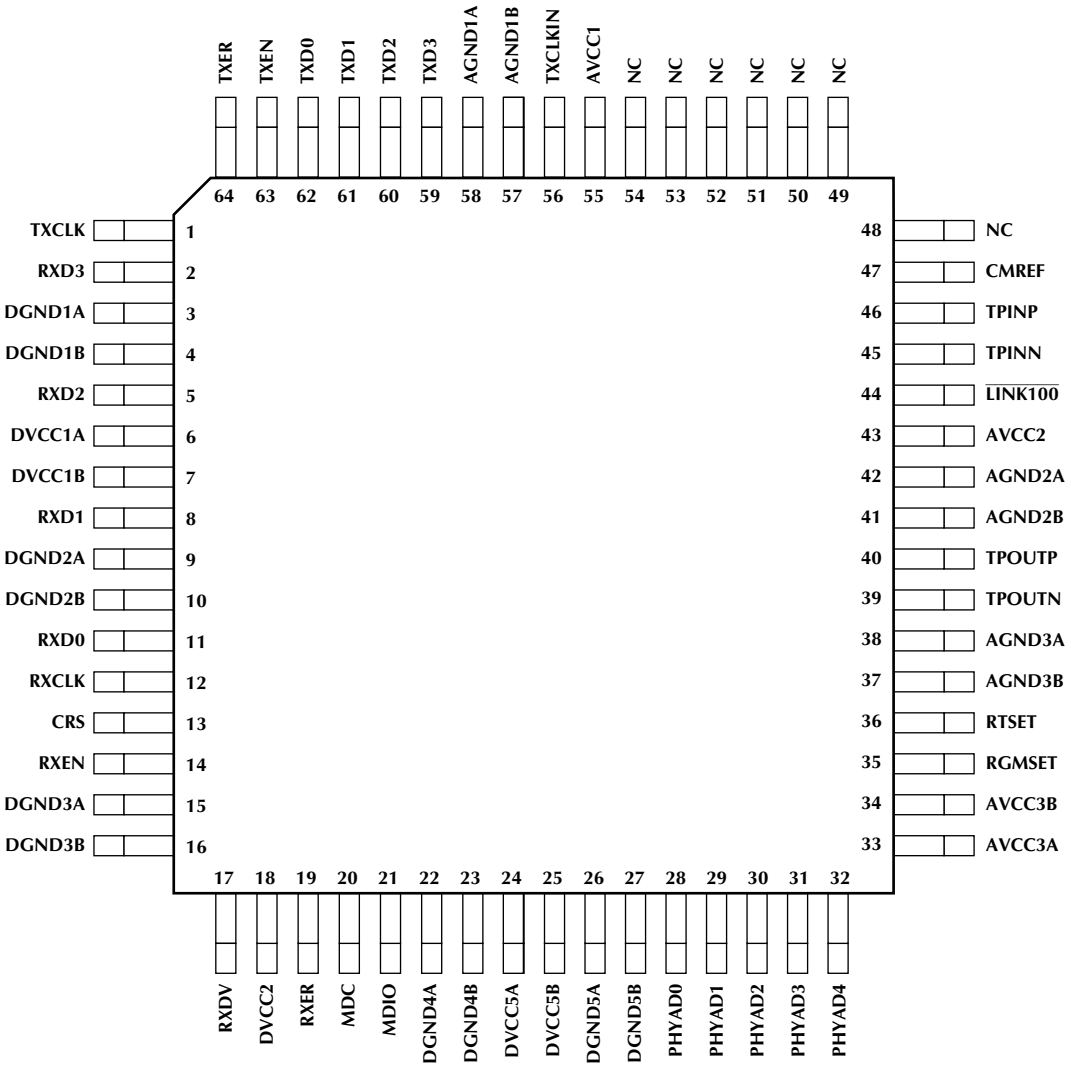
PIN CONFIGURATION

ML6697
52-Pin PLCC (Q52)



PIN CONFIGURATION (Continued)

ML6697
64-Pin TQFP (H64-10)



PIN DESCRIPTION (Pin numbers for TQFP package in parentheses)

PIN		NAME	DESCRIPTION
1	(56)	TXCLKIN	Transmit clock TTL input. This 25MHz clock is the frequency reference for the internal transmit PLL clock multiplier. This pin should be driven by an external 25MHz clock at TTL or CMOS levels.
2	(58, 57)	AGND1	Analog ground.
3, 4 5, 6	(59,60, 61,62)	TXD<3:0>	Transmit data TTL inputs. TXD<3:0> inputs accept TX data from the MII. Data appearing at TXD<3:0> are clocked into the ML6697 on the rising edge of TXCLK.
7	(63)	TXEN	Transmit enable TTL input. Driving this input high indicates to the ML6697 that transmit data are present at TXD<3:0>. TXEN edges should be synchronous with TXCLK.
8	(64)	TXER	Transmit error TTL input. Driving this pin high with TXEN also high causes the part to continuously transmit scrambled H symbols. When TXEN is low, TXER has no effect.
9	(1)	TXCLK	Transmit clock TTL output. This 25MHz clock is phase-aligned with the internal 125MHz TX bit clock. Data appearing at TXD<3:0> are clocked into the ML6697 on the rising edge of this clock.
10, 12, 14, 16	(2, 5, 8, 11)	RXD<3:0>	Receive data TTL outputs. RXD<3:0> outputs are valid on RXCLK's rising edge.
11	(3, 4)	DGND1	Digital ground.
13	(6, 7)	DVCC1	Digital +5V power supply.
15	(9, 10)	DGND2	Digital ground.
17	(12)	RXCLK	Recovered receive clock TTL output. This 25MHz clock is phase-aligned with the internal 125MHz bit clock recovered from the signal received at TPINP/N. Receive data at RXD<3:0> changes on the falling edges and should be sampled on the rising edges of this clock. RXCLK is phase aligned to TXCLKIN when the 100BASE-TX signal is not present at TPINP/N.
18	(13)	CRS	Carrier Sense TTL output. CRS goes high in the presence of non-idle signals at TPINP/N. CRS goes low when receive is idle.
19	(14)	RXEN	Receive enable TTL input. When this input is high, all the MII TTL outputs are enabled. When this input is low, all the MII TTL outputs are in high impedance mode. This input does not affect MDIO, TXCLK and CRS.
20	(15, 16)	DGND3	Digital ground.
21	(17)	RXDV	Receive data valid TTL output. This output goes high when the ML6697 is receiving a data packet. RXDV should be sampled synchronously with RXCLK's rising edge.
22	(18)	DVCC2	Digital +5V power supply.
23	(19)	RXER	Receive error TTL output. This output goes high to indicate error or invalid symbols within a packet, or corrupted idle between packets. RXER should be sampled synchronously with RXCLK's rising edge.
24	(20)	MDC	MII Management Interface clock TTL input. A clock at this pin clocks serial data into or out of the ML6697's MII management registers through the MDIO pin. The maximum clock frequency at MDC is 2.5MHz.

PIN DESCRIPTION (Continued)

PIN		NAME	DESCRIPTION
25	(21)	MDIO	MII Management Interface data TTL input/output. Serial data are written to and read from the ML6697's management registers through this I/O pin. Input data is sampled on the rising edge of MDC. Data output should be sampled synchronously with MDC's rising edge.
26	(22, 23)	DGND4	Digital ground.
27	(24, 25)	DVCC5	Digital +5V power supply.
28	(26, 27)	DGND5	Digital ground.
29	(28)	PHYAD0	MII Serial Management Interface address bit 0.
30	(29)	PHYAD1	MII Serial Management Interface address bit 1.
31	(30)	PHYAD2	MII Serial Management Interface address bit 2.
32	(31)	PHYAD3	MII Serial Management Interface address bit 3.
33	(32)	PHYAD4	MII Serial Management Interface address bit 4.
34	(33)	AVCC3A	Analog +5V power supply.
35	(34)	AVCC3B	Analog +5V power supply.
36	(35)	RGMSET	Equalizer bias resistor input. An external 9.53kΩ, 1% resistor connected between RGMSET and AGND3 sets internal time constants controlling the receive equalizer transfer function.
37	(36)	RTSET	Transmit level bias resistor input. An external 2.49kΩ, 1% resistor connected between RTSET and AGND3 sets a precision constant bias current for the twisted pair transmit level.
38	(37, 38)	AGND3	Analog ground.
39, 40	(39, 40)	TPOUTN/P	Transmit twisted pair outputs. This differential current output pair drives MLT-3 waveforms into the network coupling transformer.
41	(41, 42)	AGND2	Analog ground.
42	(43)	AVCC2	Analog +5V power supply.
43	(44)	$\overline{\text{LINK100}}$	100BASE-TX link activity open-drain output. $\overline{\text{LINK100}}$ pulls low when there is 100BASE-TX activity at TPINP/N in 100BASE-TX or auto-negotiation modes. This output is capable of driving an LED directly.
44, 45	(45, 46)	TPINN/P	Receive twisted pair inputs. This differential input pair receives 100BASE-TX signals from the network.
46	(47)	CMREF	Receiver common-mode reference output. This pin provides a common-mode bias point for the twisted-pair media line receiver, typically (V_{CC} – 1.26)V.
52	(55)	AVCC1	Analog +5V power supply.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} Supply Voltage Range ..... GND –0.3V to 6V
Input Voltage Range
  Digital Inputs ..... GND –0.3V to V_{CC} +0.3V
  TPINP, TPINN, ... GND –0.3V to V_{CC} +0.3V
Output Current
  TPOUTP, TPOUTN 60mA
  All other outputs 10mA
Junction Temperature ..... 150°C
Storage Temperature .....–65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Thermal Resistance (θ_{JA})
  PLCC ..... 40°C/W
  TQFP ..... 52°C/W

OPERATING CONDITIONS

V_{CC} Supply Voltage ..... 5V ± 5%
  All V_{CC} supply pins *must* be within 0.1V of each other.
  All GND pins *must* be within 0.1V of each other.
T_A, Ambient temperature ..... 0°C to 70°C
RGMSET ..... 9.53kΩ ± 1%
RTSET ..... 2.49kΩ ± 1%
Receive transformer insertion loss ..... <–0.5dB

DC ELECTRICAL CHARACTERISTICS

Over full range of operating conditions unless otherwise specified (Note 1).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER						
V_{ICM}	TPINP/N Input Common-Mode Voltage (CMREF)			V_{CC} – 1.26		V
V_{ID}	TPINP-TPINN Differential Input Voltage Range		–3.0		3.0	V
R_{IDR}	TPINP-TPINN Differential Input Resistance		10.0k			Ω
I_{ICM}	TPINP/N Common-Mode Input Current				+10	µA
I_{RGM}	RGMSET Input Current	RGMSET = 9.53kΩ		130		µA
I_{RT}	RTSET Input Current	RTSET = 2.49kΩ		500		µA
LED OUTPUT ($\overline{LINK100}$)						
I_{OLS}	Output Low Current				5	mA
I_{OHS}	Output Off Current				10	µA
TRANSMITTER						
I_{TD}	TPOUTP/N Differential Output Current	Note 2, 3	±19		±21	mA
I_{TOFF}	TPOUTP/N Off-State Output	R_L = 200, 1%	0		1.5	mA
I_{TXI}	TPOUTP/N Differential Output Current Imbalance	R_L = 200, 1%			500	µA
X_{ERR}	TPOUTP/N Differential Output Current Error	V_{OUT} = V_{CC}; Note 3	–5.0		+5.0	%
X_{CMP}	TPOUTP/N Current Compliance Error	V_{OUT} = V_{CC} ± 2.2V; referred to I_{OUT} at V_{CC}	–2.0		+2.0	%

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY CURRENT						
I_{CC}	Supply Current, Transmitting	Current into all V_{CC} pins		200	300	mA
TTL INPUTS (TXD<3:0>, TXCLKIN, MDC, MDIO, TXEN, TXER, RXEN)						
V_{IL}	Input Low Voltage	I_{IL} = –400µA			0.8	V
V_{IH}	Input High Voltage	I_{IH} = 100µA	2.0			V
I_{IL}	Input Low Current	V_{IN} = 0.4V	–200			µA
I_{IH}	Input High Current	V_{IN} = 2.7V			100	µA
MII TTL OUTPUTS (RXD<3:0>, RXCLK, RXDV, RXER, CRS, MDIO, TXCLK)						
V_{OLT}	Output Low Voltage	I_{OL} = 4mA			0.4	V
V_{OHT}	Output High Voltage	I_{OH} = –4mA	2.4			V
CMOS INPUTS (PHYAD<4:0>)						
V_{ILC}	Input Low Voltage				0.2 x V_{CC}	V
V_{IHC}	Input High Voltage			0.8 x V_{CC}		V

Note 1. Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

AC ELECTRICAL CHARACTERISTICS

Over full range of operating conditions unless otherwise specified (Note 1).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER (Note 3)						
$t_{TR/F}$	TPOUTP-TPOUTN Differential Rise/Fall Time	Notes 5, 6; for any legal code sequence	3.0		5.0	ns
t_{TM}	TPOUTP-TPOUTN Differential Rise/Fall Time Mismatch	Notes 5, 6; for any legal code sequence	–0.5		0.5	ns
t_{TDC}	TPOUTP-TPOUTN Differential Output Duty Cycle Distortion	Notes 4, 6	–0.5		0.5	ns
t_{TJT}	TPOUTP-TPOUTN Differential Output Peak-to-Peak Jitter	Note 6		300	1400	ps
X_{OST}	TPOUTP-TPOUTN Differential Output Voltage Overshoot	Notes 6, 7			5	%
t_{CLK}	TXCLKIN – TXCLK Delay		6	8	11	ns
t_{TXP}	Transmit Bit Delay	Note 8			10.5	bit times
RECEIVER						
t_{RXDC}	Receive Bit Delay (CRS)	Note 9			15.5	bit times
t_{RXDR}	Receive Bit Delay (RXDV)	Note 10			25.5	bit times
MII (Media-Independent Interface)						
X_{BTOL}	TX Output Clock Frequency Tolerance	25MHz frequency	–100		+100	ppm
t_{TPWH}	TXCLKIN pulse width HIGH		14			ns
t_{TPWL}	TXCLKIN pulse width LOW		14			ns
t_{RPWH}	RXCLK pulse width HIGH		14	18		ns
t_{RPWL}	RXCLK pulse width LOW		14	22		ns
t_{TPS}	Setup time, TXD<3:0> Data Valid to TXCLK Rising Edge (1.4V point)		15			ns
t_{TPH}	Hold Time, TXD<3:0> Data Valid After TXCLK Rising Edge (1.4V point)		0			ns
t_{RCS}	Time that RXD<3:0> Data are Valid Before RXCLK Rising Edge (1.4V point)		10	20		ns
t_{RCH}	Time that RXD<3:0> Data are Valid After RXCLK Rising Edge (1.4V point)		10	19		ns
t_{RPCR}	RXCLK 10% – 90% Rise Time				6	ns
t_{RPCF}	RXCLK 90%-10% Fall Time				6	ns
t_{REND}	RXEN high to RXD<3:0>, RXDV, RXER, RXCLK Driving		2		10	ns
t_{RENZ}	RXEN low to RXD<3:0>, RXDV, RXER, RXCLK High Impedence		2		10	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MDC-MDIO (MII Management Interface)						
t_{SPWS}	Write Setup Time, MDIO Data Valid to MDC Rising Edge 1.4V Point		10			ns
t_{SPWH}	Write Hold Time, MDIO Data Valid After MDC Rising Edge 1.4V Point		10			ns
t_{SPRS}	Read Setup Time, MDIO Data Valid to MDC Rising Edge 1.4V Point		100			ns
t_{SPRH}	Read Hold Time, MDIO Data Valid After MDC Rising Edge 1.4V Point		0			ns
t_{CPER}	Period of MDC		400			ns
t_{CPW}	Pulsewidth of MDC	Positive or negative pulses	160			ns

Note 1. Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

Note 2. Measured using the test circuit shown in fig. 1, under the following conditions:
R_{LP} = 200Ω, R_{LS} = 49.9Ω, R_{TSET} = 2.49kΩ.
All resistors are 1% tolerance.

Note 3. Output current amplitude is $I_{OUT} = 40 \times 1.25V/RTSET$.

Note 4. Measured relative to ideal negative and positive signal 50% points, using the four successive MLT-3 transitions for the 01010101 bit sequence.

Note 5. Time difference between 10% and 90% levels of the transition from the baseline voltage (nominally zero) to either the positive or negative peak signal voltage. The times specified here correlate to the transition times defined in the ANSI X3T9.5 TP-PMD Rev 2.0 working draft, section 9.1.6, which include the effects of the external network coupling transformer and EMI/RFI emissions filter.

Note 6. Differential test load is shown in fig. 1 (see note 2).

Note 7. Defined as the percentage excursion of the differential signal transition beyond its final adjusted value during the symbol interval following the transition. The adjusted value is obtained by doing a straight line best-fit to an output waveform containing 14 bit-times of no transition preceded by a transition from zero to either a positive or negative signal peak; the adjusted value is the point at which the straight line fit meets the rising or falling signal edge.

Note 8. From first rising edge of TXCLK after TXEN goes high, to first bit of J at the MDI.

Note 9. From first bit of J at the MDI, to CRS.

Note 10. From first bit of J at the MDI, to first rising edge of RXCLK after RXDV goes high.

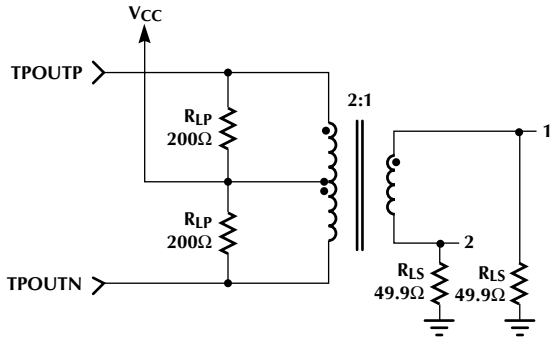


Figure 1.

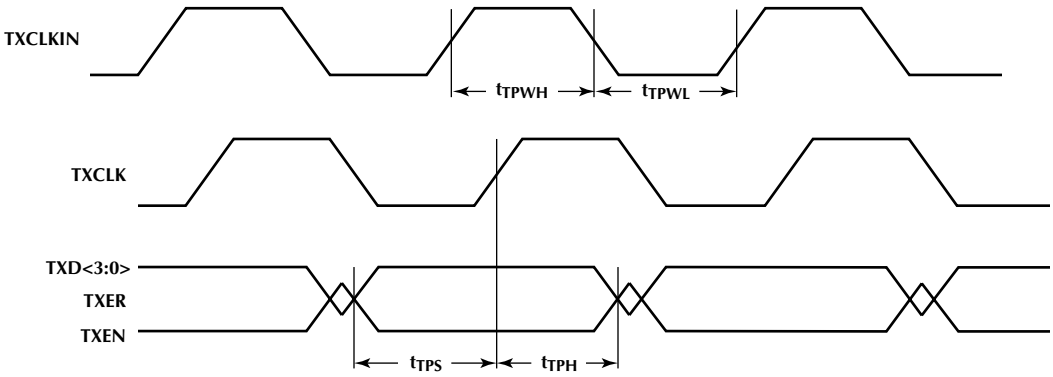


Figure 2. MII Transmit Timing

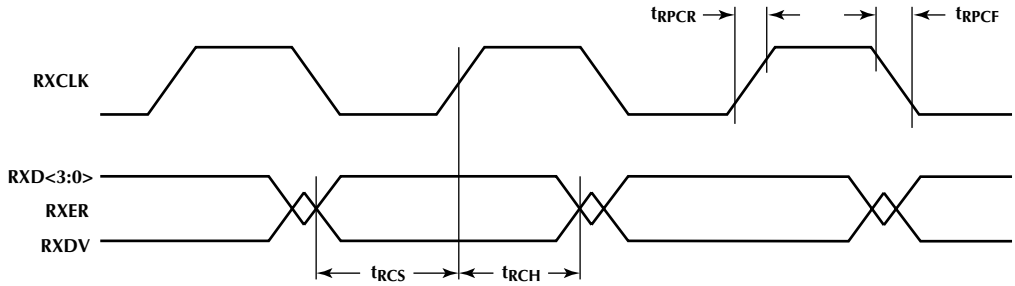


Figure 3. MII Receive Timing

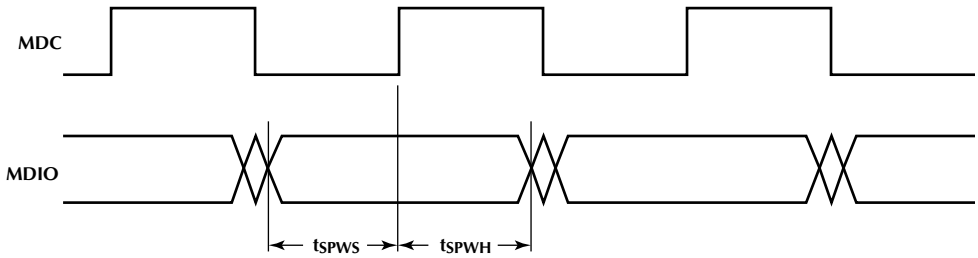


Figure 4. MII Management Interface Write Timing

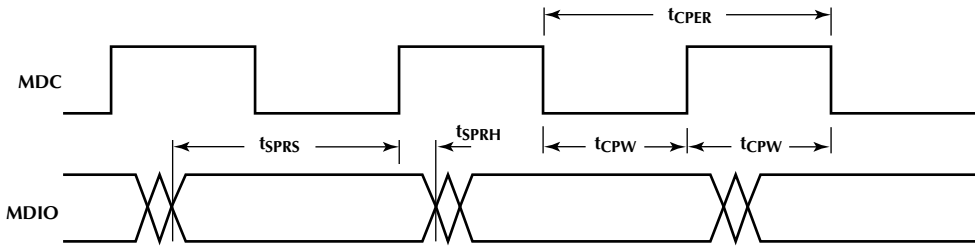


Figure 5. MII Management Interface Read Timing

FUNCTIONAL DESCRIPTION

TRANSMIT SECTION

The transmitter includes everything necessary to accept 4-bit data nibbles clocked in at 25MHz at the MII and output scrambled, 5-bit encoded MLT-3 signals into twisted pair at 100Mbps. The on-chip transmit PLL converts a 25MHz TTL-level clock at TXCLKIN to an internal 125MHz bit clock. TXCLK from the ML6697 clocks transmit data from the MAC into the ML6697's TXD<3:0> input pins upon assertion of TXEN. Data from the TXD<3:0> inputs are 5-bit encoded, scrambled, and converted from parallel to serial form at the 125MHz clock rate. The serial transmit data is converted to MLT-3 3-level code and driven differentially out of the TPOUTP and TPOUTN pins at nominal ±2V levels with the proper loads. The transmitter is designed to drive a center-tapped transformer with a 2:1 winding ratio, so a differential 400Ω load is used on the transformer primary to properly terminate the 100Ω cable and termination on the secondary. The transformer's center tap must be tied to V_{CC}. A 2:1 transformer allows using a ±20mA output current. Using a 1:1 transformer would have required twice the output current and increased the on-chip power dissipation. An external 2.49kΩ, 1% resistor at the RTSET pin creates the correct output levels at TPOUTP/N.

Driving TXER high when TXEN is high causes the H symbol (00100) to appear in scrambled MLT-3 form at TPOUTP/N. The media access controller asserts TXER synchronously with TXCLK rising edge, and the H symbol appears at least once in place of a valid symbol in the current packet.

With no data at TXD<3:0> scrambled idle appears at TPOUTP/N.

RECEIVE SECTION

The receiver includes all necessary functions for converting 3-level MLT-3 signals from the twisted-pair media to 4-bit data nibbles at RXD<3:0> with extracted clock at RXCLK. The adaptive equalizer compensates for cable distortion and attenuation, corrects for DC baseline wander, and converts the MLT-3 signal to 2-level NRZ. The receive PLL extracts clock from the equalized signal, providing additional jitter attenuation, and clocks the signal through the serial to parallel converter. The resulting 5-bit nibbles are descrambled, aligned and decoded, and appear at RXD<3:0>. The ML6692 asserts RXDV when it's ready to present properly decoded receive data at RXD<3:0>. The extracted clock appears at RXCLK. Resistor RGMSET sets internal time constants controlling the adaptive equalizer's transfer function. RGMSET must be set to 9.53kΩ (1%).

The receiver will assert RXER high if it detects code errors in the receive data packet, or if the idle symbols between packets are corrupted.

CRS goes high whenever there is non-idle receive activity in the network.

ML6697 PHY MANAGEMENT FUNCTIONS

The ML6697 has management functions controlled by the register locations given in Tables 1 and 2. There are two 16-bit MII Management registers, with several unused locations. Register 0 (Table 1) is the basic control register (read/write). Register 1 (Table 2) is the basic status register (read-only). The ML6697 powers on with all management register bits set to their default values.

See IEEE 802.3u section 22.2.4 for a discussion of MII management functions and status/control register definitions.

MII MANAGEMENT INTERFACE REGISTERS

TABLE 1: CONTROL REGISTER

BIT(s)	NAME	DESCRIPTION	R/W	DEFAULT
0.15	Reset	1 = reset all register bits to defaults 0 = normal operation	R/W, SC	0
0.14	Loopback	1 = PMD loopback mode 0 = normal operation	R/W	0
0.13	Manual Speed Select	1 = 100Mb/s 0 = 10Mb/s	RO	1
0.11	Power down	1 = power down 0 = normal operation	R/W	0
0.12, 0.10-0.0	Not Used		RO	0

TABLE 2: STATUS REGISTER

BIT(s)	NAME	DESCRIPTION	R/W	DEFAULT
1.14	100BASE-TX full duplex	1 = full duplex 100BASE-TX capability 0 = No full duplex 100BASE-TX capability	RO	0
1.13	100BASE-TX half duplex	1 = half duplex 100BASE-TX capability 0 = no half duplex 100BASE-TX capability	RO	1
1.2	Link status	1 = 100BASE-TX line is up 0 = 100BASE-TX link is down	RO/LL	latch low after link fail until read
1.0	Extended capability	1 = extended register capabilities 0 = basic register set only	RO	0
1.15, 1.12-1.3, 1.1	Not used		RO	0

NOTE: All unnamed or unused register locations will return a 0 value when accessed.
KEY: LL = latch low until read, R/W = read/write, RO = read only, SC = self-clearing.

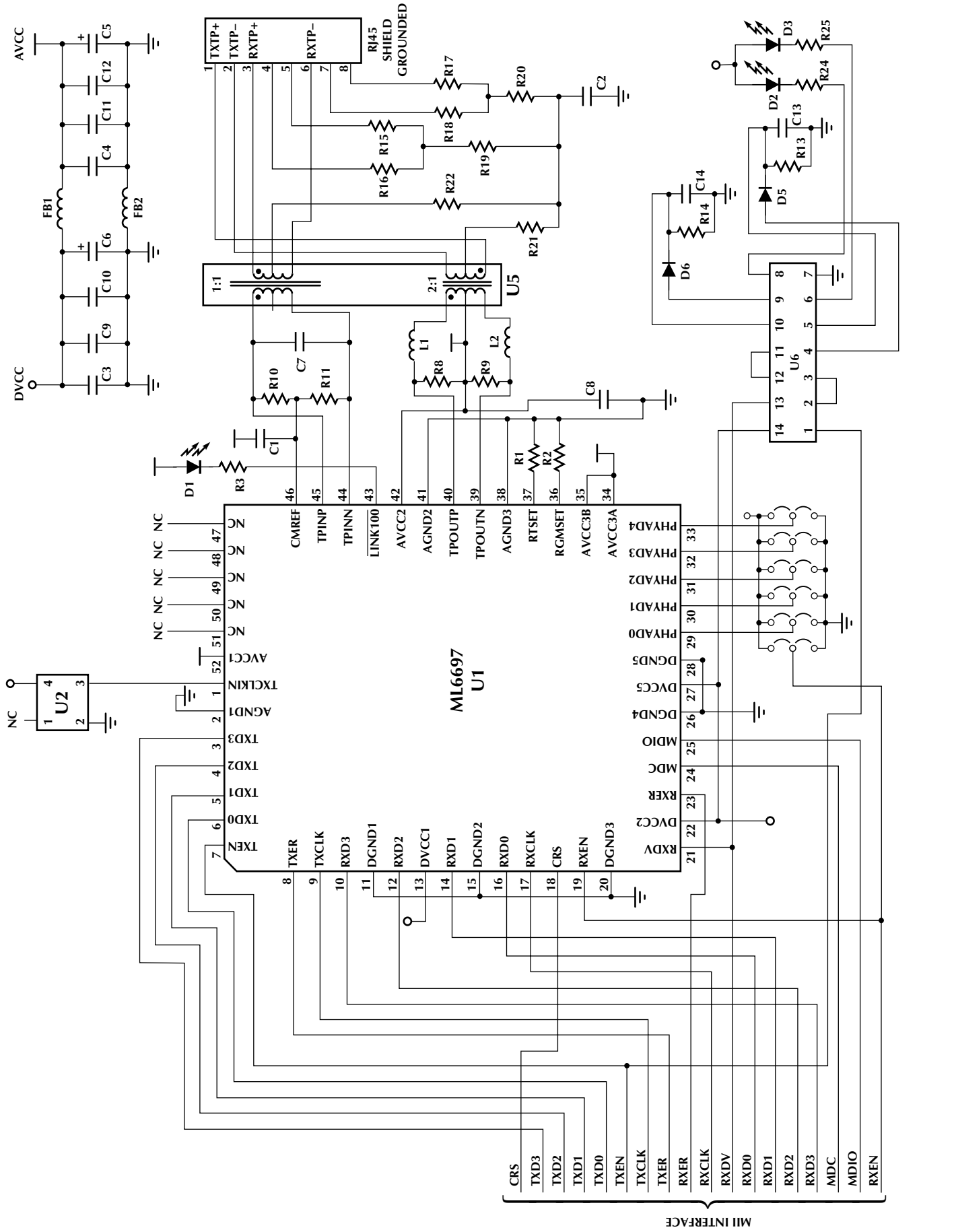


Figure 6. Applications Circuit

ML6697 SCHEMATIC

Figure 6 shows a general ML6697 design.

The inductors L1 and L2 are for the purpose of improving return loss. Capacitor C7 is recommended. It decouples some noise at the inputs of the ML6697, and improves the Bit Error Rate (BER) performance of the board. We recommend having a 0.1µF Cap on every V_{CC} pin as indicated by C3, 4, 9-12. Also, we recommend splitting the V_{CC}, AV_{CC}, AGND and DGND. It is recommended that AGND and DGND planes are large enough for low inductance. If splitting the two grounds and keeping the ground planes large enough is not possible due to board space, you could join them into one larger ground plane.

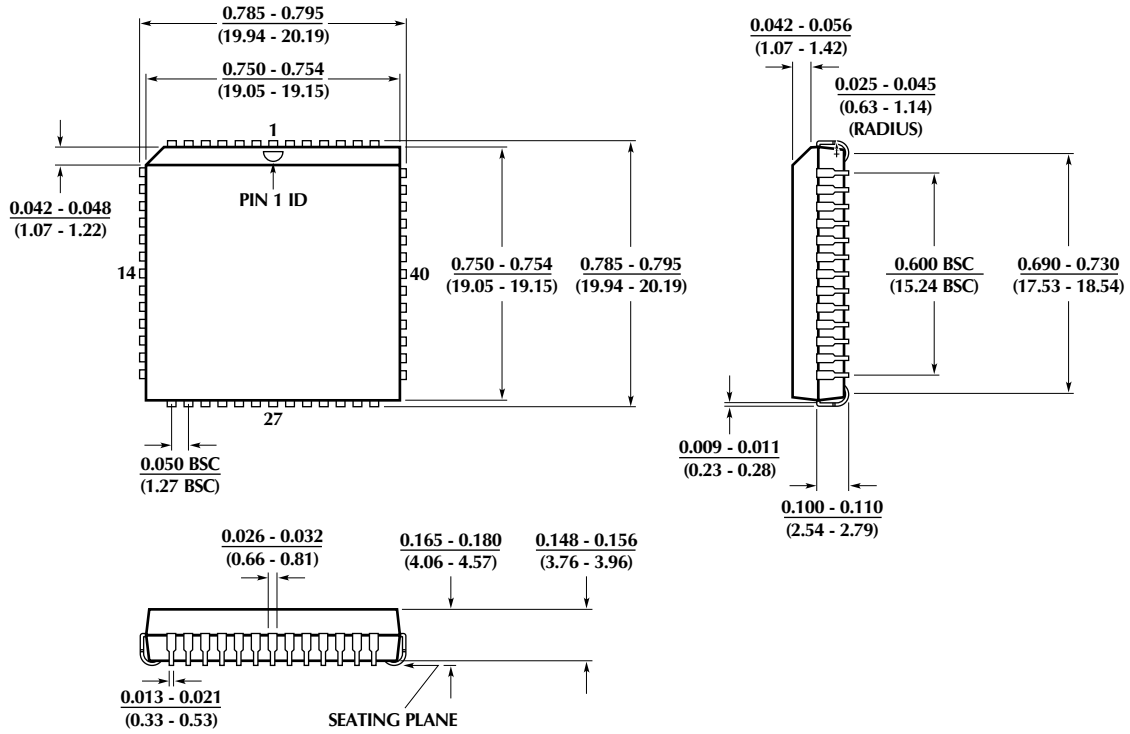
ML6697 PARTS LIST

COMPONENT	DESCRIPTION
U1	ML6697 52-Pin PLCC surface mount
U2	Can Crystal Oscillator, 25MHz 4-pin surface mount
U5	Transformer Module
U6	HEX Inverter 74HC04
FB1, FB2	Fair-Rite SM Bead P/N 2775019447
L1, L2	130nH inductors rated at 50MHz
R1	2.49kΩ 1% 1/8W surface mount
R2	9.53kΩ 1% 1/8W surface mount
R3, R24, R25	750Ω 5% 1/8W surface mount
R8, R9	200Ω 1% 1/8W surface mount

COMPONENT	DESCRIPTION
R10, R11	50Ω 1% 1/8W surface mount
R13, R14	100kΩ 10% 1/8W surface mount
R15–R20	49.9Ω 5% 1/8W surface mount
R21, R22	75Ω 5% 1/8W surface mount
C1,C3, C4, C8-12	0.1µF Ceramic Chip Cap
C5, C6	10µF Tantalum Cap.
C7	10pF Cap
C2	Board layer Cap (2V rated)
C13, C14	22nF Cap
D1-D3	LED Diodes
D5-D6	Diodes Phillips PMLL 4148

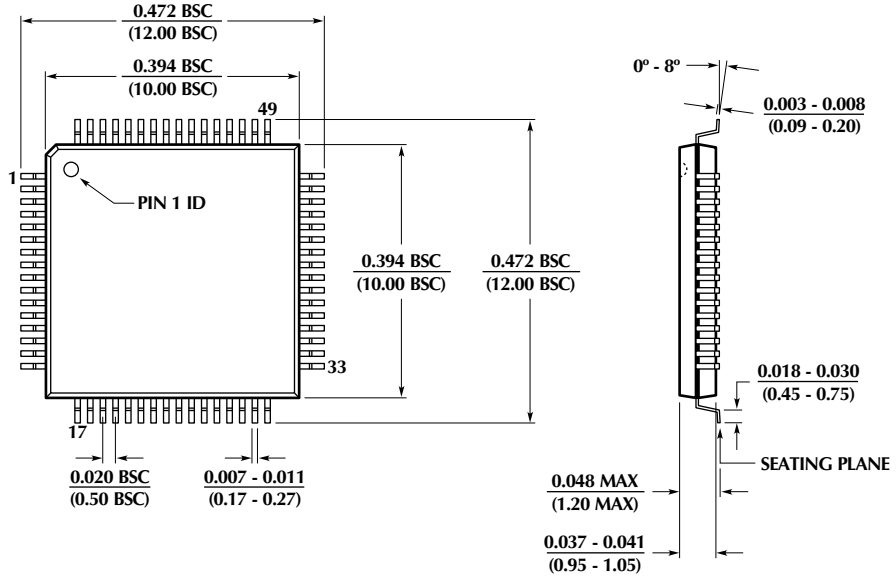
PHYSICAL DIMENSIONS inches (millimeters)

Package: Q52
52-Pin PLCC



PHYSICAL DIMENSIONS inches (millimeters)

Package: H64-10
64-Pin (10 x 10 x 1mm) TQFP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6697CQ	0°C to 70°C	52-Pin PLCC (Q52)
ML6697CH	0°C to 70°C	64-Pin TQFP (H64-10)

2092 Concourse Drive
San Jose, CA 95131
Tel: 408/433-5200
Fax: 408/432-0295