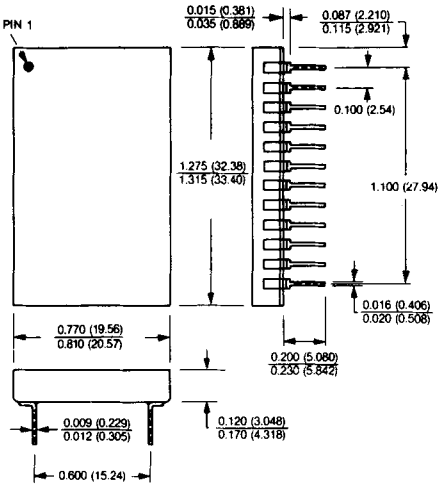
# High-speed 8-bit A/D Converters with 3-state Outputs

## FEATURES

- Fast 2.5μsec Conversion Time
- 3-State Output Buffer
- ±1/2LSB Linearity and No Missing Codes Over Temperature
- Adjustment-Free No Gain or Offset Adjustments Necessary
- Fully Specified 0°C to +70°C (MN5150) or −55°C to +125°C (MN5150H and MN5150H/B)

### 24 PIN DIP




Dimensions in Inches (millimeters)

## DESCRIPTION

MN5150 is a high-speed, 8-bit, successive approximation analog-to-digital converter with a three-state output buffer for easy interfacing to microprocessor and microcomputer data buses. Other performance features include a 2.5μsec maximum conversion time, ±½LSB linearity and "no missing codes" guaranteed over the entire operating temperature range, and ±1LSB unadjusted absolute accuracy. Convenience features include hermetic dual-in-line packaging, 7 user-selectable input ranges, and thanks to the stability of our own laser-trimmed thin-film resistor networks, the absence of external gain and offset adjusting potentiometers.

Units are available for either 0°C to +70°C or −55°C to +125°C operation with performance fully specified and guaranteed over the entire operating temperature range. Environmentally Stress Screened models (H/B) are available for high-reliability applications in military/aerospace systems.

Units are available for either 0°C to +70°C or −55°C to +125°C operation with performance fully specified and guaranteed over the entire operating temperature range. High-reliability processing, screening and qualification according to MIL-PRF-38534, are available for military/aerospace applications.

MN5150's 3-state output buffer simplifies interfacing to microprocessor and microcomputer data buses. In memory-mapped applications, MN5150 looks like a RAM location with a 2.5μsec access time. It should be considered for high-speed industrial monitoring and automatic test equipment.

| Part Number | Temperature Range for Guaranteed No Missing Codes | |
|---|---|---|
| MN5150 | 8 Bits | 0°C to +70°C |
| MN5150H | 8 Bits | −55°C to +125°C |
| MN5150H/B | 8 Bits | −55°C to +125°C |

# MN5150 HIGH-SPEED 8-Bit A/D with 3-STATE BUFFER

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Operating Temperature Range | −55°C to +125°C |
| Specified Temperature Range: | |
| MN5150 | 0°C to +70°C |
| MN5150H, MN5150H/B | −55°C to +125°C |
| Storage Temperature | −65°C to +150°C |
| +15V Supply (+Vcc, Pin 16) | −0.5 to +18 Volts |
| −15V Supply (−Vcc, Pin 13) | +0.5 to −18 Volts |
| +5V Supply (+Vdd, Pin 6) | −0.5 to +7 Volts |
| Analog Input (Pins 11, 12) | ±20 Volts |
| Digital Inputs (Pins 15, 23, 24) | −0.5 to +5.5 Volts |

## ORDERING INFORMATION

PART NUMBER — MN5150H/B

Standard part is specified for 0°C to +70°C operation.
Add "H" for specified −55°C to +125°C operation.
Add "/B" to "H" models for Environmental Stress Screening.

## SPECIFICATIONS ($T_A$ = +25°C, $\pm V_{cc}$ = ±15V, $+V_{dd}$ = +5V unless otherwise indicated) (Note 1)

| ANALOG INPUTS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|
| Input Voltage Ranges: Unipolar Negative | | 0 to −5, 0 to −10 | | Volts |
| Unipolar Positive | | 0 to +5, 0 to +10 | | Volts |
| Bipolar | | ±2.5, ±5, ±10 | | Volts |
| Input Impedance (Note 2): 0 to −5V, 0 to +5V, ±2.5V | | 2.5 | | kΩ |
| 0 to −10V, 0 to +10V, ±5V | | 5 | | kΩ |
| ±10V | | 10 | | kΩ |
| **DIGITAL INPUTS (Start, Clock, $\overline{OE}$)** | | | | |
| Logic Levels: Start, Clock: Logic "1" | +2.0 | | | Volts |
| Logic "0" | | | +0.8 | Volts |
| $\overline{OE}$: Logic "1" | +3.5 | | | Volts |
| Logic "0" | | | +1.5 | Volts |
| Logic Currents: Start: Logic "1" ($V_{IH}$ = +2.4V) | | | +80 | μA |
| Logic "0" ($V_{IL}$ = +0.4V) | | | −1.6 | mA |
| Clock: Logic "1" ($V_{IH}$ = +2.4V) | | | +40 | μA |
| Logic "0" ($V_{IL}$ = +0.4V) | | | −1.6 | mA |
| $\overline{OE}$: Logic "1" ($V_{IH}$ = +5.0V) | | | ±10 | μA |
| Logic "0" ($V_{IL}$ = 0.0V) | | | ±10 | μA |
| **TRANSFER CHARACTERISTICS** | | | | |
| Resolution | | 8 | | Bits |
| Linearity Error: Initial (+25°C) | | ±¼ | ±½ | LSB |
| Over Temperature | | ±¼ | ±½ | LSB |
| Temperature Range for Guaranteed No Missing Codes: | | | | |
| MN5150 | 0 | | +70 | °C |
| MN5150H, MN5150H/B | −55 | | +125 | °C |
| Full Scale Absolute Accuracy Error (Notes 4, 6): | | | | |
| Initial (+25°C) | | ±½ | ±1 | LSB |
| Over Temperature (Note 5) | | ±1 | ±2 | LSB |
| Unipolar Offset Error (Notes 4, 7): Initial (+25°C) | | ±¼ | ±½ | LSB |
| Over Temperature (Note 5) | | ±½ | ±1 | LSB |
| Bipolar Zero Error (Notes 4, 8): Initial (+25°C) | | ±¼ | ±½ | LSB |
| Over Temperature (Note 5) | | ±½ | ±1 | LSB |
| **DIGITAL OUTPUTS (Parallel, Serial, Status)** | | | | |
| Output Coding (Note 9): Unipolar Ranges | | SB | | |
| Bipolar Ranges | | OB | | |
| Logic Levels: | | | | |
| Parallel Outputs: Logic "1" ($I_{source} \leq 1.6mA$) | +2.4 | | | Volts |
| Logic "0" ($I_{sink} \leq 1.6mA$) | | | +0.4 | Volts |
| Status, Serial Outputs: Logic "1" ($I_{source} \leq 400\mu A$) | +2.4 | | | Volts |
| Logic "0" ($I_{sink} \leq 8mA$) | | | +0.4 | Volts |
| Leakage (Parallel Outputs) in High-Z State (Note 2) | | ±20 | | μA |
| **REFERENCE OUTPUT** | | | | |
| Internal Reference (Note 2): Voltage | | +6.3 | | Volts |
| Accuracy | | ±10 | | % |
| Tempco | | ±10 | | ppm/°C |
| External Current | | | 200 | μA |

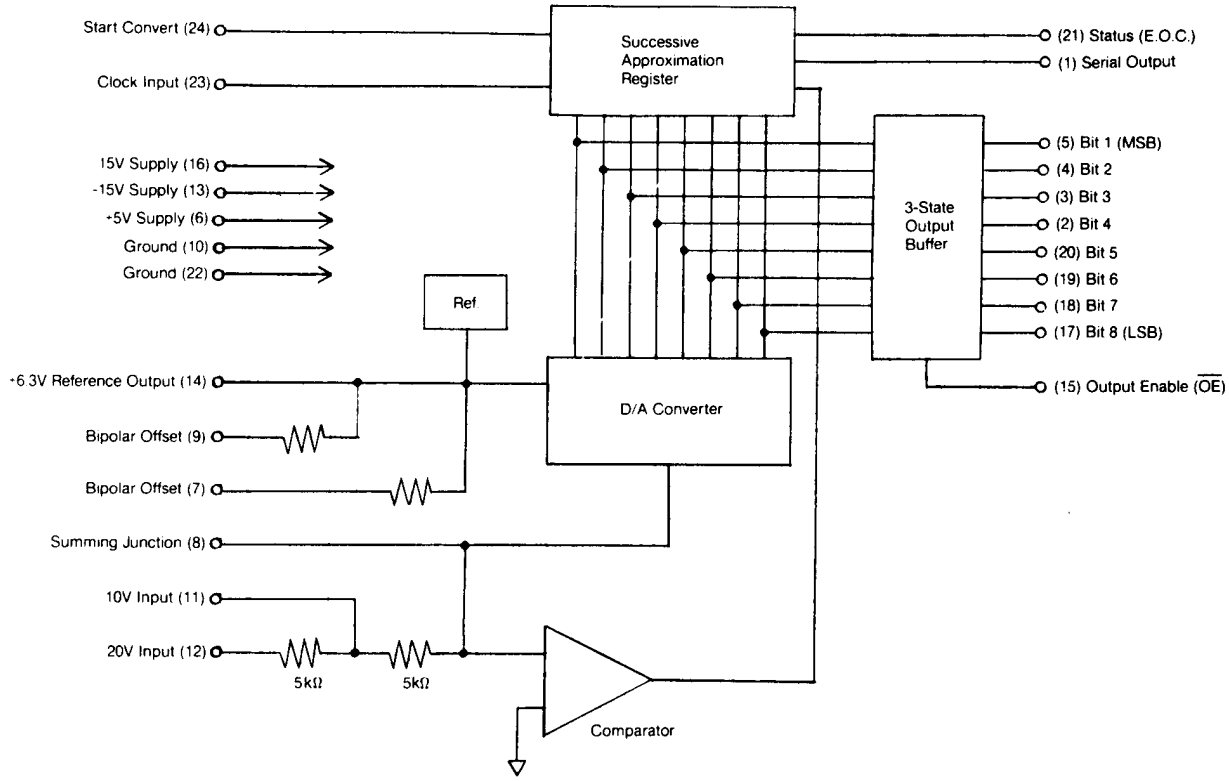
| DYNAMIC CHARACTERISTICS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|
| Conversion Time (Note 10) | | | 2.5 | μsec |
| External Clock Frequency | | | 3.2 | MHz |
| Clock Pulse Width (Note 2): High | 25 | | | nsec |
| Low | 50 | | | nsec |
| Setup Time Start Low to Clock (Note 2) | 20 | | | nsec |
| **POWER SUPPLIES** | | | | |
| Power Supply Range: +15V Supply | +14.55 | +15 | +15.45 | Volts |
| −15V Supply | −14.55 | −15 | −15.45 | Volts |
| +5V Supply | +4.75 | +5 | +5.25 | Volts |
| Power Supply Rejection (Notes 2,3,11): +15V Supply | | ±0.03 | | %FSR/%Supply |
| −15V Supply | | ±0.01 | - | %FSR/%Supply |
| Current Drain: +15V Supply | | +12 | +16 | mA |
| −15V Supply | | −10 | −18 | mA |
| +5V Supply | | +70 | +101 | mA |
| Power Consumption | | 680 | 1015 | mW |

**SPECIFICATION NOTES:**

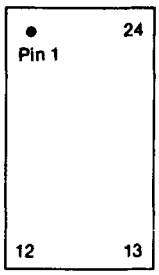
1. Listed specifications apply for all part numbers unless specifically indicated.
2. These parameters are listed for reference and are not tested.
3. FSR = full scale range, and it is equal to the nominal peak-to-peak voltage of the selected input voltage range. A unit connected for ±10V operation has a 20V FSR. A unit connected for 0 to +10V, 0 to −10V or ±5V operation has a 10V FSR. A unit connected for 0 to +5V, 0 to −5V or ±2.5V operation has a 5V FSR.
4. 1LSB for 8 bits in 20V FSR is 78mV.
   1LSB for 8 bits jn 10V FSR is 39mV.
   1LSB for 8 bits in 5V FSR is 19.5mV.
5. Listed specifications apply over the 0°C to +70°C temperature range for standard products and over the −55°C to +125°C range for "H" products.
6. Full scale absolute accuracy error includes offset, gain, linearity, noise and all other errors. Full scale accuracy specifications apply at positive full scale for unipolar positive input ranges, at negative full scale for unipolar negative input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 to 1111 1110 for unipolar positive and bipolar input ranges. Additionally it describes the accuracy of the 0000 0000 to 0000 0001 transition for unipolar negative and bipolar input ranges. The former transition ideally occurs at an input voltage 1 LSB below the nominal positive full scale voltage. The latter ideally occurs 1 LSB above the nominal negative full scale voltage. See Digital Output Coding.
7. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 to 0000 0001 when operating MN5150 on a unipolar postive range. The ideal value at which this transition should occur is +1 LSB. When operating MN5150 on a unipolar negative range, unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1110 to 1111 1111. The ideal value at which this transition should occur is −1 LSB. See Digital Output Coding.
8. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 to 1000 0000 when operating the MN5150 on a bipolar range. The ideal value at which this transition should occur is 0 Volts. See Digital Output Coding.
9. SB = straight binary. OB = offset binary.
10. Conversion time is defined as the width of Status (E.O.C.).
11. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1110 to 1111 1111 or 0000 0000 to 0000 0001 output transitions occur versus a change in power-supply voltage.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

## BLOCK DIAGRAM



## PIN DESIGNATIONS




| | | | |
|---|---|---|---|
| 1 | Serial Output | 24 | Start Convert |
| 2 | Bit 4 | 23 | Clock Input |
| 3 | Bit 3 | 22 | Ground |
| 4 | Bit 2 | 21 | Status (E.O.C.) |
| 5 | Bit 1 (MSB) | 20 | Bit 5 |
| 6 | +5V Supply (+Vdd) | 19 | Bit 6 |
| 7 | Bipolar Offset | 18 | Bit 7 |
| 8 | Summing Junction | 17 | Bit 8 (LSB) |
| 9 | Bipolar Offset | 16 | +15V Supply (+ Vcc) |
| 10 | Ground | 15 | Output Enable ($\overline{OE}$) |
| 11 | 10V Input | 14 | Reference Output (+6.3V) |
| 12 | 20V Input | 13 | −15V Supply (− Vcc) |

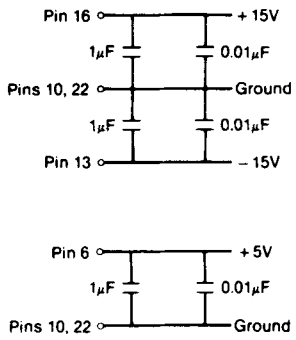
## APPLICATIONS INFORMATION

**DESCRIPTION OF OPERATION**—The Successive Approximation Register (SAR) is a set of flip flops (and control logic) whose outputs act as both the direct (parallel) data outputs of the Analog to Digital Converter (A/D) and the digital drive for the A/D's internal Digital to Analog converter (D/A). See Block Diagram. Holding the A/D's Start Convert (pin 24) low during a clock low to high transition resets the SAR. In this state, the output of the MSB flip flop is set to logic "0", the outputs of the other bit flip flops are set to logic "1", and the Status output (pin 21) is set to logic "1" (See Timing Diagram). The Start Convert must now be brought high again for the conversion to continue. If the Start is not brought high, the converter will remain in the reset state.

The D/A internal to the A/D continuously converts the A/D's digital output back to an analog signal which the comparator continuously compares to the analog input signal. The comparator output ("1" or "0") informs the SAR whether the present digital output (0111 1111 in the reset state) is "greater than" or "less than" the analog input. Depending upon which is greater, on the first rising clock edge after the Start has returned high, the SAR will set the MSB to its final state ("1" or "0") and bring bit 2 down to a "0". The digital output is now X011 1111. The D/A converts this to an analog value, and the comparator determines whether this value is greater or less than the analog input. On the next rising clock edge, the SAR reads the comparator feedback, sets bit 2 to its final value, and brings bit 3 down to a logic "0". The digital output is now XX01 1111. This successive approximation procedure continues until all the output bits are set. The rising clock edge that sets the LSB (bit 8) also drops the Status output to a "0" signaling that the conversion is complete. Output data is now valid and will remain so until another conversion is started. The clock does not have to be turned off. At this point, output data may be read by bringing Output Enable ($\overline{OE}$, pin 15) low. Output data will be valid 120nsec. maximum after Output Enable is low. Output data bits are returned to the high-impedance state by bringing Output Enable high.

**LAYOUT CONSIDERATIONS**—Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN5150. The unit's two ground pins (pins 10 and 22) are not connected internally. They should be tied together as close to the package as possible and connected to system analog ground, preferably through a large ground plane underneath the package. If the grounds cannot be tied together and must be run separately, a non-polarized 0.01μF bypass capacitor should be connected between pins 10 and 22 as close to the unit as possible and wide conductor runs employed.

Power supplies should be decoupled with tantalum or electrolytic type capacitors located close to the converter. For optimum performance and noise rejection, 1μF capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.

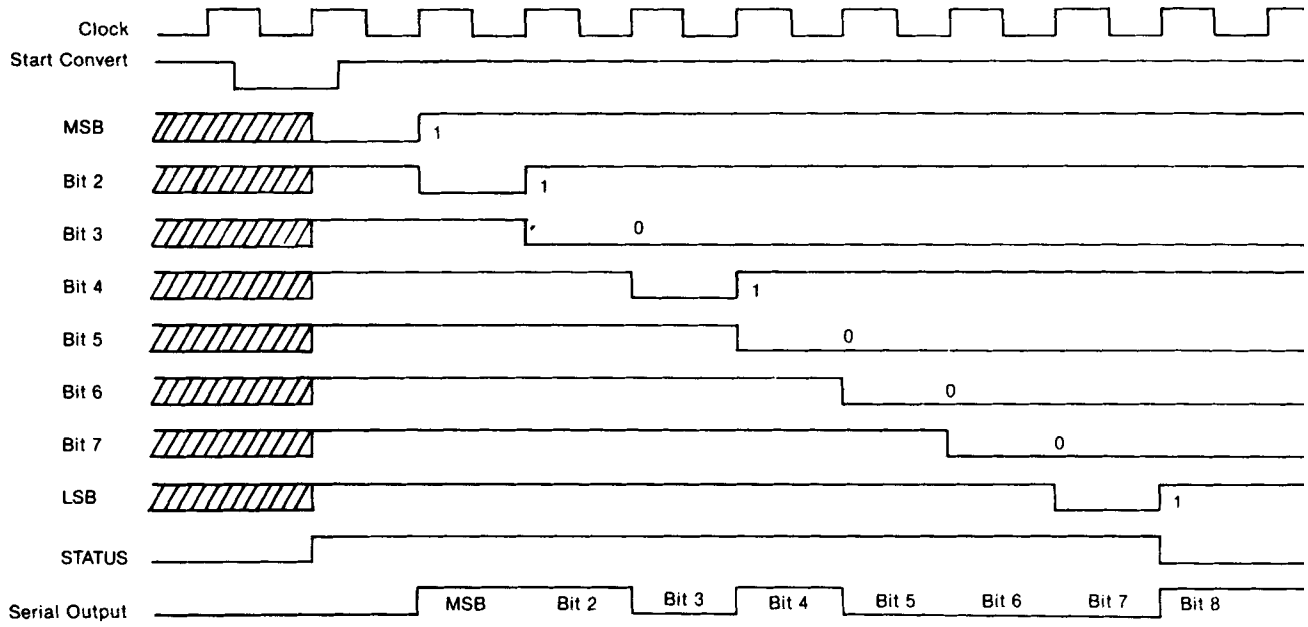



**POWER SUPPLY DECOUPLING**

**CONTINUOUS CONVERTING**—MN5150 A/D converter can be made to continuously convert by tying the Status output (pin 21) to the Start Convert input (pin 24). In this configuration, Status (Start Convert) will go low at the end of a conversion (see Timing Diagram) and the next rising clock edge will reset the converter bringing Status (Start Convert) high again. The MSB will be set on the next rising clock edge. The result is that the Status will go low for approximately one clock period following each conversion. Please read the section describing the Status output.

**STATUS OUTPUT**—Status or End of Conversion (E.O.C., pin 21) output will be set to a logic "1" when the converter is reset; will remain high during conversion; and will drop to a logic "0" when conversion is complete. Due to propagation delays, the least significant bit (LSB) of a given conversion may not be valid until a maximum of 100nsec after Status has returned low. Therefore, an adequate delay must be provided if Status is to be used to strobe latches to hold output data. Simple gate delays can be employed or the Status can be connected to the input of a D flip flop whose clock input is the same as the converter clock. In this situation, the Q output will change one clock period after Status changes.

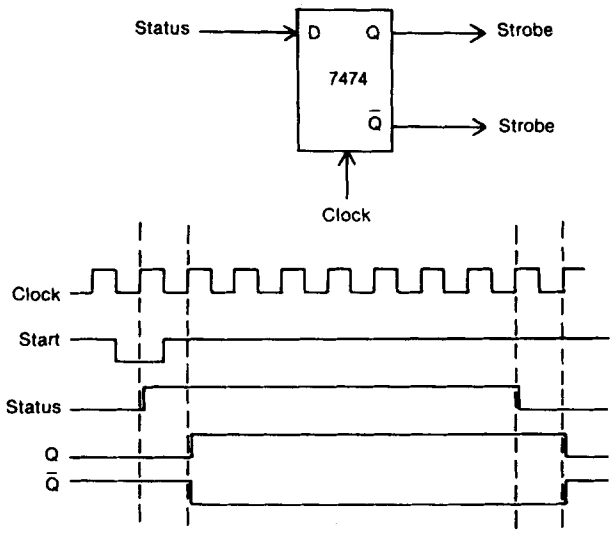
## TIMING DIAGRAM




**TIMING DIAGRAM NOTES:**

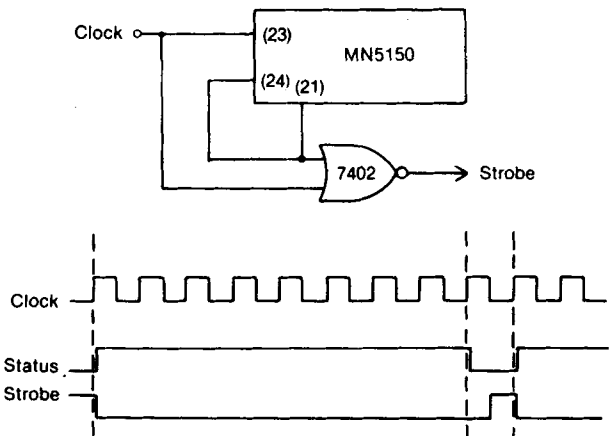
1. Operation shown is for the digital word 1101 0001 which corresponds to 8.164V on the 0 to +10V input range. See Output Coding.
2. Conversion Time is defined as the width of the Status (E.O.C.) pulse.
3. The converter is reset (MSB = "0", all other bits = "1", Status = "1") by holding the Start Convert low during a low to high clock transition. The Start Convert must be low for a minimum of 20nsec prior to the clock transition. Holding the Start low will hold the converter in the reset state. Actual conversion will begin on the next rising clock edge after the Start has returned high.
4. The delay between the resetting clock edge and Status actually rising to a "1" is 50nsec maximum.
5. The Start Convert may be brought low at any time during a conversion to reset and begin converting again.
6. Both serial and parallel data bits become valid on the same rising cloc edges. Serial data is valid on subsequent falling clock edges, and thes edges can be used to clock serial data into receiving registers.
7. Output data will be valid 100nsec (maximum) after the Status (E.O.C.) outpu has returned low. Parallel output data will remain valid and the Status outpu low until another conversion is initiated.
8. Parallel output data can be enabled by bringing Output Enable ($\overline{OE}$, pin 1 low. Parallel output bits can be returned to the high-impedance state by se ting output enable high.
9. For continuous conversion, connect the Status output (pin 21) to the Sta Convert Input (pin 24). See section on Continuous Converting.
10. When the converter is initially "powered up", it may come on at any poir in the conversion cycle.

## LATCHING OUTPUT DATA

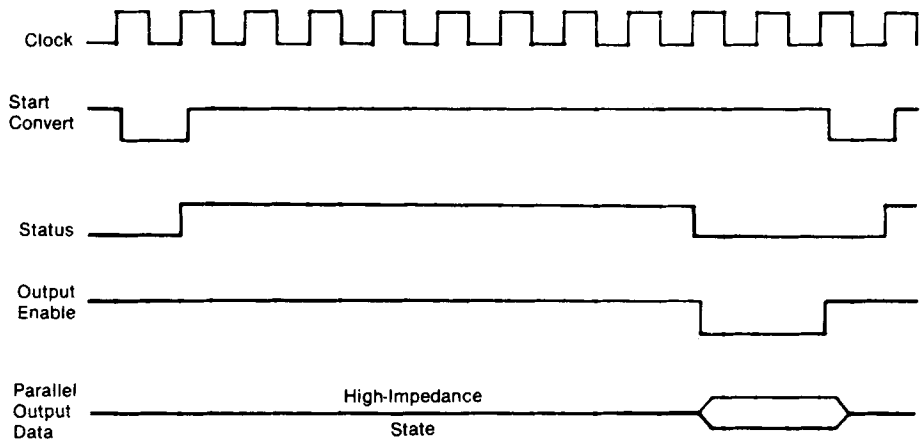



If continuously converting, the Status (E.O.C.) output can b NORed with the converter clock, as shown below, to prc duce a postive strobe pulse ½ period wide, ½ period afte the Status output has gone low. The rising edge of this puls can be used to latch data after each conversion.

## LATCHING DATA CONTINUOUS CONVERSIONS



**OUTPUT ENABLE**—Output Enable ($\overline{OE}$, pin 15) controls the state of the parallel outputs. When a conversion is complete, valid parallel output data may be enabled by bringing Output Enable low. Data will be available 120nsec maximum after Output Enable is low. Output data is returned to the high-impedance state by bringing Output Enable high. See diagram below.




## INPUT RANGE SELECTION

| Pin Connections | Analog Input Voltage Range | | | | | | |
|---|---|---|---|---|---|---|---|
| | 0 to +5V | 0 to +10V | ±2.5V | ±5V | ±10V | 0 to −5V | 0 to −10V |
| Connect Input to Pin | 11 | 11 | 11 | 11 | 12 | 11 | 11 |
| Connect Pin 7 to Pin | Ground | Ground | Ground | Ground | Ground | 8,9,12 | 9 |
| Connect Pin 8 to Pin | 12 | Open | 9,12 | 9 | 9 | 7,9,12 | 7,9 |
| Connect Pin 9 to Pin | Ground | Ground | 8,12 | 8 | 8 | 7,8,12 | 7,8 |
| Input Impedance (kΩ) | 2.5 | 5 | 2.5 | 5 | 10 | 2.5 | 5 |

## DIGITAL OUTPUT CODING

| Analog Input Voltage Range | | | | | | | Digital Output | |
|---|---|---|---|---|---|---|---|---|
| 0 to +5V | 0 to +10V | ±2.5V | ±5V | ±10V | 0 to −5V | 0 to −10V | MSB | LSB |
| +5.000 | +10.000 | +2.500 | +5.000 | +10.000 | 0.000 | 0.000 | 1111 | 1111 |
| +4.981 | +9.961 | +2.481 | +4.961 | +9.922 | −0.019 | −0.039 | 1111 | 111Ø* |
| +2.519 | +5.039 | +0.019 | +0.039 | +0.078 | −2.481 | −4.961 | 1000 | 000Ø* |
| +2.500 | +5.000 | 0.000 | 0.000 | 0.000 | −2.500 | −5.000 | ØØØØ | ØØØØ* |
| +2.481 | +4.961 | −0.019 | −0.039 | −0.078 | −2.519 | −5.039 | 0111 | 111Ø* |
| +0.019 | +0.039 | −2.481 | −4.961 | −9.922 | −4.981 | −9.961 | 0000 | 000Ø* |
| 0.000 | 0.000 | −2.500 | −5.000 | −10.000 | −5.000 | −10.000 | 0000 | 0000 |

**DIGITAL OUTPUT CODING NOTES:**

1. For unipolar input ranges, output coding is straight binary.
2. For bipolar input ranges, output coding is offset binary.
3. For 0 to +5V, 0 to −5V or ±2.5V ranges, 1LSB for 8 bits = 19.5mV.
4. For 0 to +10V, 0 to −10V or +5V input ranges, 1LSB for 8 bits = 39mV.
5. For ±10V input range, 1LSB for 8 bits = 78mV.

*Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from "1" to "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For an MN5150 operating on its ±10V input range, the transition from digital output 0000 0000 to 0000 0001 (or vice versa) will ideally occur at an input voltage of −9.961 volts. Subsequently, any input voltage more negative than −9.961 volts will give a digital output of all "0's". The transition from digital output 1000 0000 to 0111 1111 will ideally occur at an input of 0.000 volts, and the 1111 1111 to 1111 1110 transition should occur at +9.961 volts. An input more positive than +9.961 volts will all give all "1's".