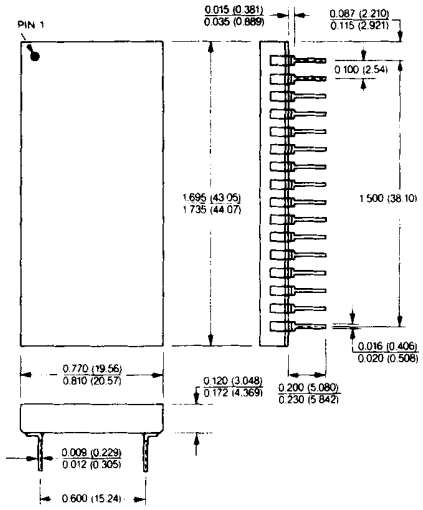
# Low-distortion Sampling 16-bit A/D Converters

## FEATURES

- 20kHz Sampling Rate With Internal T/H Amplifier
- 10kHz Full-Power Input Bandwidth
- 84dB Signal-to-Noise Ratio Over Full Bandwidth
- −88dB Harmonics Over Full Bandwidth
- FFT Testing
- Serial and Parallel Outputs
- 1.5 Watts Max Power
- Standard 32-Pin DIP
- Fully Specified 0°C to +70°C (J and K Models) or −55°C to +125°C (S and T Models)

### 32 PIN DIP

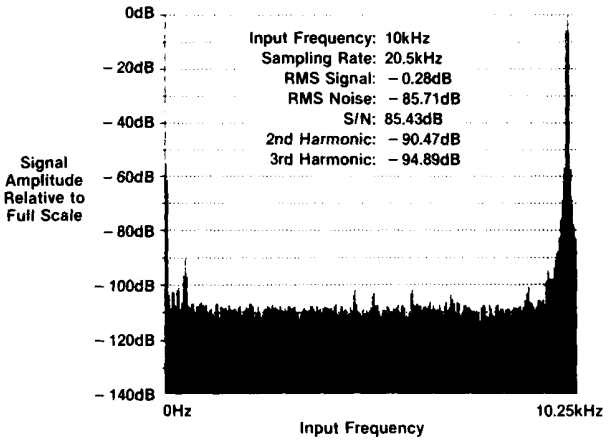



Dimensions in Inches (millimeters)

## DESCRIPTION

The MN6290 Series of Low-Distortion, 16-Bit, Sampling, A/D Converters offers an outstanding combination of resolving power, conversion speed, low noise, and low harmonic distortion. These SA type A/D's are packaged in small, 32-pin, double-wide DIP's and have internal track-hold (T/H) amplifiers that enable them to accurately sample and digitize 10kHz full-scale input signals at rates up to 20kHz. Each device is fully FFT (Fast Fourier Transform) tested using contemporary DSP technology and guarantees up to 84dB signal-to-noise ratio (SNR, rms-to-rms) and up to −88dB harmonics and spurious noise.

MN6290 (10V input span) and MN6291 (20V input span) are configured in a manner that makes their internal T/H completely user transparent. A high-impedance (5MΩ) input buffer isolates the T/H from its signal source, and the T/H's operational mode is internally controlled by the A/D's status line. Users need only supply start-convert pulses at the desired sampling rate. Each device is fully tested both statically, in the traditional manner, and dynamically with a series of 512-point FFT's. This type of configuration and testing eliminates the need for potentially confusing and misleading T/H specifications like aperture delay, aperture jitter, charge injection, etc., and also eliminates historically frustrating attempts to translate data-converter time-domain specifications into frequency-domain performance.



# MN6290, MN6291 SAMPLING 16-Bit A/D CONVERTERS

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Operating Temperature Range | −55°C to +125°C |
| Specified Temperature Range: | |
| MN6290J, K; MN6291J, K | 0°C to +70°C |
| MN6290S, S/B, T, T/B | −55°C to +125°C |
| MN6291S, S/B, T, T/B | −55°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Positive Supply (+Vcc, Pin 27) | 0 to +16.5 Volts |
| Negative Supply (−Vcc, Pin 23) | 0 to −16.5 Volts |
| Logic Supply (+Vdd, Pin 29) | 0 to +7 Volts |
| Digital Inputs (Pins 30, 32) | 0 to +5.5 Volts |
| Analog Inputs (Pins 7, 8) | ±15 Volts |
| Analog Ground (Pins 9, 26) to Digital Ground (Pin 31) | ±1 Volt |
| Ref Out (Pin 8) Short Circuit Duration | Continuous to Ground |

## ORDERING INFORMATION

PART NUMBER ——— **MN6290T/B**

Select MN6290 or MN6291

Select suffix J, K, S, or T for desired performance and specified temperature range.

Add "/B" to "S" or "T" models for Environmental Stress Screening.

**DESIGN SPECIFICATIONS ALL UNITS ($T_A$ = +25°C, $\pm V_{cc}$ = ±15V, $+V_{dd}$ = +5V unless otherwise indicated) (Note 1)**

| ANALOG INPUTS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|
| Input Voltage Ranges: MN6290<br>MN6291 | | 0 to +10, ±5<br>±10 | | Volts<br>Volts |
| Input Impedance (Note 17): Resistance<br>Capacitance | | 5<br>50 | | Mohm<br>pF |
| Input Bias Current Over Full Temperature Range | | | ±600 | nA |
| **DIGITAL INPUTS (Start, Short Cycle)** | | | | |
| Logic Levels: Logic "1"<br>Logic "0" | +2.0 | | <br>+0.8 | Volts<br>Volts |
| Logic Currents: Logic "1" ($V_{IH}$ = +2.4V)<br>Logic "0" ($V_{IL}$ = +0.4V) | | | +40<br>−0.8 | μA<br>mA |
| **DIGITAL OUTPUTS (Serial, Parallel, Status, Clock)** | | | | |
| Output Coding (Note 2): Unipolar Ranges<br>Bipolar Ranges | | Straight Binary<br>Offset Binary | | |
| Logic Levels: Logic "1" ($I_{source} \leq 320\mu A$)<br>Logic "0" ($I_{sink} \leq 3.2mA$) | +2.4 | | <br>+0.4 | Volts<br>Volts |
| **INTERNAL REFERENCE** | | | | |
| Reference Output (Pin 24): Voltage<br>Drift (Note 17)<br>Output Current (Notes 3, 17) | +9.9 | +10<br>±15 | +10.1<br><br>1 | Volts<br>ppm/°C<br>mA |
| **POWER SUPPLY REQUIREMENTS** | | | | |
| Power Supply Range: $\pm V_{cc}$ Supply<br>$+V_{dd}$ Supply | ±14.5<br>+4.5 | ±15<br>+5 | ±15.5<br>+5.5 | Volts<br>Volts |
| Power Supply Rejection (Note 14): $+V_{cc}$<br>$-V_{cc}$<br>$+V_{dd}$ | | ±0.003<br>±0.003<br>±0.001 | ±0.02<br>±0.02<br>±0.01 | %FSR/% Supply<br>%FSR/% Supply<br>%FSR/% Supply |
| Current Drains: $+V_{cc}$ Supply<br>$-V_{cc}$ Supply<br>$+V_{dd}$ Supply | | +33<br>−34<br>+28 | +48<br>−40<br>+35 | mA<br>mA<br>mA |
| Power Consumption | | 1150 | 1500 | mW |

**PERFORMANCE SPECIFICATIONS (Typical at $T_A$ = +25°C, ±$V_{CC}$ = ±15V, +$V_{dd}$ = +5V unless otherwise indicated)**

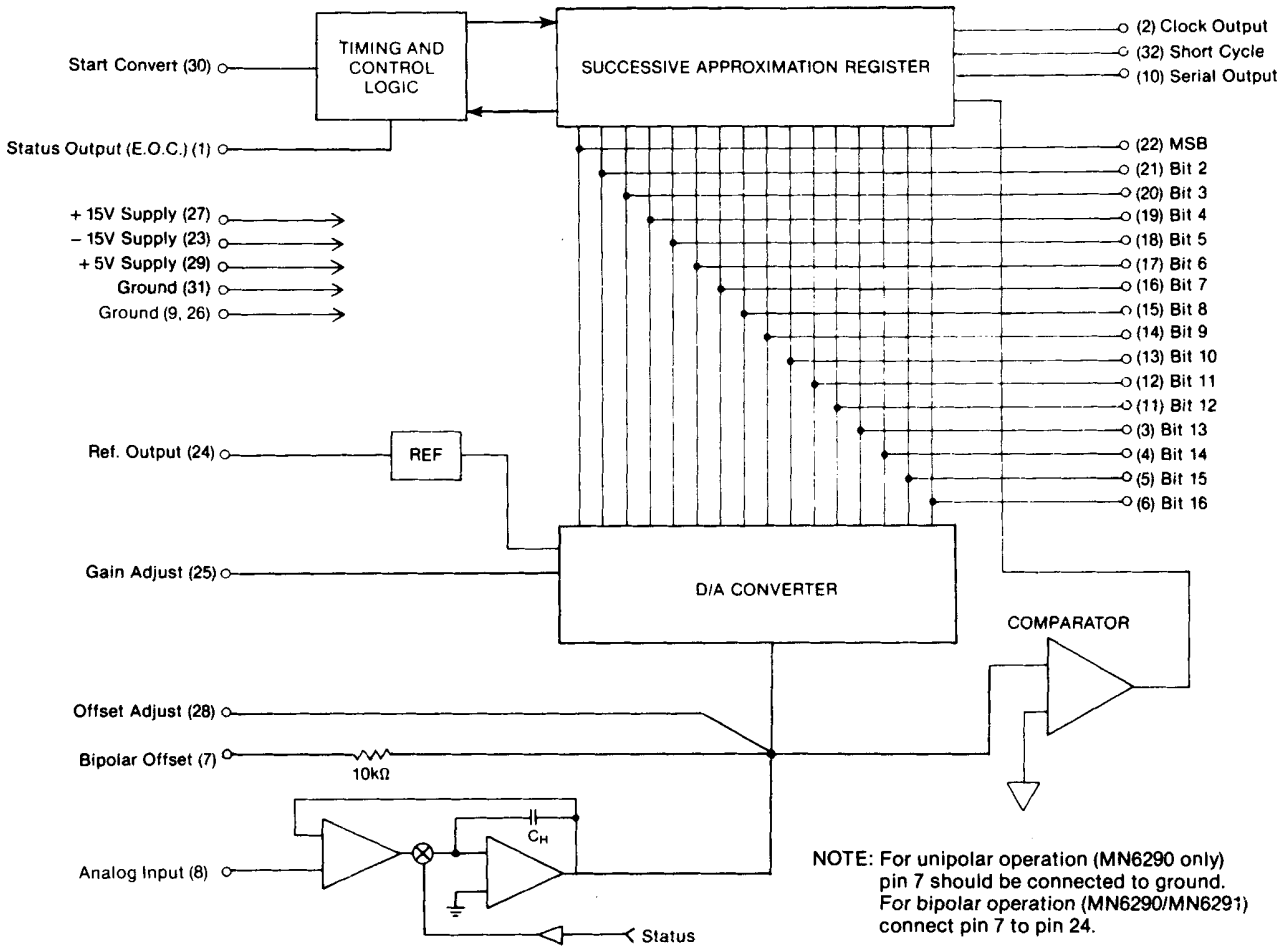
| DYNAMIC CHARACTERISTICS | MN6290J MN6291J | MN6290K MN6291K | MN6290S MN6291S | MN6290T MN6291T | UNITS |
|---|---|---|---|---|---|
| Minimum Guaranteed Sampling Rate (Note 4) | 20 | 20 | 20 | 20 | kHz |
| Maximum A/D Conversion Time (Note 5) | 40 | 40 | 40 | 40 | µsec |
| Signal-to-Noise Ratio (SNR, Note 6): | | | | | |
| Initial (+25°C) (Minimum) | 80 | 84 | 80 | 84 | dB |
| $T_{min}$ to $T_{max}$ (Minimum, Note 7) | 78 | 82 | 78 | 82 | dB |
| Harmonics and Spurious Noise (Note 8): | | | | | |
| Initial (+25°C) (Minimum) | −85 | −88 | −85 | −88 | dB |
| $T_{min}$ to $T_{max}$ (Minimum, Note 7) | −82 | −85 | −82 | −85 | dB |
| Input Signal Full-Scale Bandwidth (Minimum, Note 9) | 10 | 10 | 10 | 10 | kHz |
| **STATIC CHARACTERISTICS** | | | | | |
| Integral Linearity Error: Initial (+25°C) (Max. Note 16) | ±0.006 | ±0.003 | ±0.006 | ±0.003 | %FSR |
| $T_{min}$ to $T_{max}$ (Maximum, Note 7) | ±0.012 | ±0.006 | ±0.012 | ±0.006 | %FSR |
| Resolution for Which No Missing Codes is Guaranteed: Initial (+25°C) | 13 | 14 | 13 | 14 | Bits |
| $T_{min}$ to $T_{max}$ (Note 7) | 13 | 14 | 13 | 14 | Bits |
| Unipolar Offset Error (Notes 10, 11): | | | | | |
| Initial (+25°C) (Maximum) | ±0.05 | ±0.05 | ±0.05 | ±0.05 | %FSR |
| Drift (Maximum) | ±15 | ±7.5 | ±15 | ±7.5 | ppm of FSR/°C |
| Max Error $T_{min}$ to $T_{max}$ (Note 15) | ±0.12 | ±0.084 | ±0.2 | ±0.125 | %FSR |
| Bipolar Zero Error (Notes 10, 12): | | | | | |
| Initial (+25°C) (Maximum) | ±0.075 | ±0.05 | ±0.075 | ±0.05 | %FSR |
| Drift (Maximum) | ±15 | ±10 | ±15 | ±10 | ppm of FSR/°C |
| Max Error $T_{min}$ to $T_{max}$ (Note 15) | ±0.15 | ±0.1 | ±0.225 | ±0.15 | %FSR |
| Full Scale Accuracy Error (Notes 10, 13): | | | | | |
| Initial (+25°C) (Maximum) | ±0.2 | ±0.1 | ±0.2 | ±0.1 | %FSR |
| Max Error $T_{min}$ to $T_{max}$ (Note 15) | ±0.35 | ±0.2 | ±0.5 | ±0.3 | %FSR |
| Drift (Maximum) | ±30 | ±20 | ±30 | ±20 | ppm of FSR/°C |

**SPECIFICATION NOTES:**

1. Detailed timing specifications appear in the Timing sections of this data sheet.
2. See table of transition voltages in section labeled Digital Output Coding.
3. In addition to supplying 1mA of current for bipolar offsetting purposes (pin 7 connected to pin 24), the internal reference is capable of driving up to 1mA into an external load. If the internal reference is used to drive an external load, the load should not change during a conversion.
4. Minimum guaranteed sampling rate refers to the fact that these devices guarantee all other performance specs while sampling and digitizing at a 20kHz rate. Obviously, devices may be operated at lower sampling frequencies if desired and typically will meet all performance specs while sampling at rates of 25kHz or higher.
5. Whenever the Status Output (pin 1) is low ("logic "0"), the internal T/H is in the track mode, and the A/D converter is not converting. When Status is high (the definition of A/D conversion time), the T/H is in the hold mode, and the A/D is performing a conversion.
6. This parameter represents the rms-signal-to-rms-noise ratio in the output spectrum (excluding harmonics) with a full-scale input sine wave (0db) at any frequency up to 10kHz.
7. MN6290J, K and MN6291J, K are fully specified for 0°C to +70°C operation. MN6290S, S/B, T, T/B and MN6291S, S/B, T, T/B are fully specified for −55°C to +125°C operation.
8. This parameter represents the peak signal to peak non-fundamental component (harmonic or spurious, inband or out of band) in the output spectrum.
9. This is the highest-frequency, full-scale, input signal for which the SNR and harmonic figures are guaranteed when sampling at a 20kHz rate.
10. Adjustable to zero with external potentiometer.
11. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 0000 to 0000 0000 0000 0001 when operating the MN6290 on its unipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
12. Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0111 1111 1111 1111 to 1000 0000 0000 0000 when operating the MN6290/6291 on a bipolar range. The ideal value at which this transition should occur is −½LSB. See Digital Output Coding.
13. Full scale accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1111 1110 to 1111 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition for bipolar input ranges. The former transition ideally occurs at an input voltage 1½LSB's below the nominal positive full scale voltage. The latter ideally occurs ½LSB above the nominal negative full scale voltage. See Digital Output Coding.
14. Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 or 0000 0000 0000 0000 to 0000 0000 0000 0001 output transitions occur versus a change in power-supply voltage.
15. Listed maximum error-over- temperature specifications for unipolar offset, bipolar zero and full-scale accuracy correspond to the combination of maximum room-temperature errors and worst-case drift conditions to describe the worst-case error that might be encountered over the entire specified temperature range.
16. ±0.006%FSR is equivalent to ±½LSB for 13 bits and is equal to ±0.6mV for a device with a 10V full scale range (0 to +10V or ±5V input range). ±0.003%FSR is equivalent to ±½LSB for 14 bits and is equal to ±0.3mV for a device with a 10V full scale range.
17. These parameters are listed for reference only and are not tested.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

## BLOCK DIAGRAM




NOTE: For unipolar operation (MN6290 only) pin 7 should be connected to ground. For bipolar operation (MN6290/MN6291) connect pin 7 to pin 24.

## APPLICATIONS INFORMATION

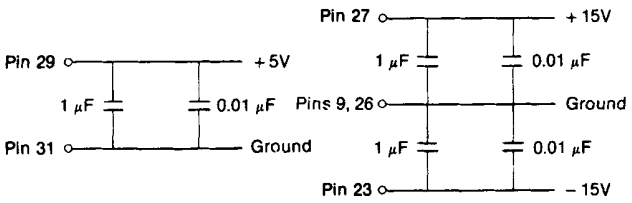
**LAYOUT CONSIDERATIONS** — Proper attention to layout and decoupling is necessary to obtain specified accuracies from the MN6290/6291. The units' three ground pins (pins 9, 26, and 31) are not connected to each other internally. They must be tied together as close to the unit as possible and all connected to system analog ground, preferably through a large analog ground plane beneath the package. If these commons must be run separately, a non-polarized 0.01μF ceramic bypass capacitor should be connected between analog ground pins (pins 9 and 26) and digital ground (pin 31) as close to the unit as possible. Wide conductor runs should be employed.

Coupling between analog inputs and digital signals should be minimized to avoid nosie pick-up. Bipolar Offset (pin 7), Analog Input (pin 8), Offset Adjust (pin 28) and Gain Adjust (pin 25) are particularly noise susceptable. Care should be taken to avoid long runs or runs close to digital lines when utiiizing these inputs. Input signal lines should be a short as possible. In bipolar operation, where Bipolar Offset (pin 7) is connected to Reference Output (pin 24), a short jumper should be used. For external offset adjustment, the series resistor(s) should be located as close to Offset Adjust (pin 28) as possible. A 0.01μF capacitor should be connected between Gain Adjust (pin 25) and Analog Ground as close to the package as possible. An 0.01μF capacitor should be connected from Reference Output (pin 24) to Analog Ground.

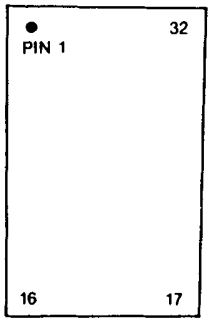
Power supplies should be decoupled with tantalum and ceramic capacitors located close to the MN6290/6291. For optimum performance and noise rejection, 1μF tantalum capacitors paralleled with 0.01μF ceramic capacitors should be used as shown in the diagrams below.

If short-cycling is not used the Short-Cycling pin (pin 32) must be connected to +5V (pin 29).

**POWER SUPPLY DECOUPLING**



## PIN DESIGNATIONS




| | | | |
|---|---|---|---|
| 1 | Status (E.O.C.) | 32 | Short Cycle |
| 2 | Clock Output | 31 | Digital Ground |
| 3 | Bit 13 | 30 | Start Convert |
| 4 | Bit 14 | 29 | +5V Supply ($+V_{dd}$) |
| 5 | Bit 15 | 28 | Offset Adjust |
| 6 | Bit 16 (LSB) | 27 | +15V Supply ($+V_{cc}$) |
| 7 | Bipolar Offset | 26 | Analog Ground |
| 8 | Analog Input | 25 | Gain Adjust |
| 9 | Analog Ground | 24 | Reference Output (+10V) |
| 10 | Serial Output | 23 | −15V Supply ($-V_{cc}$) |
| 11 | Bit 12 | 22 | Bit 1 (MSB) |
| 12 | Bit 11 | 21 | Bit 2 |
| 13 | Bit 10 | 20 | Bit 3 |
| 14 | Bit 9 | 19 | Bit 4 |
| 15 | Bit 8 | 18 | Bit 5 |
| 16 | Bit 7 | 17 | Bit 6 |

## APPLICATIONS INFORMATION

**DESCRIPTION OF OPERATION**—MN6290 and MN6291 are 16-bit, sampling, A/D converters. Each contains a 16-bit successive-approximation type A/D and a companion track-hold (T/H) amplifier. The T/H's enable MN6290 and MN6291 to accurately and repetitively sample and digitize dynamically changing input signals in both traditional data-acquisition and contemporary DSP-type applications.

Successive approximation (SA) type A/D converters, when operated without the aid of T/H amplifiers, are severely limited in their ability to accurately convert changing analog input signals. The traditional rule of thumb for guaging such performance is that the A/D's are incapable of accurately converting signals that are slewing faster than (± ½LSB)/(conversion time). For a 14-bit A/D with an input range of ± 10V and a conversion time of 40μsec, this corresponds to an input slew-rate limit of ± 7.6μV/μsec. If one wishes to express the slew-rate limit as a bandwidth for a full-scale input sinusoid, it corresponds to 0.24Hz.

The proliferating use of A/D converters in DSP applications has resulted in significantly greater demands on A/D's to be able to convert dynamic signals, particularly sinusoids. More and more frequently, T/H amplifiers are used with A/D's to enable them to accomplish this task.

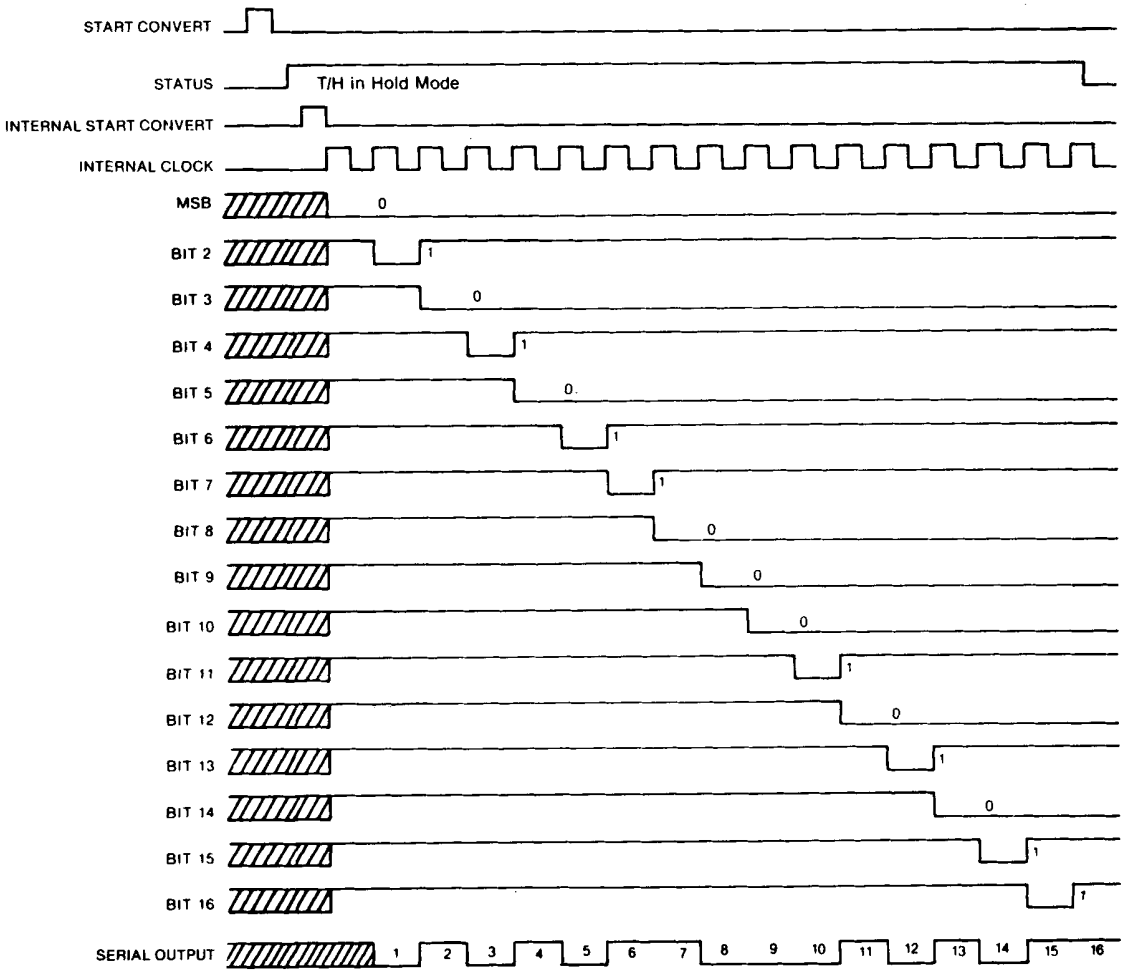
MN6290/6291 are extremely user friendly. They have been configured in a manner that virtually eliminates all of the problems encountered when mating T/H's and successive approximation A/D's and driving the pair from real-world signal sources. The T/H is truly transparent. A high-impedance (5Mohm) input buffer isolates it from the external signal source, and its output is internally connected directly to the input of the A/D converter. The output current, impedance and transient-response characteristics of the T/H have been optimized for driving the 16-bit SA A/D. More importantly, the critical dynamic characteristics of the T/H (aperture delay, aperture jitter, small and large signal bandwidths, droop rate, etc.) have been similarly optimized. Most importantly, the critical inter-device timing relationships (T/H mode control, transient decay time, etc.) are internally controlled by MN6290/6291's timing and control circuitry. All that users need to provide externally is the start convert pulse.

The falling edge of the start convert pulse activates MN6290/6291's internal timing circuitry. Immediately, the T/H (which has been in the track or signal-acquisition mode up until this time) is driven into the hold mode instantaneously "freezing" the value of the analog input signal. Simultaneously, MN6290/6291's status output (also called "End of Conversion" or E.O.C.) is set to a logic "1" indicating that the T/H is now in hold; that an A/D conversion is now in progress; and that the parallel output data (from the previous conversion) is no longer valid. MN6290/6291's internal timing logic now provides approximately 1 μsec of delay to permit the track-to-hold switching transient at the output of the T/H to decay. Subsequently, the internal clock is started, and the 16-bit A/D conversion of the held signal proceeds.

The value of the hold capacitor used in MN6290/6291's internal T/H has been selected so that T/H output droop, even over temperature, is not significant (greater than ± ½LSB) during the A/D's conversion time. Similarly, the offset and pedestal voltages, as well as the gain error, of the T/H do not contribute to the overall accuracy of the sampling A/D because they are effectively nulled out during our active laser trimming of the A/D converter.

At the completion of the A/D conversion, MN6290/6291's internal control logic turns off the internal clock; drops the status output back to a logic "0"; and commands the T/H back into the track mode to acquire a new input signal. Status going low signifies that the conversion is complete and that the parallel output data is valid. A 20nsec delay has been added between the finalization of the LSB and the falling edge of status. This ensures that all output bits are valid when status falls and permits the use of this trailing edge to clock data into output latches. Output data remains valid until the falling edge of the next start convert pulse.

## TIMING DIAGRAM



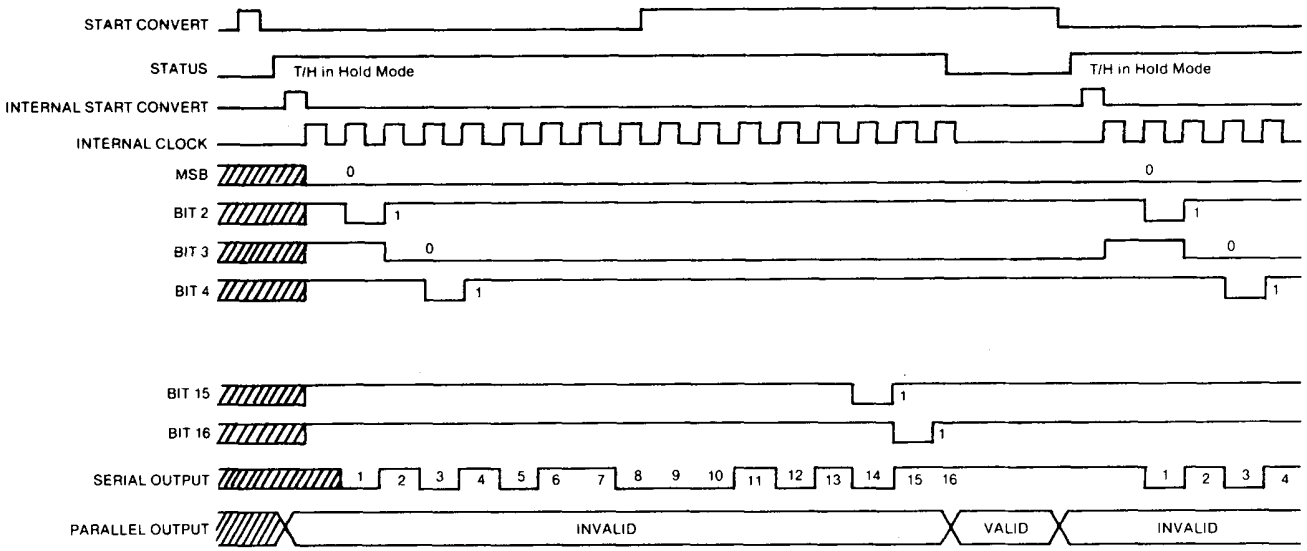

**SPECIFICATIONS ($T_A$ = +25°C, supply voltages ±15V and +5V unless otherwise specified)**

| DYNAMIC CHARACTERISTICS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|
| Conversion Time (16 Bits) (Note 6) | | 35 | 40 | μsec |
| Internal Clock Frequency (Notes 4, 8) | 404 | 462 | | kHz |
| Start Convert Pulse Width (Notes 2, 7) | 40 | | | nsec |
| Delay Falling Edge of Start to (Note 8): Status = "1"<br>Clock Output = "1" | | 30<br>400 | | nsec<br>nsec |
| Delay Rising Clock Edge to Output Data Valid (Parallel, Serial, Status) (Note 8) | 20 | 100 | | nsec |
| Delay LSB Valid to Falling Edge of Status (Notes 3, 8) | 20 | 40 | | nsec |

**TIMING DIAGRAM NOTES:**

1. Operation shown is for the digital word 0101 0110 0010 1011.
2. The Start Convert command can be either a positive or negative pulse at least 40nsec wide. Conversions are initiated on the falling edge of the Start Convert command.
3. Data will be valid 20nsec prior to the falling edge of Status (E.O.C.).
4. The internal clock is enabled and the conversion commences following an internal delay which allows for T/H switching and settling.
5. When the converter is initially "powered up" it may come on at any point in the conversion cycle.
6. Conversion time is defined as the width of the Status (E.O.C.) pulse.
7. The minimum time between falling edges of the Start Convert command is 50μsec.
8. These parameters are listed for reference only and are not tested.

## APPLICATIONS INFORMATION




**TIMING DIAGRAM** — The above timing diagram illustrates the relationships of the external and internal timing pulses discussed in the following sections. Additionally, the above diagram shows the beginning of a second conversion and of particular interest, the relationship of Start Convert, Status (E.O.C.), Serial Output and Parallel Output from one conversion to another.

**START CONVERT** — The falling edge of the start convert signal initiates the sampling/digitizing cycle. Either positive, negative or symetrical pulses can be used to initiate conversions provided that the start convert signal has a minimum positive pulse width of 40nsec. To achieve guaranteed performance, the maximum repetition rate of the start convert signal is 20kHz. Obviously, MN6290/6291 may be operated at lower sampling rates if desired. If necessary, the start convert signal may be set to a logic "1" after the conversion has begun, however, the next falling edge should not occur until the ongoing conversion is complete and a minimum of 10$\mu$sec has been allowed for the internal T/H amplifier to acquire and track the next analog input voltage to be sampled and digitized. See diagram above.

**STATUS OUTPUT** — The Status Output (End of Conversion (E.O.C.), pin 1) will be set to a logic "1" 30nsec (typical) after the falling edge of Start Convert; will remain a logic "1" during the conversion; and will be set to a logic "0" when the conversion is complete. The falling edge of status occurs a minimum of 20nsec after the LSB output bit is set to its final value (delay from LSB bit valid to falling edge of Status is 20nsec min). Therefore, the Status Output may be used to latch valid digital output data. If the latches selected require more than 20nsec of set-up time, simple gate delays can be used to delay the falling edge of Status. See diagram above.

**SHORT CYCLE** — For applications requiring fewer than 16 bits of resolution, MN6290/6291 can be truncated or short cycled to the desired number of bits with a proportionate decrease in the A/D conversion time. To truncate at n bits, simply connect the n + 1 bit output to the Short Cycle input (pin 32). For example, to truncate at 14 bits, connect Bit 15 (pin 5) to the Short Cycle input (pin 32); converting will stop and the Status Output (End of Conversion (E.O.C.), pin 1) will be set to a logic "0" a minimum of 20nsec after bit 14 has been set.

**PARALLEL OUTPUTS** — During the succesive approximation process the weight of each bit is compared to the value of the analog input voltage. The converter is reset to MSB-0111 1111 1111 1111-LSB by the rising edge of the first clock pulse. Subsequent rising clock edges set the bit previously tested to its final state and brings the next bit to be tested to a logic "0". This process continues until all bits have been tested and the Status Output returns to a logic "0". Valid parallel output data can only be latched at the end of the sample/conversion cycle.

The LSB bit is valid 20nsec prior to the falling edge of Status Output (E.O.C.), therefore, this edge may be used to latch parallel output data. While the converter is idling (Status Output is "0"), the parallel output data from the most recent conversion remains valid until the start of the next conversion cycle.

**SERIAL OUTPUT** — Serial output data is provided only during the conversion process and is in a NRZ (non-return to zero) format. The data is coded the same as parallel output data and is synchronous with the internal clock. Each serial output bit is valid 20nsec after the rising clock edge (serial output data lags parallel output by one clock cycle, see timing diagram) and can be strobed into a shift register by rising edges of the internal clock.

## DIGITAL OUTPUT CODING

| ANALOG INPUT | | | DIGITAL OUTPUT | | | |
|---|---|---|---|---|---|---|
| 0 to +10V | ±5V | ±10V | MSB | | | LSB |
| +F.S. | +F.S. | | 1111 | 1111 | 1111 | 1111 |
| +F.S. − 3/2 LSB | +F.S. − 3/2 LSB | | 1111 | 1111 | 1111 | 111Ø* |
| +½F.S. + ½ LSB | + ½ LSB | | 1000 | 0000 | 0000 | 000Ø* |
| +½F.S. − ½ LSB | − ½ LSB | | ØØØØ | ØØØØ | ØØØØ | ØØØØ* |
| +½ F.S. − 3/2 LSB | − 3/2 LSB | | 0111 | 1111 | 1111 | 111Ø* |
| + ½ LSB | −F.S. + ½ LSB | | 0000 | 0000 | 0000 | 000Ø* |
| 0 | −F.S. | | 0000 | 0000 | 0000 | 0000 |

**CODING NOTES:**

1. For 10 Volts FSR, 1LSB for 16 Bits = 152.6μV. 1LSB for 14 Bits = 610.4μV.
2. For 20 Volts FSR, 1LSB for 16 Bits = 305.2μV. 1LSB for 14 Bits = 1.22mV.
3. For unipolar ranges, the coding is straight binary.
4. For bipolar ranges, the coding is offset binary.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the MN6290/MN6291 continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

EXAMPLE: For the ±10V range, the transition from output code 1111 1111 1111 1111 to output code 1111 1111 1111 1110 (or vice versa) will ideally occur at an input of +9.999542V (+F.S. − 3/2LSB). Subsequently, any voltage greater than +9.999542V will give a digital output of all "1's." The transition from digital output 0111 1111 1111 1111 to 1000 0000 0000 0000 (or vice versa) will ideally occur at an input of −0.000153 volts. The 0000 0000 0000 0000 to 0000 0000 0000 0001 transition will occur at −9.999847V. An input more negative than this level will give all "0's."

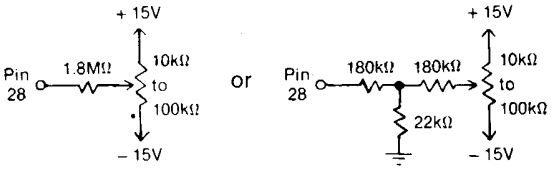
## INPUT RANGE SELECTION

| Part Number | Range | Connect Pin 7 to Pin |
|---|---|---|
| 6290 | 0 to +10V | Ground |
| 6290 | ±5V | 24 |
| 6291 | ±10V | 24 |

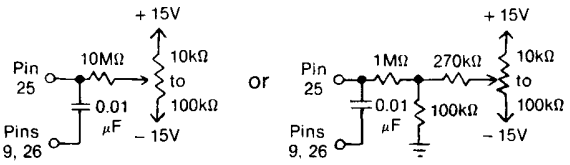
**OPTIONAL EXTERNAL ZERO AND GAIN ADJUSTMENTS** — Initial zero and gain errors may be trimmed to zero using external potentiometers as shown in the following diagrams. Adjustments should be made following warmup, and to avoid interaction, zero should be adjusted before gain. Fixed resistors can be ±20% carbon composition or better. Multiturn potentiometers with TCR's of 100ppm/°C or less are recommended to minimize drift with temperature. If these adjustments are not used, pin 28 should be left open. A 0.01μf capacitor should be tied from Gain Adjust (pin 25) to Analog Ground (pins 9,26).

**ZERO ADJUSTMENT** — Connect the zero adjust potentiometer as shown below. For unipolar ranges (MN6290 only), apply the input voltage at which the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition is ideally supposed to occur. While continuously converting, adjust the zero potentiometer until all bits are "0" and the LSB "flickers" on and off.

For bipolar ranges (MN6290 and MN6291), apply the input voltage at which the 0111 1111 1111 1111 to 1000 0000 0000 0000 transition is ideally supposed to occur. While continuously converting, adjust the zero potentiometer until all bits are "flickering."




**GAIN ADJUSTMENT** — Connect the gain potentiometer as shown below and apply the input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 transition is ideally supposed to occur. While continuously converting, adjust the gain potentiometer until all the output bits are "1" and the LSB "flickers" on and off. A 0.01μf capacitor should be connected from Gain Adjust (pin 25) to Analog Ground (pins 9, 26).



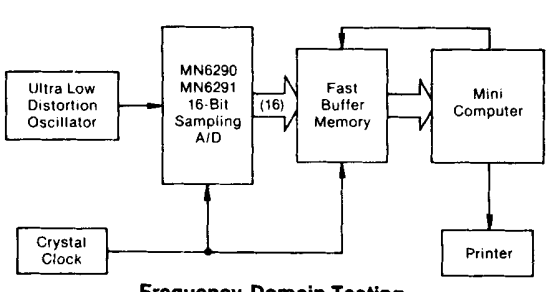

## THE INTERNAL T/H AMPLIFIER

As stated in the Description of Operation, MN6290/6291's internal T/H amplifier is transparent to the user. The T/H's output is connected directly to the A/D's input and its operational mode is controlled by the Timing and Control Logic (see Block Diagram). The user is not required to supply additional support timing circuits sometimes necessary when mating an A/D with its companion T/H. Additionally, MN6290/6291 users need not concern themselves with oftentimes confusing T/H specifications like acquisition time, aperture-delay time, aperture jitter, droop rate, etc.. These parameters are not specified for MN6290/6291 and are, in fact, impossible to directly test because the T/H's output and control line are not accessable at the device pins. Frequency-domain specifications like input bandwidth, sampling rate, signal-to-noise ratio, harmonic distortion, etc. obviates the need for knowing the specific T/H time-domain specifications, however, the table on the following page does supply typical values for those critical T/H performance specifications.

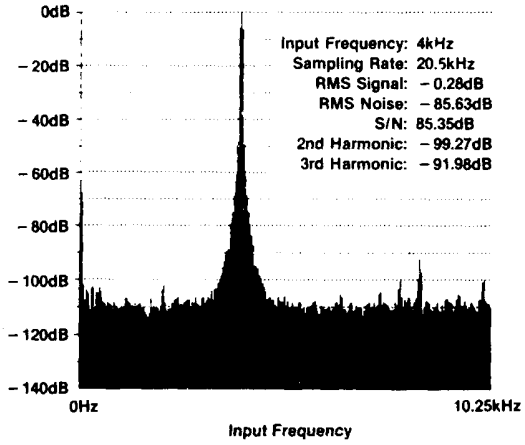
Note that the static errors (gain error, track-mode offset error, and pedestal) of the T/H function add directly to the corresponding errors of the A/D converter but that both are effectively nulled with the functional laser trimming of the A/D. T/H offset error and pedestal, for example, add directly to A/D-converter offset error. However, when the A/D offset is functionally laser trimmed, it is done with the whole device sampling at a 20kHz rate and the T/H is in the hold mode whenever trimming is actually performed. Consequently, all error sources are compensated for. All static errors on MN6290/6291 (accuracy error, unipolar offset error, bipolar zero error, etc.) are tested and specified as full input-output transfer specifications and include both the T/H and A/D.

| Typical T/H Performance Specifications | |
|---|---|
| Gain Error<br>Gain Linearity Error | ± 0.01%<br>± 0.001% FSR |
| Track Mode Output Offset Error<br>Pedestal | ± 0.5mV<br>± 0.5mV |
| Acquisition Time: 10V step to ± 0.003%<br>20V step to ± 0.003% | 5μsec<br>6μsec |
| Track-Hold Transient Settling (to ± 1mV) | 250nsec |
| Slew Rate<br>Full Power Bandwidth | ± 4V/μsec<br>50kHz |
| Effective Aperture Delay Time<br>Aperture Jitter | – 25nsec<br>0.5nsec |
| Droop Rate<br>Hold-Mode Feedthrough Attenuation | ± 0.05μV/μsec<br>– 86dB |

**FREQUENCY-DOMAIN TESTING** — MN6290/6291 is specified and tested statically in the traditional manner (linearity, accuracy, offset error, current drains, etc.) and dynamically in the frequency domain. In the dynamic tests, MN6290/6291 is operated in a manner that resembles an application as a digital spectrum analyzer. A very low distortion signal generator (harmonics – 100dB) is used to generate a pure, full-scale, 10kHz sine wave that MN6290/6291 samples and digitizes at a 20.5kHz rate. These conditions (signal period = 100μsec, sampling interval = 48.8μsec) approach the Nyquist sampling limit (at least 2 samples per signal cycle; sampling frequency greater than 2 times signal frequency). A total of 512 sample-and-convert operations are performed, and the digital output data is stored in a high-speed, FIFO, buffer-memory box. The 512 data points are then accessed by a microcomputer which executes a 512-point Fast Fourier Transform (FFT) after applying a Hanning (raised cosine) window function to the data. The resulting spectrum shows the amplitude and frequency content of the converted signal along with any errors (noise, harmonic distortion, spurious signals, etc.) introduced by the A/D converter. Subsequently, signal-to-noise ratio (SNR) and harmonic distortion measurements are read from the spectrum. A functional block diagram of the test setup appears below, and a sample spectrum appears above.




**Frequency-Domain Testing of A/D Converters**

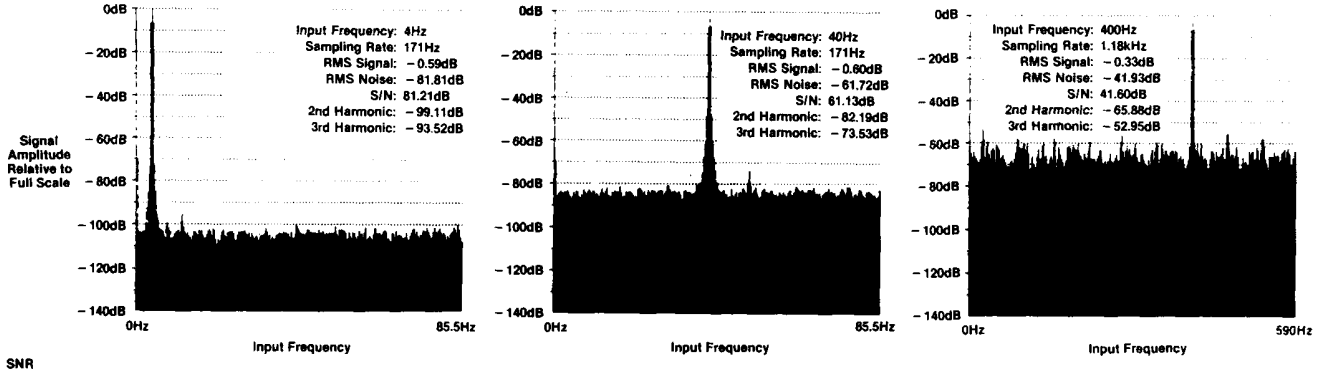


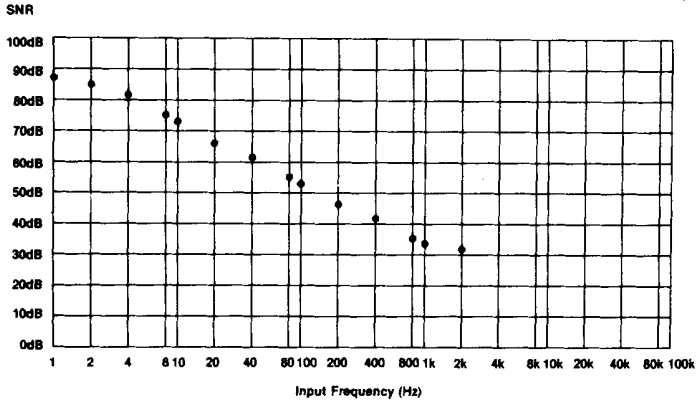

The spectrum above is the real portion (imaginary portions of spectra are discarded) of a 512-point FFT. The horizontal axis is the frequency axis, and its rightmost end is equal to ½ the sampling rate (10.25kHz in this case). The horizontal axis is divided into 256 frequency bins, each with a width of 40.04Hz. Recall that the highest frequency on the frequency axis of the spectrum of a sampled signal is equal to one-half the sampling rate and that input signals with frequencies higher than ½ the sampling rate are effectively "undersampled" and aliased back into the spectrum.

The vertical axis of the spectrum corresponds to signal amplitude in rms volts relative to a full-scale sinusoidal input signal (0dB). The sample spectrum above is the result of averaging 10 512-point FFT's run on data taken from an MN6290 operating on its bipolar input range (± 5V) with a full-scale input sine wave ($v(t) = 5\sin\omega t$) at a frequency of 4kHz. In the spectrum, the full-scale input signal appears at 4kHz at a level of – 0.28dB. Full-scale rms signals do not appear at – 3dB levels because our FFT program has been normalized to bring them to zero. The d.c. component in the spectrum is effectively the offset error of the MN6290 combined with that of the signal generator and test fixture. A second harmonic, if it were either present in the input signal or created by the MN6290, would appear at 8kHz. If a third harmonic were present, it would be aliased back into the spectrum and appear at 8.5kHz. Harmonic distortion and spurious noise levels are calculated as the ratio (in dB) of the signal level to the strongest harmonic or spurious (nonharmonic) signal in the spectrum. In the sample spectrum above, the strongest harmonic is the third. It appears at a level of – 92.26dB, and the signal to harmonics ratio is equal to 91.98dB. Rms noise is calculated as the rms summation of all nonfundamental and nonharmonic components in the output spectrum, and SNR is calculated as the ratio of the rms signal to the rms noise. For the above spectrum, the normalized rms signal level is – 0.28dB; the rms noise level is – 85.63dB; and the SNR is 85.35dB.

The term "noise" is generally used to describe what remains in the output spectrum after all fundamental, harmonic, d.c., and outstanding spurious components have been removed. It generally appears across all frequency bins at some relatively flat level sometimes referred to as the "noise floor". The rms noise, as described above, represents the broadband noise that would appear superimposed on the sinusoidal input signal if that signal were perfectly recreated from the stored digital output data. Virtually all the noise in the output spectrum is created either by the act of digitizing or by the A/D converter itself.

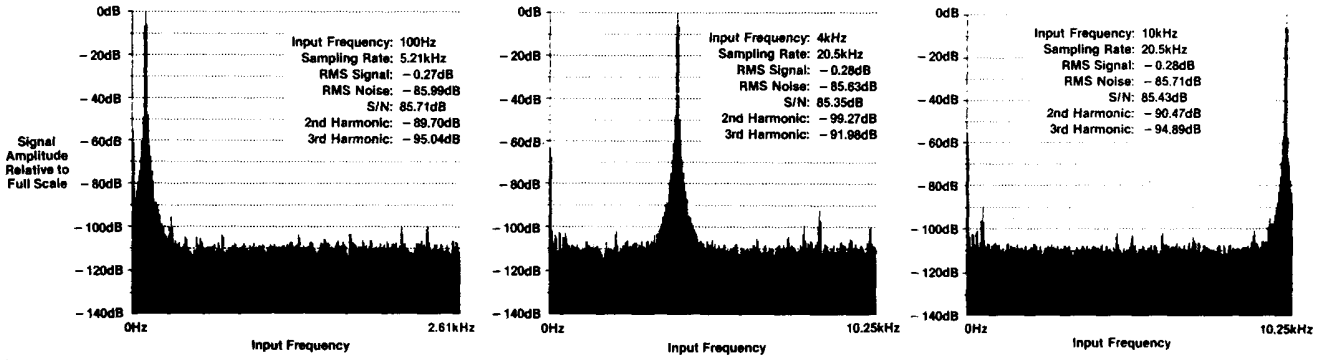
## Effective Resolution v.s. Input Frequency
## MN5290, 40μsec, 16-Bit A/D

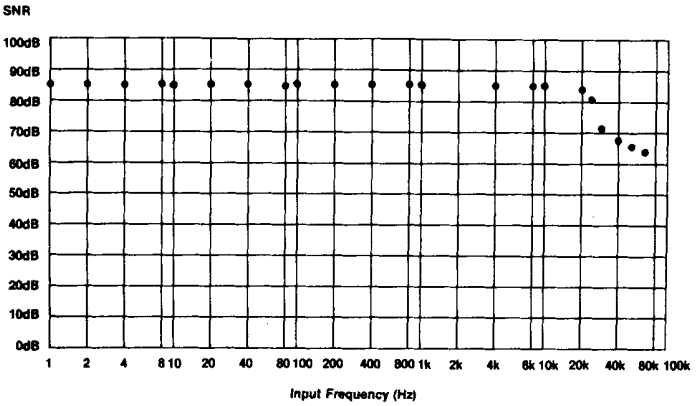



The three spectra above are each the result of averaging 10 512-pt FFT's run on an MN5290 type 16-bit A/D converter without a companion T/H amplifier. The input signal frequencies are respectively 4Hz, 40Hz, and 400Hz. The A/D's conversion time is approximately 40μsec, and the sampling rates are respectively 171Hz, 171Hz, and 1.18kHz. The accompanying plot shows the rapid (6dB/octave) degradation of SNR (effective resolution) with increasing input frequency when SA type A/D converters are used to digitize dynamically changing input signals without the aid of a T/H amplifier.

## Effective Resolution v.s. Input Frequency
## MN6290, 20kHz, 16-Bit, Sampling A/D




The three spectra above are each the result of averaging 10 512-pt FFT's run on an MN6290 16-bit sampling A/D. The input signal frequencies are respectively 100Hz, 4kHz, and 10kHz, and the sample/convert rates are respectively 5.21kHz, 20.5kHz, and 20.5kHz. The accompanying plot shows that MN6290's internal T/H amplifier enables the device to maintain near ideal SNR independent of increasing input frequencies. The aperture jitter of the T/H is small enough to maintain SNR for undersampled input frequencies, i.e., for frequencies greater than 10kHz.

In a simple, first- order analysis, the noise in the output spectrum of an A/D converter can be traced to three sources. All three of these noise sources have the potential to manifest themselves as quasi-random relative-accuracy errors in any single A/D conversion of a static signal and subsequently, the potential to manifest themselves as broadband noise in a series of conversions of a dynamically changing signal. Two of these noise sources (quantization noise and converter noise) are effectively constant and do not change with input-signal frequency. The third (aperture noise) usually varies linearly as a function of input-signal frequency, basically doubling whenever input frequency doubles.

Digitizing an analog signal quantizes it or "rounds it off". Digitizing or quantizing an analog signal with a 16-bit A/D effectively "rounds off" the signal to one of 65,536 possible discrete levels. This rounding off produces an inherent accuracy error in that the digital output no longer **exactly** represents the analog input. If one has an ideal A/D converter with all other accuracy-error sources driven to zero, the actual value of rounding-off error or quantization error can be as small as zero or as large as ± ½LSB from conversion to conversion. In a single conversion of a static input signal, quantization error is simply an accuracy error. It is impossible for a given conversion of an unknown signal to be more accurate than ± ½LSB. In a series of conversions of a dynamically changing signal, actual instantaneous quantization error varies from sample to sample and manifests itself as broadband noise. In the output spectrum, this noise limits the theoretically achievable signal-to-noise ratio to the following:

$$\text{Ideal SNR} = (6.02n + 1.76)\text{dB}$$

n = number of bits

For an ideal 16-bit A/D, the theoretical noise floor in a 512-point FFT occurs around − 122dB, and the theoretical SNR is 98dB. For an ideal 14-bit A/D and a 512-point FFT, the numbers are − 110dB and 86dB respectively.

The second type of single-conversion accuracy error that manifests itself as broadband noise in the output spectrum results from the actual noise of the A/D converter. This "converter noise" is frequently referred to as "transition noise" and manifests itself, among other ways, by allowing certain fixed, static, input signals to produce either of two adjacent output codes from one conversion to the next. In most A/D converters, the transition from one given digital output code to the next (or vice versa) does not always occur at exactly the same analog input voltage. The "transition voltage" varies from conversion to conversion, and this "transition noise" (the band of adjacent-code uncertainty) is normally on the order of ± 1/10 to ± 1/3 LSB. It is caused by broadband noise and timing jitter in the A/D's constituent components (especially its comparator and reference circuit). In a single given A/D conversion, transition noise adds (or subtracts) to the device's static differential linearity error. Again, this phenomenon will manifest itself as an accuracy error in any single conversion and as noise in any series of conversions of a changing input signal.

This second noise component should be thought of simply as the "converter noise". Recall that quantization noise is a result of the digitizing process, and it limits SNR to some theoretical value. Its effect is independent of the type or kind of A/D converter used. Converter noise is a function of how "noisy" a selected A/D converter may be, and it reduces actual measured SNR's to a level something below ideal. Hence MN6290/6291 K and T models guarantee 84dB and not 86dB initial room-temperature SNR.

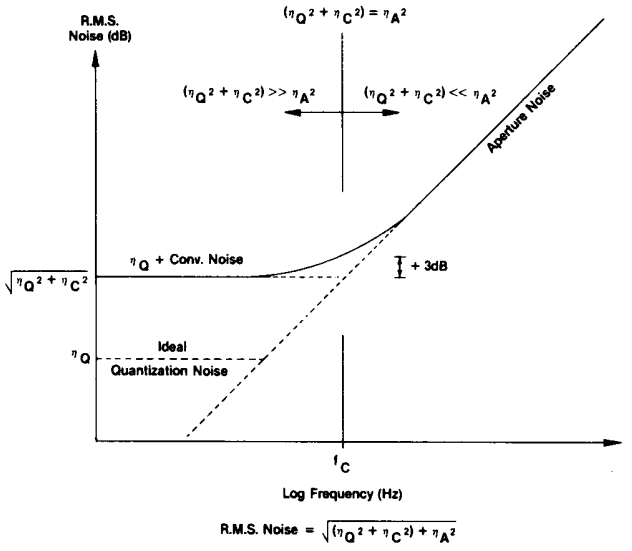
The third component of A/D converter noise derives from the fact that SA type A/D converters (without companion T/H amplifiers) cannot accurately convert dynamically changing input signals. Because of the nature of the technique of successive approximations, it is imperative that A/D's using this technique maintain a stable input signal during their conversion (aperture) time. Slew rates in excess of (± ½LSB) / (conversion time) can cause accuracy errors in any individual conversion. In a series of conversions of a sinusoidal signal, the slew rate varies from sample to sample, and the consequent aperture (slew-rate) errors manifest themselves as broadband noise.

This third component of A/D noise is effectively eliminated by MN6290/6291's internal T/H. The T/H's ability to instantaneously freeze the slewing input signal (limited only by the T/H's aperture jitter) and hold it constant results in the A/D seeing a series of d.c. signals and not the sinusoid itself. MN6290/6291's ability to maintain SNR over its full input bandwidth (up to the "Nyquist frequency" or ½ the sampling rate) is the result of the T/H's ability to limit the overall noise to the quantization noise plus the noise inherent in the A/D.

The plots on the previous page demonstrate that an A/D without a companion T/H is effectively incapable of accurately converting analog input signals above some critical frequency (slew rate) and that the A/D's SNR or "effective resolution" deteriorates at approximately 6dB/octave above that frequency. Basically, the A/D's quantization and converter noise remain constant while its aperture noise doubles each time the input frequency doubles.

MN6290/6291's internal T/H effectively eliminates aperture noise allowing the A/D to maintain "low-frequency SNR" as the actual input frequency increases.

The plot below graphically illustrates the principles we have been discussing and focuses on A/D converter noise, not on SNR. Earlier, we discussed quantization noise ($\eta_Q$), converter noise ($\eta_C$) and slew rate or aperture noise ($\eta_A$) and how each individually contributes to broadband noise in an A/D's output spectrum. The plot below illustrates the relationship of the three noise components to each other as input signal frequency increases. If each of the three noise components is expressed in r.m.s. terms, the total r.m.s. noise ($\eta_T$) of the A/D converter will be the square root of the sum of the squares of its respective noise components. The vertical axis of the plot is the r.m.s. value of the A/D converter's total noise expressed in dB. The horizontal axis is the frequency of the A/D's analog input signal plotted on a logarithmic scale.



At very low (approaching d.c.) input frequencies, aperture noise effectively makes no contribution, and the total noise is equal to the r.m.s. summation of quantization noise and converter noise. As explained earlier, this initial noise level is greater than that solely attributable to theoretical quantization noise and is a constant term in the total r.m.s. noise equation shown below.

$\eta_Q$ = Quantization Noise

$\eta_C$ = Converter Noise

$\eta_A$ = Aperture Noise (slew-rate noise)

$$\eta_{Total\ (r.m.s.)} = \sqrt{\eta_{Q\ (r.m.s.)}^2 + \eta_{C\ (r.m.s.)}^2 + \eta_{A\ (r.m.s.)}^2}$$

$$\eta_T = \sqrt{(\eta_Q^2 + \eta_C^2) + \eta_A^2}$$

Constant Term

Frequency Dependent Term

As the input frequency increases, aperture noise begins to come into play. At some critical frequency ($f_C$), the contribution made by aperture noise will be equal to that of quantization plus converter noise, and the total noise will have risen 3dB above its initial value (SNR drops 3dB). Aperture noise increases 6dB for every octave increase in input frequency and eventually overwhelms the other noise components which have essentially remained constant. If one maintains a constant input level while increasing the input signal frequency through many decades, the plot of the A/D's SNR vs. input frequency should look like the inverse of the noise plot shown on the previous page. This is demonstrated in the actual plots of SNR vs. frequency for the MN5290 shown previously.

## ORDERING INFORMATION

| Part Number | Input Voltage Range | | Specified Temperature Range | No Missing Codes | Integral Linearity | Minimum Sampling Rate | Minimum Input Bandwidth | SNR | Harmonics |
|---|---|---|---|---|---|---|---|---|---|
| | Unipolar | Bipolar | | | | | | | |
| MN6290J | 0 to +10V | ±5V | 0°C to +70°C | 13 Bits | ±0.006%FSR | 20kHz | 10kHz | 80dB | –85dB |
| MN6290K | 0 to +10V | ±5V | 0°C to +70°C | 14 Bits | ±0.003%FSR | 20kHz | 10kHz | 84dB | –88dB |
| MN6290S | 0 to +10V | ±5V | –55°C to +125°C | 13 Bits | ±0.006%FSR | 20kHz | 10kHz | 80dB | –85dB |
| MN6290S/B | 0 to +10V | ±5V | –55°C to +125°C | 13 Bits | ±0.006%FSR | 20kHz | 10kHz | 80dB | –85dB |
| MN6290T | 0 to +10V | ±5V | –55°C to +125°C | 14 Bits | ±0.003%FSR | 20kHz | 10kHz | 84dB | –88dB |
| MN6290T/B | 0 to +10V | ±5V | –55°C to +125°C | 14 Bits | ±0.003%FSR | 20kHz | 10kHz | 84dB | –88dB |
| MN6291J | N.A. | ±10V | 0°C to +70°C | 13 Bits | ±0.006%FSR | 20kHz | 10kHz | 80dB | –85dB |
| MN6291K | N.A. | ±10V | 0°C to +70°C | 14 Bits | ±0.003%FSR | 20kHz | 10kHz | 84dB | –88dB |
| MN6291S | N.A. | ±10V | –55°C to +125°C | 13 Bits | ±0.006%FSR | 20kHz | 10kHz | 80dB | –85dB |
| MN6291S/B | N.A. | ±10V | –55°C to +125°C | 13 Bits | ±0.006%FSR | 20kHz | 10kHz | 80dB | –85dB |
| MN6291T | N.A. | ±10V | –55°C to +125°C | 14 Bits | ±0.003%FSR | 20kHz | 10kHz | 84dB | –88dB |
| MN6291T/B | N.A. | ±10V | –55°C to +125°C | 14 Bits | ±0.003%FSR | 20kHz | 10kHz | 84dB | –88dB |

Contact factory for availability of CH device types.