Micro Networks
An Integrated Circuit Systems Company

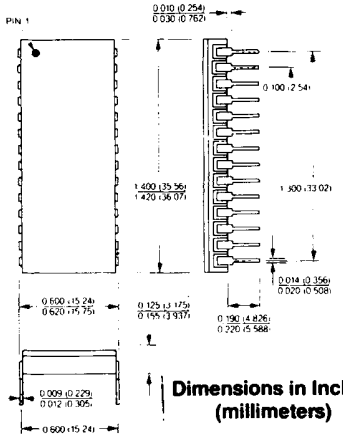
MN6400

50kHz, 16-bit Self-Calibrating Sampling A/D Converter

FEATURES

- Self-Calibrating A/D Provides True 16-bit Performance
- 50kHz Sampling Rate with Inherent T/H Function
- 16-Bit No-Missing-Codes Guaranteed Over Full Operating Temperature Range
- Complete Contains:
  - T/H Function
  - Analog Input Buffer
  - Reference
  - Timing and Control Logic
  - μP Interface
  - Parallel Data Bus Driver
- ±1LSB Integral Linearity
- 88dB SNR, −98dB Harmonics
- 785mW Maximum Power Consumption
- Fully specified 0°C to +70°C (J and K Models) or −55°C to +125°C (S Model)
- MIL-PRF-38534 Screening Optional

28 PIN SIDE-BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN6400 is a complete self-calibrating, 16-bit, 50kHz Sampling A/D converter. Each Sampling A/D contains an inherent T/H function, analog input buffer amplifier, reference, timing and control logic circuitry, microprocessor interface and parallel data bus driver making it the most complete device of its kind. These Sampling A/D converters are packaged in small, 28-pin, side-brazed, double-wide DIPs. The inherent T/H function allows these devices to accurately sample and digitize dynamically changing analog input signals at rates up to 50kHz. The package, including all of the functions, is smaller than that of most stand-alone 16-bit A/Ds. Each device is fully tested using contemporary FFT (Fast Fourier Transform) technology and guarantees frequency-domain performance — no more guesswork in converting time-domain specifications (linearity, accuracy, etc.) into frequency-domain performance.

The MN6400 offers four analog input voltage ranges (0 to +5V, 0 to +10V, ±5V and ±10V) whose Bipolar and Unipolar operation is digitally controlled. These devices may be operated from the internal clock, or for critical sampling applications, these devices may be operated from a low-jitter crystal clock circuit. Serial output data is provided synchronized to the serial clock output. The internal parallel data bus driver with its 3-state outputs enables the MN6400 to connect directly to system data buses without loading concerns.

The MN6400 offers users three electrical performance grades (J, K, and S models) and two operating temperature ranges (0°C to +70°C and −55°C to +125°C). In addition, S models are available with environmental stress screening or fully compliant with MIL-PRF-38534, class H requirements.

MN6400 50kHz 16-Bit SELF-CALIBRATING SAMPLING A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN6400 J, K	0°C to +70°C
MN6400 S	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+V_{CC}, Pin 15)	0 to +16.5 Volts
−15V Supply (−V_{CC}, Pin 14)	0 to −16.5 Volts
+5V Supply (+V_{DD}, Pin 21)	−0.3 to +6.0 Volts
Digital Inputs:	
(Pins 10, 11, 12, 13, 22, 23, 24)	−0.3 to +V_{DD} +0.3V
Analog Inputs: (Pins 17, 18)	±V_{CC}

ORDERING INFORMATION

PART NUMBER **MN6400S/B CH**

Select suffix J, K, or S for desired performance and specified temperature range.
Add "/B" suffix to "S" model for Environmental Stress Screening.
Add "CH" to "S/B" models for MIL-PRF-38534 compliant devices.

DESIGN SPECIFICATIONS (T_A = +25°C, ±V_{CC} = ±15V, +V_{DD} = +5V unless otherwise specified) (Note 10)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges: 5V Input		0 to +5		Volts
		−5 to +5		Volts
10V Input		0 to +10		Volts
		−10 to +10		Volts
Input Impedance: 5V Input		5		kΩ
10V Input		10		kΩ
DIGITAL INPUTS				
Logic Levels: Logic "1"	+2.0			Volts
Logic "0"			+0.8	Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V)			±10	μA
Logic "0" (V_{IL} = +0.4V)			±10	μA
DIGITAL OUTPUTS				
Logic Levels: Logic "1" (I_{OH} = +6.0mA)	+3.9	+4.3		Volts
Logic "0" (I_{OL} = −6.0mA)		+0.16	+0.26	Volts
3-State Leakage Current			±10	μA
INTERNAL REFERENCE				
Reference Output: Voltage (Note 11)	+4.45	+4.5	+4.55	Volts
Drift		±3	±10	ppm/°C
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±V_{CC} Supply	±11.4	±15	±16.5	Volts
+V_{DD} Supply	+4.5	+5	+5.5	Volts
Power Supply Rejection: +V_{CC} Supply		±.0001	±.001	%FS/%VS
−V_{CC} Supply		±.0001	±.001	%FS/%VS
+V_{DD} Supply		±.0001	±.001	%FS/%VS
Current Drains: +V_{CC} Supply		+5	+13	mA
−V_{CC} Supply		−20	−31	mA
+V_{DD} Supply		+14	+25	mA
Power Consumption		445	785	mW

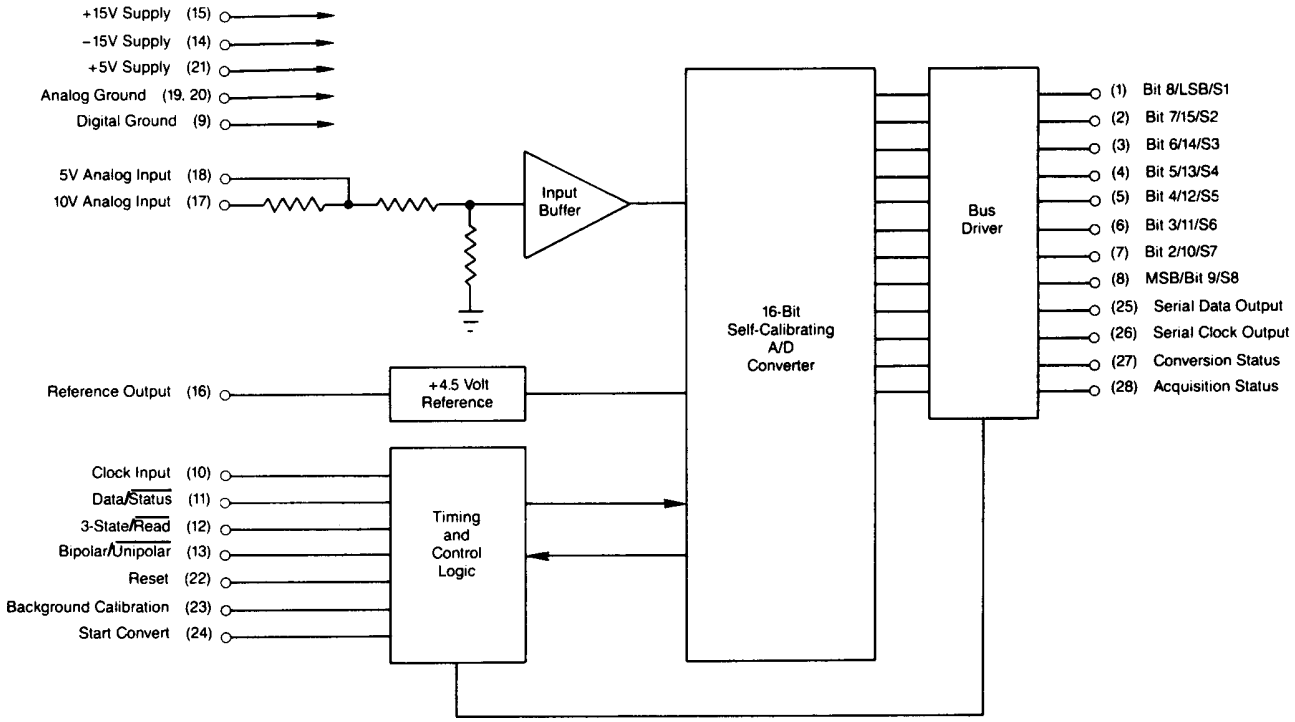
SPECIFICATION NOTES:

1. External Master Clock frequency set to 4MHz, synchronous sampling mode and background calibration disabled.
2. Specification listed applies after calibration at any temperature within the specified temperature range.
3. Specification listed applies over the specified temperature range after initial calibration at 25°C.
4. Specification listed applies after calibration at 25°C.
5. Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output changes from 0000 0000 0000 0000 to 0000 0000 0000 0001 when operating the MN6400 on a unipolar range.
6. Bipolar zero error is defined as the difference between the ideal and actual input voltage at which the digital output changes from 0111 1111 1111 1111 to 1000 0000 0000 0000 when operating the MN6400 on a bipolar range.
7. Full scale absolute accuracy error includes offset, gain, linearity, noise, and all other errors. Full scale absolute accuracy specifications apply at positive full scale for unipolar input ranges and at both positive and negative full scales for bipolar input ranges. Full scale absolute accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output changes from 1111 1111 1111 1110 to 1111 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 0001 to 0000 0000 0000 0000 transition for bipolar input ranges.
8. This parameter represents the rms-signal-to-rms-noise ratio in the output spectrum (excluding harmonics) with a full scale analog input sine wave (0dB) at the specified frequencies.
9. This parameter represents the peak-to-peak non-fundamental component (harmonic or spurious, inband or out of band) in the output spectrum.
10. External Master Clock frequency set to 4MHz and operated in the synchronous sampling mode.
11. Reference output is to be bypassed to Analog Ground with a 10μF capacitor in parallel with an 0.1μF capacitor. Reference must not be used for applications circuits without buffering.

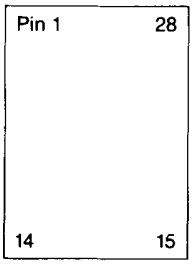
PERFORMANCE SPECIFICATIONS (Typical at +25°C, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V unless otherwise indicated) (Note 1)

STATIC CHARACTERISTICS	MN6400J	MN6400K	MN6400S	UNITS
Integral Linearity Error (Max) (Note 2) Integral Linearity Error (Max) (Note 3)	±0.0015 ±0.0022	±0.0015 ±0.0015	±0.0015 ±0.0022	%FSR %FSR
Minimum Resolution for Which No Missing Codes is Guaranteed (Note 3)	16	16	16	Bits
Unipolar Offset Error (Notes 4, 5) Initial (Maximum) Drift (Maximum)	 ±0.03 ±4	 ±0.02 ±2.5	 ±0.03 ±4	 %FSR ppm of FSR/°C
Bipolar Zero Error (Notes 4, 6) Initial (Maximum) Drift (Maximum)	 ±0.03 ±4	 ±0.02 ±2.5	 ±0.03 ±4	 %FSR ppm of FSR/°C
Full Scale Accuracy Error (Notes 4, 7) Initial (Maximum) Drift (Maximum)	 ±0.1 ±15	 ±.05 ±10	 ±0.1 ±15	 %FSR ppm of FSR/°C
DYNAMIC CHARACTERISTICS				
Minimum Guaranteed Sampling Rate Maximum A/D Conversion Time	50 16.25	50 16.25	50 16.25	kHz µsec
Signal-to-Noise Ratio (Notes 3, 8): Initial (+25°C): 1kHz Full Scale Input (Minimum) 12kHz Full Scale Input (Minimum) T_{min} to T_{max}: 1kHz Full Scale Input (Minimum) 12kHz Full Scale Input (Minimum)	 85 81 83 79	 88 84 85 82	 85 81 83 79	 dB dB dB dB
Harmonics and Spurious Noise (Notes 3, 9): Initial (+25°C): 1kHz Full Scale Input (Maximum) 12kHz Full Scale Input (Maximum) T_{min} to T_{max}: 1kHz Full Scale Input (Maximum) 12kHz Full Scale Input (Maximum)	 −96 −90 −94 −88	 −98 −92 −96 −90	 −96 −90 −94 −88	 dB dB dB dB

BLOCK DIAGRAM



PIN DESIGNATIONS



1	Bit 8 /Bit 16 (LSB) or S1	28	Acquisition Status
2	Bit 7 /Bit 15 or S2	27	Conversion Status
3	Bit 6 /Bit 14 or S3	26	Serial Clock Output
4	Bit 5 /Bit 13 or S4	25	Serial Data Output
5	Bit 4 /Bit 12 or S5	24	Start Convert
6	Bit 3 /Bit 11 or S6	23	Background Calibration
7	Bit 2 /Bit 10 or S7	22	Reset
8	Bit 1 (MSB)/Bit 9 or S8	21	+5V Supply ($+V_{DD}$)
9	Digital Ground	20	Analog Ground
10	Clock Input	19	Analog Ground
11	Data/$\overline{\text{Status}}$	18	5V Analog Input
12	3-State/$\overline{\text{Read}}$	17	10V Analog Input
13	Bipolar/$\overline{\text{Unipolar}}$	16	Reference Output (+4.5V)
14	−15V/−12V Supply ($-V_{CC}$)	15	+15V/+12V Supply ($+V_{CC}$)

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION — The MN6400 is a 16-bit Sampling A/D converter containing an inherent, user-transparent T/H function and features self-calibration, μP-interface logic and an 8-bit parallel data bus driver. Self-calibration and the inherent T/H function enable the MN6400 to accurately sample and digitize dynamically changing analog input signals at a 50kHz throughput rate.

The MN6400 is designed to operate from ±12 or ±15V and +5V power supplies and an external or internally generated Master Clock. After power-up, the MN6400 must be reset by bringing Reset (pin 22) high for a minimum of 100nsec. Bringing Reset high clears the internal logic circuitry while returning Reset low initiates a full calibration cycle. Full calibration cycles require 1,441,020 Master Clock cycles (360.255msec with external 4MHz Master Clock applied). Conversion Status (pin 27) is high during calibration and returns low when complete.

After calibration, conversions can be initiated by the falling edge of Start Convert. The signal applied to Start Convert (pin 24) must remain low for a minimum of one Master Clock cycle plus 50nsec. This translates into 300nsec with the use of an external 4MHz clock. Start Convert must return high prior to the end of the conversion cycle (65 clock cycles, 16.25μsec with 4MHz clock) to allow sufficient time for the next sample to be acquired.

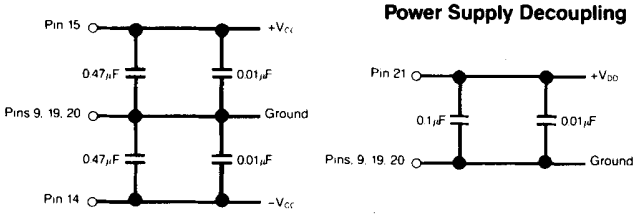
With the conversion complete, output data and converter status information may be read using various combinations of input control lines. Both serial and parallel data are available. Serial data is available at Serial Data Output (pin 25) and is syncronous and valid with the rising edges of Serial Data Clock Output (pin 26). Serial data is presented MSB first, and is only available during the conversion cycle. Parallel data is available in two 8-bit bytes. Once a conversion is complete and Data/$\overline{\text{Status}}$ (pin 11) is set high, parallel output data is read by bringing 3-State/$\overline{\text{Read}}$ low. MSB-byte data (MSB-bit 8) is first to be presented to data output lines (pins 1-8). Toggling 3-State/$\overline{\text{Read}}$ (that is, to bring it high and then low again) presents LSB-byte data. Output data lines are in the high-impedance state when 3-State/$\overline{\text{Read}}$ is high.

In addition to conversion data, device status information can also be accessed via the 8-bit data lines (pins 1-8). Status information is presented when Data/$\overline{\text{Status}}$ is set low. A detailed description of the types of status information which is provided and the pin locations of this information appear in the section labeled Parallel Output Pin Description - Status Information.

POWER SUPPLIES AND LAYOUT — The MN6400 is powered from standard supply voltages of +12/15V (pin 15), −12/15V (pin 14) and +5V (pin 21). The analog ground (pins 19,20) and digital ground (pin 9) are separated to minimize analog and digital circuit interaction. The analog ground is internally used as a reference point, therefore it should be used as the system analog ground reference point. Care must be taken to reduce the system noise to a level below the MN6400's high-resolution conversion capability.

It is recommended that the power supplies be decoupled in the following manner. The +12/15V and −12/15V supplies should be bypassed with a 0.01 μF capacitor in parallel with a 0.47 μF capacitor to analog ground. The +5V supply, which powers both analog and digital internal circuitry, should be bypassed with a 0.1 μF capacitor in parallel with a 0.01 μF capacitor to analog ground. The optimum value decoupling capacitors to use may vary depending on the users system noise characteristics.

Power Supply Decoupling



DEVICE CALIBRATION — The MN6400 features two user-controlled self-calibration modes of operation. Self-calibration insures optimum performance at any temperature and at any time throughout the lifetime of the device. Self-calibration also eliminates the need for additional external circuitry to maintain operation of the device within specification.

The first mode of calibration is called reset, and its initiation is controlled with Reset (pin 22). A reset calibration must be performed after the device is powered-up, and can be repeated optionally after the device reaches its operating temperature. The required initial reset is initiated by strobing the Reset pin high for a minimum of 100 nsec. When Reset is brought high, internal logic clears. When Reset returns low, a single full calibration lasting 1,441,020 master clock cycles begins (360.255 msec w/ 4 MHz clock). During reset the Conversion Status (pin 27) output will be in a high state, and will fall low upon completion of calibration.

The reset mode of calibration can be initiated by either hardware using a power-up reset circuit or by software in microprocessor control applications. Care must be taken to avoid an inadvertent reset brought about by bringing 3-State/Read (12), Data/Status (pin 11) and Start Convert (pin 24) low simultaneously.

The second mode of calibration is called background calibration, which is activated by either tying Background Calibration (pin 23) to digital ground or bringing Background Calibration and 3-State/Read (pin 12) both low. This mode differs from reset calibration in that a fractional portion of the total calibration time is added to the end of each conversion. After 72,051 conversions, the calibration cycle is complete. The conversion time of the device when background calibration is active is extended by 20 master clock cycles (5μsec w/4 MHz clock). Except for the decrease in throughput rate, the background calibration mode is transparent to the user.

MASTER CLOCK — The MN6400 operates from a master clock that can be supplied externally or generated internally depending upon the signal applied to Clock Input (pin 10). A logic low on this pin will activate the 2 MHz minimum internal clock. Optionally, the user can supply a TTL or CMOS system clock with a maximum frequency of 4MHz (100kHz minimum) to the Clock Input. All device timing characteristics scale to the master clock frequency. The internal oscillator exhibits relatively high jitter compared to crystal oscillators, which may affect performance in some sampling applications.

INITIATING CONVERSIONS — A falling edge on the Start Convert (pin 24) digital input will set the device into the hold mode and initiate a conversion cycle. The Start Convert input must remain low for a minimum of one master clock cycle plus 50 nsec (300 nsec w/4 MHz clock). It must return high before the minimum conversion time of 65 clock cycles (16.25μsec w/4 MHz clock) to allow sufficient time for acquisition of the next sample.

T/H ACQUISITION — The MN6400 is a sampling A/D converter, therefore it requires a finite amount of time to accurately acquire an analog input signal before performing a conversion. At the completion of a conversion, signalled by the falling of Conversion Status (pin 27), the device automatically enters the acquisition mode and begins to track the analog input. A minimum acquisition time of six master clock cycles plus 2.25μsec (3.75μsec w/4 MHz clock) is required to acquire the input signal. When sufficient time has elapsed after a conversion for the acquisition of the input signal, the Acquisition Status (pin 28) output will fall low. It returns high on initiation of a new conversion cycle. When driving the MN6400 from a high source impedance, the necessary acquisition time should be extended to allow for the resultant increase in the input settling time constant.

The MN6400's acquisition circuitry operates from a delayed and divided down internal clock frequency of ¼ times the master clock. If sampling is not synchronized to this internal clock, a sample will be synchronously taken but may not be converted until up to four master clock cycles later (1μsec w/ 4 MHz clock). In other words, when Start Convert goes low and is not synchronous with the internal clock, a maximum of four master clock cycles may occur before Conversion Status goes high. This asynchronous uncertainty adds these four master clock cycles plus 235 nsec of internal clock delay (1.235μsec w/4 MHz clock) to the conversion time.

When performing an asynchronous sampling operation, the device can operate at 69 master clock cycles plus 235 nsec for conversion and six master clock cycles plus 2.25 μsec for acquisition for a total of 75 master clock cycles plus 2.485μsec (21.235μsec w/4 MHz clock). This corresponds to a 47.1 kHz maximum throughput rate. Although the sample is asynchronously converted, the sample itself is taken synchronously upon the falling edge of Start Convert. This is particularly important to users in DSP applications.

To synchronize the sampling operation to the internal clock, the Acquisition Status (pin 28) output can be connected to the Start Convert (pin 24) input. The Acquisition Status output is synchronized to the internal clock, thereby eliminating the sampling uncertainty and enabling device operation at 65 master clock cycles for conversion and 15 master clock cycles for acquisition for a total of 80 master clock cycles (20μsec w/4 MHz clock). This corresponds to a 50kHz maximum throughput rate.

ANALOG INPUTS — The MN6400 can be operated in four user-selectable input voltage range configurations. They are 0 to +5V, ±5V, 0 to +10V and ±10V. The 5V Analog Input (pin 18) is used for 5V full scale analog inputs, and the 10V Analog Input (pin 17) is used for 10V full scale analog inputs. Selection of a unipolar or bipolar input transfer function is made with the Bipolar/Unipolar digital input (pin 13). A logic high on this pin selects a bipolar transfer function of analog input voltage between −Full Scale and +Full Scale. A logic low on this pin selects a unipolar transfer function of analog input voltages between 0V and +Full Scale.

The unipolar voltage ranges are digitally represented at the output in Straight Binary format. An all zero's output corresponds to 0V at the input, and an all ones output corresponds to +FS range voltage at the input. The bipolar voltage ranges produce digital outputs in Offset Binary format. An all zeros output corresponds to an analog input voltage of −Full Scale Range.

The MN6400 contains an input buffer configured to condition the analog input signal for optimum acquisition and conversion performance. Additional signal-conditioning circuitry meeting 16 bit performance levels can be used to drive the analog inputs.

REFERENCE OUTPUT — The MN6400 contains an internal +4.5V low drift precision reference. This reference voltage appears at Reference Output (pin 16) to allow for the attachment of a 0.1μF capacitor in parallel with a 10μF tantalum capacitor. These capacitors are required to allow the reference to exhibit a low output impedance throughout the frequency range of device operation. The optimum value for these capacitors will vary depending on the master clock frequency being used.

It is recommended not to use the Reference Output pin for any additional circuitry requirements. If absolutely necessary, the Reference Output can be buffered and used to fulfill additional circuitry requirements.

DIGITAL OUTPUTS — The MN6400 supplies converted data and device status information on outputs capable of driving system bus connections directly. The device presents both parallel data in an 8-bit MSB/LSB byte format and serial data with serial clock output. In addition to digital output data, device status information can be read via the parallel data bit outputs.

The information present on the 8-bit bus is controlled by the state of Data/Status (pin 11). When high, converted data can be read on the bus.

When low, the status register can be read on the bus. Converted data appears on the bus in parallel MSB/LSB byte format. A read operation is executed by bringing the 3-State/Read (pin 12) input low. The first read operation following a conversion will bring the bus out of the 3-state condition and present the eight MSBs (MSB on pin 8 through bit 8 on pin 1). On the second read operation following a conversion, executed by bringing 3-State/Read back high and then low again, the eight LSBs will be presented (Bit 9 on pin 8 through LSB on pin 1). On subsequent reads before the next conversion is complete, the MSB/LSB byte will toggle. Data is valid after a delay of 100 nsec from the falling edge of Conversion Status, and remains valid until the next Conversion Status falling edge.

PARALLEL OUTPUT PIN DESCRIPTION

PIN#	MSB BYTE	LSB BYTE	STATUS BIT	STATUS INFORMATION
1	Bit 8	LSB	S1	Same as Conversion Status (pin 27).
2	Bit 7	Bit 15	S2	Reserved for factory use.
3	Bit 6	Bit 14	S3	LSB/MSB byte indicates which data byte will appear on next read operation.
4	Bit 5	Bit 13	S4	Same as Acquisition Status (pin 28)
5	Bit 4	Bit 12	S5	Reserved for factory use.
6	Bit 3	Bit 11	S6	Tracking — high when device is tracking the input.
7	Bit 2	Bit 10	S7	Converting — high when the device is converting the input.
8	MSB	Bit 9	S8	Calibrating — high when the device is calibrating.

Device status information can be read on the bus whenever Data/Status is low. Status bit pin locations and definitions appear under the section labeled Parallel Output Pin Description.

Converted data is available in Serial format (MSB first) at the Serial Data Output (pin 25). Serial data is present at the output when it is determined during conversion. Serial data is valid and can be latched with the rising edge of Serial Clock Output (pin 26).

The Conversion Status (pin 27) and Acquisition Status (pin 28) outputs provide the user with device status information detailed in the Pin Description Section. Conversion Status will remain low for four master clock cycles if 3-State/Read is held low. These status outputs along with the serial data and clock output are not 3-stateable, but have direct bus-driver output capability.

PIN DESCRIPTION

POWER SUPPLY CONNECTIONS

Pin Designation	Function
+15V/+12V Supply (+V_{CC}, Pin 15)	Positive analog power supply. Devices will operate from nominal +12V or +15V supplies.
−15V/−12V Supply (−V_{CC}, Pin 14)	Negative analog power supply. Devices will operate from nominal −12V or −15V supplies.
+5V Supply (+V_{DD}, Pin 21)	Positive digital and analog power supply. Device operates from nominal +5V.

ANALOG INPUTS

Pin Designation	Function
10V Analog Input (Pin 17)	When in the Unipolar mode (Bipolar/Unipolar is set to logic "0"), accepts 0 to +10V analog input signals. When in Bipolar mode (Bipolar/Unipolar is set to logic "1"), accepts ±10V analog input signals.
5V Analog Input (Pin 18)	When in the Unipolar mode (Bipolar/Unipolar is set to logic "0"), accepts 0 to +5V analog input signals. When in the Bipolar mode (Bipolar/Unipolar is set to logic "1"), accepts ±5V analog input signals.

ANALOG OUTPUTS

Pin Designation	Function
Reference Output (Pin 16)	Provides reference voltage of +4.5V to be bypassed to Analog Ground with an external 10μF tantalum capacitor in parallel with a 0.1μF ceramic disk capacitor. Use of this reference in additional circuit applications requires the use of an external, low-input-current buffer amplifier.

DIGITAL OUTPUTS

Pin Designation	Function
Parallel Data Outputs (Pins 1-8)	3-stated output byte offers converted data in MSB-byte, LSB-byte format or status register information (S1-S8). Data Output is controlled by 3-State/Read input and is dependent on state of Data/Status. See Digital Output section for a detailed description of data output pins.
Serial Data Output (Pin 25)	Presents serial output data valid on the rising edge of Serial Clock Output (pin 26). Data is available only during conversion, and is presented MSB first.
Serial Clock Output (Pin 26)	Provides clock edges to facilitate latching of serial output data.
Conversion Status (Pin 27)	Indicates A/D Converter status. When high (Logic "1"), the A/D is busy in a conversion or calibration cycle. Returns high on first read cycle or the beginning of new conversion cycle.
Acquisition Status (Pin 28)	Indicates the status of the inherent T/H function. When high (Logic "1"), the device is acquiring and tracking the analog input signal. Acquisition Status returns low indicating that sufficient time has elapsed since the last conversion and a new conversion can be initiated. The device continues to track until a conversion is initiated.

DIGITAL INPUTS

Pin Designation	Function
Clock Input (Pin 10)	Connect external Master Clock signal (TTL or CMOS level @ 4MHz maximum) or tie to digital ground to activate the internal clock.
Data/Status (Pin 11)	Selects the type of information presented to digital output pins 1-8 during the read operation. When high (Logic "1"), convertered output data is presented to parallel output pins 1-8; when low (Logic "0"), status register is presented to digital outputs.
3-State/Read (Pin 12)	Selects state of digital data output pins 1-8. When high (Logic "1"), data is disabled and parallel output bits are in high-impedance state. When low (Logic "0"), converted data (Data/Status, pin 11=Logic "1") or status information (Data/Status, pin 11=Logic "0") is presented to output pins 1-8. Converted output data is presented in two 8-bit bytes. The first read cycle (initiated when 3-State/Read =Logic "0") after a conversion is complete enables the MSB data byte. Toggling 3-State/Read (that is bringing it high and then low again) enables the LSB data byte. The MSB and LSB data bytes will toggle on subsequent read operations. Additionally, falling edges latch the state of Background Calibration.

Pin Designation	Function
Bipolar/$\overline{\text{Unipolar}}$ (Pin 13)	Selects either unipolar or bipolar operation. When high (Logic "1"), the analog input range is bipolar (–Full Scale to +Full Scale). When low (Logic "0"), the analog input range is unipolar (0V to +Full Scale). The analog input voltage pins select the desired full scale range.
Reset (Pin 22)	Controls the device clear and calibration cycle initiation. When brought high, the internal logic is cleared. When returned low (after being high for 100nsec minimum) a full device calibration cycle is initiated.
Background Calibration (Pin 23)	Controls the device active calibration mode. When latched low by the falling edge of 3-State/$\overline{\text{Read}}$, the device interleaves conversions and calibration cycles. Full calibration cycle extends over 72,051 conversions at the expense of extended conversion time.
Start Convert (Pin 24)	The falling edge of Start Convert initiates the conversion cycle. Start Convert must remain low for at least one Master Clock cycle plus 50nsec.

DIGITAL OUTPUT CODING

ANALOG INPUT		DIGITAL OUTPUT
UNIPOLAR RANGES	BIPOLAR RANGES	MSB LSB
+F.S.	+F.S.	1111 1111 1111 1111
+F.S. – 3/2LSB	+F.S. – 3/2LSB	1111 1111 1111 111Ø*
+½F.S. + ½LSB	+½LSB	1000 0000 0000 000Ø*
+½F.S. – ½LSB	–½LSB	ØØØØ ØØØØ ØØØØ ØØØØ*
+½F.S. – 3/2LSB	–3/2LSB	0111 1111 1111 111Ø*
+½LSB	–F.S. + ½LSB	0000 0000 0000 000Ø*
0	–F.S.	0000 0000 0000 0000

CODING NOTES:

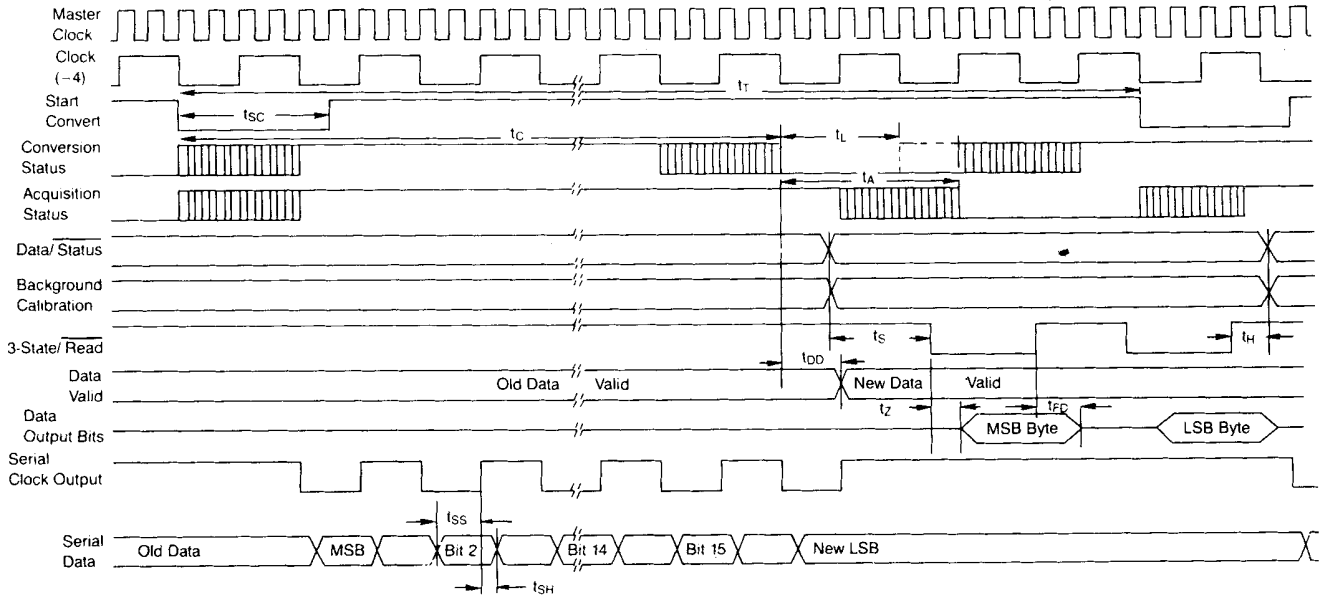
1. For 5 Volt FSR, 1LSB for 16 Bits =76.3μV.
2. For 10 Volt FSR, 1LSB for 16 Bits =152.6μV.
3. For 20 Volt FSR, 1LSB for 16 Bits =305.2μV.
4. For unipolar ranges, the coding is straight binary.
5. For bipolar ranges, the coding is offset binary.

*Analog voltages listed are the theoretical values for the transition indicated. Ideally, with the MN6400 continuously converting, the output bits indicated as Ø will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

INPUT RANGE SELECTION

PIN CONNECTIONS	ANALOG INPUT VOLTAGE RANGE			
	0 to +5V	0 to +10V	±5V	±10V
Connect Pin 18 to	Analog Input	Open	Analog Input	Open
Connect Pin 17 to	Open	Analog Input	Open	Analog Input
Connect Pin 13 to Logic	"0"	"0"	"1"	"1"

TIMING DIAGRAM



Notes: 1. Clock (÷4) signal not available. For reference only.
2. Asynchronous mode shown. In synchronous mode, timing uncertainty (, four Master Clock Cycles) is eliminated.

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}, $\pm V_{CC} = \pm 15V$, $+V_{DD} = +5V$, $C_L = 50pF$)

PARAMETER	MIN	TYP	MAX	UNITS
Master Clock Frequency (f_{CLK}): Internal External	 2 0.1		 4	 MHz MHz
Start Convert Pulse Width (t_{SC}) (Note 1)	$1/f_{CLK} + 0.05$		t_C	μsec
Conversion Time (t_C) (Note 1)	$65/f_{CLK}$		$69/f_{CLK} + 0.235$	μsec
Acquisition Time (t_A) (Note 1)			$6/f_{CLK} + 2.25$	μsec
Throughput Time (t_T): (Note 1) Synchronous Sampling Asynchronous Sampling			 $80/f_{CLK}$ $75/f_{CLK} + 2.485$	 μsec μsec
Set Up Times (t_S): Background Calibration, Data/Status to 3-State/Read Low	20	10		nsec
Hold Times (t_H): 3-State/Read High to Background Calibration, Data/Status Invalid	50	30		nsec
Data Delay Time (t_{DD})		40	100	nsec
Data Access Time (t_Z): 3-State/Read Low to Data Valid		80	150	nsec
Output Float Delay (t_{FD}): 3-State/Read High to Output High Z		80	150	nsec
Set Up Times (t_{SS}): Serial Data to Serial Clock Output Rising Edge (Note 1)	$2/f_{CLK} - 0.05$	$2/f_{CLK}$		μsec
Hold Time (t_{SH}): Serial Clock Output Rising Edge to Serial Data (Note 1)	$2/f_{CLK} - 0.1$	$2/f_{CLK}$		μsec

Notes: 1. Formulas in the table are for f_{CLK} expressed in MHz.