

**MOSEL VITELIC****V54C3128(16/80/40)4V(BGA)****PRELIMINARY****128Mbit SDRAM****3.3 VOLT, BGA PACKAGE****8M X 16****16M X 8****32M X 4**

	<b>6</b>	<b>7PC</b>	<b>7</b>	<b>8PC</b>
System Frequency ( $f_{CK}$ )	166 MHz	143 MHz	143 MHz	125 MHz
Clock Cycle Time ( $t_{CK3}$ )	6 ns	7 ns	7 ns	8 ns
Clock Access Time ( $t_{AC3}$ ) $\overline{CAS}$ Latency = 3	5.4 ns	5.4 ns	5.4 ns	6 ns
Clock Access Time ( $t_{AC2}$ ) CAS Latency = 2	5.4 ns	5.4 ns	6 ns	6 ns

**Features**

- 4 banks x 2Mbit x 16 organization
- 4 banks x 4Mbit x 8 organization
- 4 banks x 8Mbit x 4 organization
- High speed data transfer rates up to 166 MHz
- Full Synchronous Dynamic RAM, with all signals referenced to clock rising edge
- Single Pulsed  $\overline{RAS}$  Interface
- Data Mask for Read/Write Control
- Four Banks controlled by BA0 & BA1
- Programmable  $\overline{CAS}$  Latency: 2, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
  - 1, 2, 4, 8 for Sequential Type
  - 1, 2, 4, 8 for Interleave Type
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Random Column Address every CLK (1-N Rule)
- Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 4096 cycles/64 ms
- Available in 60 Pin WBGA
- LVTTTL Interface
- Single +3.3 V  $\pm$ 0.3 V Power Supply

**Description**

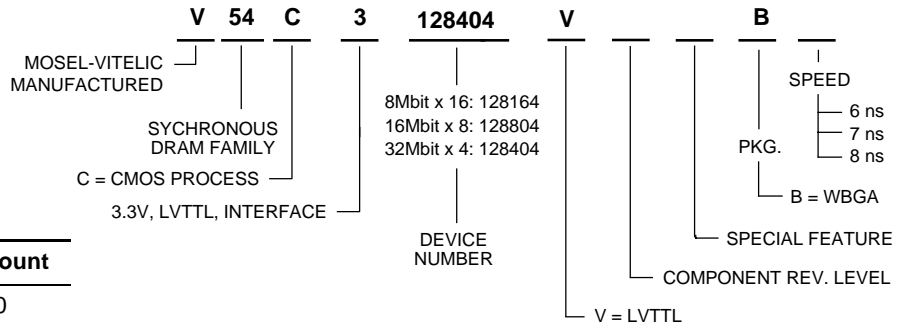
The V54C3128(16/80/40)4V(BGA) is a four bank Synchronous DRAM organized as 4 banks x 2Mbit x 16, 4 banks x 4Mbit x 8, or 4 banks x 8Mbit x 4. The V54C3128(16/80/40)4V(BGA) achieves high speed data transfer rates up to 166 MHz by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleaved fashion allows random access operation to occur at higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 166 MHz is possible depending on burst length,  $\overline{CAS}$  latency and speed grade of the device.

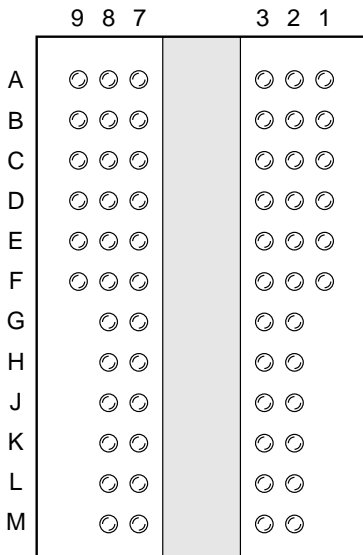
**Device Usage Chart**

Operating Temperature Range	Package Outline	Access Time (ns)				Power		Temperature Mark
	B	6	7PC	7	8PC	Std.	L	
0°C to 70°C	•	•	•	•	•	•	•	Blank



Description	Pkg.	Pin Count
WBGA	B	60

**60 Pin WBGA PIN CONFIGURATION  
Top View**



9	8	7	x16	3	2	1
VCCQ	DQ0	VCC	A	VSS	DQ15	VSSQ
DQ1	VSSQ	DQ2	B	DQ13	VCCQ	DQ14
DQ3	VCCQ	DQ4	C	DQ11	VSSQ	DQ12
DQ5	VSSQ	DQ6	D	DQ9	VCCQ	DQ10
DQ7	NC	NC	E	NC	NC	DQ8
NC	VCC	LDQM	F	UDQM	VSS	Vref
	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	G	NC	CLK	
	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	H	CKE	A12	
	BA0	BA1	J	A9	A11	
	A10/AP	A0	K	A7	A8	
	A1	A2	L	A5	A6	
	A3	VCC	M	VSS	A4	

9	8	7	x8	3	2	1
VCCQ	DQ1	VCC	A	VSS	DQ7	VSSQ
NC	VSSQ	DQ1	B	DQ6	VCCQ	NC
NC	VCCQ	DQ2	C	DQ5	VSSQ	NC
NC	VSSQ	DQ3	D	DQ4	VCCQ	NC
NC	NC	NC	E	NC	NC	NC
NC	VCC	NC	F	DQM	VSS	Vref
	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	G	NC	CLK	
	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	H	CKE	A12	
	BA0	BA1	J	A9	A11	
	A10/AP	A0	K	A7	A8	
	A1	A2	L	A5	A6	
	A3	VCC	M	VSS	A4	

9	8	7	x4	3	2	1
VCCQ	NC	VCC	A	VSS	NC	VSSQ
NC	VSSQ	DQ0	B	DQ3	VCCQ	NC
NC	VCCQ	NC	C	NC	VSSQ	NC
NC	VSSQ	DQ1	D	DQ2	VCCQ	NC
NC	NC	NC	E	NC	NC	NC
NC	VCC	NC	F	DQM	VSS	Vref
	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	G	NC	CLK	
	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	H	CKE	A12	
	BA0	BA1	J	A9	A11	
	A10/AP	A0	K	A7	A8	
	A1	A2	L	A5	A6	
	A3	VCC	M	VSS	A4	

**Capacitance\***

T<sub>A</sub> = 0 to 70°C, V<sub>CC</sub> = 3.3 V ± 0.3 V, f = 1 Mhz

Symbol	Parameter	Max.	Unit
C <sub>I1</sub>	Input Capacitance (A0 to A11)	3.8	pF
C <sub>I2</sub>	Input Capacitance RAS, CAS, WE, CS, CLK, CKE, DQM	3.8	pF
C <sub>IO</sub>	Output Capacitance (I/O)	6	pF
C <sub>CLK</sub>	Input Capacitance (CLK)	3.5	pF

\*Note: Capacitance is sampled and not 100% tested.

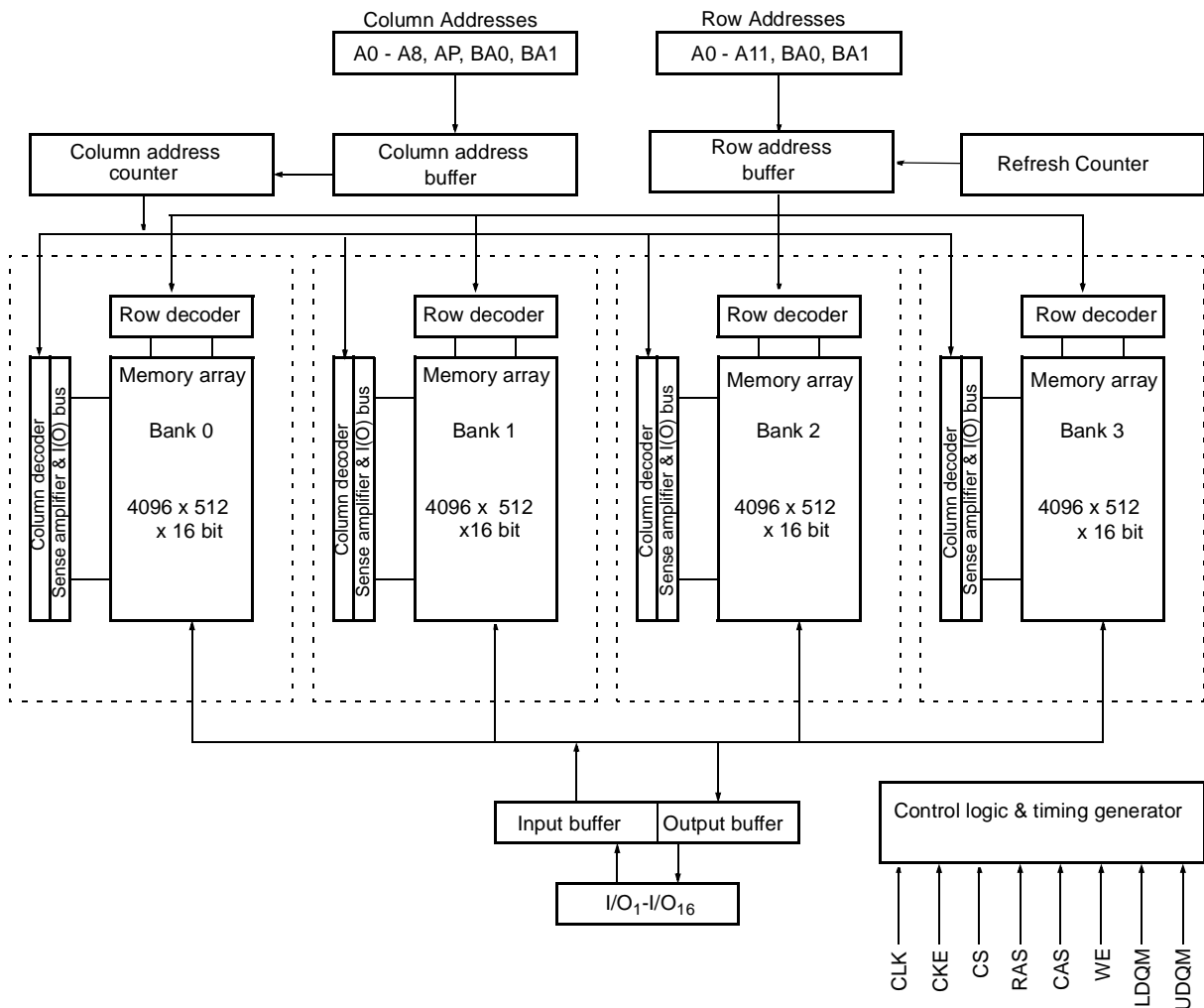
**Absolute Maximum Ratings\***

Operating temperature range ..... 0 to 70 °C  
 Storage temperature range ..... -55 to 150 °C  
 Input/output voltage ..... -0.3 to (V<sub>CC</sub>+0.3) V  
 Power supply voltage ..... -0.3 to 4.6 V  
 Power dissipation ..... 1 W  
 Data out current (short circuit) ..... 50 mA

\*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

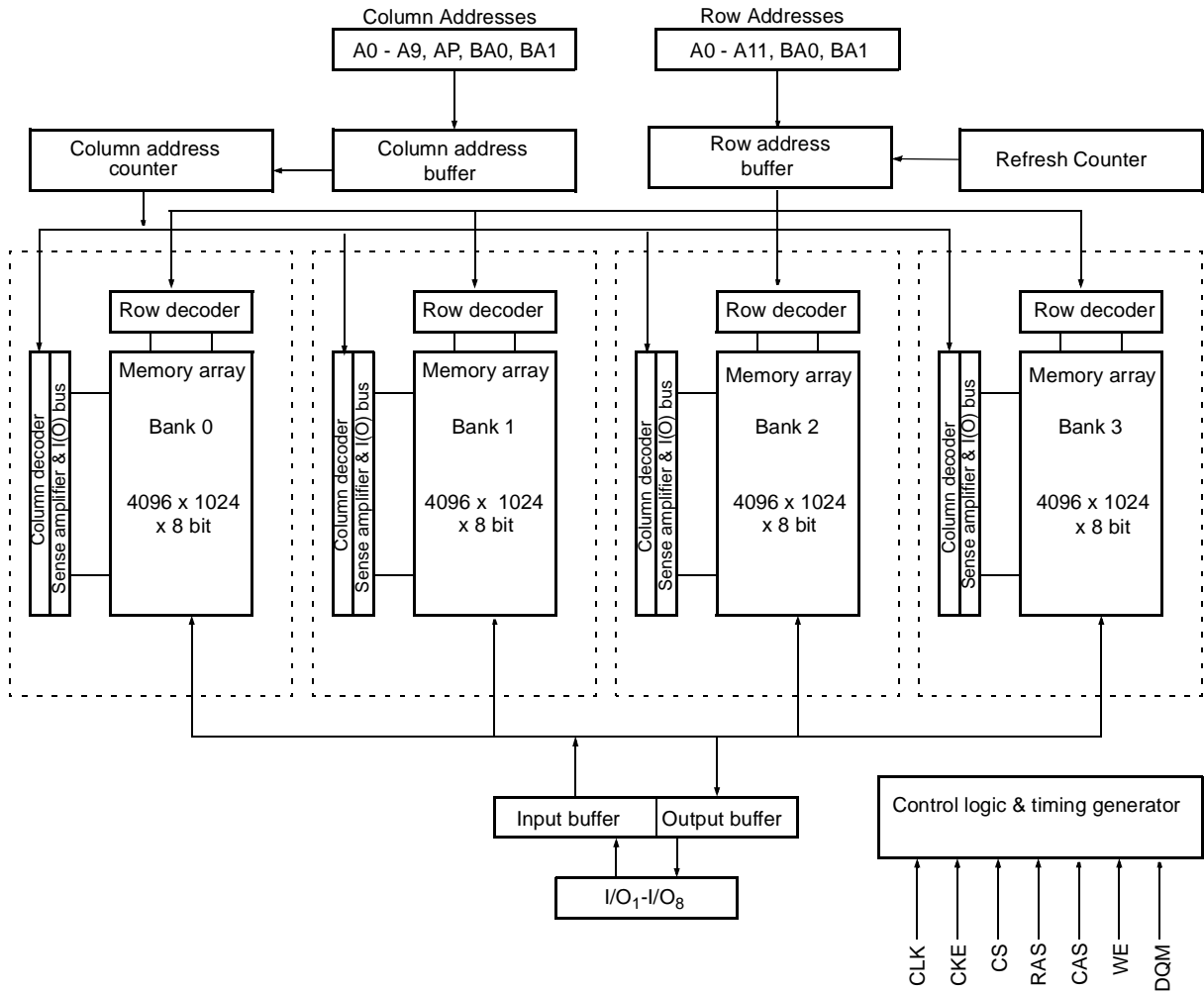
**Block Diagram**

**x16 Configuration**



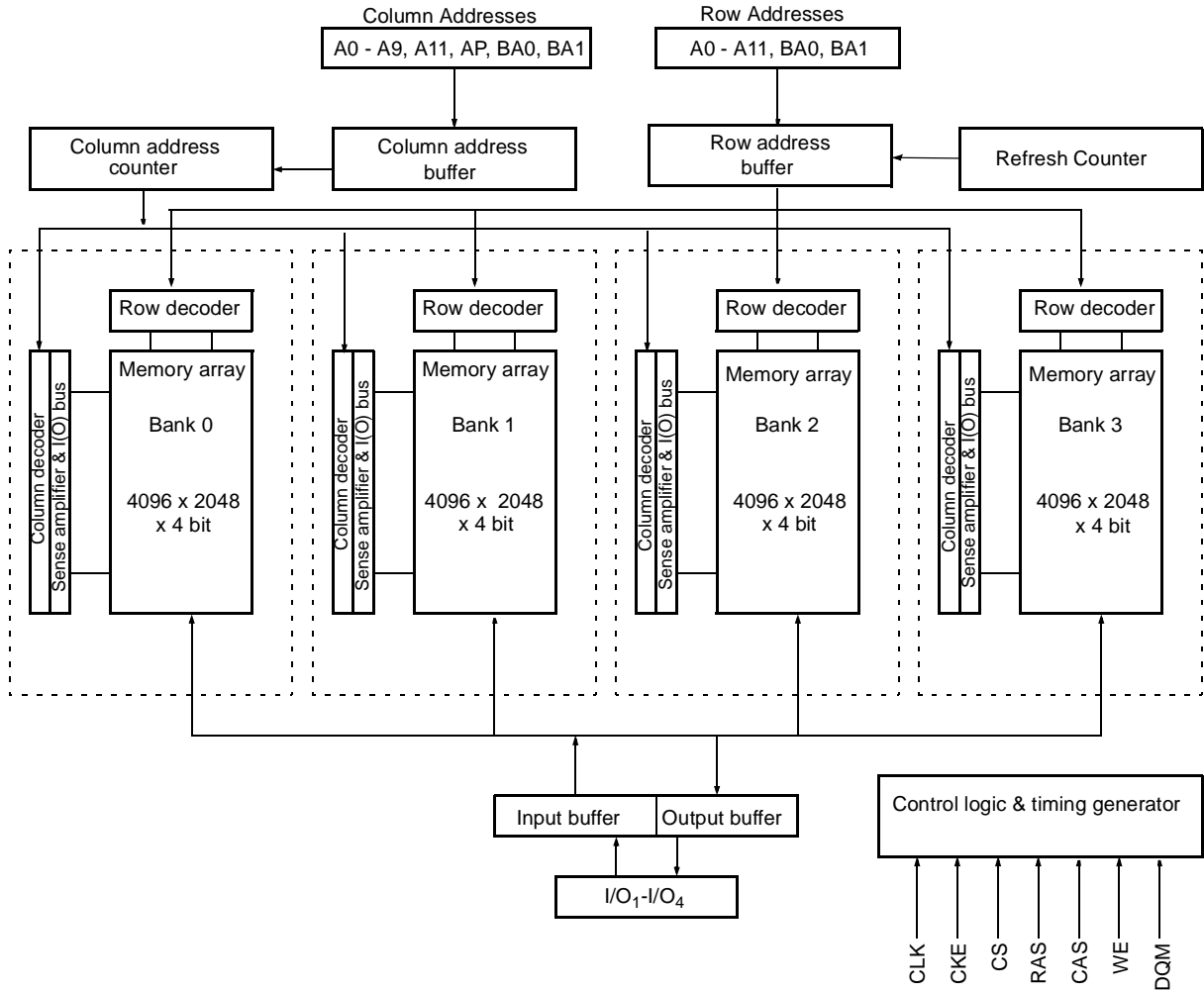
**Block Diagram**

**x8 Configuration**



**Block Diagram**

**x4 Configuration**



**Signal Pin Description**

Pin	Type	Signal	Polarity	Function
CLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$ , $\overline{RAS}$ , and $\overline{WE}$ define the command to be executed by the SDRAM.
A0 - A11	Input	Level	—	<p>During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge.</p> <p>During a Read or Write command cycle, A0-An defines the column address (CA0-CAn) when sampled at the rising clock edge. CAn depends from the SDRAM organization:</p> <ul style="list-style-type: none"> <li>• 32M x 4 SDRAM CA0–CA9, CA11.</li> <li>• 16M x 8 SDRAM CA0–CA9.</li> <li>• 8M x 16 SDRAM CA0–CA8.</li> </ul> <p>In addition to the column address, A10(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10(=AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will BA0 and BA1 are used to define which bank to precharge.</p>
BA0, BA1	Input	Level	—	Selects which bank is to be active.
DQx	Input Output	Level	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
LDQM UDQM	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.
VCC, VSS	Supply			Power and ground for the input buffers and the core logic.
VCCQ VSSQ	Supply	—	—	Isolated power supply and ground for the output buffers to provide improved noise immunity.

**Operation Definition**

All of SDRAM operations are defined by states of control signals  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ , and DQM at the positive edge of the clock. The following list shows the thruth table for the operation commands.

Operation	Device State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A0-9, A11	A10	BS0 BS1
Row Activate	Idle <sup>3</sup>	H	X	L	L	H	H	X	V	V	V
Read	Active <sup>3</sup>	H	X	L	H	L	H	X	V	L	V
Read w/Autoprecharge	Active <sup>3</sup>	H	X	L	H	L	H	X	V	H	V
Write	Active <sup>3</sup>	H	X	L	H	L	L	X	V	L	V
Write with Autoprecharge	Active <sup>3</sup>	H	X	L	H	L	L	X	V	H	V
Row Precharge	Any	H	X	L	L	H	L	X	X	L	V
Precharge All	Any	H	X	L	L	H	L	X	X	H	X
Mode Register Set	Idle	H	X	L	L	L	L	X	V	V	V
No Operation	Any	H	X	L	H	H	H	X	X	X	X
Device Deselect	Any	H	X	H	X	X	X	X	X	X	X
Auto Refresh	Idle	H	H	L	L	L	H	X	X	X	X
Self Refresh Entry	Idle	H	L	L	L	L	H	X	X	X	X
Self Refresh Exit	Idle (Self Refr.)	L	H	H	X	X	X	X	X	X	X
				L	H	H	X				
Power Down Entry	Idle Active <sup>4</sup>	H	L	H	X	X	X	X	X	X	X
				L	H	H	X				
Power Down Exit	Any (Power Down)	L	H	H	X	X	X	X	X	X	X
				L	H	H	L				
Data Write/Output Enable	Active	H	X	X	X	X	X	L	X	X	X
Data Write/Output Disable	Active	H	X	X	X	X	X	H	X	X	X

**Notes:**

1. V = Valid , x = Don't Care, L = Low Level, H = High Level
2. CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are provided.
3. These are state of bank designated by BS0, BS1 signals.
4. Power Down Mode can not entry in the burst cycle.

***Power On and Initialization***

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all VCC and VCCQ pins must be built up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power on voltage must not exceed  $VCC+0.3V$  on any of the input pins or VCC supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200  $\mu s$  is required followed by a precharge of both banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required. These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

***Programming the Mode Register***

The Mode register designates the operation mode at the read or write cycle. This register is divided into 4 fields. A Burst Length Field to set the length of the burst, an Addressing Selection bit to program the column access sequence in a burst cycle (interleaved or sequential), a CAS Latency Field to set the access time at clock cycle and a Operation mode field to differentiate between normal operation (Burst read and burst Write) and a special Burst Read and Single Write mode. The mode set

operation must be done before any activate command after the initial power up. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in pre-charged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of  $\overline{RAS}$ ,  $\overline{CAS}$ , and  $\overline{WE}$  at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

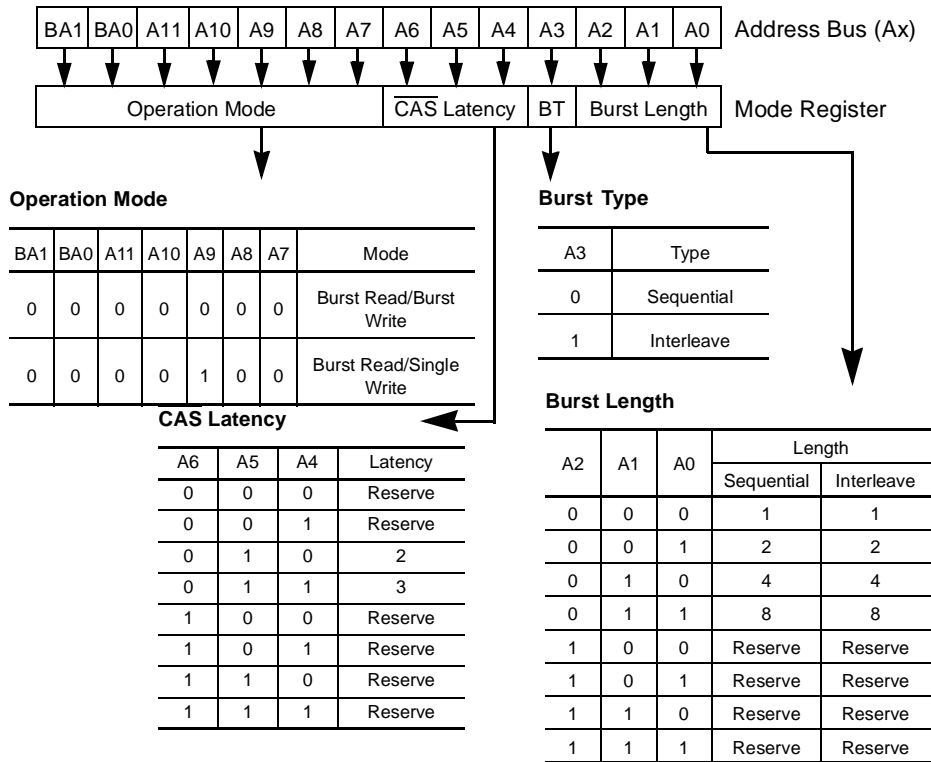
***Read and Write Operation***

When  $\overline{RAS}$  is low and both  $\overline{CAS}$  and  $\overline{WE}$  are high at the positive edge of the clock, a RAS cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A  $\overline{CAS}$  cycle is triggered by setting  $\overline{RAS}$  high and  $\overline{CAS}$  low at a clock timing after a necessary delay,  $t_{RCD}$ , from the  $\overline{RAS}$  timing.  $\overline{WE}$  is used to define either a read ( $\overline{WE} = H$ ) or a write ( $\overline{WE} = L$ ) at this stage.

SDRAM provides a wide variety of fast access modes. In a single CAS cycle, serial data read or write operations are allowed at up to a 125 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4, 8. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the CAS timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is '2', then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.



**Address Input for Mode Set (Mode Register Operation)**



Similar to the page mode of conventional DRAM's, burst read or write accesses on any column address are possible once the RAS cycle latches the sense amplifiers. The maximum  $t_{RAS}$  or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycles is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies

with an operation change from a read to a write is possible by exploiting DQM to avoid bus contention. When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be done between different pages.

**Burst Length and Sequence:**

Burst Length	Starting Address (A2 A1 A0)	Sequential Burst Addressing (decimal)	Interleave Burst Addressing (decimal)
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	001	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	010	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	011	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	100	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	101	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	110	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	111	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0

**Refresh Mode**

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the CAS-before-RAS refresh of conventional DRAMs. All of banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when RAS and CAS are held low and CKE and WE are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum tRC time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the Self Refresh mode is available. It enters the mode when RAS, CAS, and CKE are low and WE is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one tRC delay is required prior to any access command.

**DQM Function**

DQM has two functions for data I/O read and write operations. During reads, when it turns to "high" at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency tDQZ ). It also provides

a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency tDQW = zero clocks).

**Power Down**

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (trp) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can't remain in Power Down mode longer than the Refresh period (tref) of the device. Exit from this mode is performed by taking CKE "high". One clock delay is required for mode entry and exit.

**Auto Precharge**

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the CAS timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the Read with Auto-Precharge function is initiated. The SDRAM automatically enters the precharge operation one clock before the last data out for CAS latencies 2, two clocks for CAS latencies 3 and three clocks for CAS latencies 4. If CA10 is high when a Write Command is issued, the Write

with **Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to  $t_{WR}$  (Write recovery time) after the last data in.

**Precharge Command**

There is also a separate precharge command available. When **RAS** and **WE** are low and **CAS** is high at a clock timing, it triggers the precharge operation. Three address bits, **BA0**, **BA1** and **A10** are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for **CAS** latency = 2, two clocks before the last data out for **CAS** latency = 3. Writes require a time delay  $t_{wr}$  from the last data out to apply the precharge command.

Bank Selection by Address Bits:

A10	BA0	BA1	
0	0	0	Bank 0
0	0	1	Bank 1
0	1	0	Bank 2
0	1	1	Bank 3
1	X	X	all Banks

**Burst Termination**

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid I/O contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the I/O pins before the Burst Stop Command is registered will be written to the memory.

**Recommended Operation and Characteristics for LV-TTL**

$T_A = 0$  to  $70$  °C;  $V_{SS} = 0$  V;  $V_{CC}, V_{CCQ} = 3.3$  V  $\pm$  0.3 V

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input high voltage	$V_{IH}$	2.0	$V_{CC}+0.3$	V	1, 2
Input low voltage	$V_{IL}$	-0.3	0.8	V	1, 2
Output high voltage ( $I_{OUT} = -4.0$ mA)	$V_{OH}$	2.4	-	V	
Output low voltage ( $I_{OUT} = 4.0$ mA)	$V_{OL}$	-	0.4	V	
Input leakage current, any input ( $0$ V < $V_{IN}$ < $3.6$ V, all other inputs = $0$ V)	$I_{I(L)}$	-5	5	$\mu$ A	
Output leakage current (DQ is disabled, $0$ V < $V_{OUT}$ < $V_{CC}$ )	$I_{O(L)}$	-5	5	$\mu$ A	

**Note:**

- All voltages are referenced to  $V_{SS}$ .
- $V_{IH}$  may overshoot to  $V_{CC} + 2.0$  V for pulse width of < 4ns with 3.3V.  $V_{IL}$  may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

**Operating Currents** ( $T_A = 0$  to  $70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ )  
 (Recommended Operating Conditions unless otherwise noted)

Symbol	Parameter & Test Condition		Max.			Unit	Note
			-6	-7 / -7PC	-8PC		
ICC1	Operating Current $t_{RC} = t_{RCMIN}$ , $t_{RC} = t_{CKMIN}$ Active-precharge command cycling, without Burst Operation	1 bank operation	190	170	150	mA	7
ICC2P	Precharge Standby Current in Power Down Mode	$t_{CK} = \text{min.}$	1.5	1.5	1.5	mA	7
ICC2PS	$\overline{CS} = V_{IH}$ , $CKE \leq V_{IL(max)}$	$t_{CK} = \text{Infinity}$	1	1	1	mA	7
ICC2N	Precharge Standby Current in Non-Power Down Mode	$t_{CK} = \text{min.}$	55	45	35	mA	
ICC2NS	$\overline{CS} = V_{IH}$ , $CKE \geq V_{IL(max)}$	$t_{CK} = \text{Infinity}$	5	5	5	mA	
ICC3N	No Operating Current $t_{CK} = \text{min}$ , $\overline{CS} = V_{IH(min)}$ bank ; active state ( 4 banks)	$CKE \geq V_{IH(MIN.)}$	65	55	45	mA	
ICC3P		$CKE \leq V_{IL(MAX.)}$ (Power down mode)	10	10	10	mA	
ICC4	Burst Operating Current $t_{CK} = \text{min}$ Read/Write command cycling		130	110	90	mA	7,8
ICC5	Auto Refresh Current $t_{CK} = \text{min}$ Auto Refresh command cycling		270	250	210	mA	7
ICC6	Self Refresh Current Self Refresh Mode, $CKE \leq 0.2\text{V}$		1.5	1.5	1.5	mA	
		L-version	800	800	800	$\mu\text{A}$	

**Notes:**

7. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of  $t_{CK}$  and  $t_{RC}$ . Input signals are changed one time during  $t_{CK}$ .
8. These parameter depend on output loading. Specified values are obtained with output open.

**AC Characteristics** <sup>1,2,3</sup>

T<sub>A</sub> = 0 to 70 °C; V<sub>SS</sub> = 0 V; V<sub>DD</sub> = 3.3 V ± 0.3 V, t<sub>T</sub> = 1 ns

#	Symbol	Parameter	Limit Values								Unit	Note
			-6		-7PC		-7		-8PC			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		

**Clock and Clock Enable**

1	t <sub>CK</sub>	Clock Cycle Time CAS Latency = 3 CAS Latency = 2	6 7.5	- -	7 7.5	- -	7 10	- -	8 10	- -	s ns ns	
2	t <sub>CK</sub>	Clock Frequency CAS Latency = 3 CAS Latency = 2	- -	166 133	- -	143 133	- -	143 100	- -	125 100	MHz MHz	
3	t <sub>AC</sub>	Access Time from Clock CAS Latency = 3 CAS Latency = 2	- -	5.4 5.4	- -	5.4 5.4	- -	5.4 6	- -	6 6	ns ns	2, 4
4	t <sub>CH</sub>	Clock High Pulse Width	2.5	-	2.5	-	2.5	-	3	-	ns	
5	t <sub>CL</sub>	Clock Low Pulse Width	2.5	-	2.5	-	2.5	-	3	-	ns	
6	t <sub>T</sub>	Transition Tim	0.3	1.2	0.3	1.2	0.3	1.2	0.5	10	ns	

**Setup and Hold Times**

7	t <sub>IS</sub>	Input Setup Time	1.5	-	1.5	-	1.5	-	2	-	ns	5
8	t <sub>IH</sub>	Input Hold Time	0.8	-	0.8	-	0.8	-	1	-	ns	5
9	t <sub>CKS</sub>	Input Setup Time	1.5	-	1.5	-	1.5	-	2	-	ns	5
10	t <sub>CKH</sub>	CKE Hold Time	0.8	-	0.8	-	0.8	-	1	-	ns	5
11	t <sub>RSC</sub>	Mode Register Set-up Time	12	-	14	-	14	-	16	-	ns	
12	t <sub>SB</sub>	Power Down Mode Entry Time	0	6	0	7	0	7	0	8	ns	

**Common Parameters**

13	t <sub>RCD</sub>	Row to Column Delay Time	12	-	15	-	15	-	20	-	ns	6
14	t <sub>RP</sub>	Row Precharge Time	15	-	15	-	15	-	20	-	ns	6
15	t <sub>RAS</sub>	Row Active Time	40	100K	42	100K	42	100K	45	100k	ns	6
16	t <sub>RC</sub>	Row Cycle Time	60	-	60	-	60	-	60	-	ns	6
17	t <sub>R RD</sub>	Activate(a) to Activate(b) Command Period	12	-	14	-	14	-	16	-	ns	6
18	t <sub>CCD</sub>	CAS(a) to CAS(b) Command Period	1	-	1	-	1	-	1	-	CLK	

**Refresh Cycle**

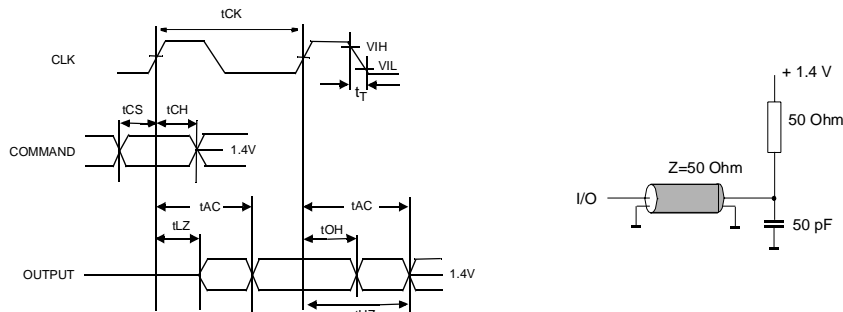
19	t <sub>REF</sub>	Refresh Period (4096 cycles)	-	64	-	64	-	64	-	64	ms	
20	t <sub>SREX</sub>	Self Refresh Exit Time	1	-	1	-	1	-	1	-	CLK	

**AC Characteristics** (Cont'd)

#	Symbol	Parameter	Limit Values								Unit	Note
			-6		-7PC		-7		-8PC			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
<b>Read Cycle</b>												
21	t <sub>OH</sub>	Data Out Hold Time	3	-	3	-	3	-	3	-	ns	2
22	t <sub>LZ</sub>	Data Out to Low Impedance Time	1	-	1	-	1	-	0	-	ns	
23	t <sub>HZ</sub>	Data Out to High Impedance Time	3	6	3	7	3	7	3	8	ns	7
24	t <sub>DQZ</sub>	DQM Data Out Disable Latency	-	2	-	2	-	2	-	2	CLK	
<b>Write Cycle</b>												
25	t <sub>WR</sub>	Write Recovery Time	2	-	2	-	2	-	2	-	CLK	
26	t <sub>DQW</sub>	DQM Write Mask Latency	0	-	0	-	0	-	0	-	CLK	

**Notes for AC Parameters:**

- For proper power-up see the operation section of this data sheet.
- AC timing tests have V<sub>IL</sub> = 0.8V and V<sub>IH</sub> = 2.0V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V<sub>IH</sub> and V<sub>IL</sub>. All AC measurements assume t<sub>T</sub> = 1 ns with the AC output load circuit shown in Figure 1.



**Figure 1.**

- If clock rising time is longer than 1 ns, a time (t<sub>T</sub>/2 - 0.5) ns has to be added to this parameter.
- If t<sub>T</sub> is longer than 1 ns, a time (t<sub>T</sub> - 1) ns has to be added to this parameter.
- These parameter account for the number of clock cycle and depend on the operating frequency of the clock, as follows:

*the number of clock cycle = specified value of timing period (counted in fractions as a whole number)*

Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t<sub>RC</sub> is satisfied once the Self Refresh Exit command is registered.

- Referenced to the time which the output achieves the open circuit condition, not to output voltage levels

***Timing Diagrams***

1. Bank Activate Command Cycle
2. Burst Read Operation
3. Read Interrupted by a Read
4. Read to Write Interval
  - 4.1 Read to Write Interval
  - 4.2 Minimum Read to Write Interval
  - 4.3 Non-Minimum Read to Write Interval
5. Burst Write Operation
6. Write and Read Interrupt
  - 6.1 Write Interrupted by a Write
  - 6.2 Write Interrupted by Read
7. Burst Write & Read with Auto-Precharge
  - 7.1 Burst Write with Auto-Precharge
  - 7.2 Burst Read with Auto-Precharge
8. Burst Termination
  - 8.1 Termination of a Burst Write Operation
  - 8.2 Termination of a Burst Write Operation
9. AC- Parameters
  - 9.1 AC Parameters for a Write Timing
  - 9.2 AC Parameters for a Read Timing
10. Mode Register Set
11. Power on Sequence and Auto Refresh (CBR)
12. Power Down Mode
13. Self Refresh (Entry and Exit)
14. Auto Refresh (CBR)

**Timing Diagrams** (Cont'd)

## 15. Random Column Read ( Page within same Bank)

15.1  $\overline{\text{CAS}}$  Latency = 215.2  $\overline{\text{CAS}}$  Latency = 3

## 16. Random Column Write ( Page within same Bank)

16.1  $\overline{\text{CAS}}$  Latency = 216.2  $\overline{\text{CAS}}$  Latency = 3

## 17. Random Row Read ( Interleaving Banks) with Precharge

17.1  $\overline{\text{CAS}}$  Latency = 217.2  $\overline{\text{CAS}}$  Latency = 3

## 18. Random Row Write ( Interleaving Banks) with Precharge

18.1  $\overline{\text{CAS}}$  Latency = 218.2  $\overline{\text{CAS}}$  Latency = 3

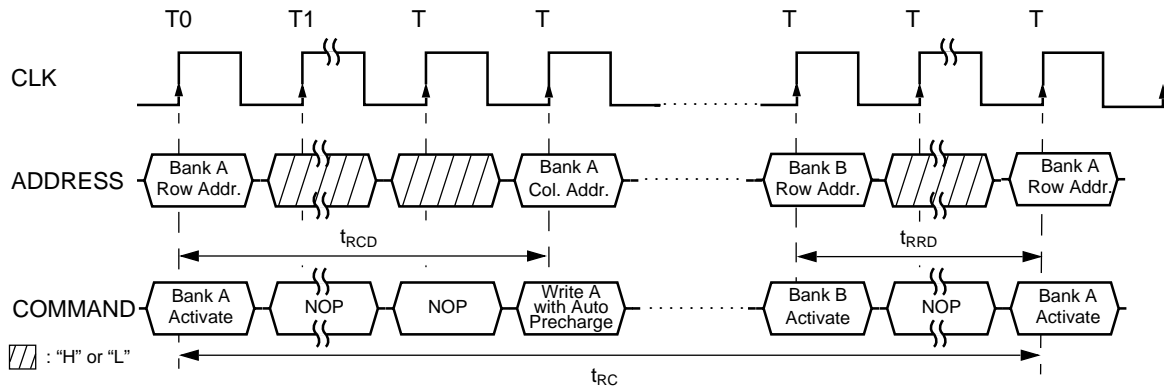
## 19. Precharge Termination of a Burst

19.1  $\overline{\text{CAS}}$  Latency = 219.2  $\overline{\text{CAS}}$  Latency = 3



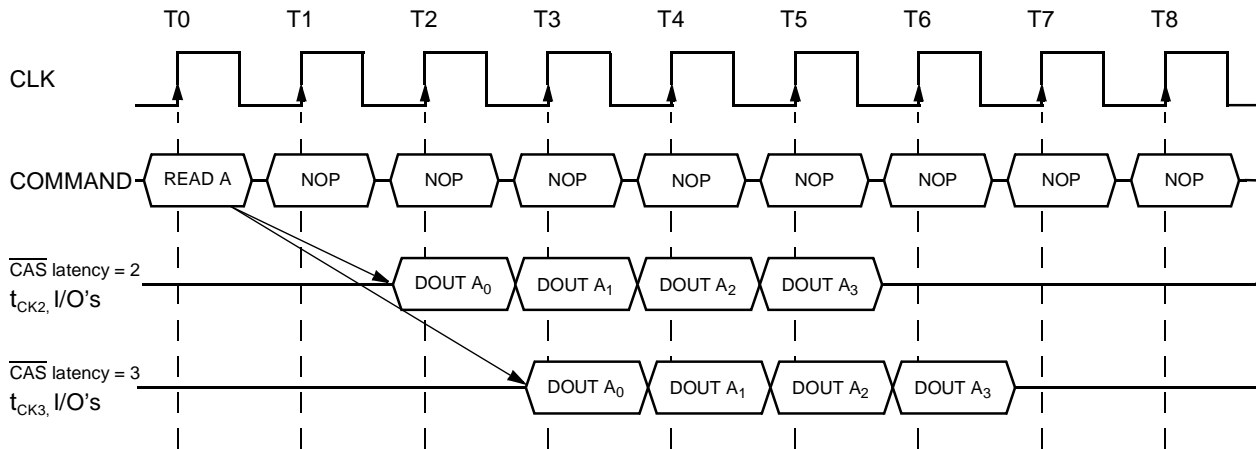
1. Bank Activate Command Cycle

( $\overline{\text{CAS}}$  latency = 3)



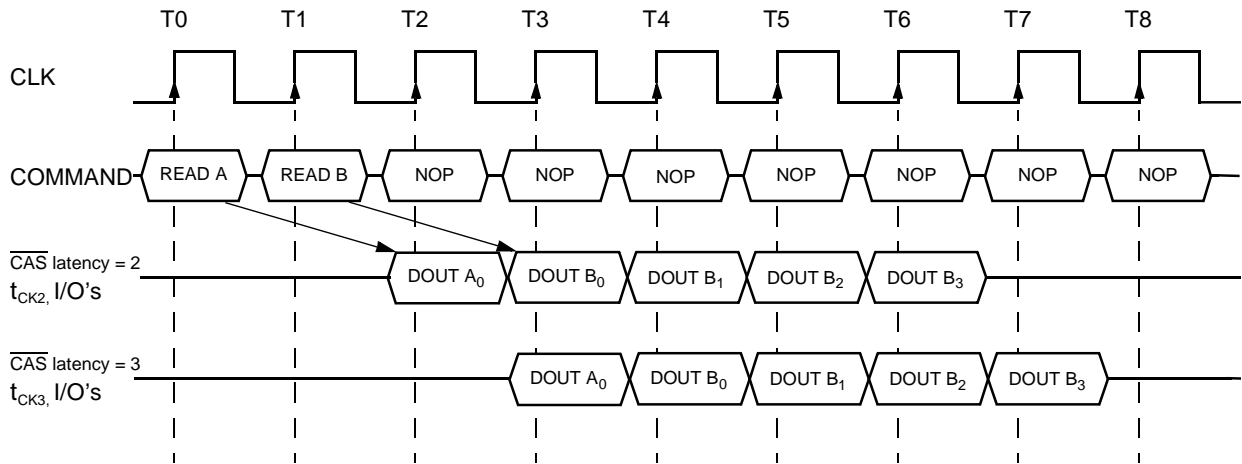
2. Burst Read Operation

(Burst Length = 4,  $\overline{\text{CAS}}$  latency = 2, 3)



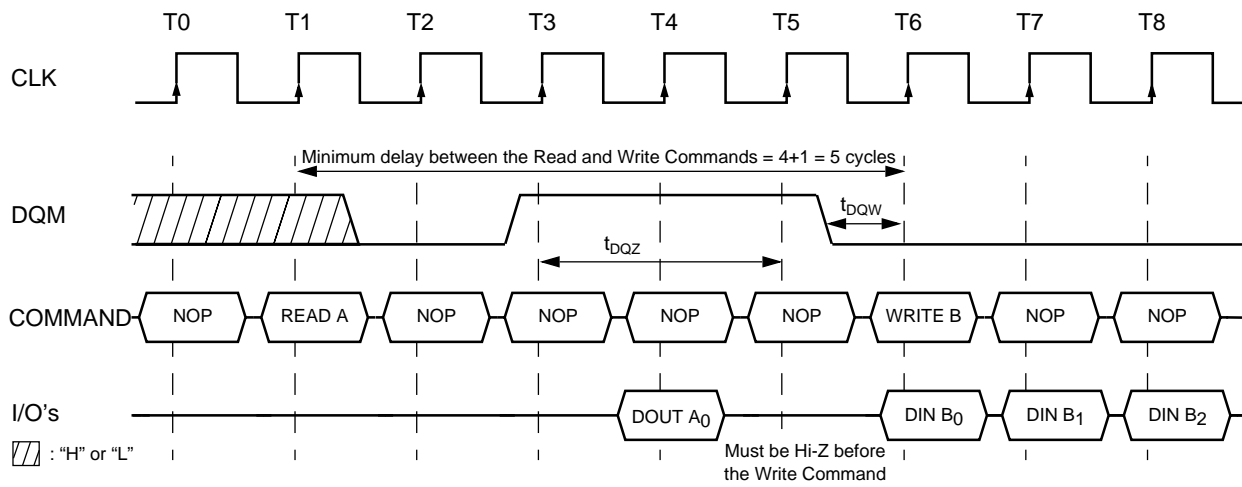
**3. Read Interrupted by a Read**

**(Burst Length = 4, CAS latency = 2, 3)**



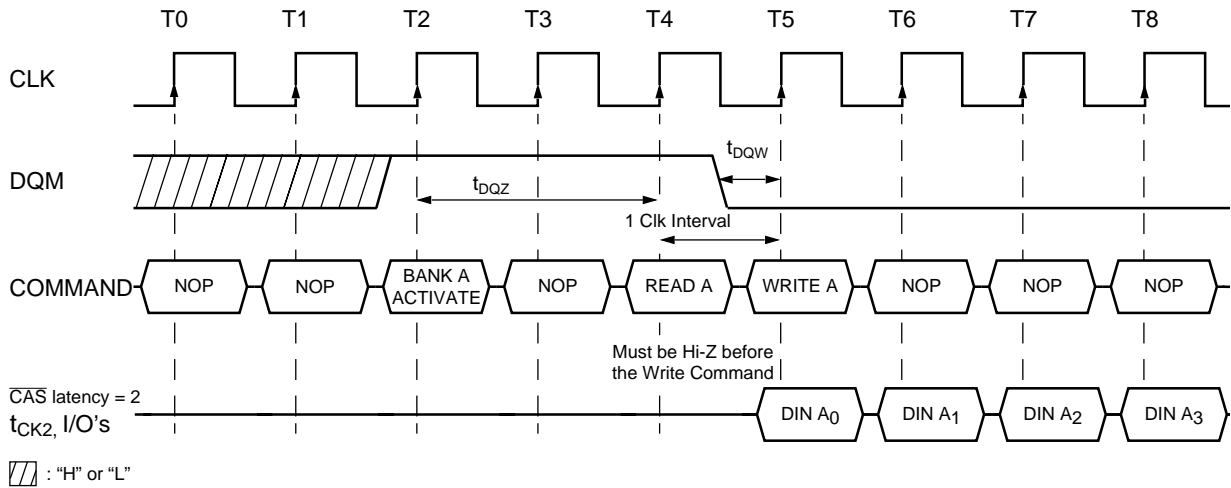
**4.1 Read to Write Interval**

**(Burst Length = 4, CAS latency = 3)**



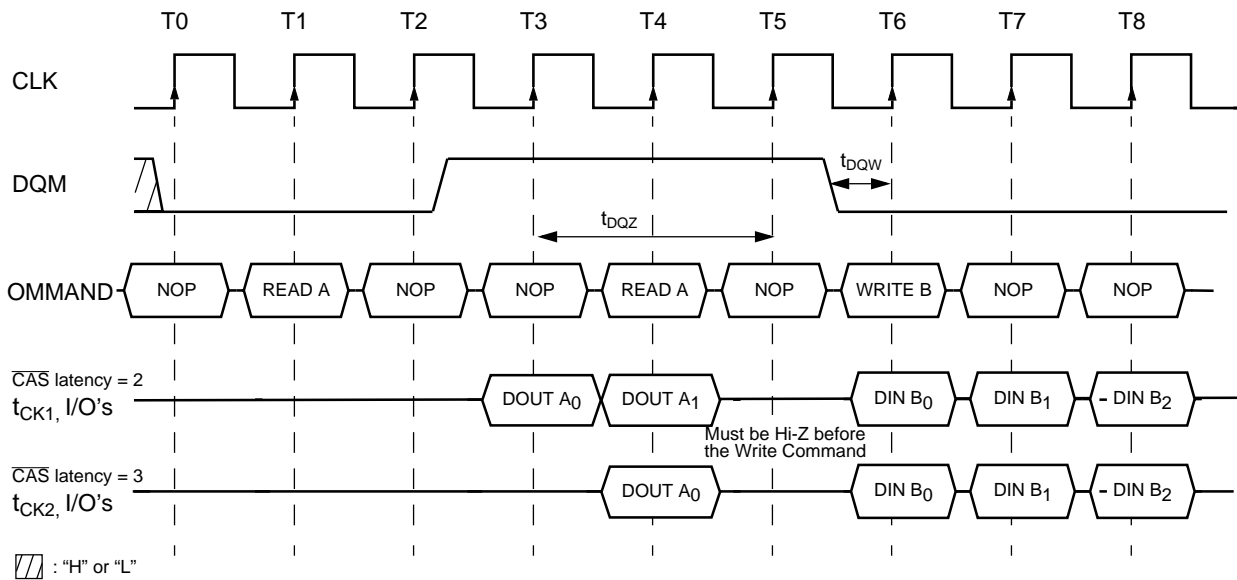
**4.2 Minimum Read to Write Interval**

**(Burst Length = 4,  $\overline{\text{CAS}}$  latency = 2)**



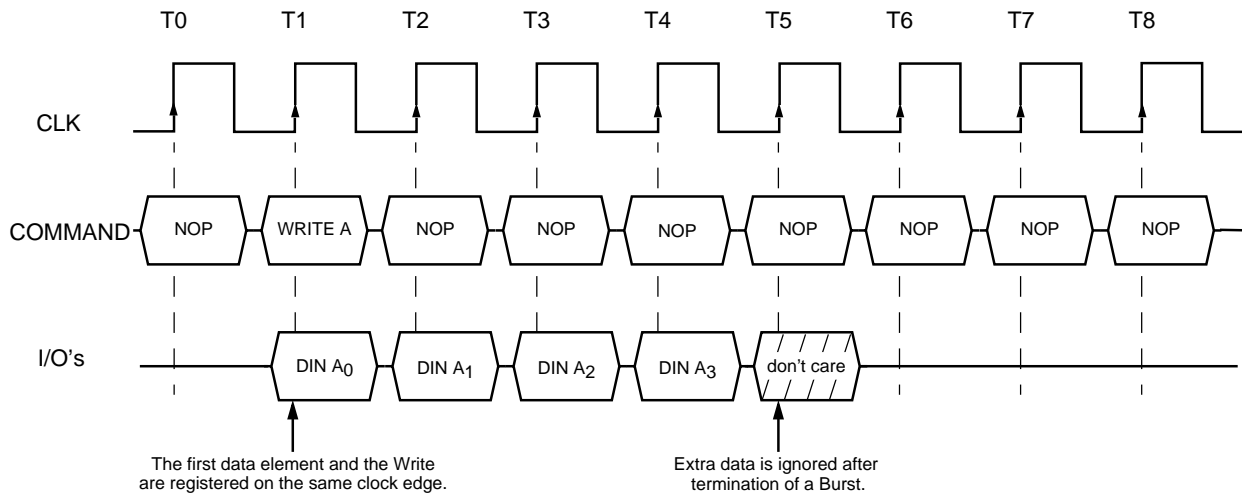
**4.3 Non-Minimum Read to Write Interval**

**(Burst Length = 4,  $\overline{\text{CAS}}$  latency = 2, 3)**



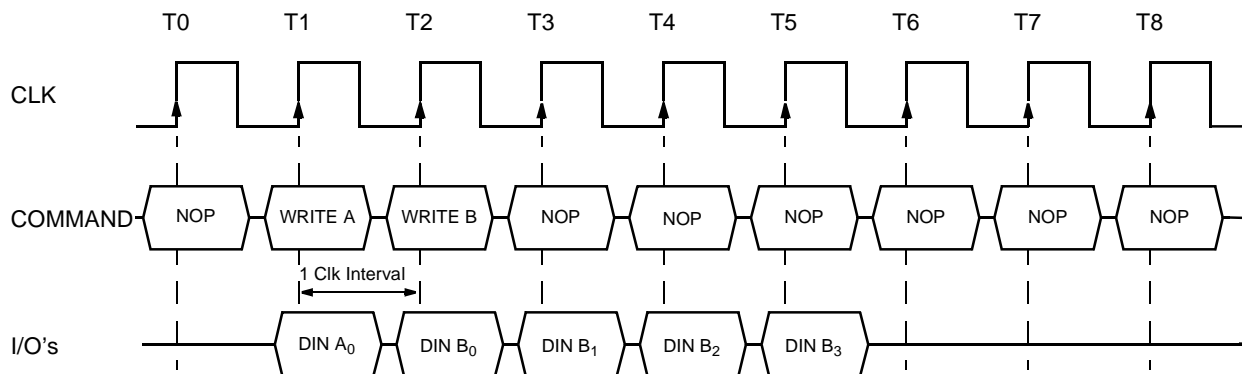
**5. Burst Write Operation**

**(Burst Length = 4,  $\overline{\text{CAS}}$  latency = 2, 3)**



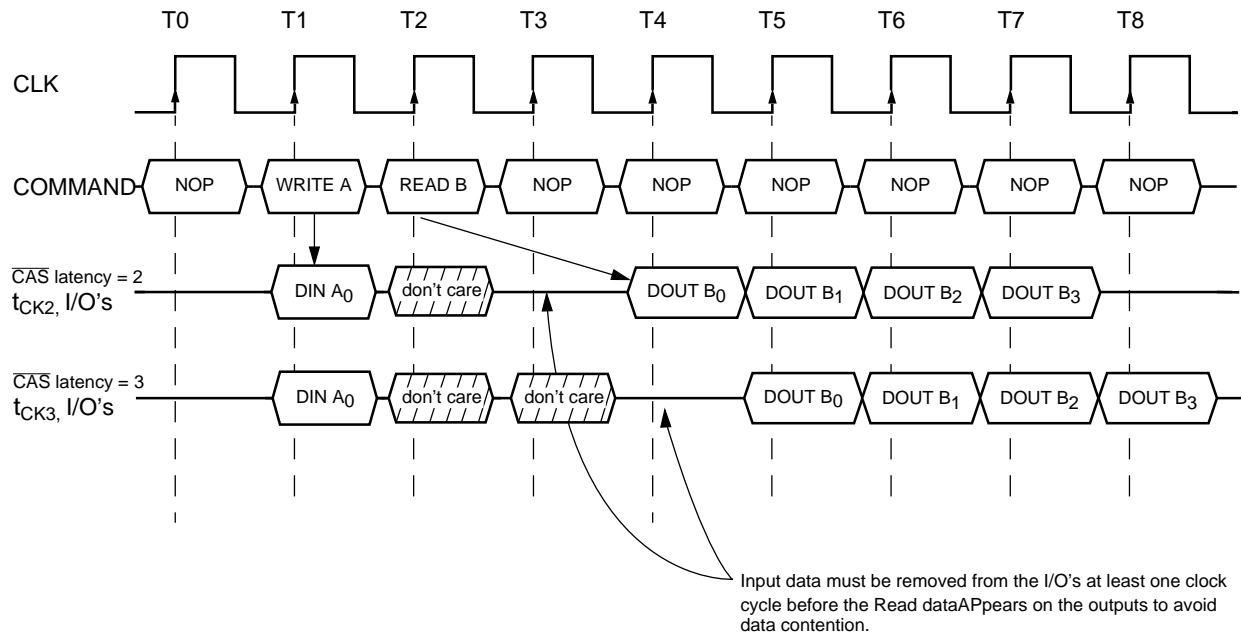
**6.1 Write Interrupted by a Write**

**(Burst Length = 4,  $\overline{\text{CAS}}$  latency = 2, 3)**



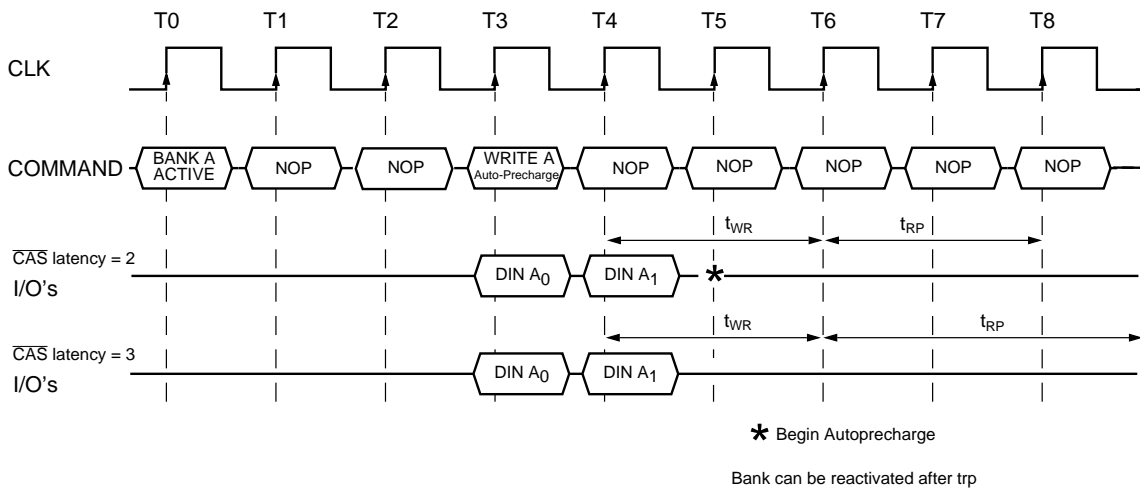
6.2 Write Interrupted by a Read

(Burst Length = 4,  $\overline{\text{CAS}}$  latency = 2, 3)



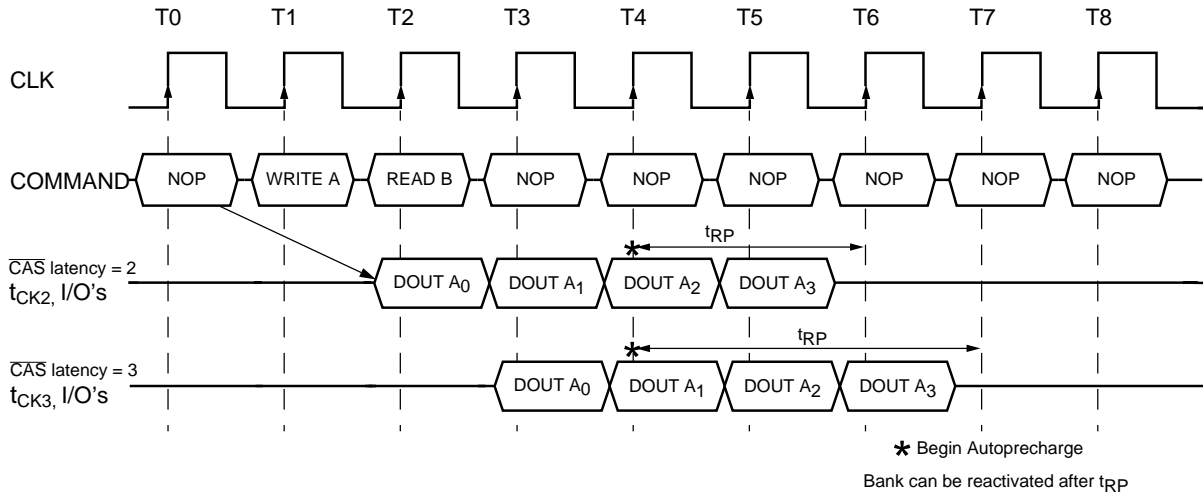
7. Burst Write with Auto-Precharge

Burst Length = 2,  $\overline{\text{CAS}}$  latency = 2, 3)



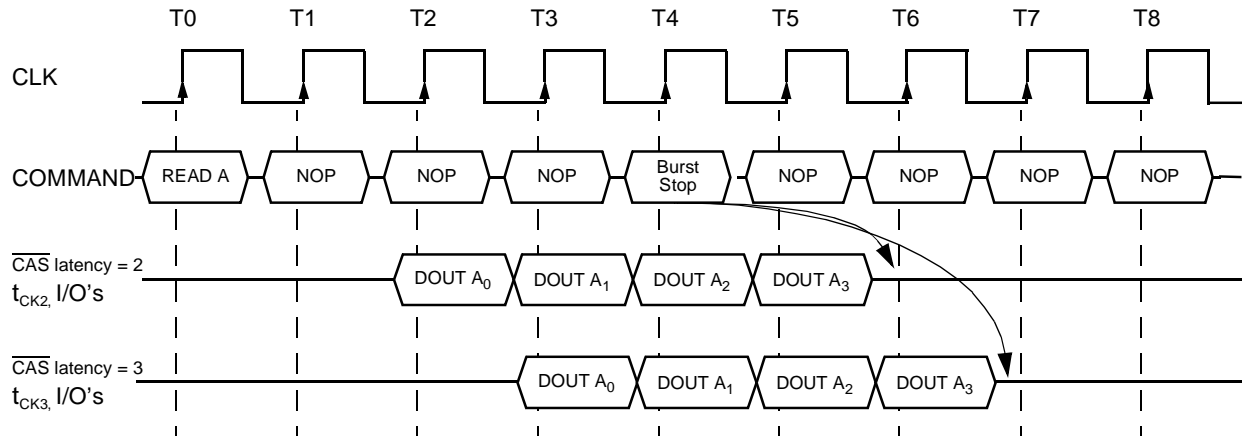
**7.2 Burst Read with Auto-Precharge**

**Burst Length = 4,  $\overline{\text{CAS}}$  latency = 2, 3)**



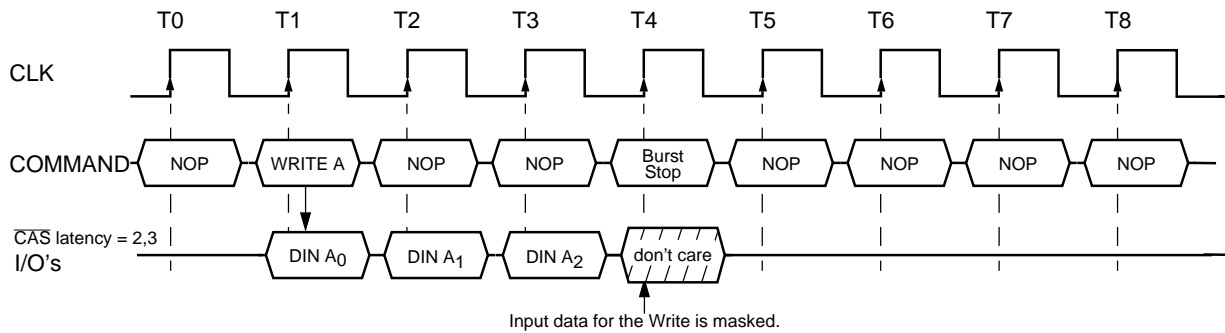
**8.1 Termination of a Burst Read Operation**

**( $\overline{\text{CAS}}$  latency = 2, 3)**



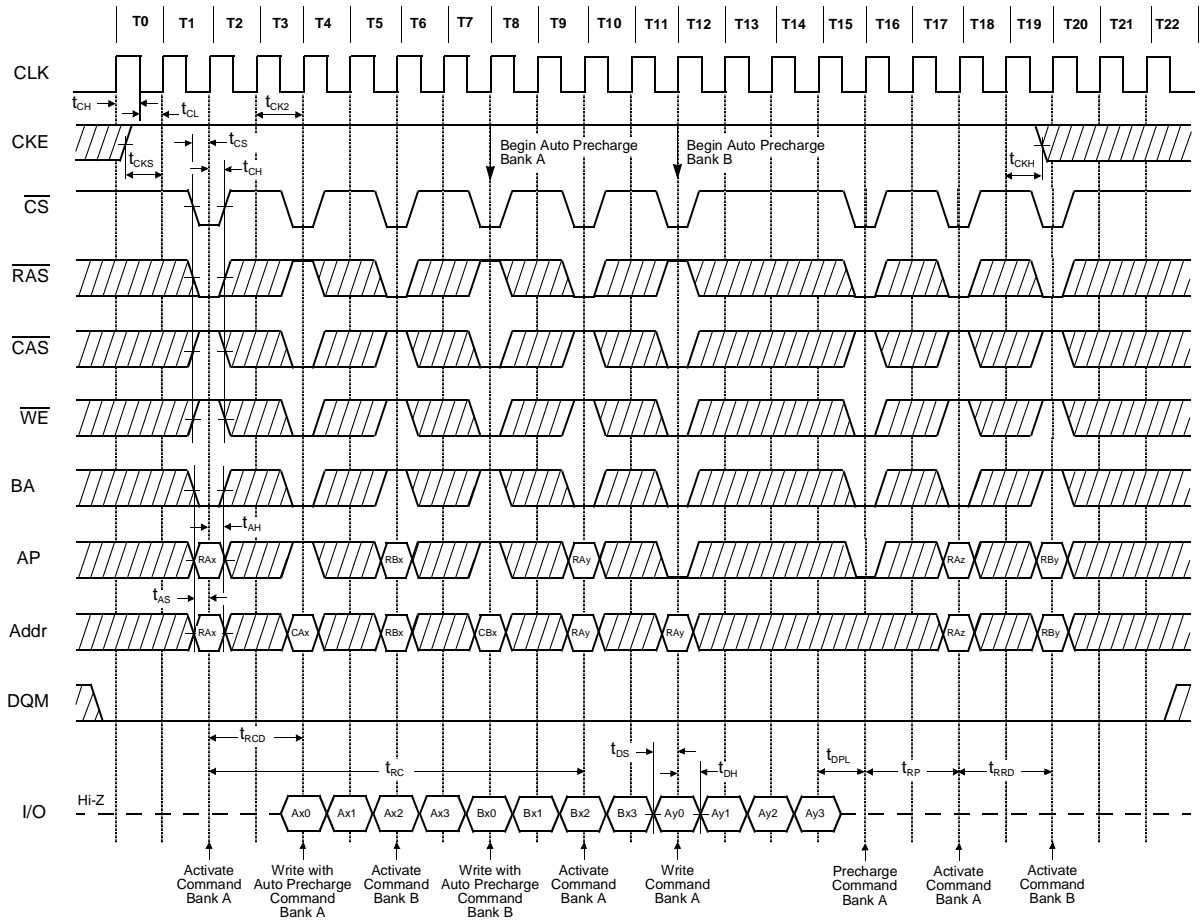
**8.2 Termination of a Burst Write Operation**

**( $\overline{\text{CAS}}$  latency = 2, 3)**



9.1 AC Parameters for Write Timing

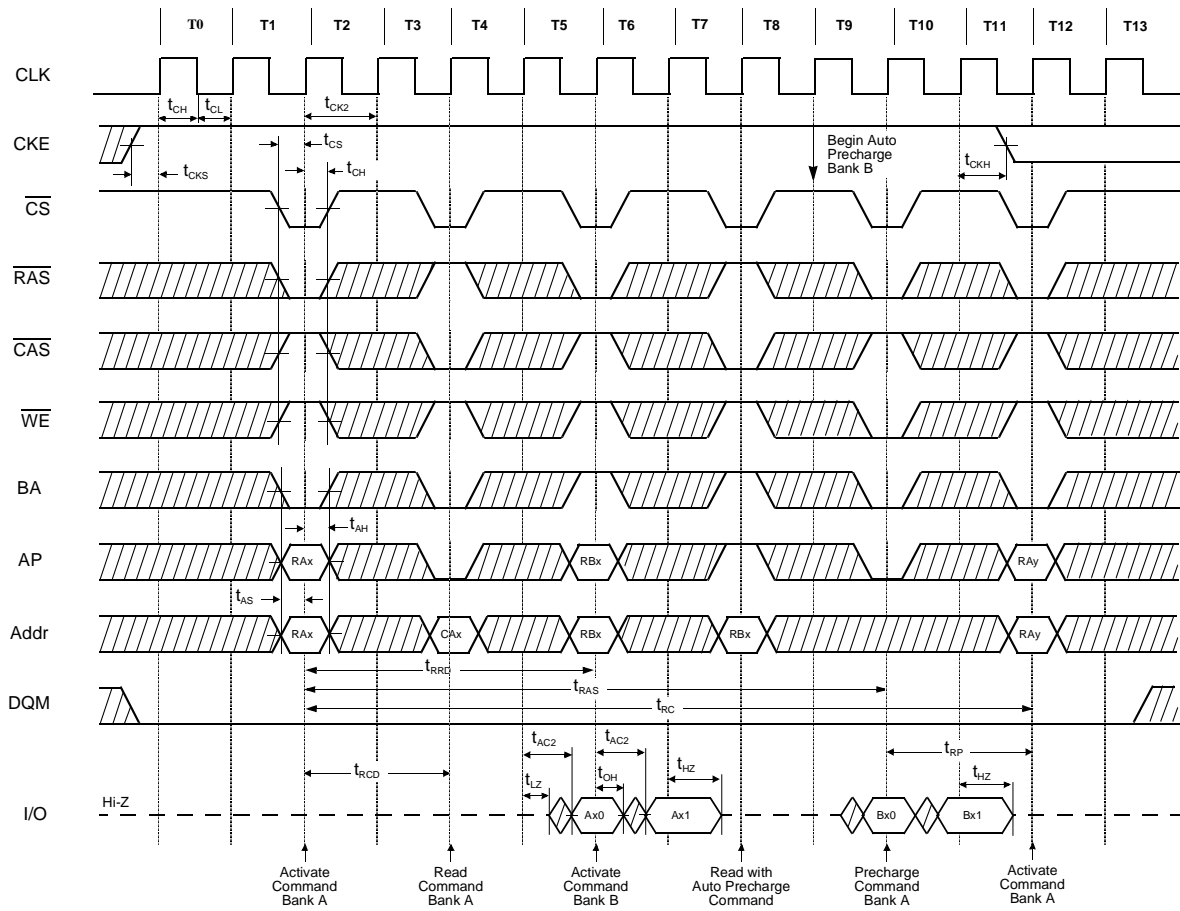
Burst Length = 4, CAS Latency = 2



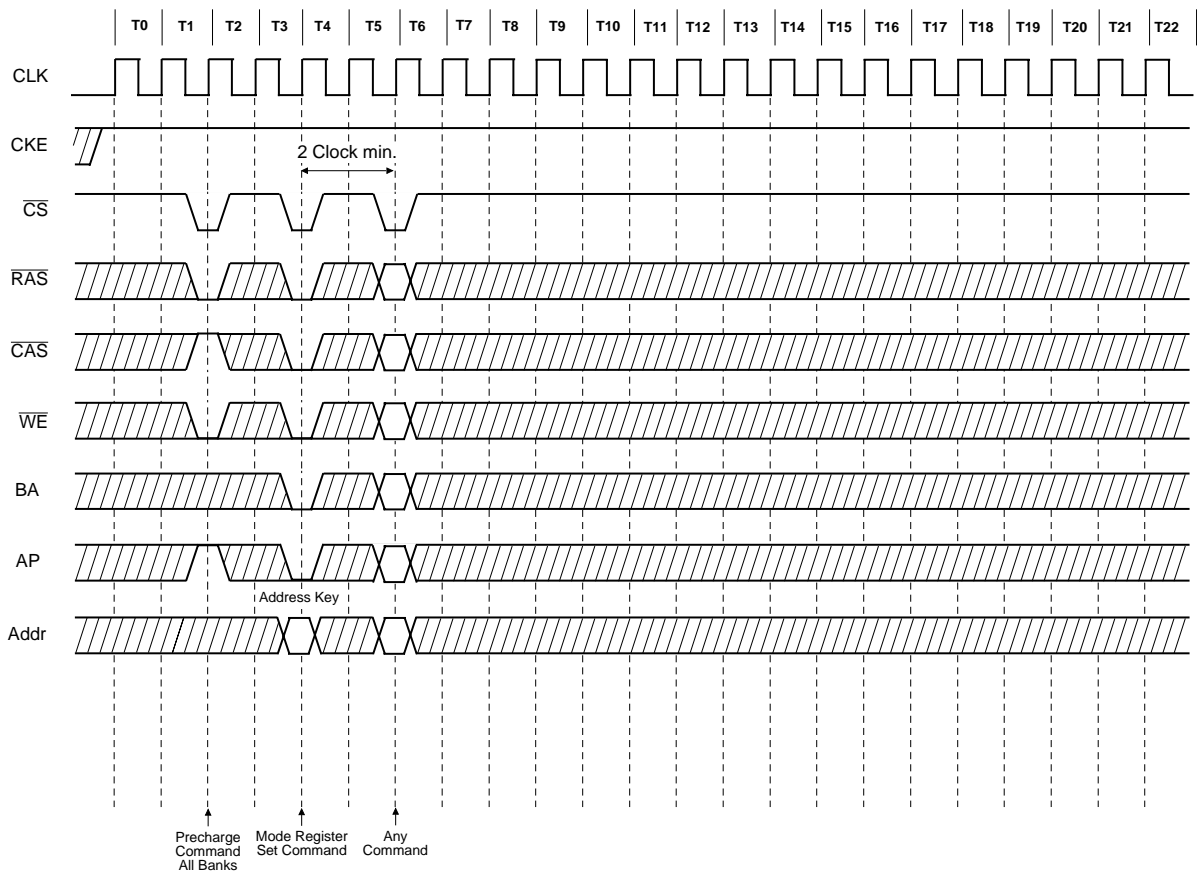


9.2 AC Parameters for Read Timing

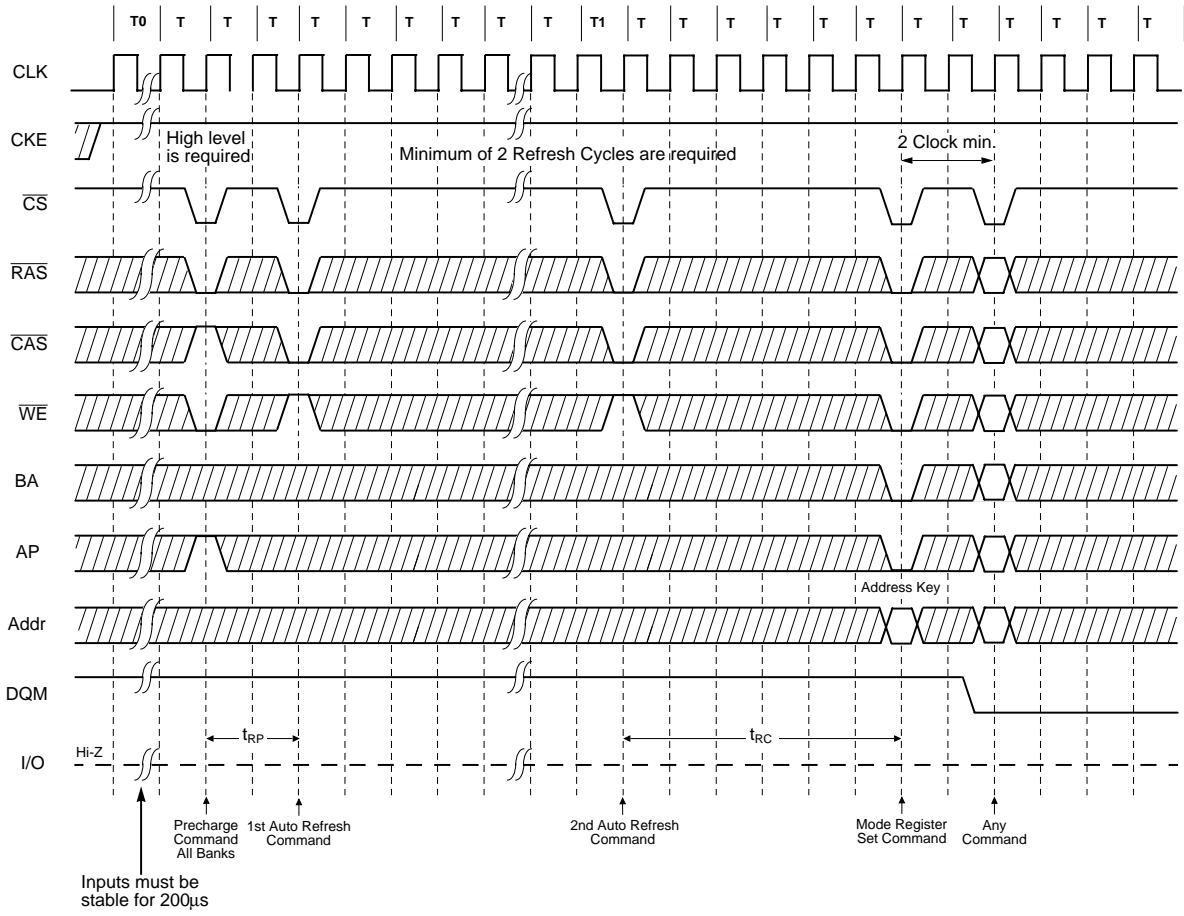
Burst Length = 2, CAS Latency = 2



**10. Mode Register Set**

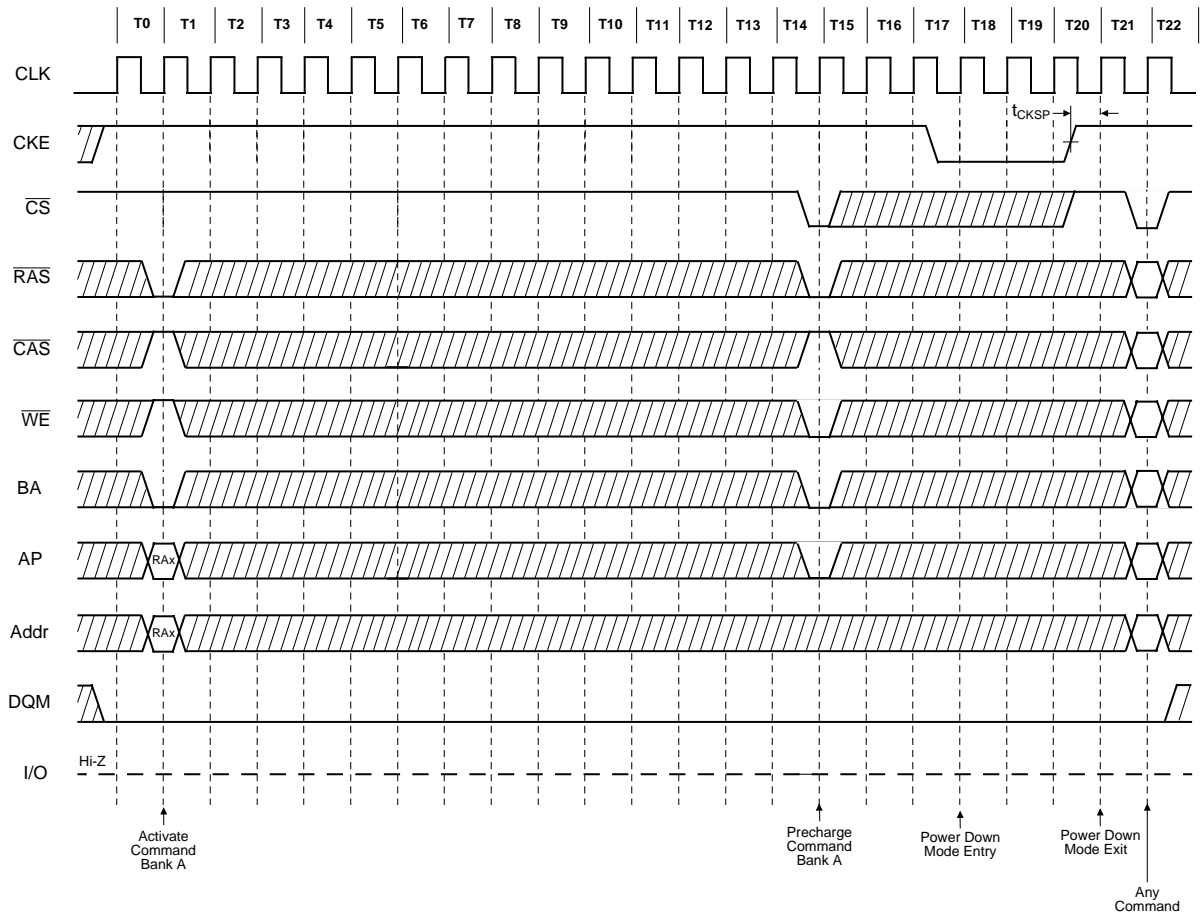


11. Power on Sequence and Auto Refresh (CBR)

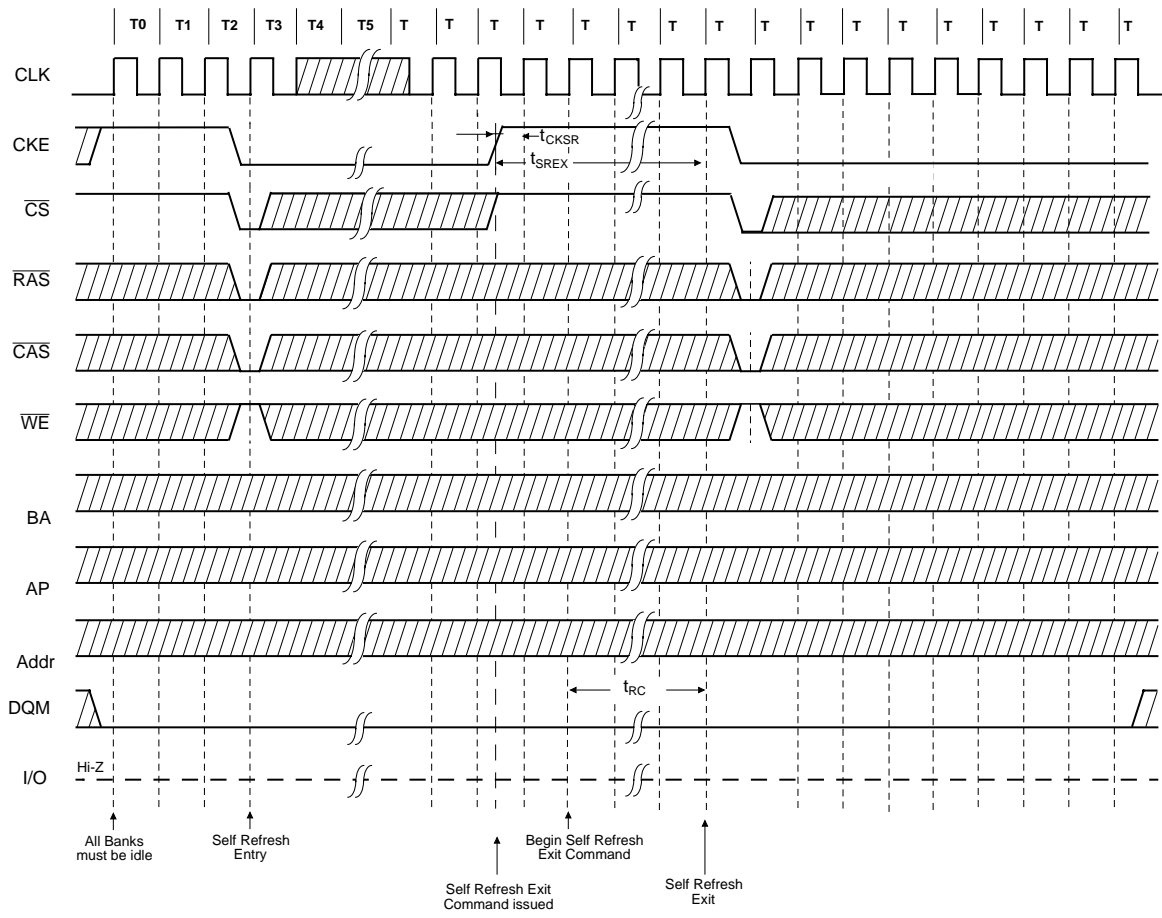


**12. Power Down Mode**

Burst Length = 4, CAS Latency = 2

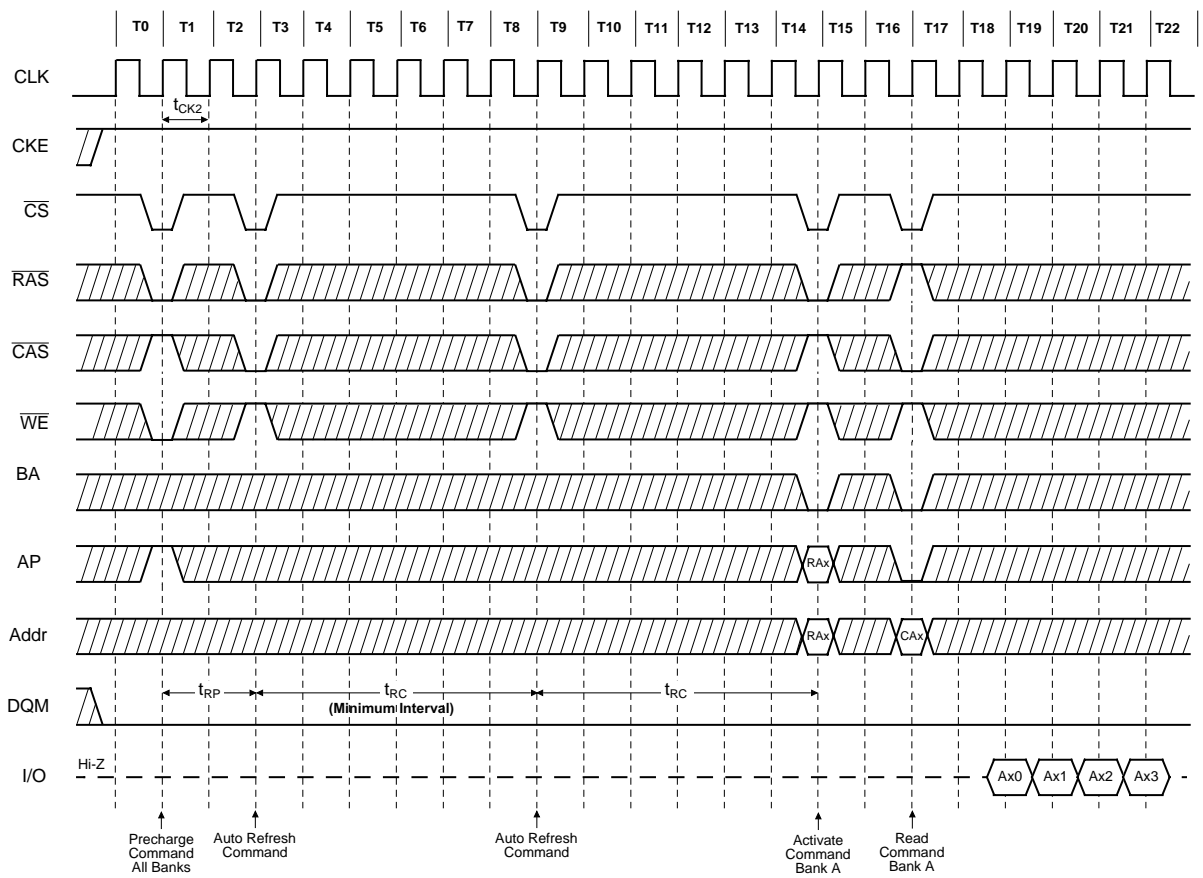


### 13. Self Refresh (Entry and Exit)



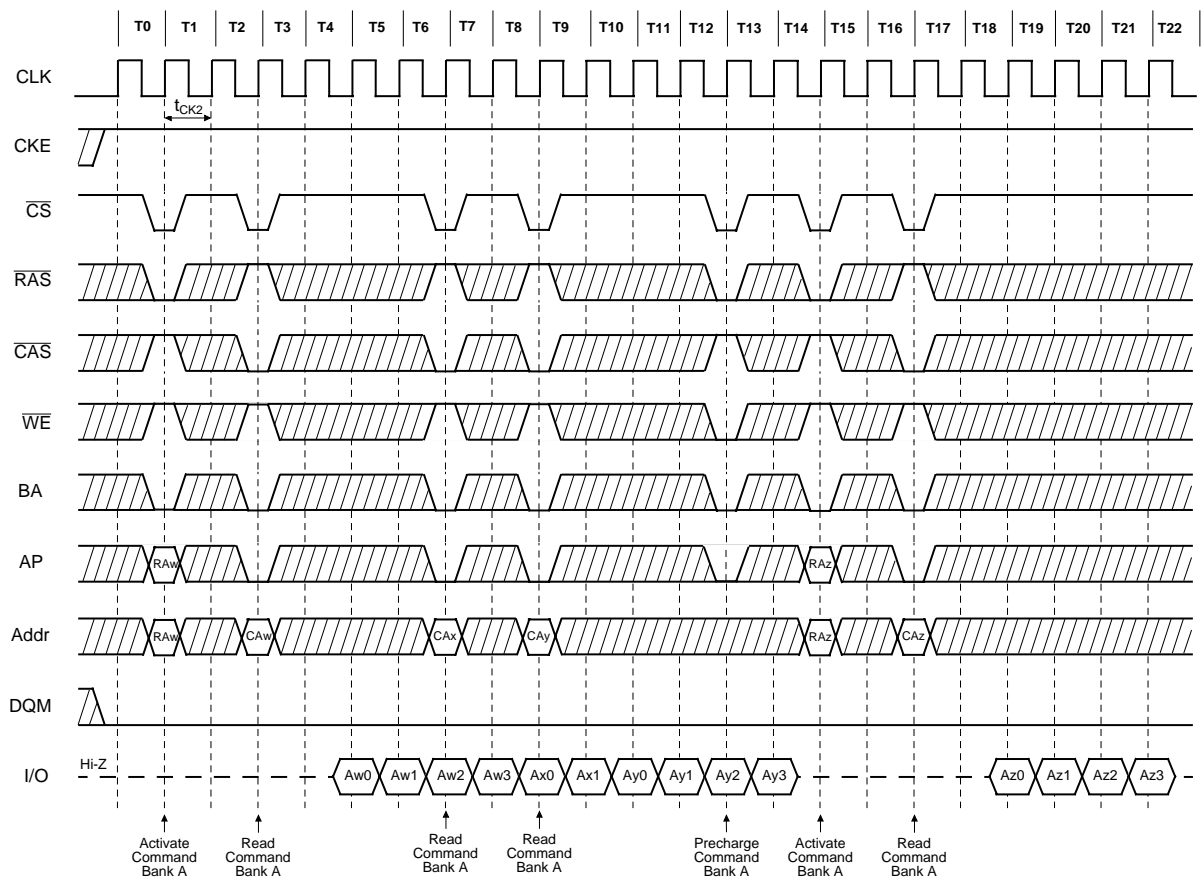
14. Auto Refresh (CBR)

Burst Length = 4,  $\overline{\text{CAS}}$  Latency = 2



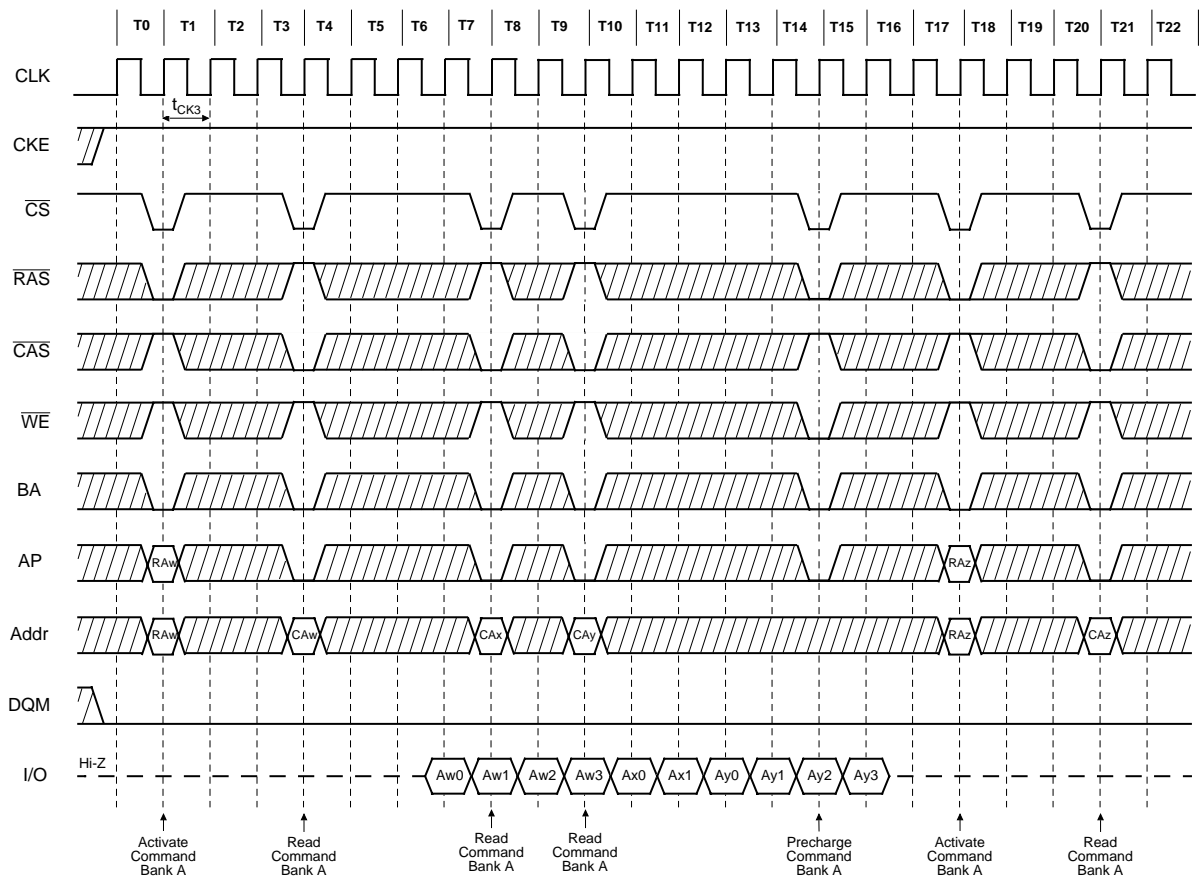
15.1 Random Column Read (Page within same Bank) (1 of 2)

Burst Length = 4, CAS Latency = 2



15.2 Random Column Read (Page within same Bank) (2 of 2)

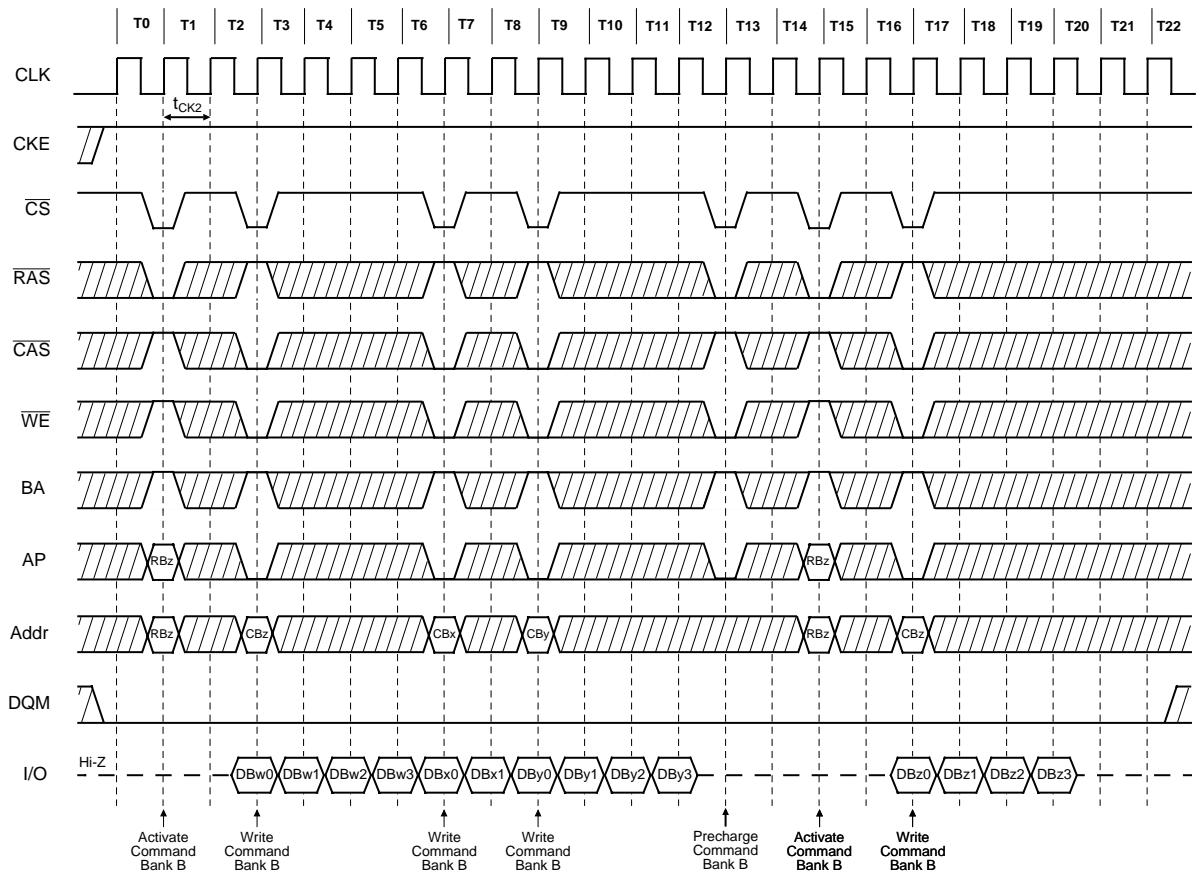
Burst Length = 4, CAS Latency = 3





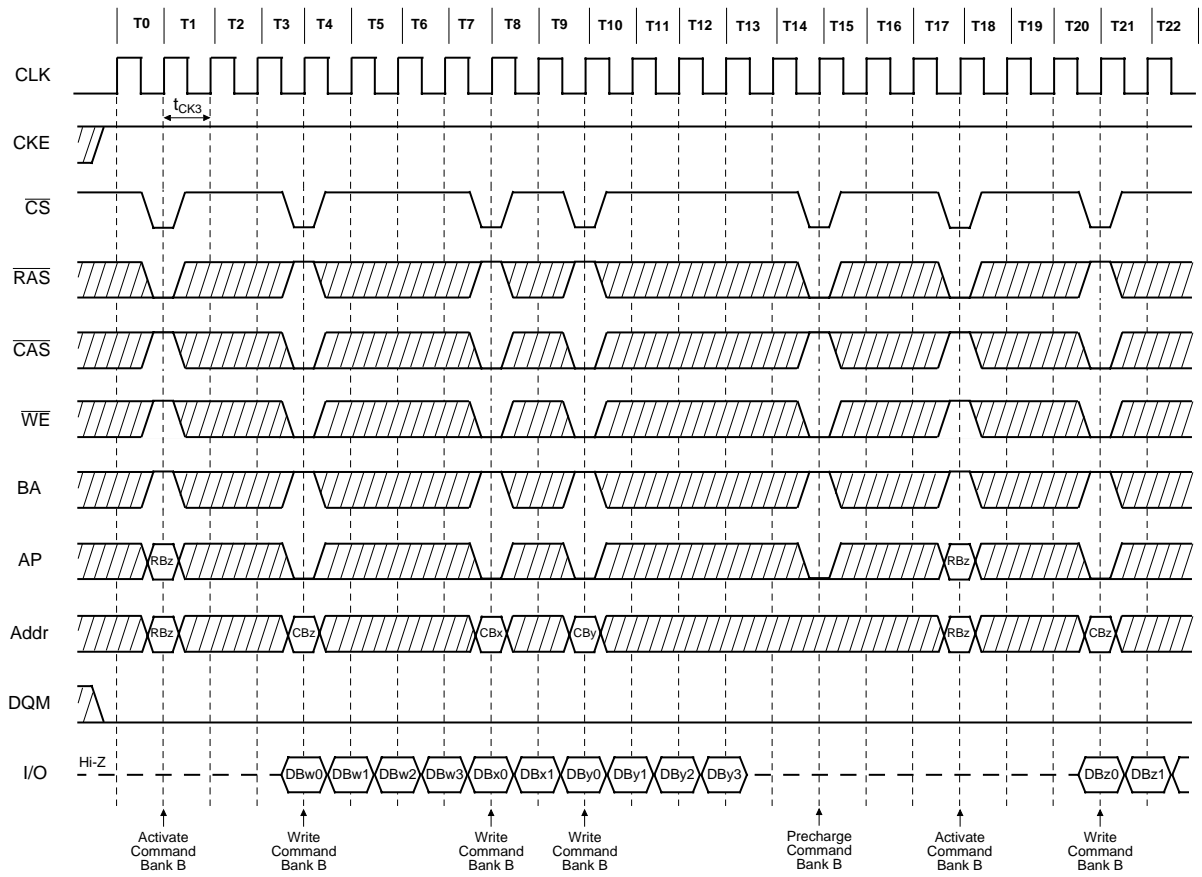
16.1 Random Column Write (Page within same Bank) (1 of 2)

Burst Length = 4, CAS Latency = 2



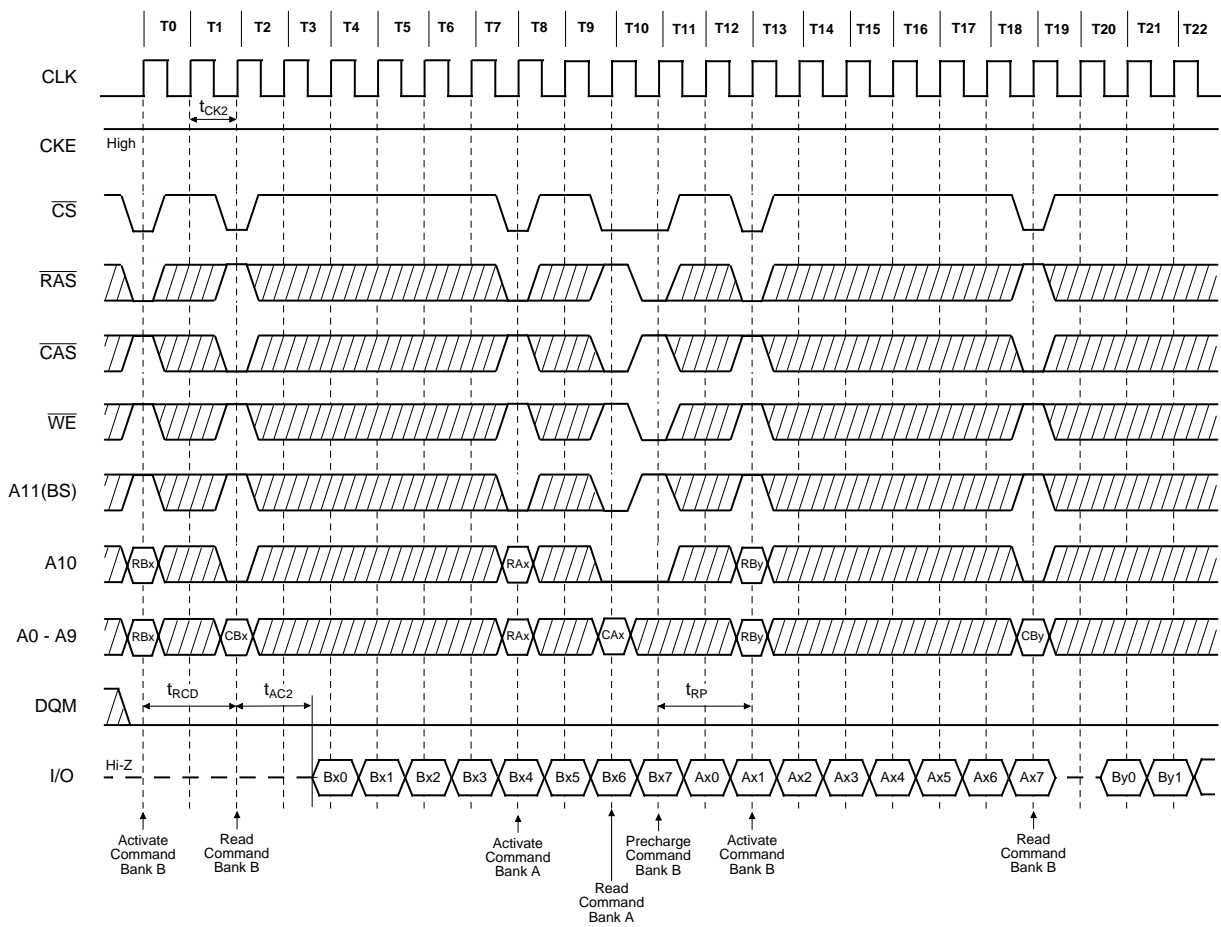
16.2 Random Column Write (Page within same Bank) (2 of 2)

Burst Length = 4, CAS Latency = 3



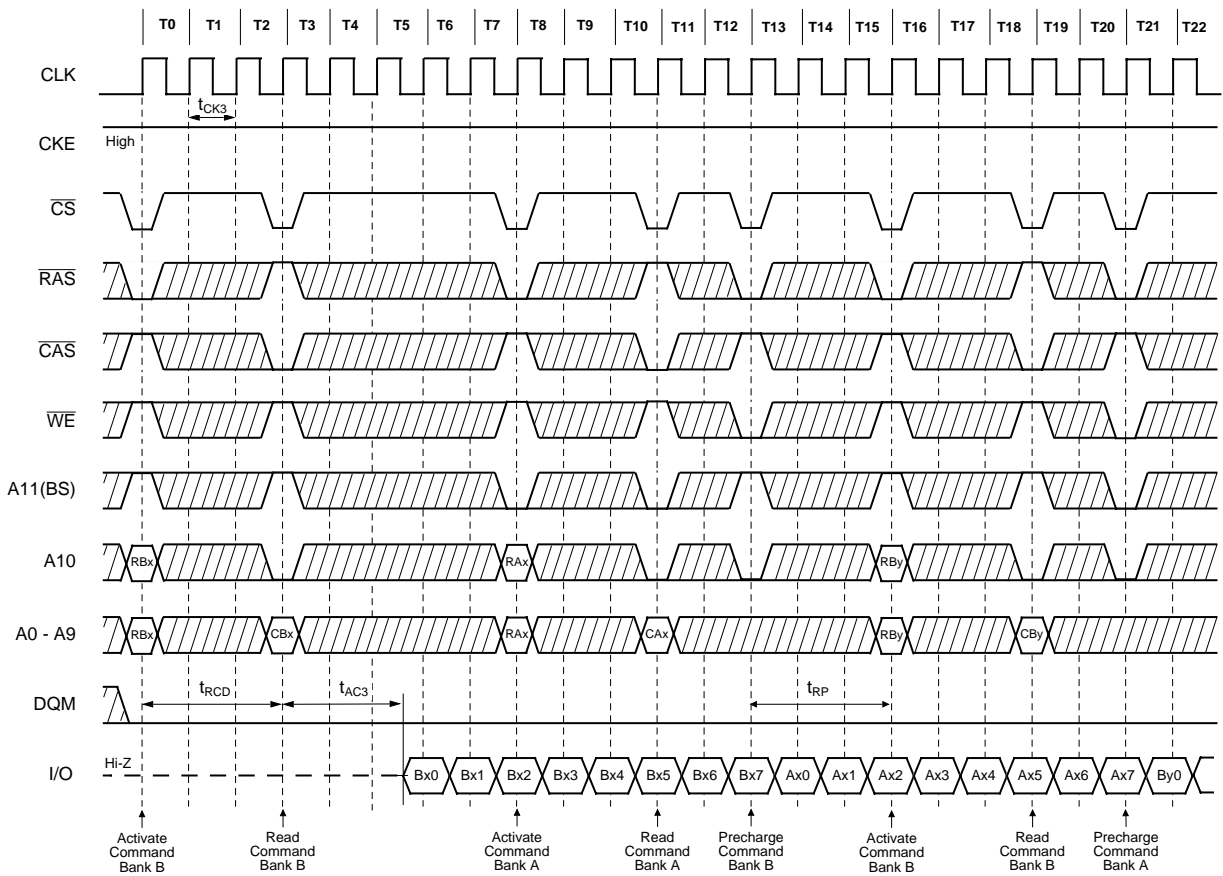
17.1 Random Row Read (Interleaving Banks) (1 of 2)

Burst Length = 8, CAS Latency = 2



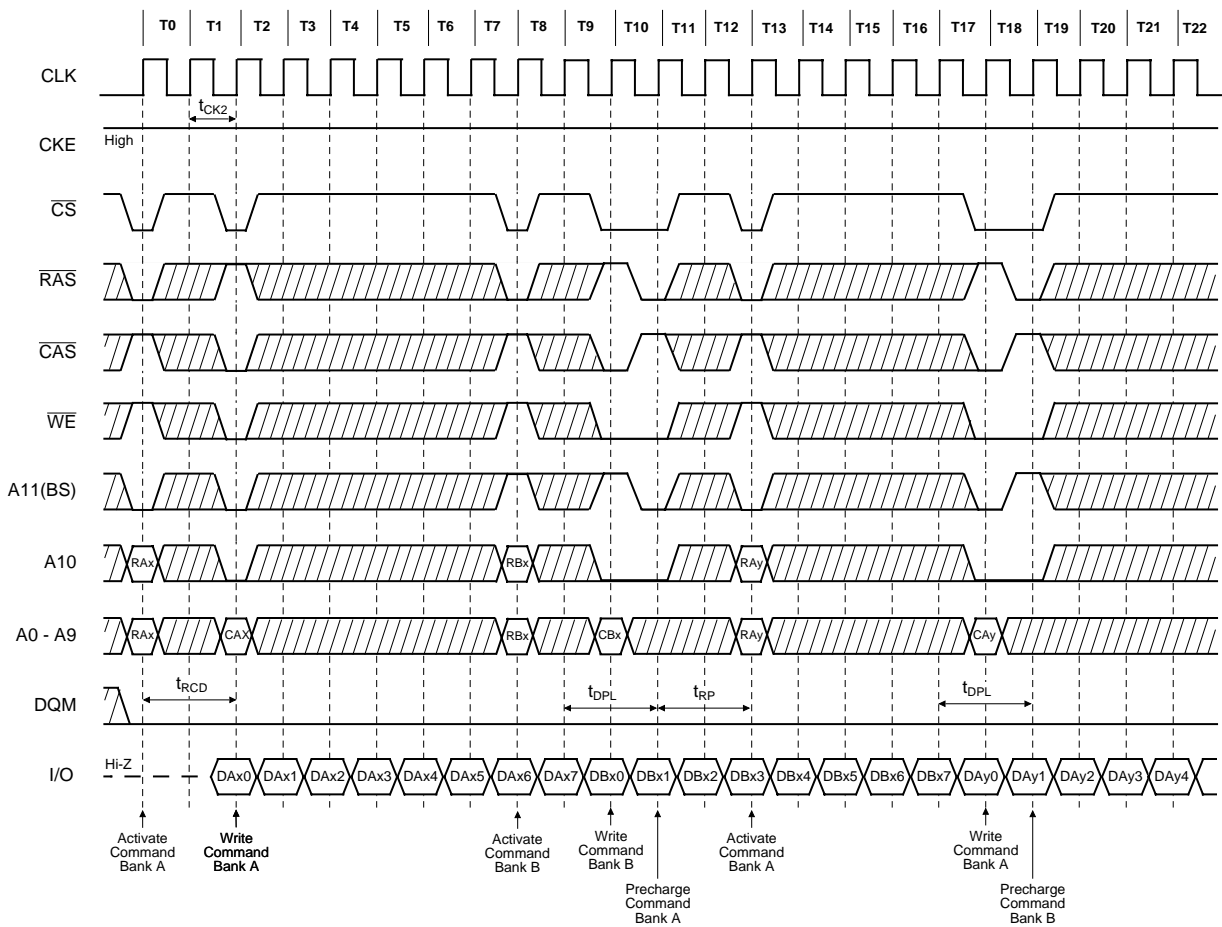
17.2 Random Row Read (Interleaving Banks) (2 of 2)

Burst Length = 8, CAS Latency = 3



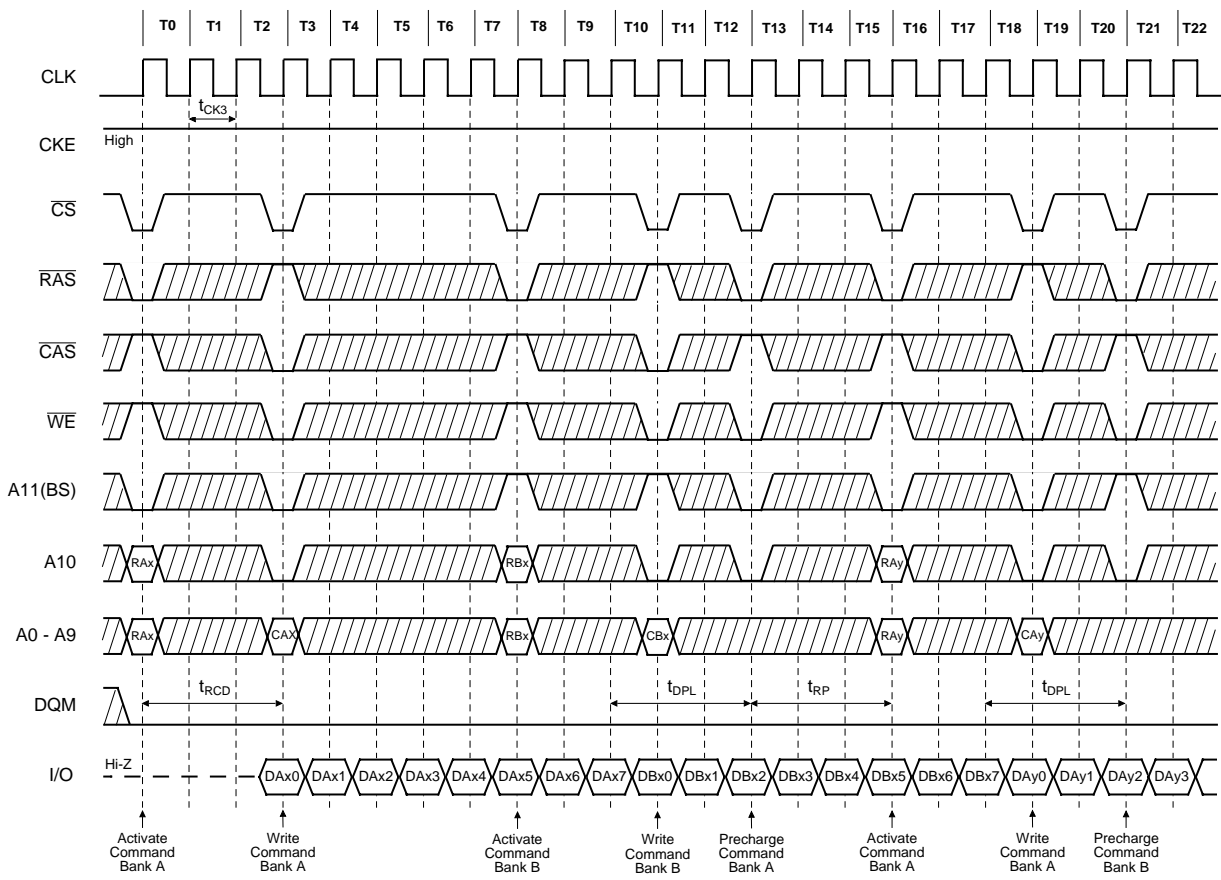
18.1 Random Row Write (Interleaving Banks) (1 of 2)

Burst Length = 8, CAS Latency = 2



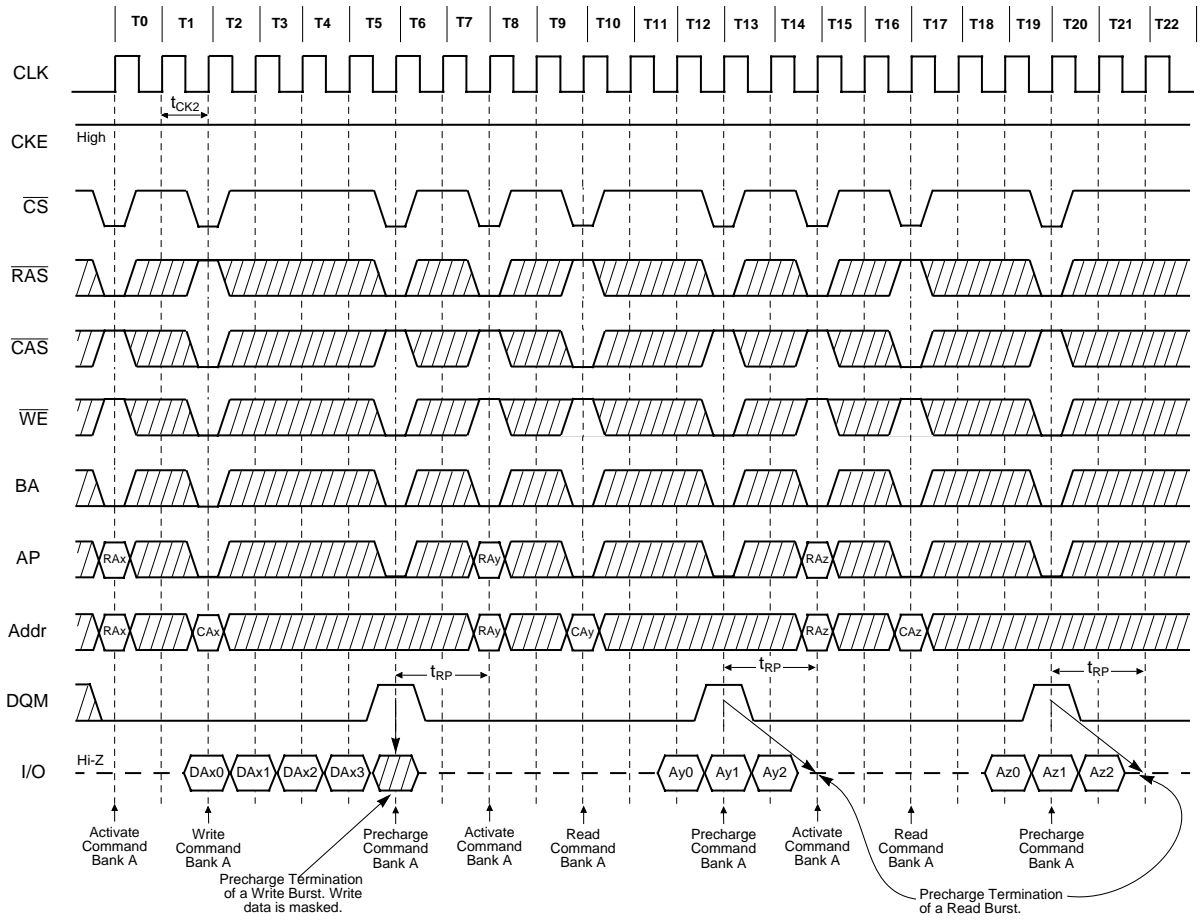
18.2 Random Row Write (Interleaving Banks) (2 of 2)

Burst Length = 8, CAS Latency = 3



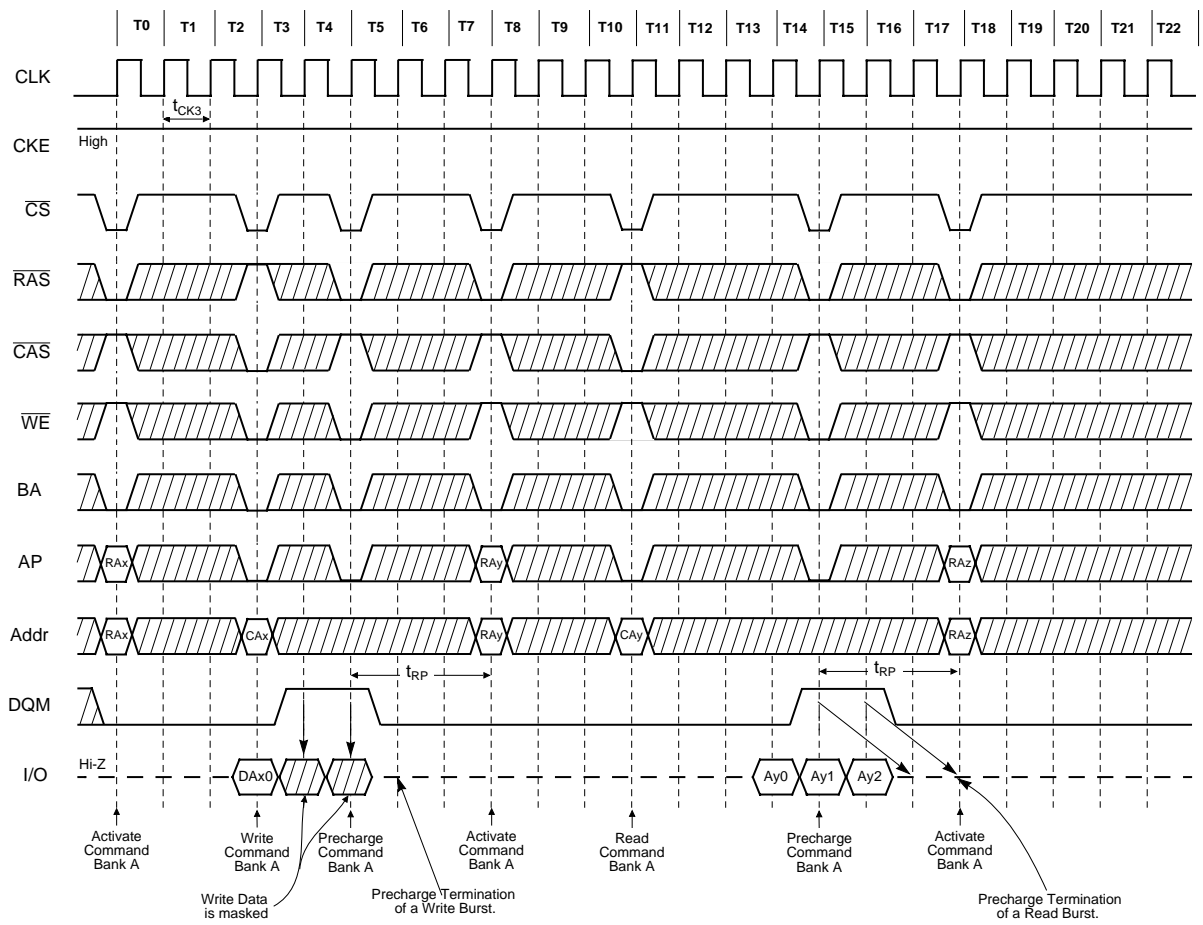
19.1 Precharge Termination of a Burst (1 of 2)

Burst Length = 8, CAS Latency = 2



19.2 Precharge Termination of a Burst (2 of 2)

Burst Length = 4, 8, CAS Latency = 3





**Complete List of Operation Commands**

**SDRAM Function Truth Table**

CURRENT STATE <sup>1</sup>	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	$\overline{\text{BS}}$	Addr	ACTION
Idle	H	X	X	X	X	X	NOP or Power Down
	L	H	H	H	X	X	NOP
	L	H	H	L	BS	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BS	X	ILLEGAL <sup>2</sup>
	L	L	H	H	BS	RA	Row (&Bank) Active; Latch Row Address
	L	L	H	L	BS	AP	NOP <sup>4</sup>
	L	L	L	H	X	X	Auto-Refresh or Self-Refresh <sup>5</sup>
	L	L	L	L	Op-	Code	Mode reg. Access <sup>5</sup>
Row Active	H	X	X	X	X	X	NOP
	L	H	H	X	X	X	NOP
	L	H	L	H	BS	CA,AP	Begin Read; Latch CA; DetermineAP
	L	H	L	L	BS	CA,AP	Begin Write; Latch CA; DetermineAP
	L	L	H	H	BS	X	ILLEGAL <sup>2</sup>
	L	L	H	L	BS	AP	Precharge
	L	L	L	X	X	X	ILLEGAL
Read	H	X	X	X	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	H	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	L	BS	X	Burst Stop Command > Row Active
	L	H	L	H	BS	CA,AP	Term Burst, New Read, DetermineAP <sup>3</sup>
	L	H	L	L	BS	CA,AP	Term Burst, Start Write, DetermineAP <sup>3</sup>
	L	L	H	H	BS	X	ILLEGAL <sup>2</sup>
	L	L	H	L	BS	AP	Term Burst, Precharge
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	H	X	X	NOP (Continue Burst to End;>Row Active)
	L	H	H	L	BS	X	Burst Stop Command > Row Active
	L	H	L	H	BS	CA,AP	Term Burst, Start Read, DetermineAP <sup>3</sup>
	L	H	L	L	BS	CA,AP	Term Burst, New Write, DetermineAP <sup>3</sup>
	L	L	H	H	BS	X	ILLEGAL <sup>2</sup>
	L	L	H	L	BS	AP	Term Burst, Precharge <sup>3</sup>
	L	L	L	X	X	X	ILLEGAL
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	L	BS	X	ILLEGAL <sup>2</sup>
	L	H	L	H	BS	X	ILLEGAL <sup>2</sup>
	L	H	L	L	X	X	ILLEGAL
	L	L	H	H	BS	X	ILLEGAL <sup>2</sup>
	L	L	H	L	BS	AP	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL

**SDRAM FUNCTION TRUTH TABLE(continued)**

CURRENT STATE <sup>1</sup>	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	$\overline{\text{BS}}$	Addr	ACTION
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End;> Precharge)
	L	H	H	L	BS	X	ILLEGAL <sup>2</sup>
	L	H	L	H	BS	X	ILLEGAL <sup>2</sup>
	L	H	L	L	X	X	ILLEGAL
	L	L	H	H	BS	X	ILLEGAL <sup>2</sup>
	L	L	H	L	BS	AP	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL
Precharging	H	X	X	X	X	X	NOP;> Idle after tRP
	L	H	H	H	X	X	NOP;> Idle after tRP
	L	H	H	L	BS	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BS	X	ILLEGAL <sup>2</sup>
	L	L	H	H	BS	X	ILLEGAL <sup>2</sup>
	L	L	H	L	BS	AP	NOP <sup>4</sup>
	L	L	L	X	X	X	ILLEGAL
Row Activating	H	X	X	X	X	X	NOP;> Row Active after tRCD
	L	H	H	H	X	X	NOP;> Row Active after tRCD
	L	H	H	L	BS	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BS	X	ILLEGAL <sup>2</sup>
	L	L	H	H	BS	X	ILLEGAL <sup>2</sup>
	L	L	H	L	BS	AP	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL
Write Recovering	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BS	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BS	X	ILLEGAL <sup>2</sup>
	L	L	H	H	BS	X	ILLEGAL <sup>2</sup>
	L	L	H	L	BS	AP	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL
Refreshing	H	X	X	X	X	X	NOP;> Idle after tRC
	L	H	H	H	X	X	NOP;> Idle after tRC
	L	H	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	ILLEGAL
	L	L	H	X	X	X	ILLEGAL
	L	L	L	X	X	X	ILLEGAL
	L	L	L	X	X	X	ILLEGAL
Mode Register Accessing	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	ILLEGAL

**Clock Enable (CKE) Truth Table:**

STATE(n)	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addr	ACTION
Self-Refresh <sup>6</sup>	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Self-Refresh, Idle after tRC
	L	H	L	H	H	H	X	EXIT Self-Refresh, Idle after tRC
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
Power-Down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	EXIT Power-Down, > Idle.
	L	H	L	H	H	H	X	EXIT Power-Down, > Idle.
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Low-Power Mode)
All. Banks Idle <sup>7</sup>	H	H	X	X	X	X	X	Refer to the function truth table
	H	L	H	X	X	X	X	Enter Power- Down
	H	L	L	H	H	H	X	Enter Power- Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	X	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self-Refresh
	L	L	X	X	X	X	X	ILLEGAL NOP

**Abbreviations:**

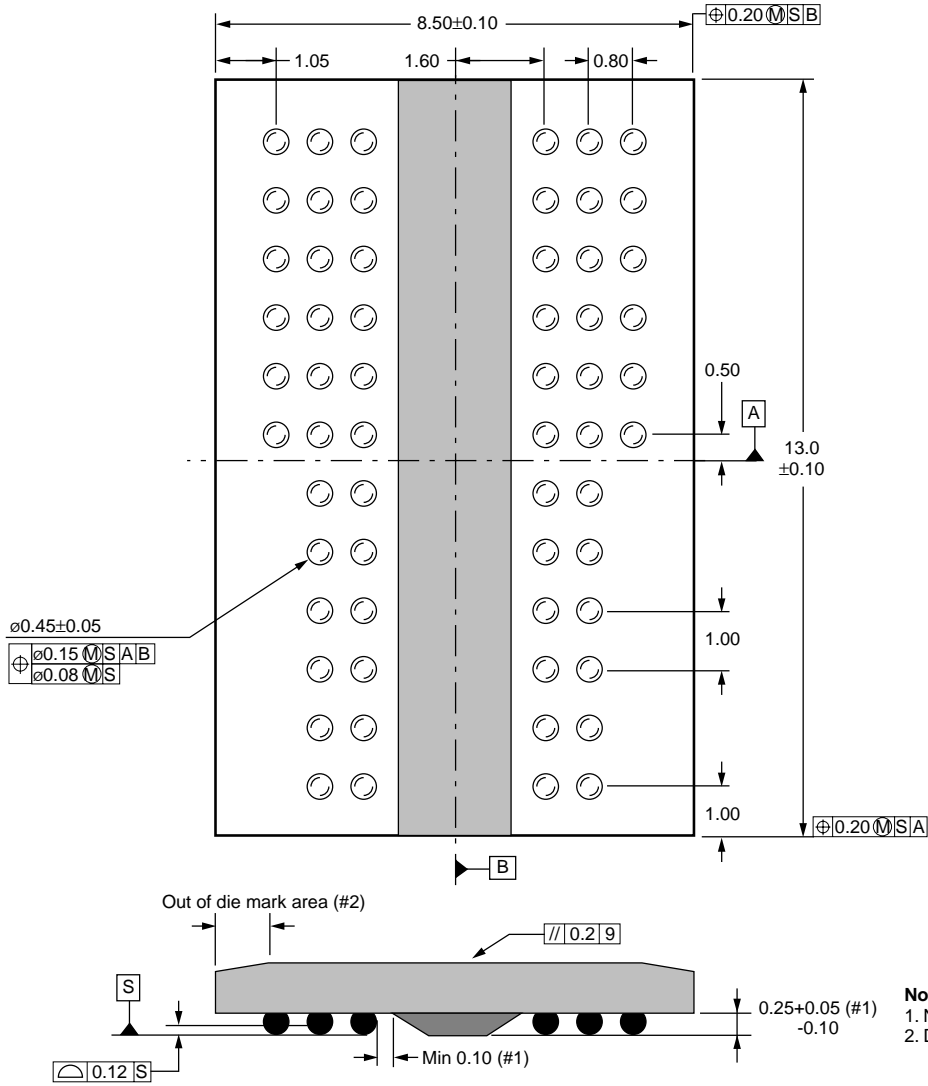
RA = Row Address                      BS = Bank Address  
 CA = Column Address                AP = Auto Precharge

**Notes for SDRAM function truth table:**

1. Current State is state of the bank determined by BS. All entries assume that CKE was active (HIGH) during the preceding clock cycle.
2. Illegal to bank in specified state; Function may be legal in the bank indicated by BS, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in Idle state. May precharge bank(s) indicated by BS (andAP).
5. Illegal if any bank is not Idle.
6. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
7. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
8. Must be legal command as defined in the SDRAM function truth table.

**Package Diagram**

**60-Pin WBGA**



- Notes:**
1. No bond figure exposed
  2. Do not measure // within this area

---

**MOSEL VITELIC WORLDWIDE OFFICES****V54C3128(16/80/40)4V(BGA)****U.S.A.**

3910 NORTH FIRST STREET  
SAN JOSE, CA 95134  
PHONE: 408-433-6000  
FAX: 408-433-0952

**TAIWAN**

7F, NO. 102  
MIN-CHUAN E. ROAD, SEC. 3  
TAIPEI  
PHONE: 886-2-2545-1213  
FAX: 886-2-2545-1209

**SINGAPORE**

10 ANSON ROAD #23-13  
INTERNATIONAL PLAZA  
SINGAPORE 079903  
PHONE: 65-3231801  
FAX: 65-3237013

**UK & IRELAND**

SUITE 50, GROVEWOOD  
BUSINESS CENTRE  
STRATHCLYDE BUSINESS  
PARK  
BELLSHILL, LANARKSHIRE,  
SCOTLAND, ML4 3NQ  
PHONE: 44-1698-748515  
FAX: 44-1698-748516

NO 19 LI HSIN ROAD  
SCIENCE BASED IND. PARK  
HSIN CHU, TAIWAN, R.O.C.  
PHONE: 886-3-579-5888  
FAX: 886-3-566-5888

**JAPAN**

ONZE 1852 BUILDING 6F  
2-14-6 SHINTOMI, CHUO-KU  
TOKYO 104-0041  
PHONE: 03-3537-1400  
FAX: 03-3537-1402

**GERMANY  
(CONTINENTAL  
EUROPE & ISRAEL)**

BENZSTRASSE 32  
71083 HERRENBERG  
GERMANY  
PHONE: +49 7032 2796-0  
FAX: +49 7032 2796 22

**U.S. SALES OFFICES****NORTHWESTERN**

3910 NORTH FIRST STREET  
SAN JOSE, CA 95134  
PHONE: 408-433-6000  
FAX: 408-433-0952

**SOUTHWESTERN**

302 N. EL CAMINO REAL #200  
SAN CLEMENTE, CA 92672  
PHONE: 949-361-7873  
FAX: 949-361-7807

**CENTRAL,  
NORTHEASTERN &  
SOUTHEASTERN**

604 FIELDWOOD CIRCLE  
RICHARDSON, TX 75081  
PHONE: 214-352-3775  
FAX: 214-904-9029

---

The information in this document is subject to change without notice.

MOSEL VITELIC makes no commitment to update or keep current the information contained in this document. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of MOSEL-VITELIC.

MOSEL VITELIC subjects its products to normal quality control sampling techniques which are intended to provide an assurance of high quality products suitable for usual commercial applications. MOSEL VITELIC does not do testing appropriate to provide 100% product quality assurance and does not assume any liability for consequential or incidental arising from any use of its products. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such applications.