

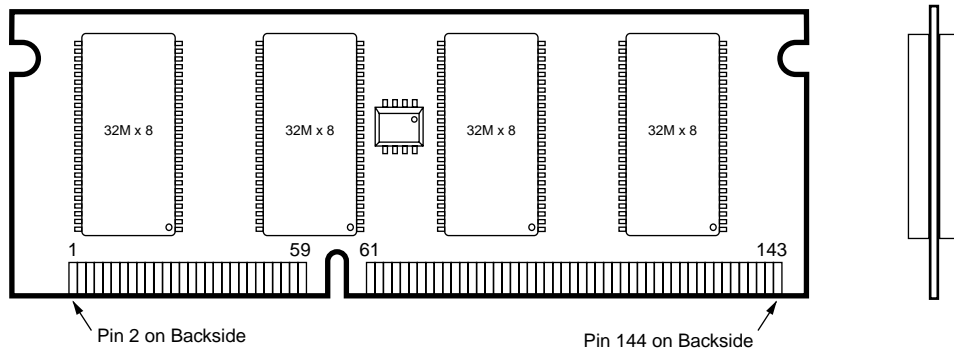
Features

- JEDEC-standard 144 pin, Small-Outline, Dual in line Memory Module (SODIMM)
- Serial Presence Detect with E²PROM
- Nonbuffered
- Fully Synchronous, All Signals Registered on Positive Edge of System Clock
- Single +3.3V (± 0.3V) Power Supply
- All Device Pins are LVTTTL Compatible
- 8192 Refresh Cycles every 64 ms
- Self-Refresh Mode
- Internal Pipelined Operation; Column Address can be changed every System Clock
- Programmable Burst Lengths: 1, 2, 4, 8
- Auto Precharge and Piecharge all Banks by A10
- Data Mask Function by DQM
- Mode Register Set Programming
- Programmable (CAS Latency:2, 3 Clocks)

Description

The V436632Z24V memory module is organized 33,554,432 x 64 bits in a 144 pin SODIMM. The 32M x 64 memory module uses 8 Mosel-Vitellic 32M x 8 SDRAM. The x64 modules are ideal for use in high performance computer systems where increased memory density and fast access times are required.

Part Number	Speed Grade	Configuration
V436632Z24VXTG-75PC	-75PC, CL=2,3 (133 MHz)	32M x 64
V436632Z24VXTG-75	-75, CL=3 (133 MHz)	32M x 64
V436632Z24VXTG-10PC	-10PC, CL=2,3 (100 MHz)	32M x 64



Pin Configurations (Front Side/Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	25	DQMB1	49	DQ13	73	NC	97	DQ22	121	DQ24
2	VSS	26	DQMB5	50	DQ45	74	CLK1	98	DQ54	122	DQ56
3	DQ0	27	VDD	51	DQ14	75	VSS	99	DQ23	123	DQ25
4	DQ32	28	VDD	52	DQ46	76	VSS	100	DQ55	124	DQ57
5	DQ1	29	A0	53	DQ15	77	NC	101	VDD	125	DQ26
6	DQ33	30	A3	54	DQ47	78	NC	102	VDD	126	DQ58
7	DQ2	31	A1	55	VSS	79	NC	103	A6	127	DQ27
8	DQ34	32	A4	56	VSS	80	NC	104	A7	128	DQ59
9	DQ3	33	A2	57	NC	81	VDD	105	A8	129	VDD
10	DQ35	34	A5	58	NC	82	VDD	106	BA0	130	VDD
11	VDD	35	VSS	59	NC	83	DQ16	107	VSS	131	DQ28
12	VDD	36	VSS	60	NC	84	DQ48	108	VSS	132	DQ60
13	DQ4	37	DQ8	61	CLK0	85	DQ17	109	A9	133	DQ29
14	DQ36	38	DQ40	62	CKE0	86	DQ49	110	BA1	134	DQ61
15	DQ5	39	DQ9	63	VDD	87	DQ18	111	A10	135	DQ30
16	DQ37	40	DQ41	64	VDD	88	DQ50	112	A11	136	DQ62
17	DQ6	41	DQ10	65	$\overline{\text{RAS}}$	89	DQ19	113	VDD	137	DQ31
18	DQ38	42	DQ42	66	$\overline{\text{CAS}}$	90	DQ51	114	VDD	138	DQ63
19	DQ7	43	DQ11	67	$\overline{\text{WE}}$	91	VSS	115	DQMB2	139	VSS
20	DQ39	44	DQ43	68	CKE1	92	VSS	116	DQMB6	140	VSS
21	VSS	45	VDD	69	$\overline{\text{CS0}}$	93	DQ20	117	DQMB3	141	SDA
22	VSS	46	VDD	70	A12	94	DQ52	118	DQMB7	142	SCL
23	DQMB0	47	DQ12	71	$\overline{\text{CS1}}$	95	DQ21	119	VSS	143	VDD
24	DQMB4	48	DQ44	72	NC	96	DQ53	120	VSS	144	VDD

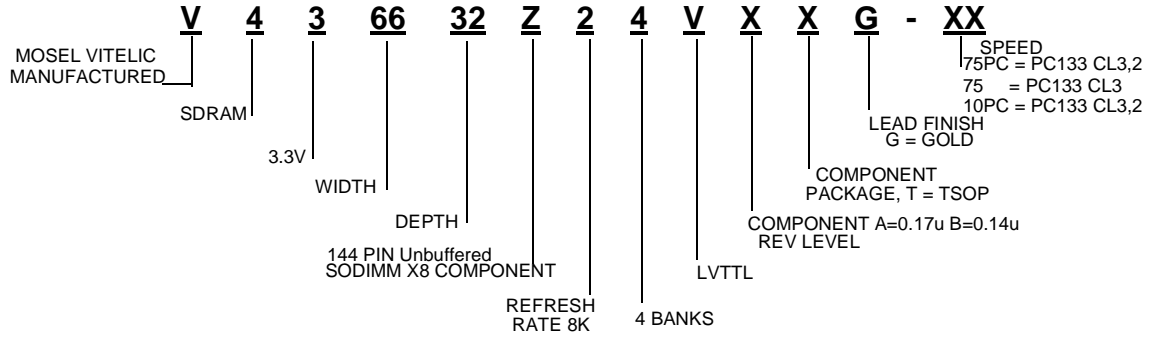
Note:

1. $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{CASx}}$, $\overline{\text{CSx}}$ are active low signals.

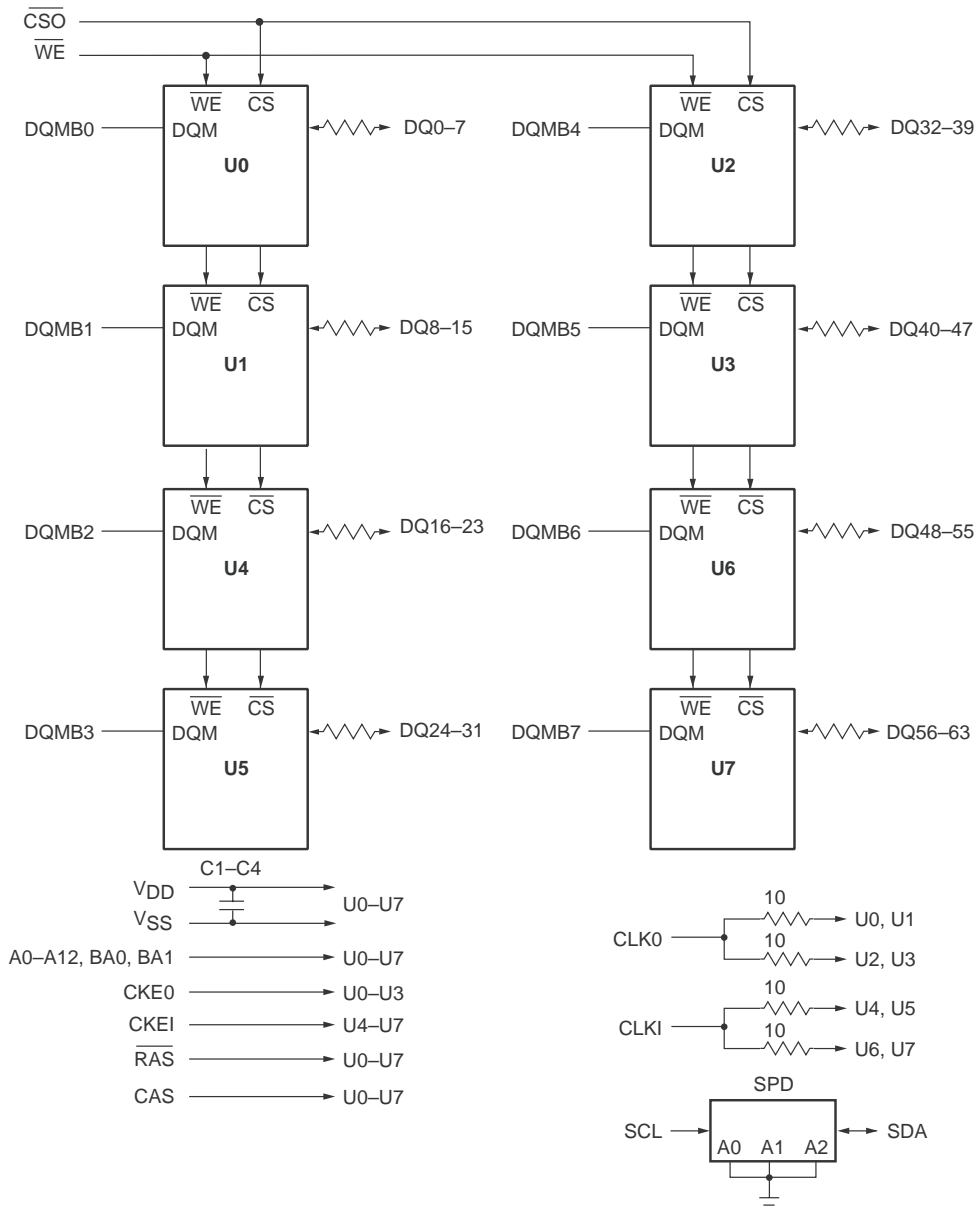
Pin Names

A0–A12, BA0, BA1	Address, Bank Select
DQ0–DQ63	Data Inputs/Outputs
$\overline{\text{RAS}}$	Row Address Strokes
$\overline{\text{CAS}}$	Column Address Strokes
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CS0}}$, $\overline{\text{CS1}}$	Chip Select
DQMB0–DQMB7	Output Enable
CKE0, CKE1	Clock Enable
CLK0, CLK1	Clock
SDA	Serial Input/Output
SCL	Serial Clock
VDD	Power Supply
VSS	Ground
NC	No Connect (Open)

Part Number Information



Block Diagram



Serial Presence Detect Information

A serial presence detect storage device - E²PROM - is assembled onto the module. Information about the module configuration, speed, etc. is

written into the E²PROM device during module production using a serial presence detect protocol (I²C synchronous 2-wire bus)

SPD-Table

Byte Number	Function Described	SPD Entry Value	Hex Value		
			-75PC	-75	-10PC
0	Number of SPD bytes	128	80	80	80
1	Total bytes in Serial PD	256	08	08	08
2	Memory Type	SDRAM	04	04	04
3	Number of Row Addresses (without BS bits)	13	0D	0D	0D
4	Number of Column Addresses (for x8 SDRAM)	10	0A	0A	0A
5	Number of DIMM Banks	1	01	01	01
6	Module Data Width	64	40	40	40
7	Module Data Width (continued)	0	00	00	00
8	Module Interface Levels	LVTTL	01	01	01
9	SDRAM Cycle Time at CL=3	7.5 ns/10.0 ns	75	75	A0
10	SDRAM Access Time from Clock at CL=3	5.4 ns/6.0 ns	54	54	60
11	Dimm Config (Error Det/Corr.)	none	00	00	00
12	Refresh Rate/Type	Self-Refresh,7.8µs	82	82	82
13	SDRAM width, Primary	x8	08	08	08
14	Error Checking SDRAM Data Width	n/a / x8	00	00	00
15	Minimum Clock Delay from Back to Back Random Column Address	t _{ccd} = 1 CLK	01	01	01
16	Burst Length Supported	1, 2, 4 & 8	0F	0F	0F
17	Number of SDRAM Banks	4	04	04	04
18	Supported $\overline{\text{CAS}}$ Latencies	CL =2, 3	06	06	06
19	$\overline{\text{CS}}$ Latencies	$\overline{\text{CS}}$ Latency = 0	01	01	01
20	$\overline{\text{WE}}$ Latencies	WL = 0	01	01	01
21	SDRAM DIMM Module Attributes	Non Buffered/Non Reg.	00	00	00
22	SDRAM Device Attributes: General	V _{cc} tol ± 10%	0E	0E	0E
23	Minimum Clock Cycle Time at $\overline{\text{CAS}}$ Latency = 2	7.5 ns/10.0 ns	75	A0	A0
24	Maximum Data Access Time from Clock for CL = 2	5.4 ns/6.0 ns	54	60	60
25	Minimum Clock Cycle Time at CL = 1	Not Supported	00	00	00
26	Maximum Data Access Time from Clock at CL = 1	Not Supported	00	00	00
27	Minimum Row Precharge Time	15 ns/20 ns	0F	14	14

SPD-Table

Byte Number	Function Described	SPD Entry Value	Hex Value		
			-75PC	-75	-10PC
28	Minimum Row Active to Row Active Delay t_{RRD}	14 ns/15 ns/16 ns	0E	0F	10
29	Minimum RAS to \overline{CAS} Delay t_{RCD}	15 ns/20 ns	0F	14	14
30	Minimum RAS Pulse Width t_{RAS}	42 ns/45 ns	2A	2D	2D
31	Module Bank Density (Per Bank)	256 Mbyte	40	40	40
32	SDRAM Input Setup Time	1.5 ns/2.0 ns	15	15	20
33	SDRAM Input Hold Time	0.8 ns/1.0 ns	08	08	10
34	SDRAM Data Input Setup Time	1.5 ns/2.0 ns	15	15	20
35	SDRAM Data Input Hold Time	0.8 ns/1.0 ns	08	08	10
62-61	Superset Information (May be used in Future)		00	00	00
62	SPD Revision	Revision 2/1.2	02	02	12
63	Checksum for Bytes 0 - 62		FD	42	B0
64	Manufacturer's JEDEC ID Code	Mosel Vitelic	40	40	40
65-71	Manufacturer's JEDEC ID Code (cont.)		00	00	00
72	Manufacturing Location	1 = US, 2 = Taiwan			
73-90	Module Part Number (ASCII)	V436632Z24V			
91-92	PCB Identification Code	Current PCB Revision			
93	Assembly Manufacturing Date (Year)	Binary Coded year (BCD)			
94	Assembly Manufacturing Date (Week)	Binary Coded week (BCD)			
95-98	Assembly Serial Number	byte 95 = LSB, byte 98 = MSB			
99-125	Reserved		00	00	00
126	Intel Specification for Frequency		64	64	64
127	Reserved		00	00	00
128+	Unused Storage Location		00	00	00

DC Characteristics

$T_A = 0^\circ\text{C}$ to 70°C ; $V_{SS} = 0\text{ V}$; $V_{DD}, V_{DDQ} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Limit Values		Unit
		Min.	Max.	
V_{IH}	Input High Voltage	2.0	$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage	-0.5	0.8	V
V_{OH}	Output High Voltage ($I_{OUT} = -4.0\text{ mA}$)	2.4	—	V
V_{OL}	Output Low Voltage ($I_{OUT} = 4.0\text{ mA}$)	—	0.4	V
$I_{I(L)}$	Input Leakage Current, any input ($0\text{ V} < V_{IN} < 3.6\text{ V}$, all other inputs = 0V)	-10	10	μA
$I_{O(L)}$	Output leakage current (DQ is disabled, $0\text{V} < V_{OUT} < V_{CC}$)	-10	10	μA

Capacitance

$T_A = 0^\circ\text{C}$ to 70°C ; $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$, $f = 1\text{ MHz}$

Symbol	Parameter	Limit Values (Max.)	Unit
C_{I1}	Input Capacitance (A0 to A11, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	40	pF
C_{I2}	Input Capacitance ($\overline{\text{CS0}}$, $\overline{\text{CS1}}$)	25	pF
C_{ICL}	Input Capacitance (CLK0-CLK1)	28	pF
C_{I3}	Input Capacitance (CKE0, CKE1)	20	pF
C_{I4}	Input Capacitance (DQMB0-DQMB7)	10	pF
C_{SC}	Input Capacitance (SCL, SA0-2)	8	pF
C_{IO}	Input/Output Capacitance	18	pF

Absolute Maximum Ratings

Parameter	Max.	Units
Voltage on VDD Supply Relative to V_{SS}	-1 to 4.6	V
Voltage on Input Relative to V_{SS}	-1 to 4.6	V
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to 125	°C
Power Dissipation	6.3	W

Standby and Refresh Currents¹

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Test Conditions	-75PC/75	-10PC	Unit	Note	
I_{CC1}	Operating Current	Burst length = 4, CL = 3 $t_{RC} > = t_{RC}(\text{min})$, $t_{CK} > = t_{CK}(\text{min})$, IO = 0 mA 2 Bank Interleave Operation	1840	1680	mA	1,2	
I_{CC2P}	Precharged Standby Current in Power Down Mode	$\text{CKE} < = V_{IL}(\text{max})$, $t_{CK} > = t_{CK}(\text{min})$	16	16	mA		
I_{CC2N}	Precharged Standby Current in Non-Power Down Mode	$\text{CKE} > = V_{IH}(\text{min})$, $t_{CK} > = t_{CK}(\text{min})$, Input changed once in 3 cycles	360	280	mA	$\overline{\text{CS}} = \text{High}$	
I_{CC3P}	Active Standby Current in Power Down Mode	$\text{CKE} < = V_{IL}(\text{max})$, $t_{CK} > = t_{CK}(\text{min})$	80	80	mA		
I_{CC3N}	Active Standby Current in Non-Power Down Mode	$\text{CKE} > = V_{IH}(\text{min})$, $t_{CK} > = t_{CK}(\text{min})$, Input changed one time	440	360	mA	$\overline{\text{CS}} = \text{High}$	
I_{CC4}	Burst Operating Current	Burst length = Full Page, $t_{RC} = \text{Infinite}$, CL = 3, $t_{CK} > = t_{CK}(\text{min})$, IO = 0 mA 2 Banks Activated	1200	960	mA	1, 2	
I_{CC5}	Auto Refresh Current	$t_{RC} > = t_{RC}(\text{min})$	1920	1760	mA	1,2	
I_{CC6}	Self Refresh Current	CKE = <0,2 V	Standard	24	24	mA	1,2
			L-Version	14	14		

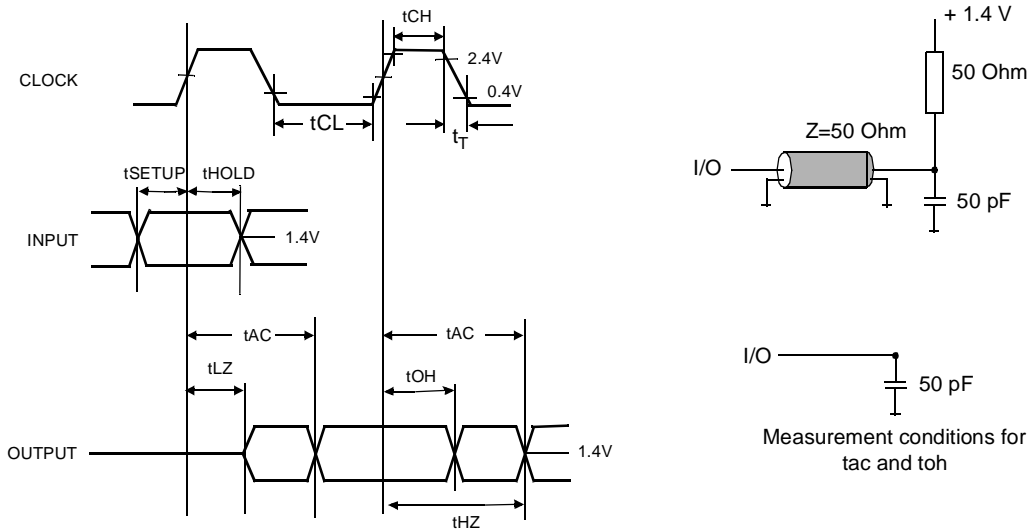
AC Characteristics ^{3,4}

T_A = 0° to 70°C; V_{SS} = 0V; V_{CC} = 3.3V ± 0.3V, t_T = 1 ns

#	Symbol	Parameter	Limit Values						Unit	Note
			-75PC		-75		-10PC			
			Min.	Max.	Min.	Max.	Min.	Max.		
Clock and Clock Enable										
1	t _{CK}	Clock Cycle Time CAS Latency = 3 CAS Latency = 2	7.5 7.5		7.5 10		10 10		ns ns	
2	f _{CK}	System frequency CAS Latency = 3 CAS Latency = 2	– –	133 133	– –	133 100	– –	100 100	MHz MHz	
3	t _{AC}	Clock Access Time CAS Latency = 3 CAS Latency = 2	– –	5.4 6	– –	5.4 6	– –	6 6	ns ns	4,5
4	t _{CH}	Clock High Pulse Width	2.5	–	2.5	–	3	–	ns	6
5	t _{CL}	Clock Low Pulse Width	2.5	–	2.5	–	3	–	ns	6
6	t _{CS}	Input Setup time	1.5	–	1.5	–	2	–	ns	7
7	t _{CH}	Input Hold Time	0.8	–	0.8	–	1	–	ns	7
8	t _{CKSP}	CKE Setup Time (Power down mode)	2.5	–	2.5	–	2	–	ns	8
9	t _{CKSR}	CKE Setup Time (Self Refresh Exit)	8	–	8	–	8	–	ns	9
10	t _T	Transition time (rise and fall)	1	–	1	–	1	–	ns	
Common Parameters										
11	t _{RCD}	RAS to CAS delay	20	–	20	–	20	–	ns	
12	t _{RC}	Cycle Time	70	120k	70	120k	70	120k	ns	
13	t _{RAS}	Active Command Period	42	–	45	–	45	–	ns	
14	t _{RP}	Precharge Time	15	–	20	–	20	–	ns	
15	t _{RRD}	Bank to Bank Delay Time	14	–	15	–	20	–	ns	
16	t _{CCD}	CAS to CAS delay time (same bank)	1	–	1	–	1	–	CLK	
Refresh Cycle										
17	t _{SREX}	Self Refresh Exit Time	10	–	10	–	10	–	ns	9
18	t _{REF}	Refresh Period (8192 cycles)	64	–	64	–	64	–	ms	8
Read Cycle										
19	t _{OH}	Data Out Hold Time	3	–	3	–	3	–	ns	4
20	t _{LZ}	Data Out to Low Impedance Time	0	–	0	–	0	–	ns	
21	t _{HZ}	Data Out to High Impedance Time	3	7.5	3	7.5	3	8	ns	10
22	t _{DQZ}	DQM Data Out Disable Latency	2	-	2	-	2	-	CLK	
Write Cycle										
23	t _{DPL}	Data input to Precharge (write recovery)	2	–	2	–	1	–	CLK	
24	t _{DAL}	Data In to Active/refresh	5	–	5	–	5	–	CLK	11
25	t _{DQW}	DQM Write Mask Latency	0	–	0	–	0	–	CLK	

Notes:

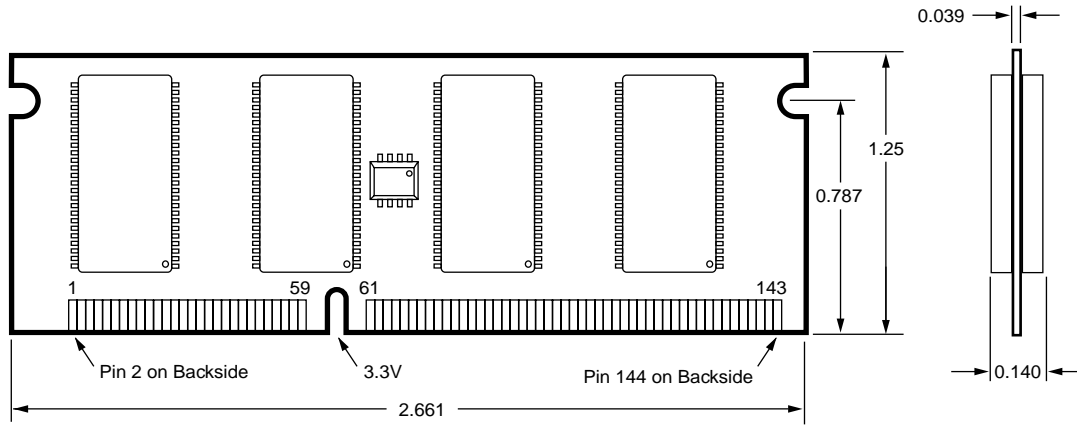
1. The specified values are valid when addresses are changed no more than once during $t_{CK}(\text{min.})$ and when No Operation commands are registered on every rising clock edge during $t_{RC}(\text{min.})$. Values are shown per module bank.
2. The specified values are valid when data inputs (DQ's) are stable during $t_{RC}(\text{min.})$.
3. All AC characteristics are shown for device level.
An initial pause of 100 μs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
4. AC timing tests have $V_{IL} = 0.4\text{V}$ and $V_{IH} = 2.4\text{V}$ with the timing referenced to the 1.4V crossover point. The transition time is measured between V_{IH} and V_{IL} . All AC measurements assume $t_T = 1 \text{ ns}$ with the AC output load circuit shown. Specific t_{ac} and t_{oh} parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0V.



5. If clock rising time is longer than 1 ns, a time $(t_T/2 - 0.5)$ ns has to be added to this parameter.
6. Rated at 1.5V
7. If t_T is longer than 1 ns, a time $(t_T - 1)$ ns has to be added to this parameter.
8. Any time that the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.
9. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
10. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.
11. t_{DAL} is equivalent to $t_{DPL} + t_{RP}$.

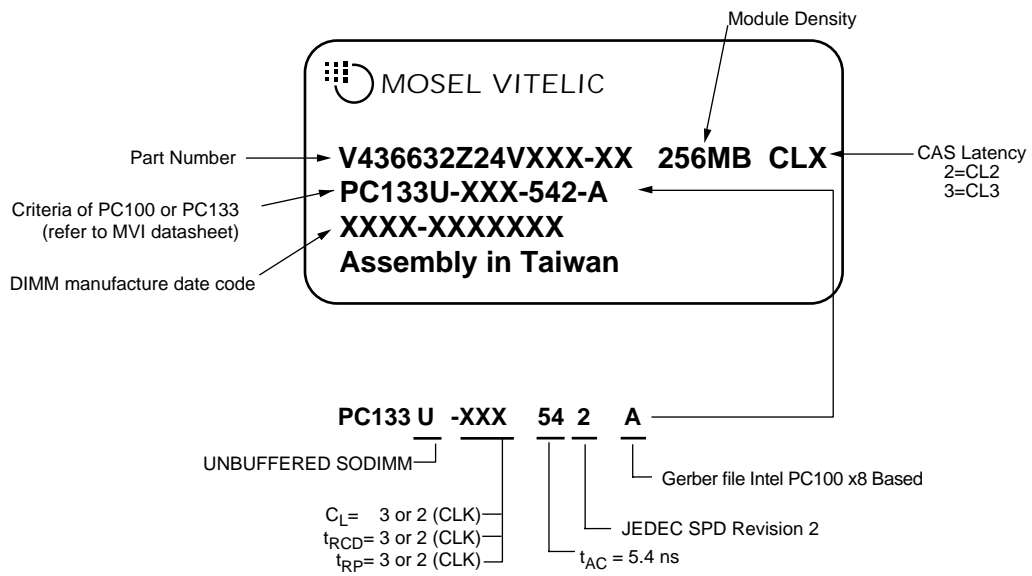
Package Diagram

144 Pin SODIMM



NOTE:
1. All dimensions in inches.
Tolerances ± 0.005 unless otherwise specified.

Module Label Information



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