

|                                | 45     | 50      | 55      | 60      |
|--------------------------------|--------|---------|---------|---------|
| System Frequency ( $f_{CK}$ )  | 225MHz | 200 MHz | 183 MHz | 166 MHz |
| Clock Cycle Time ( $t_{CK3}$ ) |        | 5 ns    | 5.5 ns  | 6 ns    |
| Clock Cycle Time ( $t_{CK4}$ ) | 4.5 ns |         |         |         |

**Features**

- 4 banks x 512K x 32 organization
- High speed data transfer rates with system frequency up to 225 MHz
- Data Mask for Write Control (DM)
- Four Banks controlled by BA0 & BA1
- Programmable CAS Latency: 3, 4
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:  
2, 4, 8 full page for Sequential Type  
2, 4, 8 full page for Interleave Type
- Automatic and Controlled Precharge Command
- Suspend Mode and Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 2048 cycles/16ms
- Available in 100-pin TQFP
- SSTL-2 Compatible I/Os
- Double Data Rate (DDR)
- Bidirectional Data Strobe (DQs) for input and output data, active on both edges
- On-Chip DLL aligns DQ and DQs transitions with CLK transitions
- Differential clock inputs CLK and  $\overline{CLK}$
- Power Supply 3.3V  $\pm$  0.3V

**Description**

The V58C3643204SAT is a four bank DDR DRAM organized as 4 banks x 512K x 32. The V58C3643204SAT achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock

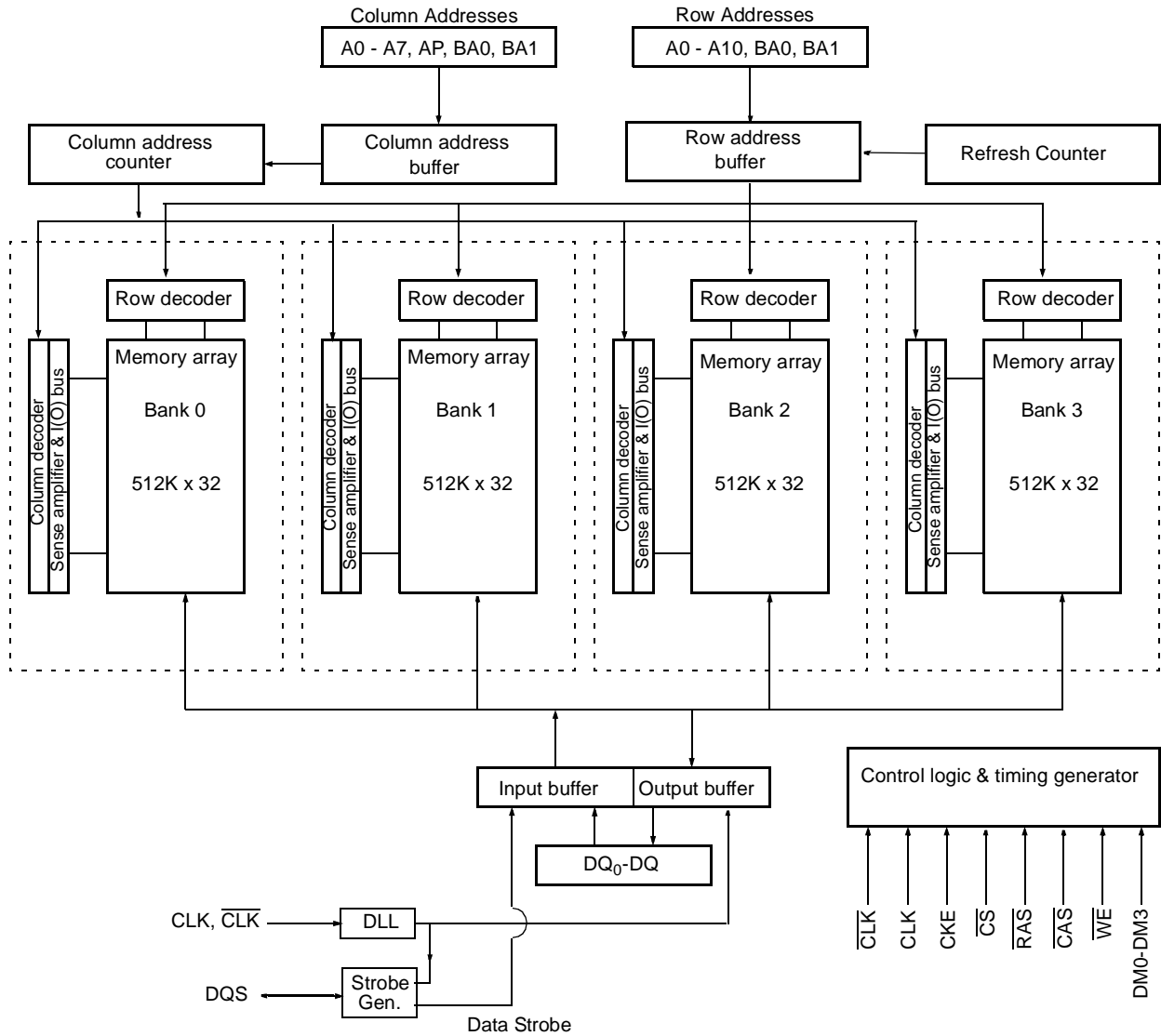
All of the control, address, circuits are synchronized with the positive edge of an externally supplied clock. I/O transactions are possible on both edges of DQS.

Operating the four memory banks in an interleaved fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

**Device Usage Chart**

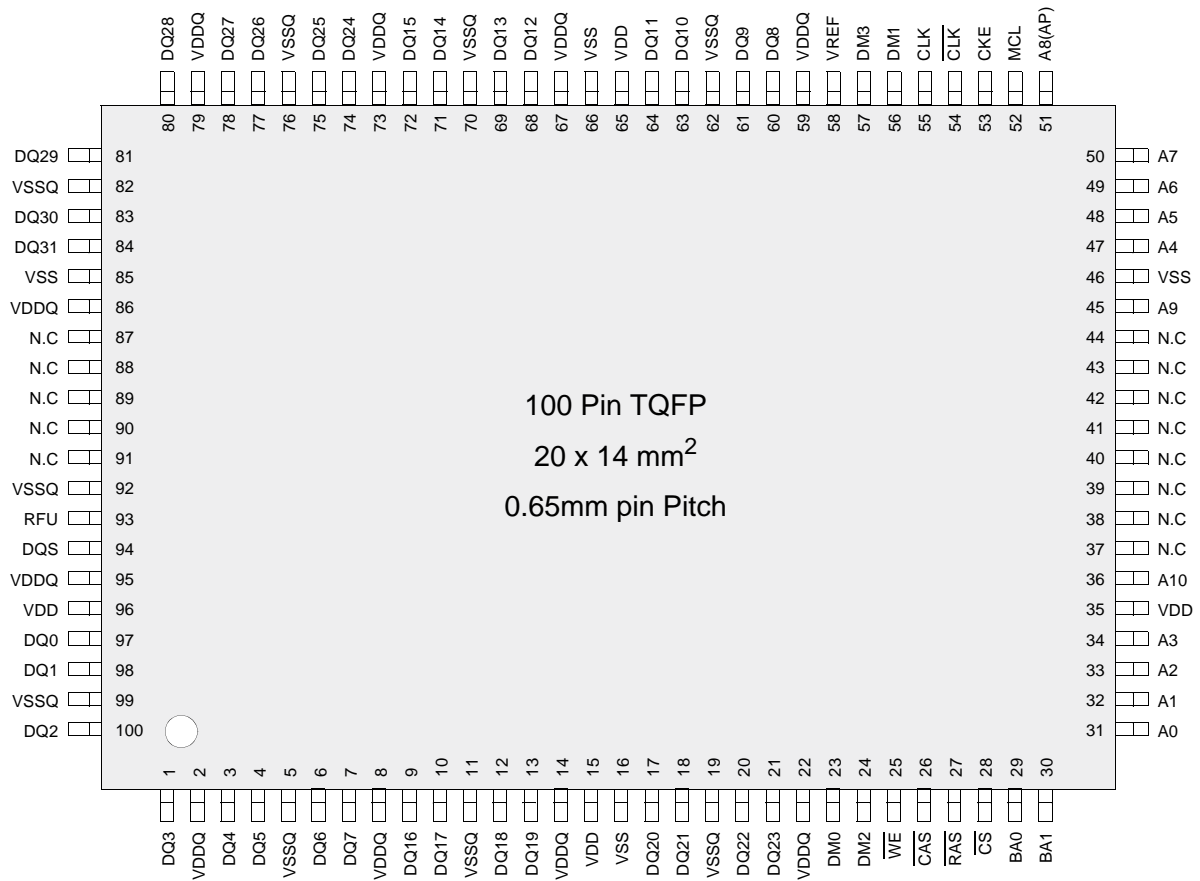
| Operating Temperature Range | Package Outline | CLK Cycle Time (ns) |     |     |     | Power |   | Temperature Mark |
|-----------------------------|-----------------|---------------------|-----|-----|-----|-------|---|------------------|
|                             | 100-pin TQFP    | -45                 | -50 | -55 | -60 | Std.  | L |                  |
| 0°C to 70°C                 | •               | •                   | •   | •   | •   | •     | • | Blank            |

Block Diagram



**100 Pin TQFP  
PIN CONFIGURATION**

**Top View**



**Pin Names**

|                                 |                             |
|---------------------------------|-----------------------------|
| CLK, $\overline{\text{CLK}}$    | Differential Clock Input    |
| CKE                             | Clock Enable                |
| $\overline{\text{CS}}$          | Chip Select                 |
| $\overline{\text{RAS}}$         | Row Address Strobe          |
| $\overline{\text{CAS}}$         | Column Address Strobe       |
| $\overline{\text{WE}}$          | Write Enable                |
| DQS                             | Data Strobe (Bidirectional) |
| A <sub>0</sub> -A <sub>10</sub> | Address Inputs              |
| BA0, BA1                        | Bank Select                 |

|                                  |                              |
|----------------------------------|------------------------------|
| DQ <sub>0</sub> -DQ <sub>7</sub> | Data Input/Output            |
| DM0-DM3                          | Data Mask                    |
| V <sub>DD</sub>                  | Power (3.3V ± 0.3V)          |
| V <sub>SS</sub>                  | Ground                       |
| V <sub>DDQ</sub>                 | Power for I/O's (+2.5V)      |
| V <sub>SSQ</sub>                 | Ground for I/O's             |
| NC                               | Not connected                |
| VREF                             | Reference Voltage for Inputs |
| RFU                              | Reserved for future use.     |

**Signal Pin Description**

| Pin  | Type             | Signal | Polarity      | Function  |
|--|------------------|--------|---------------|---|
| CLK<br>CLK   | Input            | Pulse  | Positive Edge | The system clock input. All inputs except DQs and DMs are sampled on the rising edge of CLK.  |
| CKE  | Input            | Level  | Active High   | Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode, Suspend mode, or the Self Refresh mode.   |
| $\overline{CS}$  | Input            | Pulse  | Active Low    | $\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.   |
| $\overline{RAS}$ , $\overline{CAS}$<br>$\overline{WE}$ | Input            | Pulse  | Active Low    | When sampled at the positive rising edge of the clock, $\overline{CAS}$ , $\overline{RAS}$ , and $\overline{WE}$ define the command to be executed by the SDRAM.  |
| DQS  | Input/<br>Output | Pulse  | Active High   | Active on both edges for data input and output.<br>Center aligned to input data<br>Edge aligned to output data  |
| A0 - A10   | Input            | Level  | —             | During a Bank Activate command cycle, A0-A10 defines the row address (RA0-RA10) when sampled at the rising clock edge.<br>During a Read or Write command cycle, A0-An defines the column address (CA0-CAn) when sampled at the rising clock edge. CAn depends from the SDRAM organization:<br>2M x 32 SDRAM CAn = CA7 (Page)<br><br>In addition to the column address, A8 is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A8 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A8 is low, autoprecharge is disabled.<br>During a Precharge command cycle, A8(=AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged simultaneously regardless of state of BA0 and BA1. |
| BA0,<br>BA1  | Input            | Level  | —             | Selects which bank is to be active.   |
| DQx  | Input/<br>Output | Level  | —             | Data Input/Output pins operate in the same manner as on conventional DRAMs.   |
| DM0-DM3  | Input            | Pulse  | Active High   | In Write mode, DM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if is high.  |
| VDD, VSS   | Supply           |        |               | Power and ground for the input buffers and the core logic.  |
| VDDQ<br>VSSQ   | Supply           | —      | —             | Isolated power supply and ground for the output buffers to provide improved noise immunity.   |
| VREF   | Input            | Level  | —             | SSTL Reference Voltage for Inputs   |

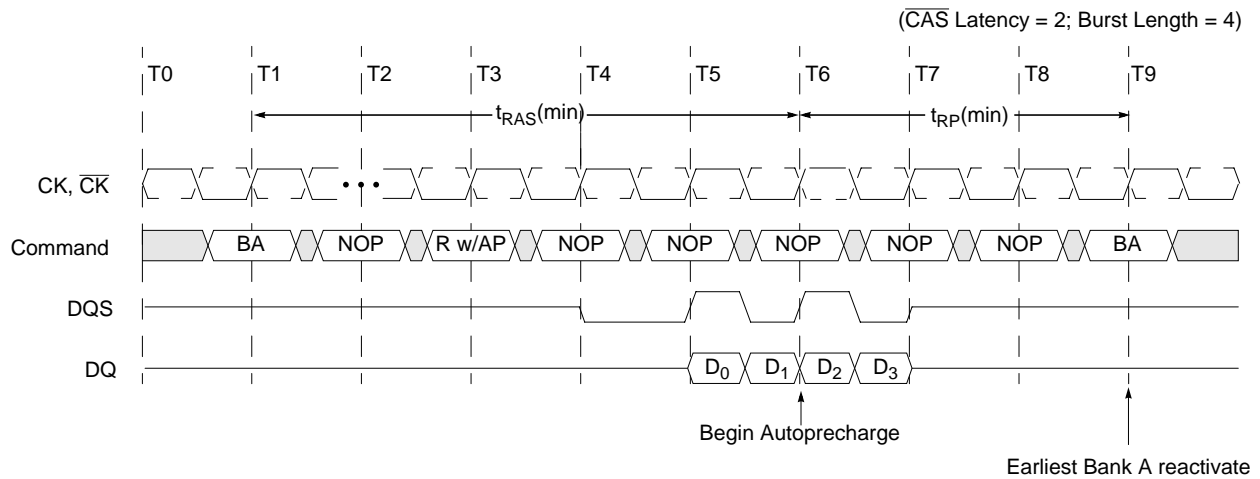
**Auto Precharge Operation**

The Auto Precharge operation can be issued by having column address  $A_8$  high when a Read or Write command is issued. If  $A_{10}$  is low when a Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. When the Auto Precharge command is activated, the active bank automatically begins to precharge at the earliest possible moment during the Read or Write cycle once  $t_{RAS}(min)$  is satisfied.

**Read with Auto Precharge**

If a Read with Auto Precharge command is initiated, the DDR SDRAM will enter the precharge operation N-clock cycles measured from the last data of the burst read cycle where N is equal to the CAS latency programmed into the device. Once the autoprecharge operation has begun, the bank cannot be reactivated until the minimum precharge time ( $t_{RP}$ ) has been satisfied.

**Read with Autoprecharge Timing**



**DC Characteristics**

Recommended operating conditions Unless Otherwise Noted,  $T_A=0$  to  $70^\circ\text{C}$

| Parameter   | Symbol     | Test Condition  | Version |     |     |     | Unit | Note |
|---|------------|---|---------|-----|-----|-----|------|------|
|   |            |   | -45     | -50 | -55 | -60 |      |      |
| Operating Current<br>(One Bank Active)              | $I_{CC1}$  | Burst Lenth = $2 t_{RC} \dot{\bar{S}} t_{RC(min)}$<br>$I_{OL}= 0mA, t_{CC} = t_{CC(min)}$           | 350     | 340 | 330 | 330 | mA   | 1    |
| Precharge Standby Current in<br>Power-down mode     | $I_{CC2P}$ | $CKE \dot{\bar{0}} V_{IL(max)}, t_{CC} = t_{CC(min)}$   | 60      |     |     |     | mA   |      |
| Precharge Standby Current in Non<br>Power-down mode | $I_{CC2N}$ | $CKE \dot{\bar{0}} V_{IH(min)}, \overline{CS} \dot{\bar{S}} V_{IH(min)},$<br>$t_{CC} = t_{CC(min)}$ | 165     | 160 | 155 | 150 | mA   |      |
| Active Standby Current power-down mode              | $I_{CC3P}$ | $CKE \dot{\bar{0}} V_{IL(max)}, t_{CC} = t_{CC(min)}$   | 95      |     |     |     | mA   |      |
| Active Standby Current in in Non<br>Power-down mode | $I_{CC3N}$ | $CKE \dot{\bar{S}} V_{IH(min)}, \overline{CS} \dot{\bar{S}} V_{IH(min)},$<br>$t_{CC} = t_{CC(min)}$ | 205     | 200 | 195 | 190 | mA   |      |
| Operating Current<br>(Burst Mode)                   | $I_{CC4}$  | $I_{OL} = 0mA, t_{CC} = t_{CC(min)},$<br>Page Burst, All Banks activated                            | 470     | 450 | 430 | 410 | mA   | 1    |
| Refresh Current                                     | $I_{CC5}$  | $t_{RC} \dot{\bar{S}} t_{RFC(min)}$   | 470     | 450 | 430 | 410 | mA   | 2    |
| Self Refresh Current                                | $I_{CC6}$  | $CKE \dot{\bar{0}} 0.2V$  | 4       |     |     |     | mA   |      |

- Notes:** 1. Measured with outputs open.  
2. Refresh period is 16ms.

**Absolute Maximum Ratings**

| Parameter                                       | Symbol            | Value      | Unit             |
|---|-------------------|------------|------------------|
| Voltage on any pin relative to $V_{SS}$         | $V_{IN}, V_{OUT}$ | -1.0 ~ 4.6 | V                |
| Voltage on $V_{DD}$ supply relative to $V_{SS}$ | $V_{DD}, V_{DDQ}$ | -1.0 ~ 4.6 | V                |
| Storage temperature                             | $T_{STG}$         | -55 ~ +150 | $^\circ\text{C}$ |
| Power dissipation                               | $P_D$             | 1.6        | W                |
| Short circuit current                           | $I_{OS}$          | 50         | mA               |

**Note:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.  
Functional operation should be restricted to recommended operating condition.  
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**Power & DC Operating Conditions (SSTL\_2 In/Out)**

Recommended operating conditions (Voltage referenced to  $V_{SS}=0V$ ,  $T_A=0$  to  $65^\circ C$ )

| Parameter                                    | Symbol    | Min                  | Typ       | Max                  | Unit    |
|--|-----------|----------------------|-----------|----------------------|---------|
| Device Supply voltage                        | $V_{DD}$  | 3.135                | 3.3       | 3.465                | V       |
| Output Supply voltage                        | $V_{DDQ}$ | 2.375                | 2.50      | 2.625                | V       |
| Reference voltage                            | $V_{REF}$ | $0.49 \cdot V_{DDQ}$ | -         | $0.51 \cdot V_{DDQ}$ | V       |
| Termination voltage                          | $V_{tt}$  | $V_{REF}-0.04$       | $V_{REF}$ | $V_{REF}+0.04$       | V       |
| Input logic high voltage                     | $V_{IH}$  | $V_{REF}+0.15$       | -         | $V_{DDQ}+0.30$       | V       |
| Input logic low voltage                      | $V_{IL}$  | -0.30                | -         | $V_{REF}-0.15$       | V       |
| Output logic high voltage $I_{OH} = -15.2mA$ | $V_{OH}$  | $V_{tt}+0.76$        | -         | -                    | V       |
| Output logic low voltage                     | $V_{OL}$  | -                    | -         | $V_{tt}-0.76$        | V       |
| Input leakage current                        | $I_{IL}$  | -5                   | -         | 5                    | $\mu A$ |
| Output leakage current                       | $I_{OL}$  | -5                   | -         | 5                    | $\mu A$ |

**AC Input Operating Conditions**

Recommended operating conditions

(Voltage referenced to  $V_{SS}=0V$ ,  $V_{DD}=3.3V \pm 5\%$ ,  $V_{DDQ}=2.5V \pm 5\%$ ,  $T_A=0$  to  $65^\circ C$ )

| Parameter  | Symbol   | Min                     | Typ | Max                     | Unit |
|--|----------|-------------------------|-----|-------------------------|------|
| Input High (Logic 1) Voltage; DQ                           | $V_{IH}$ | $V_{REF}+0.35$          | -   | -                       | V    |
| Input Low (Logic 0) Voltage; DQ                            | $V_{IL}$ | -                       | -   | $V_{REF}-0.35$          | V    |
| Clock Input Differential Voltage; CK and $\overline{CK}$   | $V_{ID}$ | 0.7                     | -   | $V_{DDQ}+0.6$           | V    |
| Clock Input Crossing Point Voltage; CK and $\overline{CK}$ | $V_{IX}$ | $0.5 \cdot V_{DDQ}-0.2$ | -   | $0.5 \cdot V_{DDQ}+0.2$ | V    |

**SSTL\_2 AC Test Conditions**

| Symbol            | Parameter                               | Value               | Units | Notes |
|-------------------|---|---------------------|-------|-------|
| $V_{REF}$         | Input Reference Voltage                 | $0.5 \cdot V_{DDQ}$ | V     | 1     |
| $V_{SWING} (max)$ | Input Signal Maximum Peak to Peak Swing | 1.5                 | V     | 1, 2  |
| SLEW              | Input Signal Minimum Slew Rate          | 1.0                 | V/ns  | 3     |

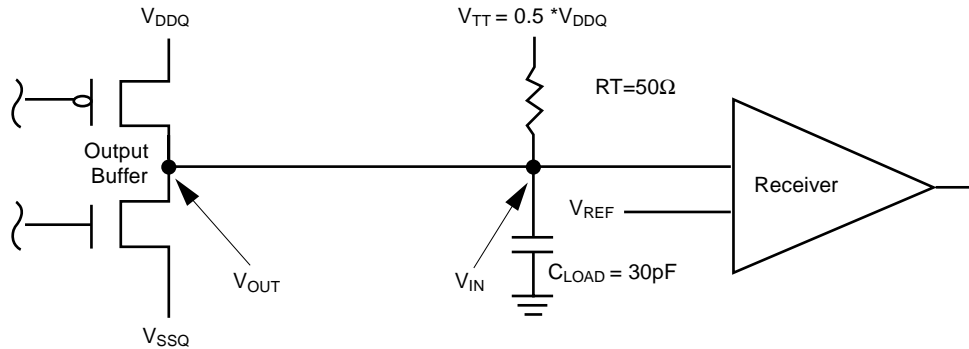
- Notes:**
1. Input waveform timing is referenced to the input signal crossing the  $V_{REF}$  level applied to the device.
  2. Compliant devices must still meet the  $V_{IH}$  (AC) and  $V_{IL}$  (AC) specifications under actual use conditions.
  3. The 1 V/ns input signal minimum slew rate is to be maintained in the  $V_{IL} \text{ max}$  (AC) to  $V_{IL} \text{ min}$  (AC) range of the input signal swing.

**SSTL\_2 Output Buffers**

The input voltage provided to the receiver depends on three parameters:

- $V_{DDQ}$  and current drive capabilities of the output buffer
- Termination voltage
- Termination resistance
- $V_{DDQ} \delta V_{DD}$

**Class II SSTL\_2 Output Buffer (Driver)**



**Capacitance** ( $V_{DD} = 3.3V, T_A = 25^\circ C, f = 1MHz$ )

| Parameter   | Symbol    | Min | Max | Unit |
|---|-----------|-----|-----|------|
| Input capacitance ( $A_0 \sim A_{10}, BA_0 \sim BA_1$ )   | $C_{IN1}$ | 2.5 | 4.5 | pF   |
| Input capacitance<br>( $CK, \overline{CK}, CKE, \overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE}$ ) | $C_{IN2}$ | 2.5 | 5.0 | pF   |
| Data & DQS input/output capacitance ( $DQ_0 \sim DQ_{31}$ )   | $C_{OUT}$ | 2.5 | 5.5 | pF   |
| Input capacitance ( $DM0 \sim DM3$ )  | $C_{IN3}$ | 2.5 | 5.5 | pF   |



**AC Characteristics**

| Parameter                                 |      | Symbol      | -45   |       | -50                           |       | -55                           |       | -60                           |       | Unit     |
|---|------|-------------|-------|-------|-------------------------------|-------|-------------------------------|-------|-------------------------------|-------|----------|
|   |      |             | Min   | Max   | Min                           | Max   | Min                           | Max   | Min                           | Max   |          |
| CK cycle time                             | CL=3 | $t_{CK}$    | •     | 7     | 5.0                           | 7     | 5.5                           | 7     | 6.0                           | 7     | ns       |
|   | CL=4 |             | 4.5   | •     | •                             | •     | •                             | •     | •                             | •     | ns       |
| CK high level width                       |      | $t_{CH}$    |       |       | 0.45                          | 0.55  | 0.45                          | 0.55  | 0.45                          | 0.55  | $t_{CK}$ |
| CK low level width                        |      | $t_{CL}$    |       |       | 0.45                          | 0.55  | 0.45                          | 0.55  | 0.45                          | 0.55  | $t_{CK}$ |
| DQS out access time from CK               |      | $t_{DQSCK}$ | -0.70 | +0.70 | -0.70                         | +0.70 | -0.75                         | +0.75 | -0.75                         | +0.75 | ns       |
| Output access time from CK                |      | $t_{AC}$    | -0.70 | +0.70 | -0.70                         | +0.70 | -0.75                         | +0.75 | -0.75                         | +0.75 | ns       |
| Data strobe edge to output data edge      |      | $t_{DQSQ}$  |       |       | -                             | 0.5   | -                             | 0.5   | -                             | 0.5   | ns       |
| Read preamble                             |      | $t_{RPRE}$  |       |       | 0.9                           | 1.1   | 0.9                           | 1.1   | 0.9                           | 1.1   | $t_{CK}$ |
| Read postamble                            |      | $t_{RPST}$  |       |       | 0.4                           | 0.6   | 0.4                           | 0.6   | 0.4                           | 0.6   | $t_{CK}$ |
| CK to valid DQS-in                        |      | $t_{DQSS}$  |       |       | 0.75                          | 1.25  | 0.75                          | 1.25  | 0.75                          | 1.25  | $t_{CK}$ |
| DQS-In setup time                         |      | $t_{WPRES}$ |       |       | 0                             | -     | 0                             | -     | 0                             | -     | ns       |
| DQS-in hold time                          |      | $t_{WPREH}$ |       |       | 0.25                          | -     | 0.25                          | -     | 0.25                          | -     | $t_{CK}$ |
| DQS write postamble                       |      | $t_{WPST}$  |       |       | 0.4                           | 0.6   | 0.4                           | 0.6   | 0.4                           | 0.6   | $t_{CK}$ |
| DQS-In high level width                   |      | $t_{DQSH}$  |       |       | 0.4                           | 0.6   | 0.4                           | 0.6   | 0.4                           | 0.6   | $t_{CK}$ |
| DQS-In low level width                    |      | $t_{DQSL}$  |       |       | 0.4                           | 0.6   | 0.4                           | 0.6   | 0.4                           | 0.6   | $t_{CK}$ |
| Address and Control input setup time      |      | $t_{IS}$    |       |       | 1.2                           | -     | 1.2                           | -     | 1.2                           | -     | ns       |
| Address and Control input hold time       |      | $t_{IH}$    |       |       | 0.9                           | -     | 0.9                           | -     | 0.9                           | -     | ns       |
| DQ and DM setup time to DQS               |      | $t_{DS}$    |       |       | 0.5                           | -     | 0.5                           | -     | 0.5                           | -     | ns       |
| DQ and DM hold time to DQS                |      | $t_{DH}$    |       |       | 0.5                           | -     | 0.5                           | -     | 0.5                           | -     | ns       |
| Clock half period                         |      | $t_{HP}$    |       |       | $t_{CLmin}$ or<br>$t_{CHmin}$ | -     | $t_{CLmin}$ or<br>$t_{CHmin}$ | -     | $t_{CLmin}$ or<br>$t_{CHmin}$ | -     | ns       |
| Output DQS valid window                   |      | $t_{QH}$    |       |       | $t_{HP}$ -<br>0.75ns          | -     | $t_{HP}$ -<br>0.75ns          | -     | $t_{HP}$ -<br>0.75ns          | -     | ns       |
| Row cycle time                            |      | $t_{RC}$    | 58    |       | 60                            |       | 60.5                          |       | 60                            |       | ns       |
| Refresh row cycle time                    |      | $t_{RFC}$   | 69    |       | 70                            |       | 71.5                          |       | 72                            |       | ns       |
| Row active time                           |      | $t_{RAS}$   |       |       | 40                            | 100K  | 44                            | 100K  | 48                            | 100K  | ns       |
| RAS to CAS delay                          |      | $t_{RCD}$   | 18    |       | 20                            |       | 22                            |       | 24                            |       | ns       |
| Row precharge time                        |      | $t_{RP}$    | 12    |       | 20                            |       | 16.5                          |       | 18                            |       | ns       |
| Row active to Row active delay            |      | $t_{RRD}$   | 9     |       | 14                            |       | 11                            |       | 12                            |       | ns       |
| Last data in to Row precharge             |      | $t_{WR}$    | 2     |       | 2                             |       | 2                             |       | 2                             |       | $t_{CK}$ |
| Last data in to Read command delay        |      | $t_{CDLR}$  | 2     |       | 2                             |       | 2                             |       | 2                             |       | $t_{CK}$ |
| Col. address to Col. address delay        |      | $t_{CCD}$   | 1     |       | 1                             |       | 1                             |       | 1                             |       | $t_{CK}$ |
| Mode register set cycle time              |      | $t_{MRD}$   | 2     |       | 2                             |       | 2                             |       | 2                             |       | $t_{CK}$ |
| Power down exit time                      |      | $t_{PEDX}$  |       |       | $1t_{CK}+t_{IS}$              |       | $1t_{CK}+t_{IS}$              |       | $1t_{CK}+t_{IS}$              |       | ns       |
| Self refresh exit to active command delay |      | $t_{XSA}$   | 69    |       | 70                            |       | 71.5                          |       | 72                            |       | ns       |
| Self refresh exit to read command delay   |      | $t_{XSR}$   |       |       | 200                           |       | 200                           |       |                               | 200   | $t_{CK}$ |
| Auto precharge write recovery + Precharge |      | $t_{DAL}$   | 6     |       | 6                             |       | 5                             |       | 5                             |       | $t_{CK}$ |
| Refresh interval time                     |      | $t_{REF}$   |       |       | 7.8                           |       | 7.8                           |       | 7.8                           |       | $\mu s$  |

## AC Characteristics

## V58C3643204SAT-45

| Frequency      | Cas Latency | t <sub>RC</sub> | t <sub>RFC</sub> | t <sub>RAS</sub> | t <sub>RCDRD</sub> | t <sub>RCDWR</sub> | t <sub>RP</sub> | t <sub>RRD</sub> | Unit            |
|----------------|-------------|-----------------|------------------|------------------|--------------------|--------------------|-----------------|------------------|-----------------|
| 250MHz (4.5ns) | 4           | 13              | 15               | 9                | 4                  | 2                  | 4               | 2                | t <sub>CK</sub> |
| 222MHz (5.0ns) | 3           | 12              | 14               | 8                | 4                  | 2                  | 4               | 2                | t <sub>CK</sub> |
| 183MHz (5.5ns) | 3           | 12              | 14               | 8                | 4                  | 2                  | 4               | 2                | t <sub>CK</sub> |
| 166MHz (6.0ns) | 3           | 10              | 12               | 7                | 3                  | 2                  | 3               | 2                | t <sub>CK</sub> |
| 143MHz (7.0ns) | 3           | 9               | 11               | 6                | 3                  | 2                  | 3               | 2                | t <sub>CK</sub> |

## V58C3643204SAT-50

| Frequency      | Cas Latency | t <sub>RC</sub> | t <sub>RFC</sub> | t <sub>RAS</sub> | t <sub>RCDRD</sub> | t <sub>RCDWR</sub> | t <sub>RP</sub> | t <sub>RRD</sub> | Unit            |
|----------------|-------------|-----------------|------------------|------------------|--------------------|--------------------|-----------------|------------------|-----------------|
| 200MHz (5.0ns) | 3           | 12              | 14               | 8                | 4                  | 2                  | 4               | 2                | t <sub>CK</sub> |
| 183MHz (5.5ns) | 3           | 12              | 14               | 8                | 4                  | 2                  | 4               | 2                | t <sub>CK</sub> |
| 166MHz (6.0ns) | 3           | 10              | 12               | 7                | 3                  | 2                  | 3               | 2                | t <sub>CK</sub> |
| 143MHz (7.0ns) | 3           | 9               | 11               | 6                | 3                  | 2                  | 3               | 2                | t <sub>CK</sub> |

## V58C3643204SAT-55

| Frequency      | Cas Latency | t <sub>RC</sub> | t <sub>RFC</sub> | t <sub>RAS</sub> | t <sub>RCDRD</sub> | t <sub>RCDWR</sub> | t <sub>RP</sub> | t <sub>RRD</sub> | Unit            |
|----------------|-------------|-----------------|------------------|------------------|--------------------|--------------------|-----------------|------------------|-----------------|
| 183MHz (5.5ns) | 3           | 12              | 14               | 8                | 4                  | 2                  | 4               | 2                | t <sub>CK</sub> |
| 166MHz (6.0ns) | 3           | 10              | 12               | 7                | 3                  | 2                  | 3               | 2                | t <sub>CK</sub> |
| 143MHz (7.0ns) | 3           | 9               | 11               | 6                | 3                  | 2                  | 3               | 2                | t <sub>CK</sub> |

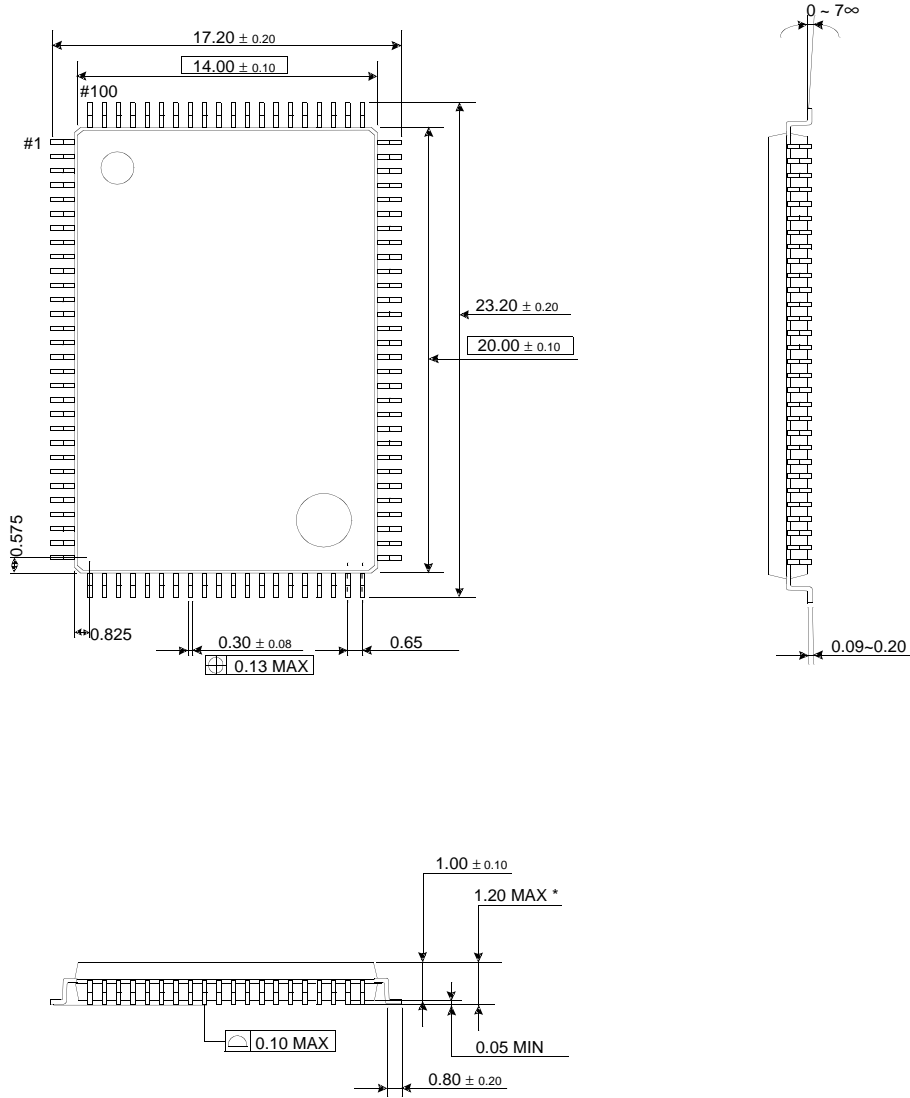
## V58C3643204SAT-60

| Frequency      | Cas Latency | t <sub>RC</sub> | t <sub>RFC</sub> | t <sub>RAS</sub> | t <sub>RCDRD</sub> | t <sub>RCDWR</sub> | t <sub>RP</sub> | t <sub>RRD</sub> | Unit            |
|----------------|-------------|-----------------|------------------|------------------|--------------------|--------------------|-----------------|------------------|-----------------|
| 166MHz (6.0ns) | 3           | 10              | 12               | 7                | 3                  | 2                  | 3               | 2                | t <sub>CK</sub> |
| 143MHz (7.0ns) | 3           | 9               | 11               | 6                | 3                  | 2                  | 3               | 2                | t <sub>CK</sub> |

*Package Diagram*

**100-Pin TQFP**

Dimensions in Millimeters



**U.S.A.**

3910 NORTH FIRST STREET  
SAN JOSE, CA 95134  
PHONE: 408-433-6000  
FAX: 408-433-0952

**TAIWAN**

7F, NO. 102  
MIN-CHUAN E. ROAD, SEC. 3  
TAIPEI  
PHONE: 886-2-2545-1213  
FAX: 886-2-2545-1209

NO 19 LI HSIN ROAD  
SCIENCE BASED IND. PARK  
HSIN CHU, TAIWAN, R.O.C.  
PHONE: 886-3-579-5888  
FAX: 886-3-566-5888

**SINGAPORE**

10 ANSON ROAD #23-13  
INTERNATIONAL PLAZA  
SINGAPORE 079903  
PHONE: 65-3231801  
FAX: 65-3237013

**JAPAN**

ONZE 1852 BUILDING 6F  
2-14-6 SHINTOMI, CHUO-KU  
TOKYO 104-0041  
PHONE: 03-3537-1400  
FAX: 03-3537-1402

**UK & IRELAND**

SUITE 50, GROVEWOOD  
BUSINESS CENTRE  
STRATHCLYDE BUSINESS  
PARK  
BELLSHILL, LANARKSHIRE,  
SCOTLAND, ML4 3NQ  
PHONE: 44-1698-748515  
FAX: 44-1698-748516

**GERMANY  
(CONTINENTAL  
EUROPE & ISRAEL)**

BENZSTRASSE 32  
71083 HERRENBERG  
GERMANY  
PHONE: +49 7032 2796-0  
FAX: +49 7032 2796 22

**U.S. SALES OFFICES****NORTHWESTERN**

3910 NORTH FIRST STREET  
SAN JOSE, CA 95134  
PHONE: 408-433-6000  
FAX: 408-433-0952

**SOUTHWESTERN**

302 N. EL CAMINO REAL #200  
SAN CLEMENTE, CA 92672  
PHONE: 949-361-7873  
FAX: 949-361-7807

**CENTRAL,  
NORTHEASTERN &  
SOUTHEASTERN**

604 FIELDWOOD CIRCLE  
RICHARDSON, TX 75081  
PHONE: 214-352-3775  
FAX: 214-904-9029

---

The information in this document is subject to change without notice.

MOSEL VITELIC makes no commitment to update or keep current the information contained in this document. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of MOSEL-VITELIC.

MOSEL VITELIC subjects its products to normal quality control sampling techniques which are intended to provide an assurance of high quality products suitable for usual commercial applications. MOSEL VITELIC does not do testing appropriate to provide 100% product quality assurance and does not assume any liability for consequential or incidental arising from any use of its products. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such applications.