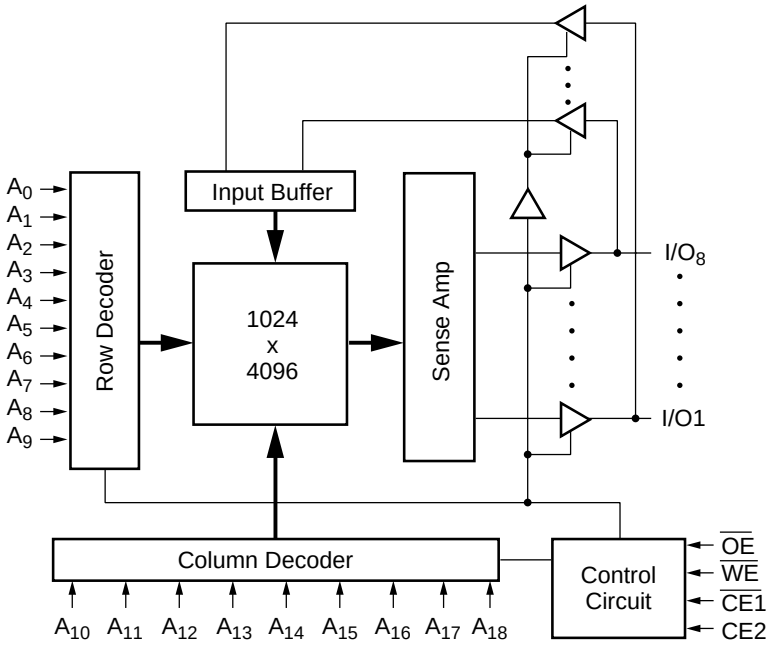
Features

- High-speed: 85, 100 ns
- Ultra low standby current of 2µA (max.)
- Fully static operation
- All inputs and outputs directly compatible
- Three state outputs
- Ultra low data retention current (V_{CC} = 1.0V)
- Operating voltage: 1.8V–2.3V
- Packages
  - 36-Ball CSP BGA (8mm x 10mm)

Description

The V62C1804096 is a very low power CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW $\overline{CE1}$, and active HIGH CE2, an active LOW $\overline{OE}$, and three static I/O's. This device has an automatic power-down mode feature when deselected.

Functional Block Diagram



Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)		Power		Temperature Mark
	B	85	100	L	LL	
0°C to 70 °C	•	•	•	•	•	Blank
–40°C to +85°C	•	•	•		•	I

Pin Descriptions

A_0–A_{18} Address Inputs
These 19 address inputs select one of the 512K x 8 bit segments in the RAM.

$\overline{CE}_1$, CE_2 Chip Enable Inputs
$\overline{CE}_1$ is active LOW and CE_2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when deselected.

$\overline{OE}$ Output Enable Input
The Output Enable input is active LOW. With chip enabled, when $\overline{OE}$ is LOW and $\overline{WE}$ HIGH, data of the selected memory location will be available on the I/O pins. When $\overline{OE}$ is HIGH, the I/O pins will be in the high impedance state.

$\overline{WE}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present at the I/O pins; when $\overline{WE}$ is LOW and $\overline{OE}$ is HIGH, the data present on the I/O pins will be written into the selected memory locations.

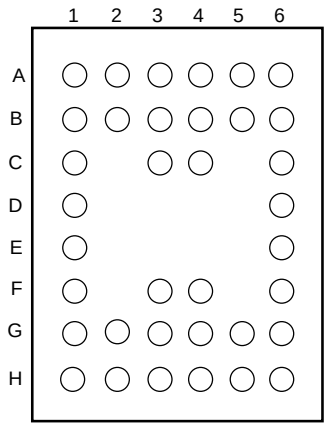
I/O_1–I/O_8 Data Input and Data Output Ports
These 8 bidirectional ports are used to read data from and write data into the RAM.

V_{CC} Power Supply

GND Ground

Pin Configurations (Top View)

36 BGA



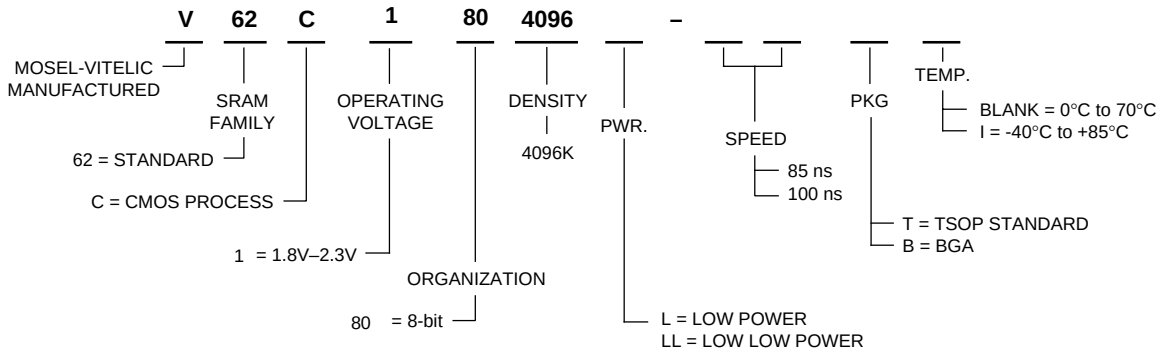
TOP VIEW

	1	2	3	4	5	6
A	A0	A1	CE2	A3	A6	A8
B	I/O5	A2	$\overline{WE}$	A4	A7	I/O1
C	I/O6	NB	NC	A5	NB	I/O2
D	VSS	NB	NB	NB	NB	VCC
E	VCC	NB	NB	NB	NB	VSS
F	I/O7	NB	A18	A17	NB	I/O3
G	I/O8	$\overline{OE}$	$\overline{CE1}$	A16	A15	I/O4
H	A9	A10	A11	A12	A13	A14

Note: NC means no connect.
NB means no ball.

TOP VIEW

Part Number Information



Absolute Maximum Ratings (1)

Symbol	Parameter	Commercial	Industrial	Units
V_{CC}	Supply Voltage	-0.5 to + V_{CC} + 0.5	-0.5 to + V_{CC} + 0.5	V
V_N	Input Voltage	-0.5 to + V_{CC} + 0.5	-0.5 to + V_{CC} + 0.5	V
V_{DQ}	Input/Output Voltage Applied	V_{CC} + 0.3	V_{CC} + 0.3	V
T_{BIAS}	Temperature Under Bias	-10 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C

NOTE:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance*

T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	8	pF

NOTE:
1. This parameter is guaranteed and not tested.

Truth Table

Mode	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O Operation
Standby	H	X	X	X	High Z
Standby	X	L	X	X	High Z
Output Disable	L	H	H	H	High Z
Read	L	H	L	H	D_{OUT}
Write	L	H	X	L	D_{IN}

NOTE:
X = Don't Care, L = LOW, H = HIGH

DC Electrical Characteristics (over all temperature ranges, V_{CC} = 1.8V–2.3V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input LOW Voltage(1,2)		-0.3	—	0.4	V
V_{IH}	Input HIGH Voltage(1)		1.6	—	V_{CC}+0.3	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	—	—	1	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{CE}_1$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	1	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 2mA	—	—	0.4	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -0.5mA	V_{CC}–0.4	—	—	V

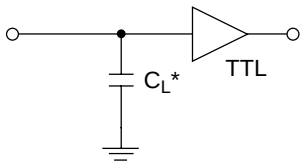
Symbol	Parameter		Comm.(3)	Ind.(3)	Units
I_{CC1}	Average Operating Current, $\overline{CE}_1$ = V_{IL}, CE_2 = V_{CC} – 0.2, Output Open, V_{CC} = Max.	f = fmax	25	30	mA
		f = 1 MHz	2	3	
I_{SB}	TTL Standby Current $\overline{CE}_1$ >=V_{IH}, CE_2 <= V_{IL}, V_{CC} = Max., f = 0	L	0.4	0.5	mA
		LL	0.3	0.3	
I_{SB1}	CMOS Standby Current, $\overline{CE}_1$ Š V_{CC} – 0.2V, CE_2 ð 0.2V, V_{IN}>= V_{CC} – 0.2V or V_{IN} <=0.2V, V_{CC} = Max., f = 0	L	5	7	µA
		LL	2	3	

NOTES:
1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. V_{IL} (Min.) = -3.0V for pulse width < t_{RC}/2.
3. Maximum value.

AC Test Conditions

Input Pulse Levels	0 to 1.6V
Input Rise and Fall Times	5 ns
Timing Reference Levels	0.9V
Output Load	see below

AC Test Loads and Waveforms



C_L = 30pF + 1TTL Load

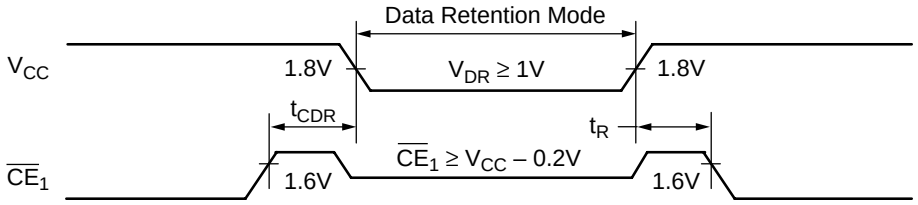
* Includes scope and jig capacitance

Data Retention Characteristics

Symbol	Parameter		Power	Min.	Typ.(2)	Max.	Units
V_{DR}	V_{CC} for Data Retention $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 < 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$			1.0	—	2.3	V
I_{CCDR}	Data Retention Current $\overline{CE}_1 \geq V_{DR} - 0.2V$, $CE_2 < 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$, $V_{DR} = 1.0V$	Com'l	L	—	1	3	µA
			LL	—	0.5	1.5	
		Ind.	L	—	—	5	
			LL	—	—	2	
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R	Operation Recovery Time (see Retention Waveform)			t_{RC}(1)	—	—	ns

NOTES:
1. t_{RC} = Read Cycle Time
2. T_A = +25°C.

Low V_{CC} Data Retention Waveform (1) ($\overline{CE}_1$ Controlled)



Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Electrical Characteristics

(over all temperature ranges)

Read Cycle

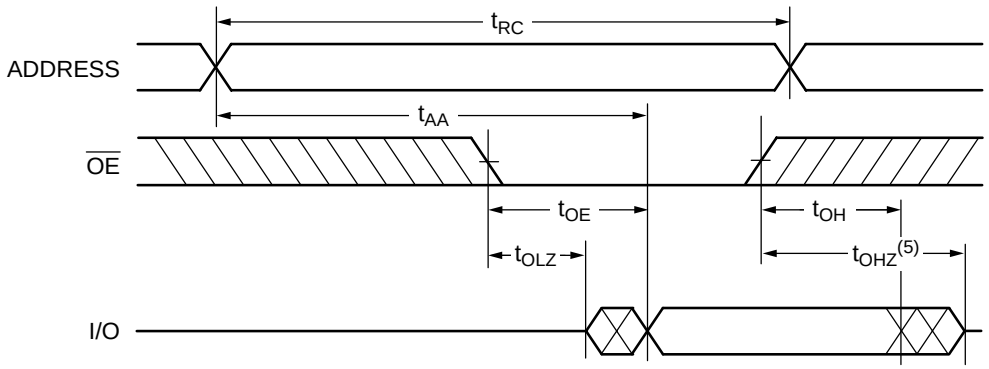
Parameter Name	Parameter	85		100		Unit
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	85	—	100	—	ns
t_{AA}	Address Access Time	—	85	—	100	ns
t_{ACS1}	Chip Enable Access Time	—	85	—	100	ns
t_{ACS2}	Chip Enable Access Time	—	85	—	100	ns
t_{OE}	Output Enable to Output Valid	—	85	—	40	ns
t_{CLZ1}	Chip Enable to Output in Low Z	10	—	15	—	ns
t_{CLZ2}	Chip Enable to Output in Low Z	10	—	15	—	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	10	—	ns
t_{CHZ}	Chip Disable to Output in High Z	—	30	—	35	ns
t_{OHZ}	Output Disable to Output in High Z	—	30	—	35	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	ns

Write Cycle

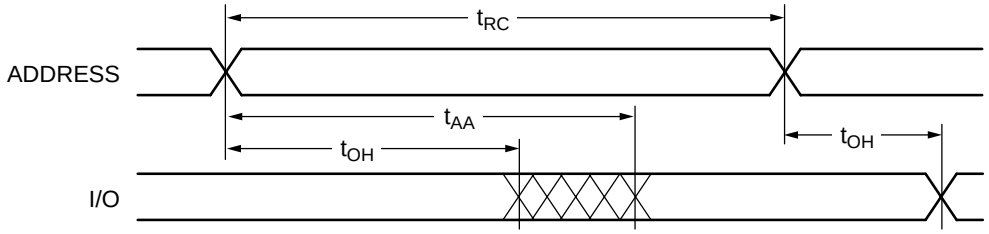
Parameter Name	Parameter	85		100		Unit
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	85	—	70	—	ns
t_{CW}	Chip Enable to End of Write	70	—	60	—	ns
t_{AS}	Address Setup Time	0	—	0	—	ns
t_{AW}	Address Valid to End of Write	70	—	60	—	ns
t_{WP}	Write Pulse Width	60	—	50	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	ns
t_{WHZ}	Write to Output High-Z	—	25	—	30	ns
t_{DW}	Data Setup to End of Write	40	—	45	—	ns
t_{DH}	Data Hold from End of Write	0	—	0	—	ns

Switching Waveforms (Read Cycle)

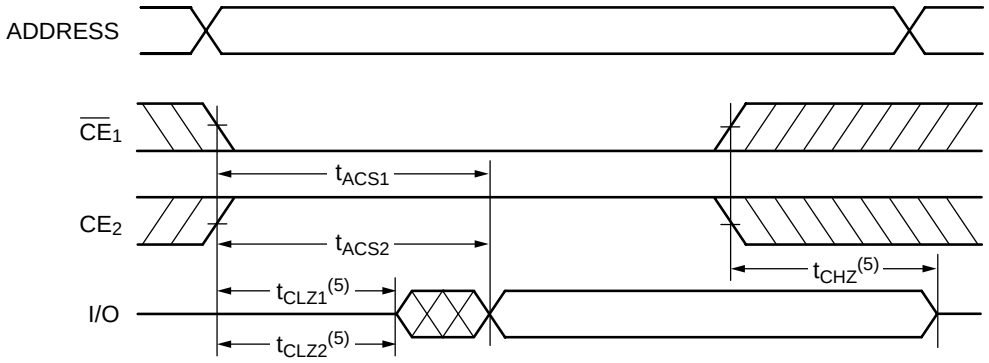
Read Cycle 1(1, 2)



Read Cycle 2(1, 2, 4)



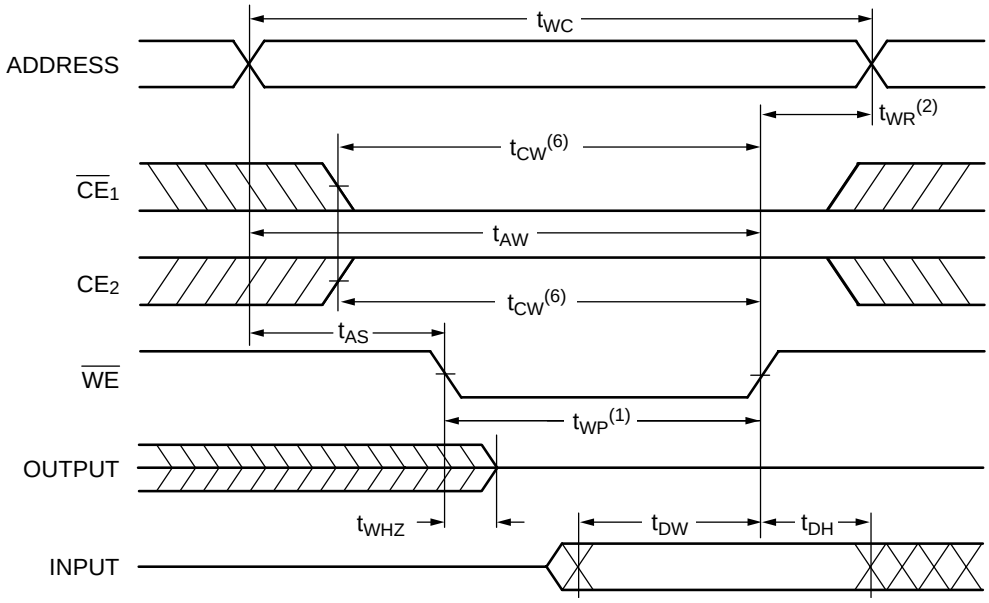
Read Cycle 3(1, 3, 4)



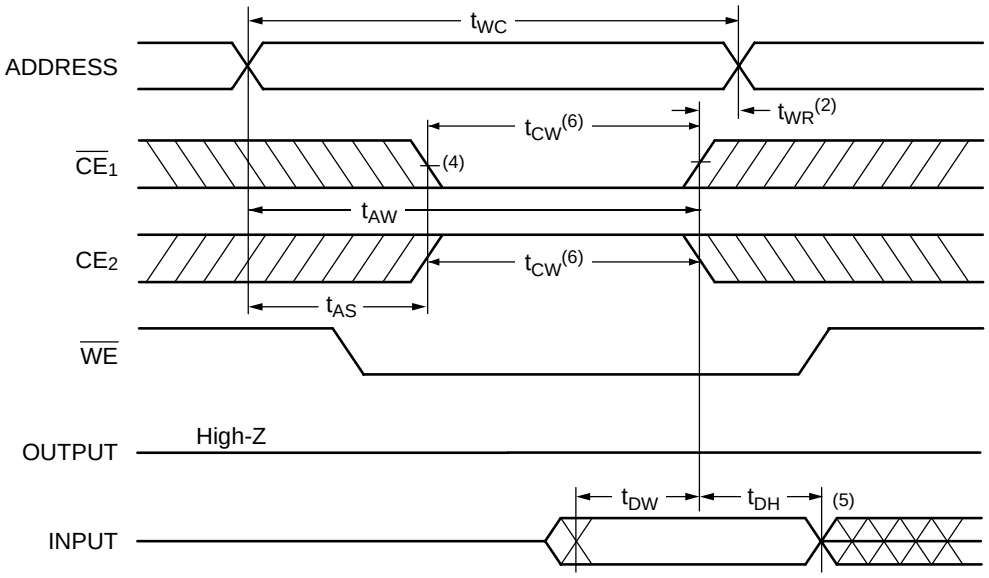
NOTES:
1. $\overline{WE}$ = V_{IH}.
2. $\overline{CE_1}$ = V_{IL} and CE_2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and/or CE_2 transition HIGH.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state with C_L = 5pF. This parameter is guaranteed and not 100% tested.

Switching Waveforms (Write Cycle)

Write Cycle 1 ($\overline{WE}$ Controlled)(4)



Write Cycle 2 (CE Controlled)(4)

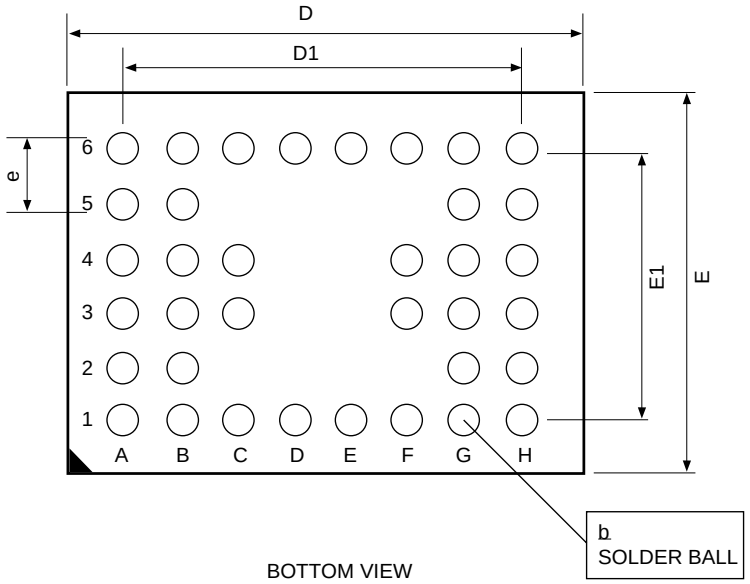


NOTES:

1. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ and CE_2 active and $\overline{WE}$ low. All signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
2. t_{WR} is measured from the earlier of $\overline{CE}_1$ or $\overline{WE}$ going high, or CE_2 going LOW at the end of the write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. $\overline{OE}$ = V_{IL} or V_{IH}. However it is recommended to keep $\overline{OE}$ at V_{IH} during write cycle to avoid bus contention.
5. If $\overline{CE}_1$ is LOW and CE_2 is HIGH during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. t_{CW} is measured from $\overline{CE}_1$ going low or CE_2 going HIGH to the end of write.

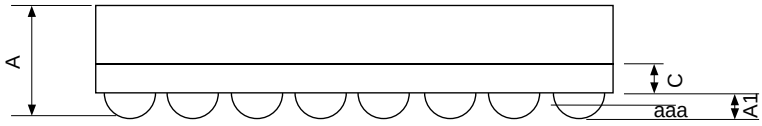
Package Diagrams

36 Ball—8x10 BGA



BOTTOM VIEW

SYMBOL	UNIT.MM
A	1.05+0.15
A1	0.25±0.05
b	0.35±.0.05
c	0.30(TYP)
D	10.00±0.10
D1	5.25
E	8.00±0.10
E1	3.75
e	0.75TYP
aaa	0.10



SIDE VIEW

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