

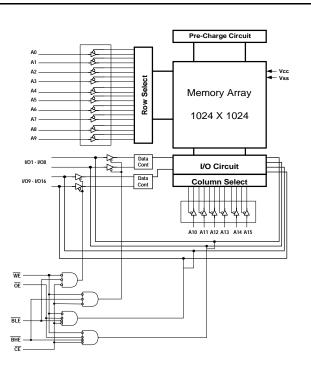
V62C3161024L(L)

Ultra Low Power 64K x 16 CMOS SRAM

Features

- Ultra Low-power consumption - Active: 40mA I_{CC} at 55ns
 - Stand-by: 5 μA (CMOS input/output) 1 μA (CMOS input/output, L version)
- 55/70/85/100 ns access time
- Equal access and cycle time
- Single +2.7V to 3.3V Power Supply
- Tri-state output
- Automatic power-down when deselected
- Multiple center power and ground pins for improved noise immunity
- Individual byte controls for both Read and Write cycles
- Available in 44 pin TSOP (II) Package

Logic Block Diagram



Functional Description

TheV62C3161024L is a Low Power CMOS Static RAM organized as 65,536 words by 16 bits. Easy memory expansion is provided by an active LOW ($\overline{\text{CE}}$) and ($\overline{\text{OE}}$) pin.

This device has an automatic power-down mode feature when deselected. Separate Byte Enable controls (BLE and BHE) allow individual bytes to be accessed. BLE controls the lower bits I/O1 - I/O8. BHE controls the upper bits I/O9 - I/O16.

Writing to these devices is performed by taking Chip Enable (\overline{CE}) with Write Enable (WE) and Byte Enable (BLE/BHE) LOW.

Reading from the device is performed by taking Chip Enable (\overline{CE}) with Output Enable (\overline{OE}) and Byte Enable (BLE/BHE) LOW while Write Enable (WE) is held HIGH.

TSOP(II)

| A4 | 1 2 3 4 5 6 7 8 9 | 44 43 42 41 40 39 38 37 36 35 | A5 A6 <u>A7</u> <u>OE</u> <u>BHE</u> J/O16 J/O15 J/O14 J/O13 |
|-------------|---|--|--|
| Vcc 🗆 | 11 | 34 | Vss |
| Vss 🗆 | 12 | 33 | Vcc |
| I/05 🗀 | 13 | 32 | I/012 |
| I/06 🖂 | 14 | 31 | I/011 |
| I/07 🗀 | 15 | 30 | I/010 |
| <u>I/08</u> | 16 | 29 | I/09 |
| WE 🗆 | 17 | 28 | NC |
| A15 🗆 | 18 | 27 | A8 |
| A14 🗆 | 19 | 26 | A9 |
| A13 🗆 | 20 | 25 | A10 |
| A12 🗆 | 21 | 24 | A11 |
| NC 🗆 | 22 | 23 | NC |
| | | | |



Absolute Maximum Ratings *

| Parameter | Symbol | Minimum | Maximum | Unit |
|------------------------------------|--------|---------|---------|----------------|
| Voltage on Any Pin Relative to Gnd | Vt | -0.5 | +4.6 | V |
| Power Dissipation | PT | _ | 1.0 | W |
| Storage Temperature (Plastic) | Tstg | -55 | +150 | ⁰ C |
| Temperature Under Bias | Tbias | -40 | +85 | OO |

* Note: Stresses greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and function operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect reliability.

Truth Table

| CE | OE | WE | BLE | BHE | I/O1-I/O8 | I/O9-I/O16 | Power | Mode |
|----|----|----|-----|-----|-----------|------------|---------|-----------------|
| Н | Х | Х | Х | Х | High-Z | High-Z | Standby | Standby |
| L | L | Н | L | Н | Data Out | High-Z | Active | Low Byte Read |
| L | L | Н | Н | L | High-Z | Data Out | Active | High Byte Read |
| L | L | Н | L | L | Data Out | Data Out | Active | Word Read |
| L | Х | L | L | L | Data In | Data In | Active | Word Write |
| L | Х | L | L | Н | Data In | High-Z | Active | Low Byte Write |
| L | Х | L | Н | L | High-Z | Data In | Active | High Byte Write |
| L | Н | Н | Х | Х | High-Z | High-Z | Active | Output Disable |
| L | Х | Х | Н | Н | High-Z | High-Z | Active | Output Disable |

* **Key:** X = Don't Care, L = Low, H = High

Recommended Operating Conditions ($T_A = 0^0 C$ to $+70^0 C / -40^0 C$ to $85^0 C^{**}$)

| Parameter | Symbol | Min | Тур | Max | Unit |
|-----------------|-----------------|-------|-----|-----------------------|------|
| Supply Voltage | V _{CC} | 2.7 | 3.0 | 3.3 | V |
| Supply voltage | Gnd | 0.0 | 0.0 | 0.0 | V |
| log at Malta an | V _{IH} | 2.2 | - | V _{CC} + 0.5 | V |
| Input Voltage | V _{IL} | -0.5* | - | 0.6 | V |

* V_{IL} min = -2.0V for pulse width less than $t_{RC}/2$.

** For Industrial Temperature



DC Operating Characteristics ($V_{cc} = 3V \pm 10\%$, Gnd = 0V, $T_A = 0^0$ C to $+70^0$ C / -40^0 C to 85^0 C)

| Parameter | Sym | Test Condition | ong | -: | 55 | -' | 70 | -8 | 85 | -100 | | Unit |
|---|------------------|---|------|-----|-----|-----|-----|-----|-----|------|-----|------|
| r al ameter | Sym | Test Condition | 0115 | Min | Max | Min | Max | Min | Max | Min | Max | Umt |
| Input Leakage Current | lı _{lı} | V_{cc} = Max, V_{in} = Gnd to V_{cc} | | - | 1 | - | 1 | - | 1 | - | 1 | μA |
| Output Leakage Current | li _{lo} | $\overline{CE} = V_{IH} \text{ or } V_{cc} = Max,$ $V_{OUT} = Gnd \text{ to } V_{cc}$ | | - | 1 | - | 1 | - | 1 | - | 1 | μA |
| Operating Power Supply Current | I _{CC} | \overline{CE} = V_{IL} , V_{IN} = V_{IH} or V_{IL} , I_{OUT} = 0 | | - | 3 | - | 3 | - | 3 | - | 3 | mA |
| Average Operating Current | I _{CC1} | I _{OUT} = 0mA, Min Cycle, 100% Duty | | - | 40 | - | 35 | - | 30 | - | 30 | mA |
| | I _{CC2} | $\label{eq:cell} \begin{array}{l} \overline{CE} \leq 0.2V \\ I_{OUT} = 0mA, \\ Cycle \ Time=1 \mu s, \ Duty=10 \end{array}$ | 0% | - | 3 | - | 3 | - | 3 | - | 3 | mA |
| Standby Power Supply Current (TTL Level) | I _{SB} | CE = V _{IH} | | - | 0.5 | - | 0.5 | - | 0.5 | - | 0.5 | mA |
| Standby Power Supply | I _{SB1} | $\overline{CE} \ge V_{cc} - 0.2V$ | L | - | 5 | - | 5 | - | 5 | - | 5 | μΑ |
| Current (CMOS Level) | | $V_{IN} \le 0.2V \text{ or}$ $V_{IN} \ge V_{CC} - 0.2V$ | LL | - | 1 | - | 1 | - | 1 | - | 1 | μΑ |
| Output Low Voltage | V _{OL} | I _{OL} = 2 mA | | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | V |
| Output High Voltage | V _{OH} | I _{OH} = -2 mA | | 2.4 | - | 2.4 | - | 2.4 | - | 2.4 | - | V |

Capacitance (f = 1MHz, $T_A = 25^{\circ}C$)

| Parameter* | Symbol | Test Condition | Max | Unit |
|-------------------|------------------|-------------------------|-----|------|
| Input Capacitance | C _{in} | $V_{in} = 0V$ | 7 | pF |
| I/O Capacitance | C _{I/O} | $V_{in} = V_{out} = 0V$ | 8 | pF |

* This parameter is guaranteed by device characterization and is not production tested.

AC Test Conditions Input Pulse Level

Reference Level

0.6V to 2.2V Input Rise and Fall Time 5ns Input and Output Timing 1.4V

Output Load Condition
$$\begin{split} C_L &= 30 pf + 1 TTL \ Load \\ C_L &= 100 pf + 1 TTL \ Load \end{split}$$
55ns/70ns/85ns Load for 100ns

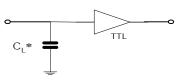


Figure A.

* Including Scope and Jig Capacitance



| Parameter | Sym | -55 | | -7 | 70 | -85 | | -100 | | Unit | Note |
|--------------------------------------|------------------|-----|-----|-----|-----|-----|-----|------|-----|------|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Read Cycle Time | t _{RC} | 55 | - | 70 | - | 85 | - | 100 | - | ns | |
| Address Access Time | t _{AA} | - | 55 | - | 70 | - | 85 | - | 100 | ns | |
| Chip Enable Access Time | t _{ACE} | - | 55 | - | 70 | - | 85 | - | 100 | ns | |
| Output Enable Access Time | t _{OE} | - | 35 | - | 40 | - | 40 | - | 50 | ns | |
| Output Hold from Address Change | t _{OH} | 10 | - | 10 | - | 10 | - | 10 | - | ns | |
| Chip Enable to Output in Low-Z | t _{LZ} | 10 | - | 10 | - | 10 | - | 10 | - | ns | 4,5 |
| Chip Disable to Output in High-Z | t _{HZ} | - | 25 | - | 30 | - | 35 | - | 40 | ns | 3,4,5 |
| Output Enable to Output in Low-Z | t _{OLZ} | 5 | - | 5 | - | 5 | - | 5 | - | ns | |
| Output Disable to Output in High-Z | t _{OHZ} | - | 25 | - | 25 | - | 30 | - | 35 | ns | |
| BLE, BHE Enable to Output in Low-Z | t _{BLZ} | 5 | - | 5 | - | 5 | - | 5 | - | ns | 4,5 |
| BLE, BHE Disable to Output in High-Z | t _{BHZ} | - | 25 | - | 25 | - | 30 | - | 35 | ns | 3,4,5 |
| BLE, BHE Access Time | t _{BA} | - | 35 | - | 40 | - | 40 | - | 50 | ns | |

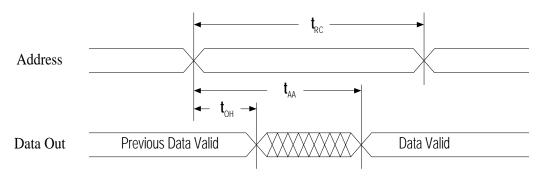
Read Cycle ⁽⁹⁾ ($V_{cc} = 3.0V \pm 0.3V$, Gnd = 0V, $T_A = 0^0 C$ to $+70^0 C / -40^0 C$ to $+85^0 C$)

Write Cycle ⁽¹¹⁾ ($V_{cc} = 3.0V \pm 0.3V$, Gnd = 0V, $T_A = 0^0C$ to $+70^0C / -40^0C$ to $+85^0C$)

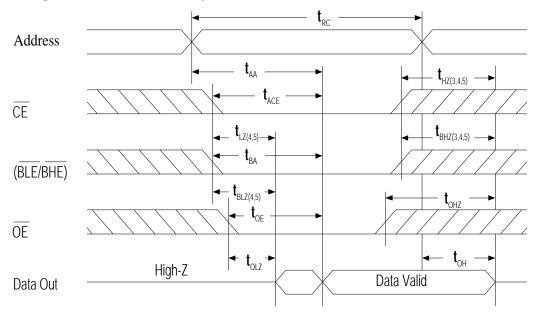
| Parameter | Symbol | - | 55 | -7 | 70 | -8 | 85 | -] | 100 | Unit | Note |
|----------------------------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Write Cycle Time | t _{WC} | 55 | - | 70 | - | 85 | - | 100 | - | ns | |
| Chip Enable to Write End | t _{CW} | 50 | - | 60 | - | 70 | - | 80 | - | ns | |
| Address Setup to Write End | t _{AW} | 50 | - | 60 | - | 70 | - | 80 | - | ns | |
| Address Setup Time | t _{AS} | 0 | - | 0 | - | 0 | - | 0 | - | ns | |
| Write Pulse Width | t _{WP} | 45 | - | 50 | - | 60 | - | 70 | - | ns | |
| Write Recovery Time | t _{WR} | 0 | - | 0 | - | 0 | - | 0 | - | ns | |
| Data Valid to Write End | t _{DW} | 25 | - | 30 | - | 35 | - | 40 | - | ns | |
| Data Hold Time | t _{DH} | 0 | - | 0 | - | 0 | - | 0 | - | ns | |
| Write Enable to Output in High-Z | t _{WHZ} | - | 25 | - | 30 | - | 35 | - | 40 | ns | |
| Output Active from Write End | t _{OW} | 5 | - | 5 | - | 5 | - | 5 | - | ns | |
| BLE, BHE Setup to Write End | t _{BW} | 50 | - | 60 | - | 70 | - | 80 | - | ns | |
| | | | 4 | | | 1 | 1 | 1 | 1 | 1 | L |



Timing Waveform of Read Cycle 1 (Address Controlled)



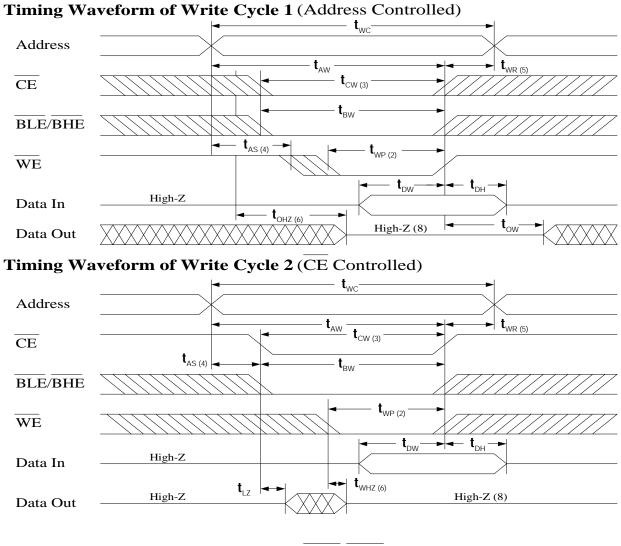
Timing Waveform of Read Cycle 2



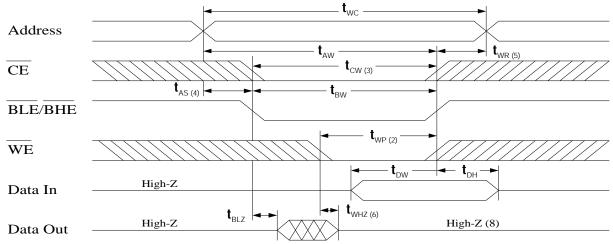
Notes (Read Cycle)

- 1. WE are high for read cycle.
- 2. All read cycle timing is referenced from the last valid address to the first transition address.
- 3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition referenced to V_{OH} or V_{OL} levels.
- 4. At any given temperature and voltage condition t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
- 5. Transition is measured \pm 200mV from steady state voltage with load. This parameter is sampled and not 100% tested.
- 6. Device is continuously selected with $\overline{CE} = V_{IL}$.
- 7. Address valid prior to coincident with \overline{CE} transition Low.
- 8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 9. For test conditions, see AC Test Condition, Figure A.





Timing Waveform of Write Cycle 3 (BLE/BHE Controlled)





Notes (Write Cycle)

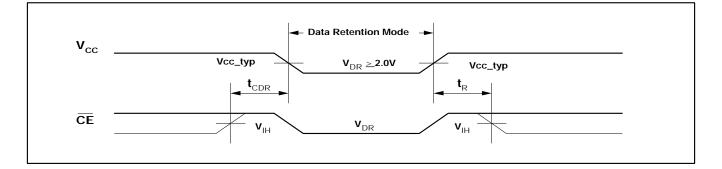
- 1. All write timing is referenced from the last valid address to the first transition address.
- 2. A write occurs during the overlap of a low \overline{CE} and \overline{WE} . A write begins at the latest transition among \overline{CE} and \overline{WE} going low: A write ends at the earliest transition among \overline{CE} going high and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
- 3. t_{cw} is measured from the later of \overline{CE} going low to end of write.
- 4. t_{AS} is measured from the address valid to the beginning of write.
- 5. t_{wR} is measured from the end of write to the address change.
- 6. If \overline{OE} , \overline{CE} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- 7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- 8. If $\overline{\text{CE}}$ goes low simultaneously with $\overline{\text{WE}}$ going low or after $\overline{\text{WE}}$ going low, the outputs remain high impedance state.
- 9. Dout is the read data of the new address.
- 10. When \overline{CE} is low: I/O pins are in the outputs state. The input signals in the opposite phase leading to the output should not be applied.
- 11. For test conditions, see AC Test Condition, Figure A & B.



Data Retention Characteristics (L Version Only)⁽¹⁾

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|--|-------------------|---|-----------------|-----|------|
| V _{CC} for Data Retention | V _{DR} | $\overline{\text{CE}} \ge \text{V}_{\text{CC}} - 0.2\text{V}$ | 2.0 | - | V |
| Data Retention Current | I _{CCDR} | | - | 1 | μA |
| Chip Deselect to Data Retention Time | t _{CDR} | $V_{\text{IN}} \geq V_{\text{CC}}$ - 0.2V or | 0 | - | ns |
| Operation Recovery Time ⁽²⁾ | t _R | $V_{IN} \leq 0.2V$ | t _{RC} | - | ns |

Data Retention Waveform (L Version Only) ($T_A = 0^0 C$ to $+70^0 C / -40^0 C$ to $+85^0 C$)



Notes

- 1. L-version includes this feature.
- 2. This Parameter is sampled and not 100% tested.
- 3. For test conditions, see AC Test Condition, Figure A.
- 4. This parameter is tested with CL = 5pF as shown in Figure B. Transition is measured $\pm 500mV$ from steady-state voltage.
- 5. This parameter is guaranteed, but is not tested.
- 6. $\overline{\text{WE}}$ is High for read cycle.
- 7. $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are LOW for read cycle.
- 8. Address valid prior to or coincident with \overline{CE} transition LOW.
- 9. All read cycle timings are referenced from the last valid address to the first transion address.
- 10. $\overline{\text{CE}}$ or $\overline{\text{WE}}$ must be HIGH during address transition.
- 11. All write cycle timings are referenced from the last valid address to the first transition address.



Ordering Information

| Device Type* | Speed | Package |
|---------------------|--------|--------------------|
| V62C3161024L-55T | 55 ns | 44-pin TSOP Type 2 |
| V62C3161024L-70T | 70 ns | |
| V62C3161024L-85T | 85 ns | |
| V62C3161024L-100T | 100 ns | |
| V62C3161024LL-55T | 55 ns | |
| V62C3161024LL-70T | 70 ns | |
| V62C3161024LL-85T | 85 ns | |
| V62C3161024LL-100T | 100 ns | |

* For Industrial temperature tested devices, an "I" designator will be added to the end of the device number.

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